## Languages & Libraries

### Testbench + Design

**From:**

SystemVerilog/Verilog

0ps

**UVM / OVM** (http://eda-playground.readthedocs.org/en/latest/intro.html#libraries-methodologies)

None

**To:**

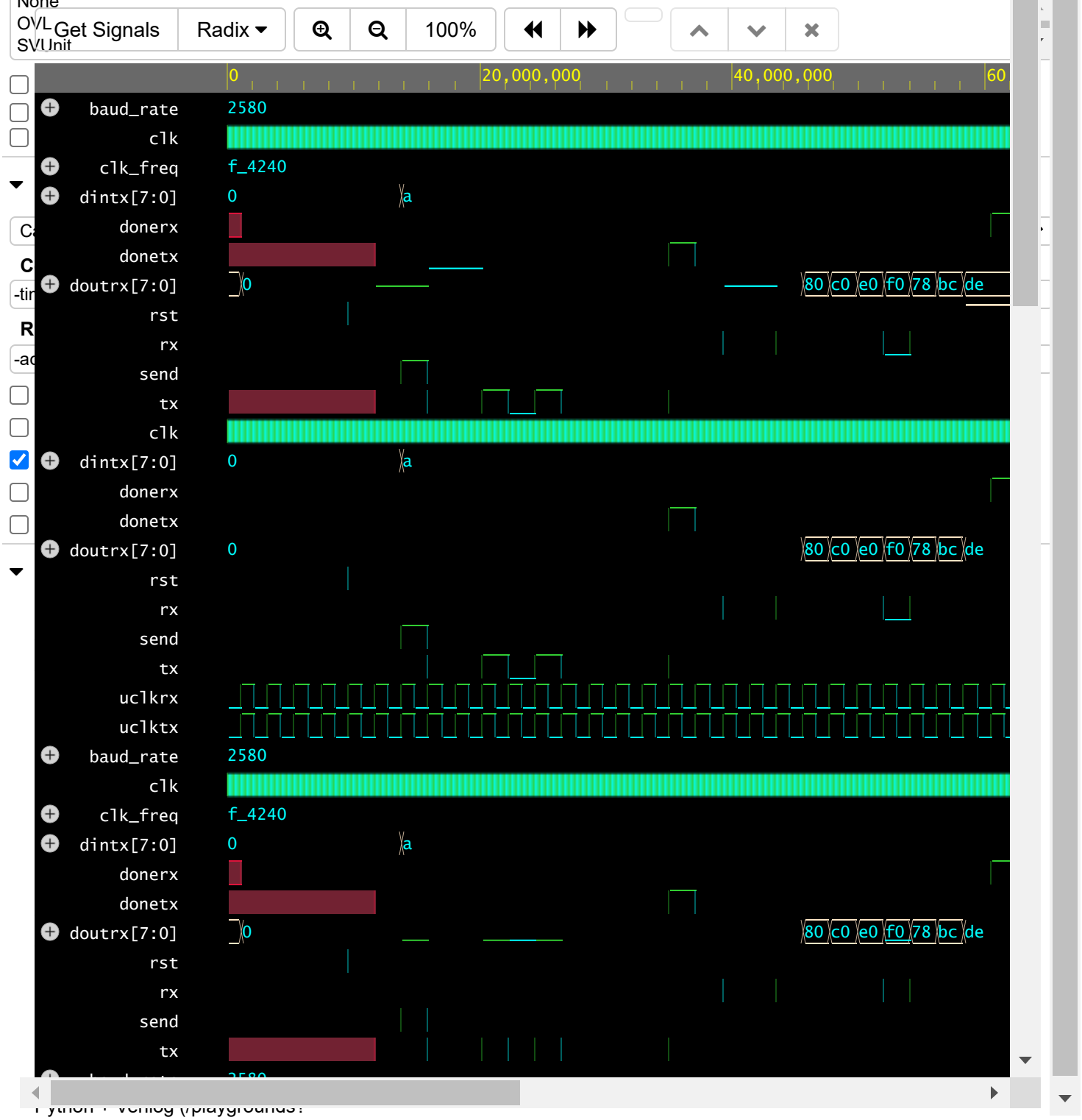
138,850,000ps

**Other Libraries** (http://eda-playground.readthedocs.org/en/latest/intro.html#libraries-methodologies)

None

OVL

SVUnit



searchString=&language=Python+%2B+SV%2FVerilog&simulator=&methodologies=&curated=true)

Python Only (/playgrounds?searchString=&language=Python+2.7+only&simulator=&methodologies=&curated=true)

C++/SystemC (/playgrounds?searchString=&language=C%2B%2B+only&simulator=&methodologies=&curated=true)

**EPWave**

Community

Collaborate

Forum (https://groups.google.com/forum/#!forum/eda-playground)

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testbench.sv testbench1.sv

## EPWave

## EPWave

## EPWave

```
191
192                end
193
194
195
196      end
197
198    endtask
199
200  endclass
201
202  /*
203
204  module tb;
205    generator gen;
206    driver drv;
207    event next;
208    event done;
209    mailbox #(transaction) mbx;
210    mailbox #(bit [7:0]) mbxt;
211
212    uart_if vif();
213
214    uart_top #(1000000, 9600) dut
   (vif.clk,vif.rst,vif.rx,vif.dintx,vif.send,vif.tx,vif.doutrx,vif.donetx, vif.donerx);
215
216
217
218      initial begin
219        vif.clk <= 0;
220      end
221
222      always #10 vif.clk <= ~vif.clk;
223
224
225
226    initial begin
227      mbx = new();
228      mbxt = new();
229      gen = new(mbx);
230      drv = new(mbxt,mbx);
231      gen.count  = 20;
232      drv.vif = vif;
233
234      gen.drvnext = next;
235
236      drv.drvnext = next;
237    end
238
239    initial begin
240
241      fork
242        gen.run();
243        drv.run();
```

## EPWave

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## EPWave

design.sv design1.sv

```
// Code your design here
`timescale 1ns / 1ps

module uart_top
#(
parameter clk_freq = 1000000,
parameter baud_rate = 9600
)
(
  input clk,rst,
  input rx,
  input [7:0] dintx,
  input send,
  output tx,
  output [7:0] doutrx,
  output donetx,
  output donerx
    );

uarttx
#(clk_freq, baud_rate)
utx
(clk, rst, send, dintx, tx, donetx);

uartrx
#(clk_freq, baud_rate)
rtx
(clk, rst, rx, donerx, doutrx);


endmodule
```

EPWave

```
32
33
34 //////////////////////////////////////////////////////////////////
35
36 module uarttx
37 #(
38 parameter clk_freq = 1000000,
39 parameter baud_rate = 9600
40 )
41 (
42 input clk,rst,
43 input send,
44 input [7:0] tx_data,
45 output reg tx,
46 output reg donetx
47 );
48
49   localparam clkcount = (clk_freq/baud_rate); ///x
50
51 integer count = 0;
52 integer counts = 0;
53
54 reg uclk = 0;
55
56 enum bit[1:0] {idle = 2'b00, start = 2'b01, transfer = 2'b10, done = 2'b11} state;
57
58  ///////////uart_clock_gen
59   always@(posedge clk)
60     begin
61       if(count < clkcount/2)
62         count <= count + 1;
63       else begin
```

## EPWave

## EPWave

Log | Share

EPWave

```
[2024-07-25 19:51:40 UTC] xrun -Q -unbuffered '-timescale' '1ns/1ns' '-sysv' '-access' '+rw' desig
TOOL:   xrun    23.09-s001: Started on Jul 25, 2024 at 15:51:41 EDT
xrun: 23.09-s001: (c) Copyright 1995-2023 Cadence Design Systems, Inc.
        Top level design units:
                $unit_0x67f934e9
                tb
Loading snapshot worklib.tb:sv ..................... Done
SVSEED default: 1
xcelium> source /xcelium23.09/tools/xcelium/files/xmsimrc
xcelium> run
[DRV] : RESET DONE
[GEN] : oper : write send : 0 TX_DATA : 00001010 RX_IN : 0 TX_OUT : 0 RX_OUT : 00000000 DONE_TX :
[DRV]: Data Sent : 10
[MON] : DATA SEND on UART TX 10
[SCO] : DRV : 10 MON : 10
DATA MATCHED
[GEN] : oper : read send : 0 TX_DATA : 11000010 RX_IN : 0 TX_OUT : 0 RX_OUT : 00000000 DONE_TX :
[DRV]: Data RCVD : 222
[MON] : DATA RCVD RX 222
[SCO] : DRV : 222 MON : 222
DATA MATCHED
[GEN] : oper : write send : 0 TX_DATA : 00000100 RX_IN : 0 TX_OUT : 0 RX_OUT : 00000000 DONE_TX :
[DRV]: Data Sent : 4
[MON] : DATA SEND on UART TX 4
[SCO] : DRV : 4 MON : 4
DATA MATCHED
[GEN] : oper : read send : 0 TX_DATA : 00011001 RX_IN : 0 TX_OUT : 0 RX_OUT : 00000000 DONE_TX :
[DRV]: Data RCVD : 26
[MON] : DATA RCVD RX 26
[SCO] : DRV : 26 MON : 26
DATA MATCHED
[GEN] : oper : read send : 0 TX_DATA : 00110101 RX_IN : 0 TX_OUT : 0 RX_OUT : 00000000 DONE_TX :
[DRV]: Data RCVD : 32
[MON] : DATA RCVD RX 32
[SCO] : DRV : 32 MON : 32
DATA MATCHED
Simulation complete via $finish(1) at time 138850 NS + 3
./testbench.sv:505      $finish();
xcelium> exit
TOOL:   xrun    23.09-s001: Exiting on Jul 25, 2024 at 15:51:42 EDT  (total: 00:00:01)
Finding VCD file...
./dump.vcd
[2024-07-25 19:51:42 UTC] Opening EPWave...
Done
```