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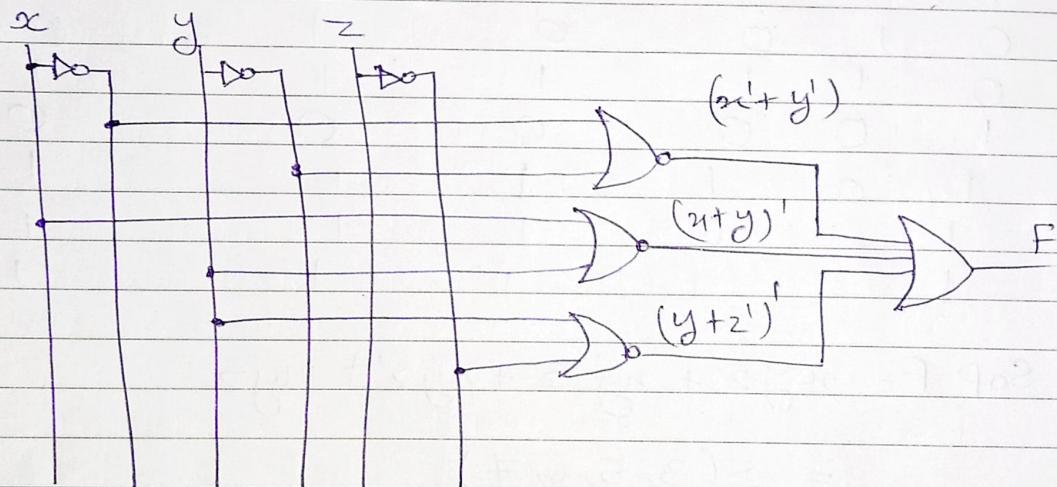
Assignment - 2

Q1) Given Boolean function

$$F = xy + x'y' + y'z$$

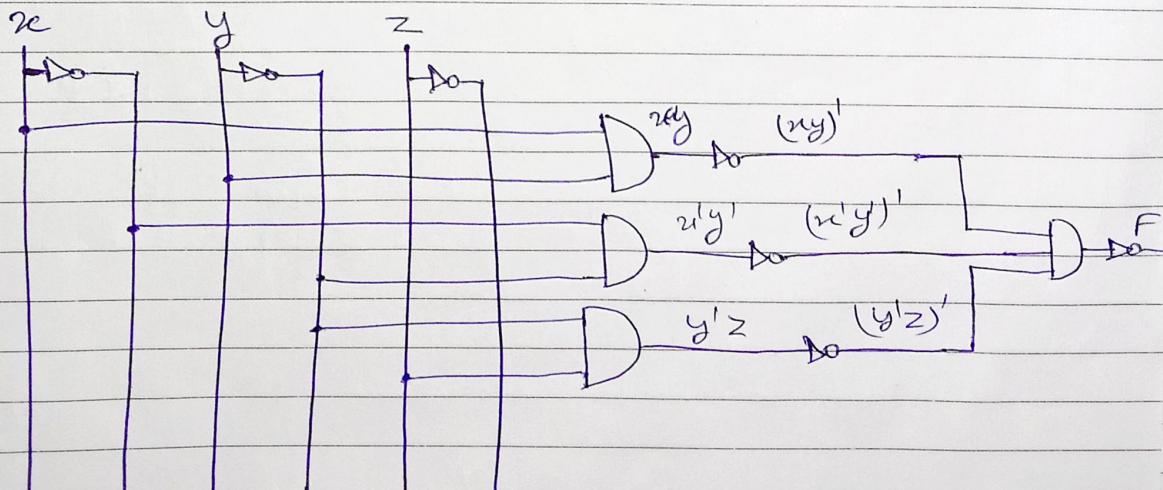
(a) Implement it with only OR & NOT gates.

$$F = xy + x'y' + y'z = (x + y')' + (x + y) + (y + z')$$



(b) Implement it with only AND & NOT gates.

$$F = xy + x'y' + y'z = [(xy)(x'y')'(y'z)']'$$



Q2 Given following Boolean function in product of
Maxterms.

$$F(x, y, z) = (xy + z)(y + xz)$$

Solⁿ $F(x, y, z) = (xy + z)(y + xz)$

x	y	z	$(xy + z)$	$(y + xz)$	F
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	0	1	0
0	1	1	1	1	1
1	0	0	0	0	0
1	0	1	1	1	1
1	1	0	1	1	1
1	1	1	1	1	1

$$\text{SOP } F = \bar{x}\bar{y}z + \bar{x}y\bar{z} + xy\bar{z}' + xyz$$

$$= \Sigma(3, 5, 6, 7)$$

$$\text{POS } F = \pi(0, 1, 2, 4)$$

Q.31 Explain briefly : SOP & POS , minterm and maxterm , canonical form, (OS) propagation delay , fan out.

Sol. SOP : Sum of Product

SOP form is a method of simplifying the Boolean expression of logic gates. In this SOP form of Boolean function representation, the variables are operated by AND (product) to form a product term are ORed (summed) together to get the final function.

It form can be formed by adding two or more product terms using a boolean addition operation. sum term is defined by using OR operation.

It forms is also called as Disjunction Normal form .

$$\text{Ex- } AB + ABC + CDE \\ (A'D')' + ABC + CDE'$$

→ POS: Product of Sum

It is a method of simplifying the boolean expressions of logic gates. In this, all the variables are ORed, i.e. written as sums to form sum terms.

All the sum terms are ANDed (multiplied) together to get the product of sum form.

This is exactly opposite to SOP form. So, it can also be said as "Dual of SOP form".

$$\text{Ex: } (A+B)^* * (A+B+C)^* * (C+D)$$

$$\text{Ex: } (A+B)' * (C+D+E')$$

→ Min Terms:

It is defined as the product term of n variables in which each of the n variables will appear once either in its complemented or un-complemented form. It is denoted as m_i where i is in the range of $0 \leq i \leq 2^n$.

If variable is complemented form, if its value is assigned to 0, and the variable is uncomplimented form

→ for 2-variables (x & y)

the possible minterms ~~are~~ are: $\bar{x}\bar{y}$, $\bar{x}y$, $x\bar{y}$, xy .

→ for 3-variables (x , y & z)

minterms are: $\bar{x}\bar{y}\bar{z}$, $\bar{x}\bar{y}z$, $\bar{x}y\bar{z}$, $\bar{x}yz$, $x\bar{y}\bar{z}$, $x\bar{y}z$, $xy\bar{z}$, xyz .

$F(\text{list of variables}) = \Sigma(\text{list of 1-min term indices})$

$$\text{Ex: } F(x,y,z) = \Sigma(3,5,6,7)$$

→ Inverse of the F is

$$F'(x,y,z) = \Sigma(0,1,2,4)$$

→ Max Terms:

Max term is defined as the product of n variables, within the range of $0 \leq i < 2^n$. The max term is denoted as m_i .
In max term, each variable is complimented.

→ $x+y, x'y, x'y' \& x'y' \rightarrow 2\text{-variable}$

→ $x+y+z, x+y+z', x+y'+z, x+y'+z', x+y+z'', x+y+z', x'+y+z', x'+y'+z', x'+y'+z'' \rightarrow 3\text{-variable}$

→ $F(\text{list of variables}) = \Pi(\text{list of 0 - max term indices})$

$$\text{Ex: } F(x,y,z) = \Pi(0,1,2,4)$$

Inverse is,

$F' = \Sigma(\text{list of 1 - manterm indices.})$

$$\text{Ex: } F'(x,y,z) = \Sigma(3,5,6,7)$$

→ Canonical Form:

- Q. → A representation that helps to describe Boolean outputs of digital circuits using Boolean functions.
- Divides into canonical SOP form and Canonical POS form.
- It is more complex
- propagation delay:

Propagation delay is defined as the amount of time required after an input signal is applied and has stabilized to the input of a circuit to the time that the output of the circuit has stabilized to the correct output signal.

→ Fan out:

It is a term that defines the maximum number of digital inputs of a single logic gate can feed. Most Transistor-transistor logic (TTL) gates can feed up to other digital gates or devices.

Thus, a typical TTL gate has a function: fan out of 10.

Q. 4)

Soln)

Q-4] What is the principle of Duality Theorem?

Soln] The principle of duality in boolean algebra states that if you have a true boolean statement (equation) then the dual of this statement is true.

The dual of this statement is true.

The dual of a boolean statement is formed by replacing the statement's symbols with their statement's symbols with their counter parts. This means

a "0" becomes a "1".

"1" becomes a "0"

"+" becomes a "

"." becomes a "+".

→ principle in boolean algebra:

$$(*) 1 + 0 = 1 \leftarrow \text{boolean statement}$$

$$(**) 0 \cdot 1 = 0 \leftarrow \text{dual statement}$$

→ The dual of the true Boolean statement (*) is (**).

We found (**) by replacing each symbol from (*) with its boolean counter part as described above, (**) is also true boolean statement.

→ The key takeaway from this principle is there is nothing intrinsically special about our denotation of "0" and "1".

Q.5. Explain briefly : standard SOP and POS forms

→ Standard SOP

A standard SOP expression is one in which all the variables in the domain appear in each product item in the expression.

$$\text{Ex: } \bar{A}\bar{B}CD + A\bar{B}\bar{C}\bar{D} + AB\bar{C}\bar{D}$$

→ It is important in:

- ⇒ Constructing truth tables.
- ⇒ The Karnaugh map simplification method.

→ Standard POS form:

A standard POS form expression is one in which all the variables in the domain appear in each sum term in the expression.

$$\text{Ex. } \Rightarrow (\bar{A} + \bar{B} + \bar{C} + \bar{D})(A + \bar{B} + C + D)$$

$$(A + B + \bar{C} + D)$$

It's expressions are important in:

- ⇒ Constructing truth tables.
- ⇒ The Karnaugh map simplification method.

Q.8) Reduce the expression:

$$(a) A + B(A'C + (B + C')D)$$

$$= A + B(A'C + BD + C'D)$$

$$= AAC + ABD + AC'D + BAC + BBD + BC'D$$

$$= AC + ABD + AC'D + ABC + BD + BC'D$$

$$= AC(B + C')(D + D') + ABD(C + C') + AC'D(B' + B) + ABC(D + D') +$$

$$BD(C + C')(A + A') + BC'D(A + A')$$

$$= ACBD + ACB'D + ACB'D + ACB'D' + ABDC + ABDC' +$$

$$AC'DB' + AC'DB + ABCD + ABCD' + BDCA + BDCA' +$$

$$BDC'A + BDC'A' + BC'DA + BC'DA'$$

$$(b) (A + (BC))' (AB' + ABC)$$

$$(A + B + C')' (AB' + ABC)$$

$$(A' B C)(AB' + ABC)$$

$$A' A B B' C + A' A B B C C$$

$$(O)(O)C + (O)(B)(C)$$

$$O + O$$

$$O$$

Q9] Define: Integrated Circuit and briefly explain SSI, MSI, LSI and VLSI

Sol] SSI (Small-Scale Integration)

An integration type for digital circuits that contain transistors numbering in the tens providing a few logic gates per chip

MSI (medium-Scale Integration)

It is a process of embedding hundreds of transistors in one integrated circuit or microchip.

LSI (large-Scale Integration)

It is the process of integrating thousands of transistors on a single silicon semiconductor microchip.

VLSI (Very Large-Scale Integration)

It is the process of creating an integrated circuit by recombining thousands of transistors into a single chip.

Q-6 What are Minterms and Minterms?

Soln Minterms:

A minterm is a product term in boolean function in which every element is present in either in normal or in complemented form.

for eg, if $f(a,b,c)$ is a boolean function then the possible minterms would be $abc, ab'd, ab'c, ab'c', a'b'c, a'b'c'$, that is for n variable boolean function there would be 2^n possible minterms

They are used for sum of product (SOP) canonical forms, which is also called disjunctive normal form (DNF). The value correspond to 1 or true is selected as minterm

Minterms:

A maxterm is a sum term in boolean function in which every element is present in either in normal or in complemented form

For eg. if $f(a,b,c)$ is a boolean function then the possible minterms would be $(a+b+c), (a+b+c'), (a+b'+c), (a+b'+c'), (a'+b+c), (a'+b'+c)$, that is

for a n variable boolean function there would be 2^n possible maxterms.

They are used for product of sum (POS) - canonical forms, which is also called conjunctive normal form (CNF). The value correspond to 0 or false is selected as maxterm.

Q-7) Define: Noise margin, Propogation delay.

Solⁿ). Noise Margin:

The noise margin is the amount of noise that could be added to a worst-case output such that the signal can still be interpreted as a valid input.

They are generally defined so that positive values ensure proper operation, and negative margins result in compromised operation, or outright failure.

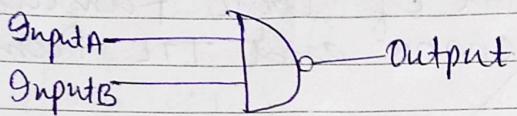
Propogation delay.

Propagation delay is the length of time taken for a signal to reach its destination. It can relate to networking, electronics or physics.

It is defined as the flight time of packets over the transmission link and is limited by the speed of light.

Q10) Draw the logic symbol and construct the truth table for each of the following.

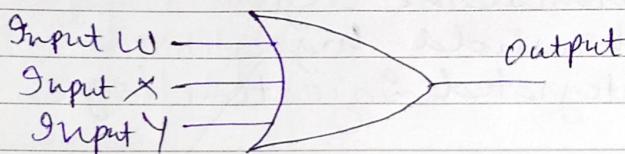
[1] Two-input NAND gate



Truth Table

A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

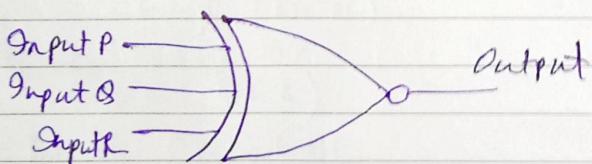
[2] Three-input OR gate



Truth Table

w	x	y	Output
0	0	0	0
0	0	1	1
0	1	1	1
0	1	0	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

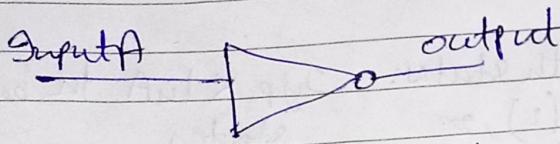
[3] Three-input Ex-NOR gate



Truth Table

P	Q	R	Output
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

(H) NOR Gate

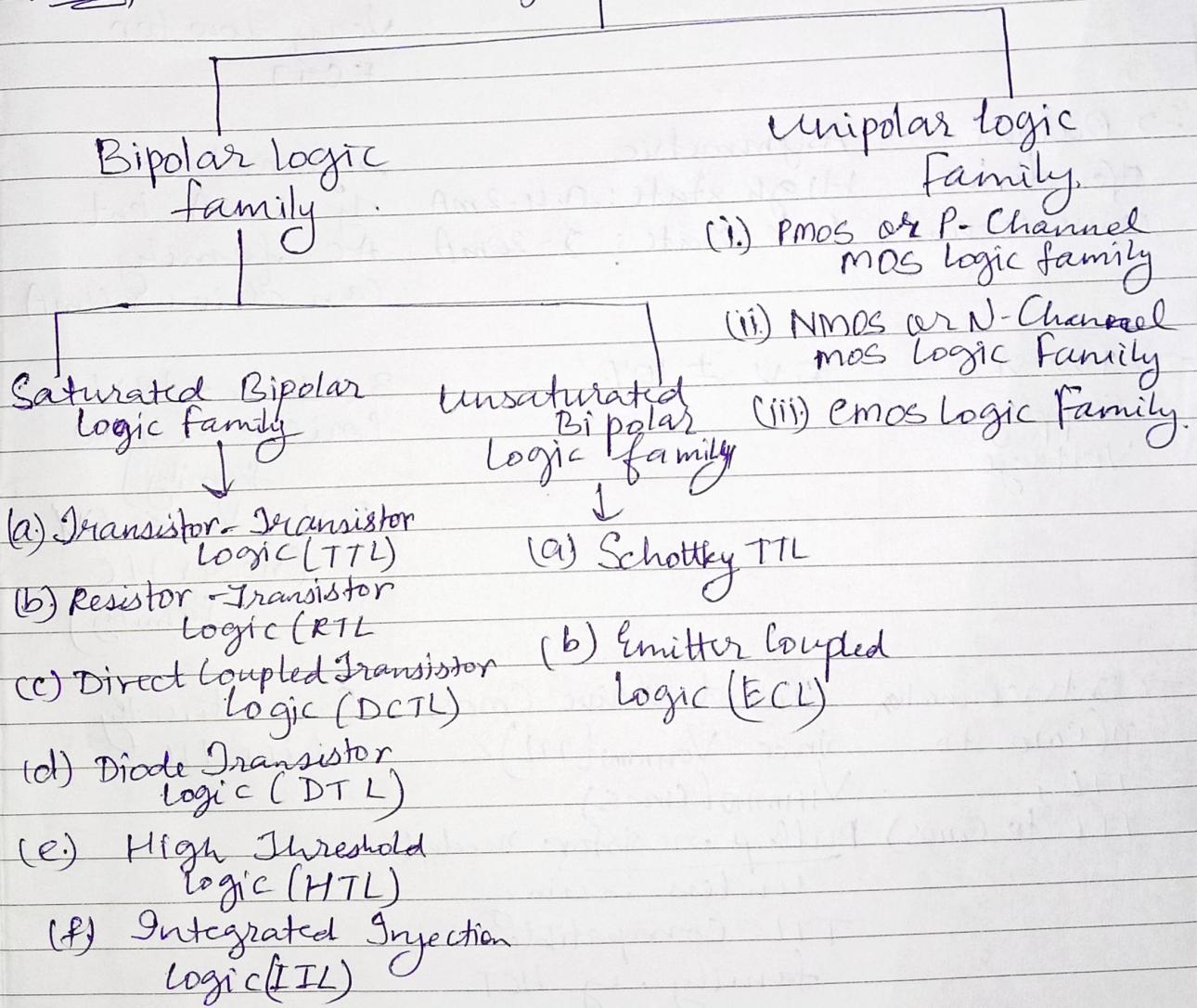


A	Output
0	1
1	0
0	1

(I) Give Classification of logic Families and Compare CMOS and TTL families.

Sol)

Logic families



	TTL	CMOS
→ Noise Margins	0.3 (high), 0.5 (low)	0.3 V _{CC}
→ Input Source Currents	High in both states: 0.2 to 2 mA (L), 20-50 nA (H)	I _{typ} < 1 nA in both states
→ Power Consumption	Relatively high, fixed. 2 mW for 74LS, 20 mW for 74Snn.	Depends on V _{CC} frequently Negligible static dissipation. Very low for FCTT
→ Output drive current	Asymmetric. High state: 0.4-2 mA Low state: 8-20 mA	Symmetric. I _Y 4 mA but AC family can drive 24 mA
→ Power Supply Voltage	5 V ± 10%	3 V ≤ V _{CC} ≤ 18 V (original 4000 family) 2 V ≤ V _{CC} ≤ 6 V (newer H C family)
→ Interconnection n(Cmos to TTL, TTL to Cmos)	Cannot drive Cmos since V _{OHMIN} (TTL) < V _{IHMIN} (Cmos)	Can directly drive TTL <u>Pullup resistor needed</u> unless using TTL compatible family e.g. HCT.

Q-12) Demonstrate by means of truth tables the validity of the following Theorems of Boolean algebra.

- (i) De Morgan's theorems for three variables
 - (ii) The distributive law of + over .

Solⁿ] (1) De Morgan's theorem for three variables

$$(xyz)' = x' + y' + z'$$

x	y	z	xyz	$(xyz)'$	x'	y'	z'	$x' + y' + z'$
0	0	0	0	1	1	1	1	1
0	0	1	0	1	1	1	0	1
0	1	0	0	1	0	1	1	1
0	1	1	0	1	1	0	0	1
1	0	0	0	1	0	1	1	1
1	0	1	0	1	0	1	0	1
1	1	0	0	1	0	0	1	1
1	1	1	1	0	0	0	0	0

(2) The distributive law of + over

$$x+yz = xy(x+y)(x+z)$$

x	y	z	yz	$x+y+z$	$x+y$	$x+z$	$(x+y)(x+z)$
0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0
0	1	0	0	0	1	0	0
0	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1
1	0	1	0	1	1	1	1
1	1	0	0	1	1	1	1
1	0	1	1	1	1	1	1
1	1	1	1	3	2	2	2

Q-13) Express the following functions in sum of min terms and product of max terms.

$$(a) F(A, B, C, D) = D(A' + B) + B'D$$

$$= A'D + BD + B'D$$

$$= A'D(B' + B) + BD(A' + A) + B'D(A' + A)$$

$$= A'DB' + A'DB + BDA' + BDA + B'DA' + B'DA$$

$$= A'B'D + A'BD + A'BD + ABD + A'B'D + ABD$$

$$= m_1 + m_3 + m_5 + m_7 + m_1 + m_5$$

$$\text{Min Term} = \sum_m (1, 3, 5, 7)$$

$$\text{Max Term} = \prod_m (0, 2, 6)$$

$$(b) F(A, B, C) = (A' + B)(\cancel{B'C}) (B' + C)$$

$$= A'B' + A'C + BB' + BC$$

$$= A'B'(C' + C) + A'C(B' + B) + BB'$$

$$BB'(A' + A)(C' + C) + BC(A' + A)$$

$$= A'B'C' + A'B'C + A'C'B' + A'C'B + (BB'A + BB'A)(C' + C) + BCA' + BCA$$

$$= A'B'C' + A'B'C + A'C'B' + A'C'B + BB'AC + BB'AC + BCA' + BCA$$

$$= A'B'C' + A'B'C + A'C'B' + A'C'B + \cancel{BB'AC} + BAC + BCA' + BCA$$

$$= m_0 + m_1 + m_2 + m_3 + 0 + 0 + m_4 + m_5 + m_6$$

$$\text{min term} = \sum_m (0, 1, 3, 7)$$

$$\text{max term} = \prod_m (2, 4, 5, 6)$$

$$(c) F(n, y, z) = 1$$

$$= (n+n') (y+y') (z+z')$$