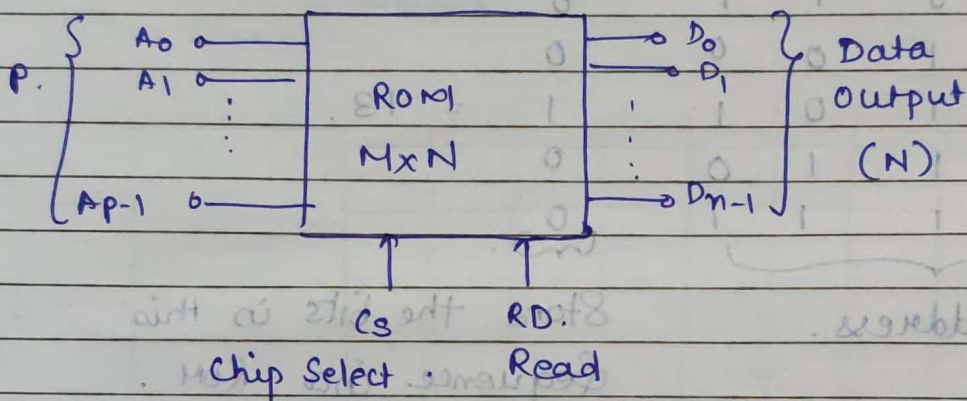


ROM:- Read Only Memory

- It is Used as Memory
- preprogrammed only once during Manufacturing
- Size of ROMs = $M \times N$.
 - M = No. of Location
 - N = Bit used.
 - P = No. of address lines for M locations.

→ Total No. of Location $M = 2^P$



Q Draw Logic diagram of circuit Using 16×1 ROM.

16×1 ROM. $M = 16$

? $N = 1$

$$2^4 = 16$$

$$2^4 = 16$$

Input = 4. i.e. A_0, A_1, A_2, A_3 ← address lines.
Thus $p = 4$.

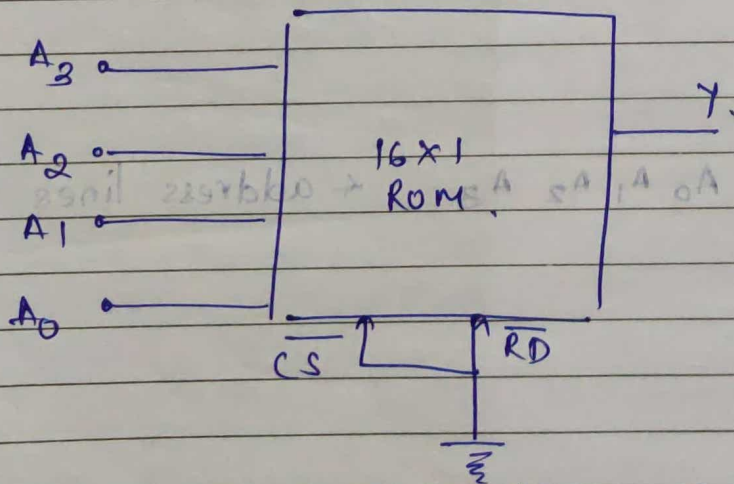
ROM: Read Only Memory

A_3	A_2	A_1	A_0	O/P.
0	0	0	0	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

address.

Store the bits in this sequence into ROM.

$$ROM\ Y = \sum_m (0, 3, 4, 5, 8, 9, 10, 13)$$



Classification of ROM.

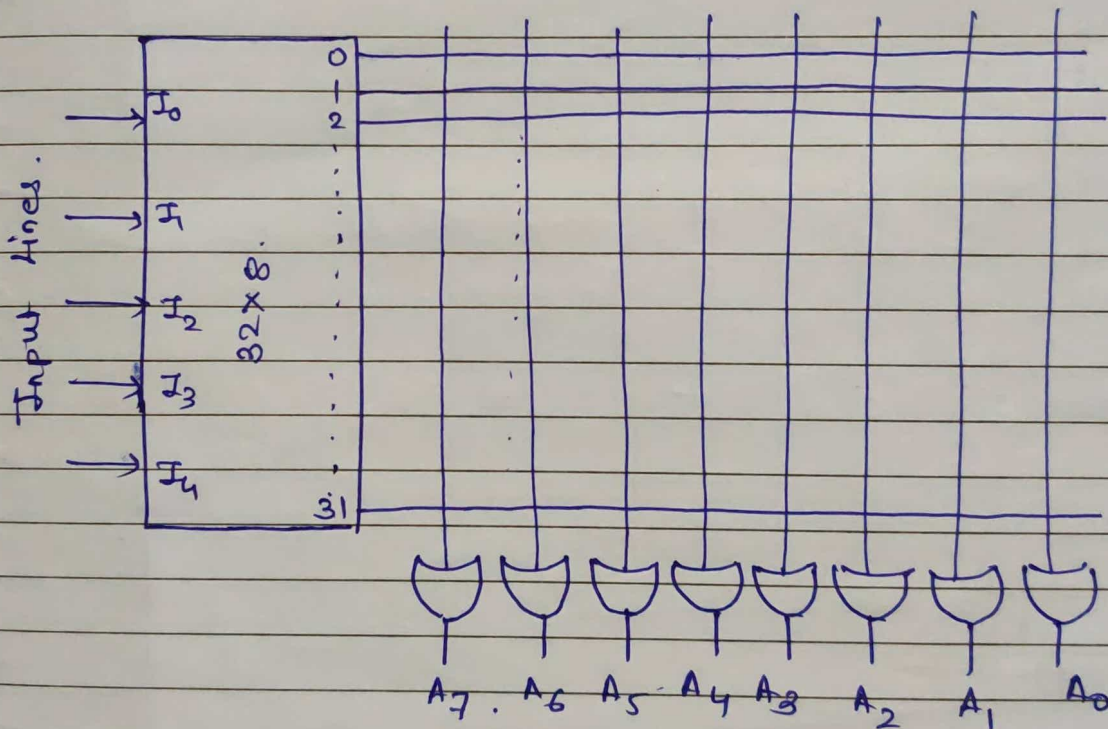
- ROM
- PROM
- EPROM
- UV EPROM.
- E^2 PROM.

PROM.

— Programmable ROM.

- Programmed Only once after fabrication.
- No data is stored into them.

32x8 ROM.



?

$$2 = 32,$$

$$2^5 = 32,$$

Input lines $P = 5$ address lines.

- Each 32 lines are connected to each 8 OR gate.
- Thus OR gate has 32 input.

Classification of ROM

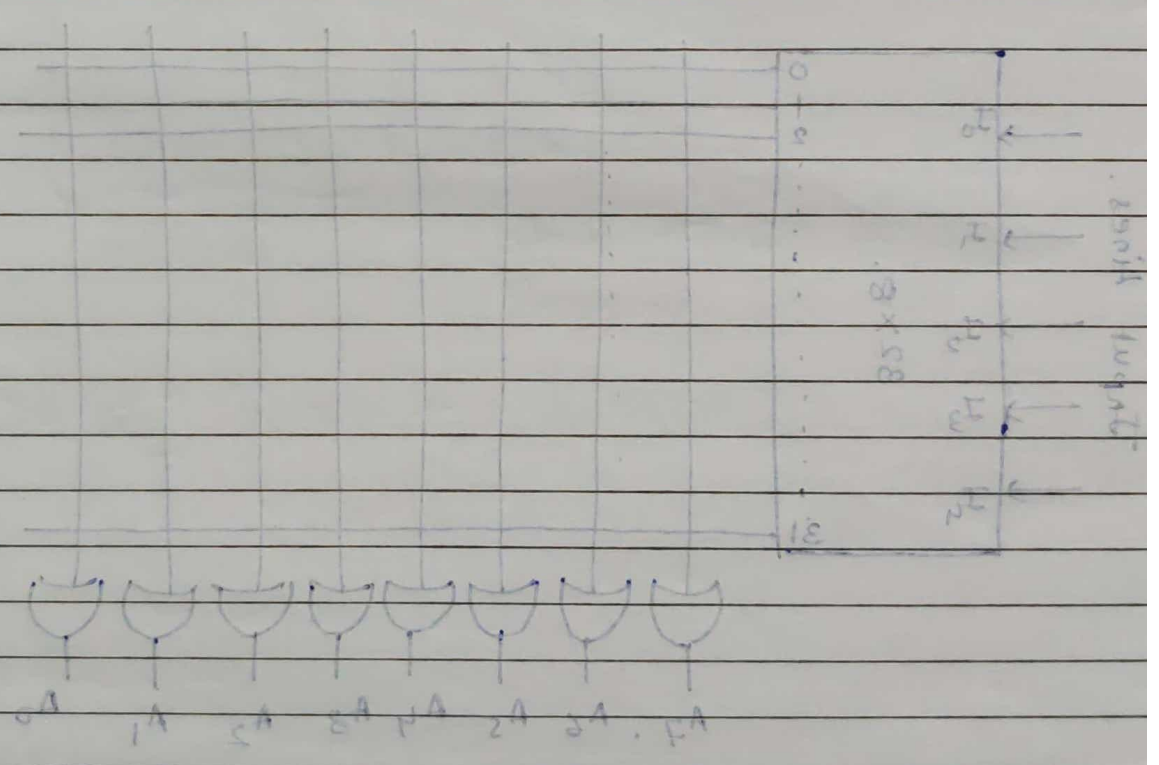
→ $32 \times 8 = 256$ Internal Connections.

- ROM
- PROM
- EPROM

— Programmable ROM

— Perma programmed Only once after fabrication.
→ No data is stored in them.

32×8 ROM



$$2^5 = 32$$

$$2^5 = 32$$

Input lines $8 = 2^3$ address lines

→ each 32 lines are connected to each 8 or data.
Then OR gate has 32 input.

Types of PLD. Unit 6 Programmable Logic Device.

PLA.

↳ Programmable Logic array.

↳ Limited or finite number of functions can be Implemented.

↳ AND array = programmable
OR array = programming.

INPUT

Programmable
AND array

Programmable
OR array

OUTPUT.

↳ Slower Speed.

↳ High Complex.

↳ High Cost.

↳ less Used.

↳ Programmable array logic.

↳ Massive number of functions can be Implemented.

↳ AND array = programmable.
OR array = Fixed.

INPUT

Programmable
AND array

Fixed OR
Array

OUTPUT.

↳ Speed is Higher

↳ less Complex

↳ low cost.

↳ Highly Used.

PLD: Programmable Logic Device.

→ It has Replaced all Small Scale IC's like multiplexer, De-mux etc.

→ It looks like small box and many programmable switches as well as logic gates.

→ Classification of PLD.

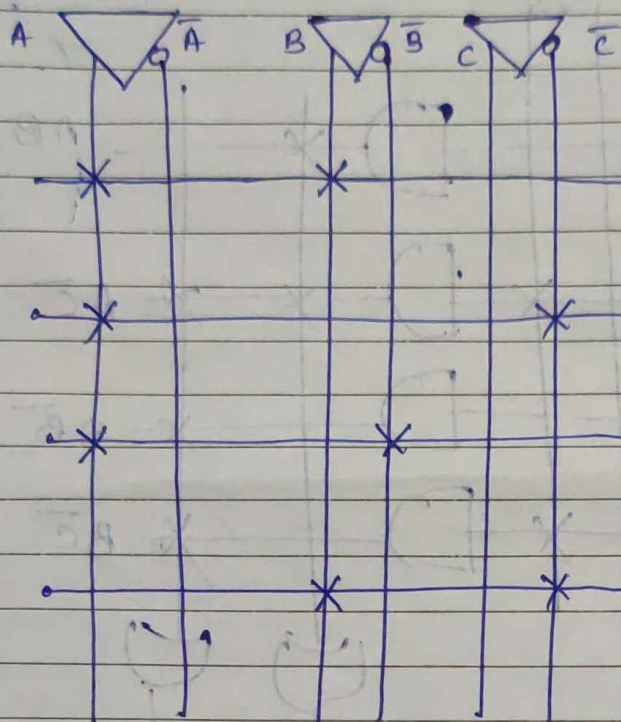
PLA PAL CPLD FPGA ROM

Advantage of PLD.

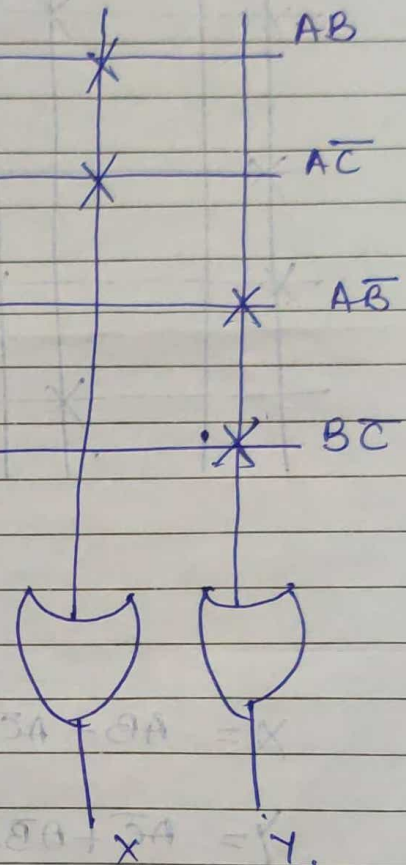
- Require less space.
- less power to operate.
- High Speed.
- High Security.
- Re-programmable.
- Flexible to design.
- Low cost.

PAL.

AND Array.



OR Array.



$$X = AB + A\bar{C}$$

$$Y = \bar{A}B + BC$$

O/p.



$$5A + 9A = X$$

$$\overline{AB} + \overline{BA} = Y$$