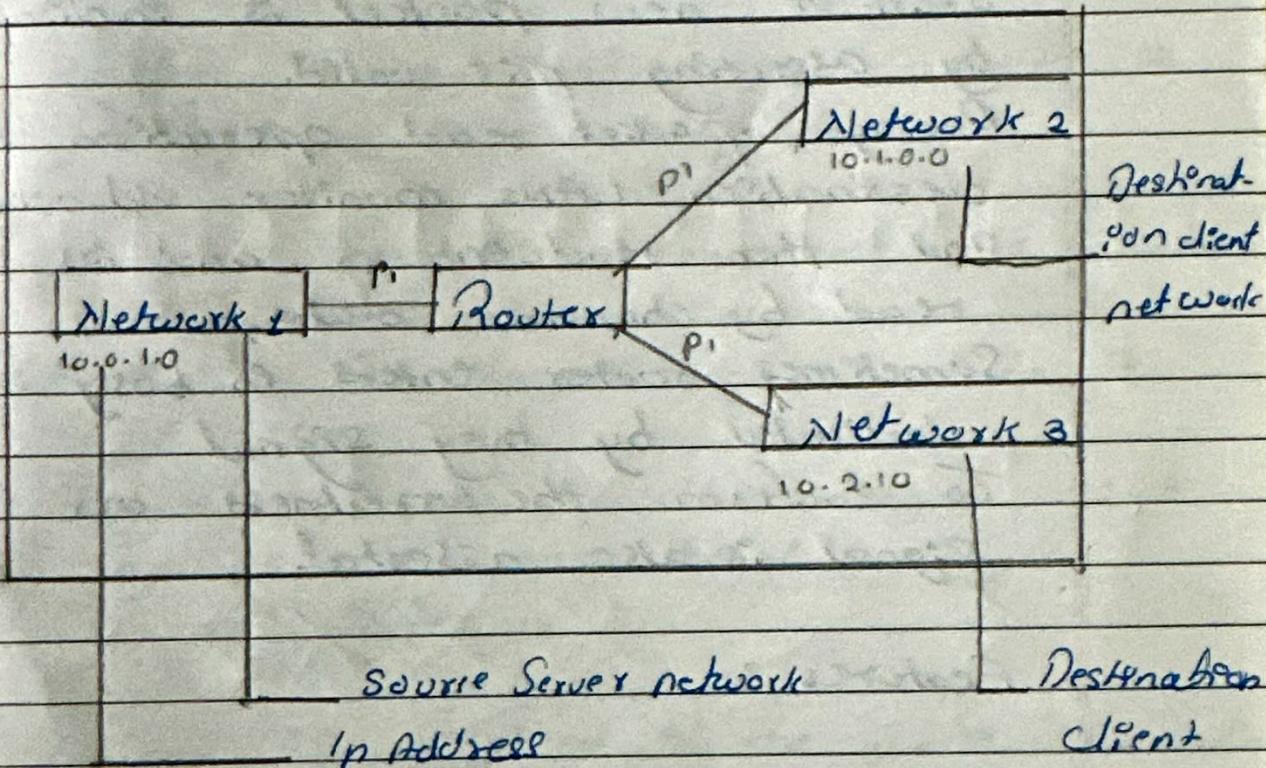


Sahil AranHalle

Router 1x3 Verification.

* Introduction

Router is a device that forwards data packets between computer networks. It is an OSI model layer 3 routing device. It drives an incoming packet to an output channel based on the address field contained in packet headers.



Top level Block	clock →	Router 1x3	→ data-out-0
	resetn →		→ data-out-1
	read-enb-0 →		→ data-out-2
	read-enb-1 →		→ valid-out-0
	read-enb-2 →		→ valid-out-1
	data-in →		→ valid-out-2
	pkt.valid →		→ err
			→ busy

* Router Specifications.

Router consists of modules such as FSM, Synchronizer, Register and 3 FIFO to route the packet.

Router receives the network packet from a source LAN using data-in on byte to byte basis.

Start of new packet is indicated by asserting pkt valid.

During packet read operation the destination LANs monitor vld_out_x and then read_enb_x, and is read by channel data_out_x.

Sometimes router enters in busy state indicated by busy signal. To confirm the correctness err signal is also asserted.

Features :-

Packet Routing :- Packet routed from the input port and is routed to any one output port.

Parity checking :- Error detection technique that checks integrity of digital data.

Reset :- It is an active low synchronous input that resets the router.

Sending Packet :- Router input protocol

Reading Packet :- Router output protocol.

Packet Routing

Packet consist of 3 parts Header, Payload, Parity such that each id of 8 bits.

Header The packet header consists 2 fields DA and length.

DA :- Destination address of the packet is of 2 bits.

length :- The length of the date is 6 bits.

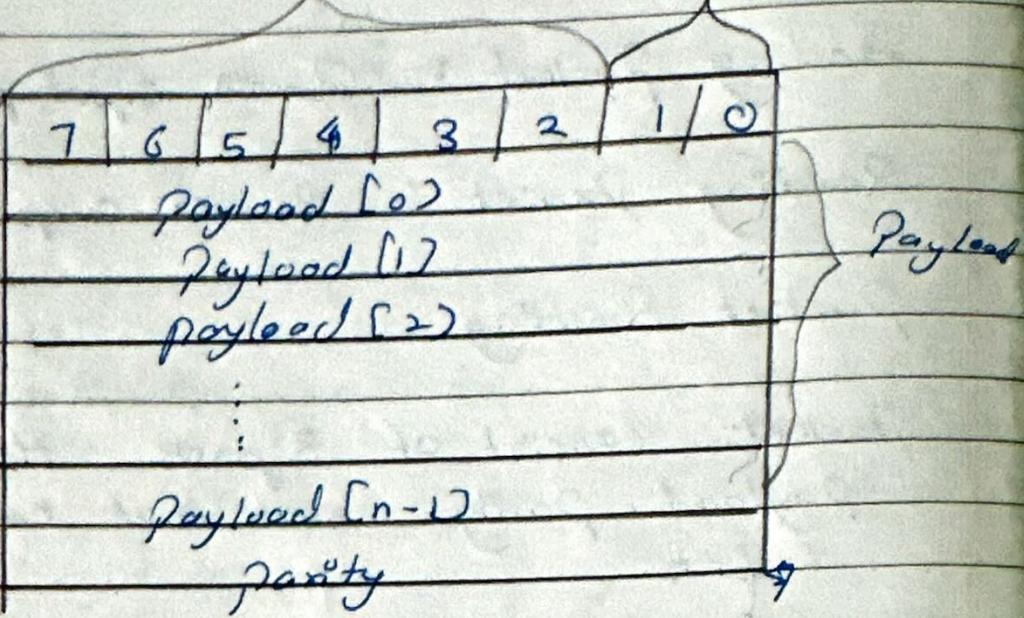
length 1 means data length 1 byte.
length 63 means the data length 63 bytes.

Payload :- Payload is the data information.

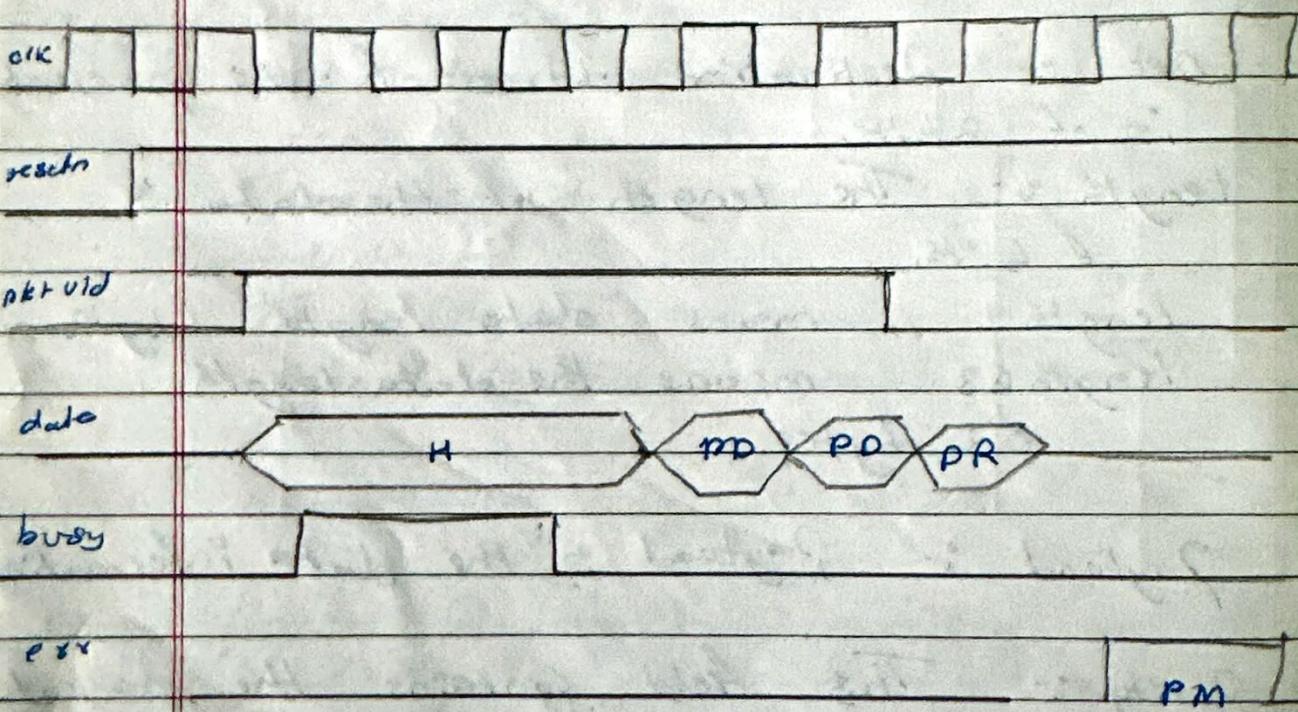
Parity :- This field contains the packet

Payload
length

Address



* Router Input Protocol



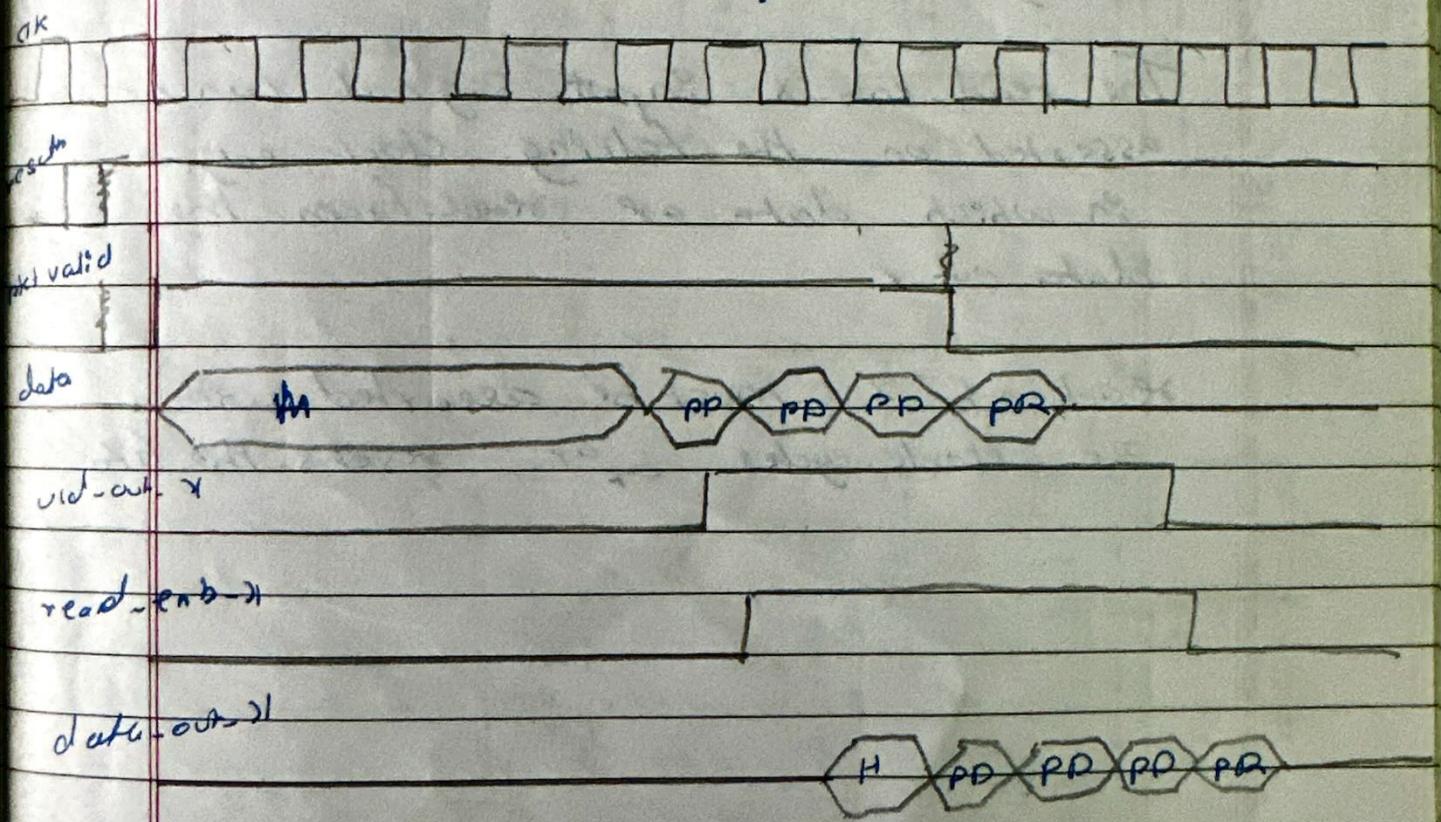
- All input signals are active high except active low reset and are synchronized to the falling edge of the clock.

Packet valid signal is asserted on the same clk edge when the header byte is driven onto the input bus.

Each subsequent byte of the payload after the header byte should be driven on the input data bus.

After last payload byte is driven,
the packet valid signal must be deaddressed and packet parity should be driven.

* Router output protocol.



All output signals are active high and are synchronized to the rising edge of the clock.

Each output port data-out_x is internally buffered by a FIFO.

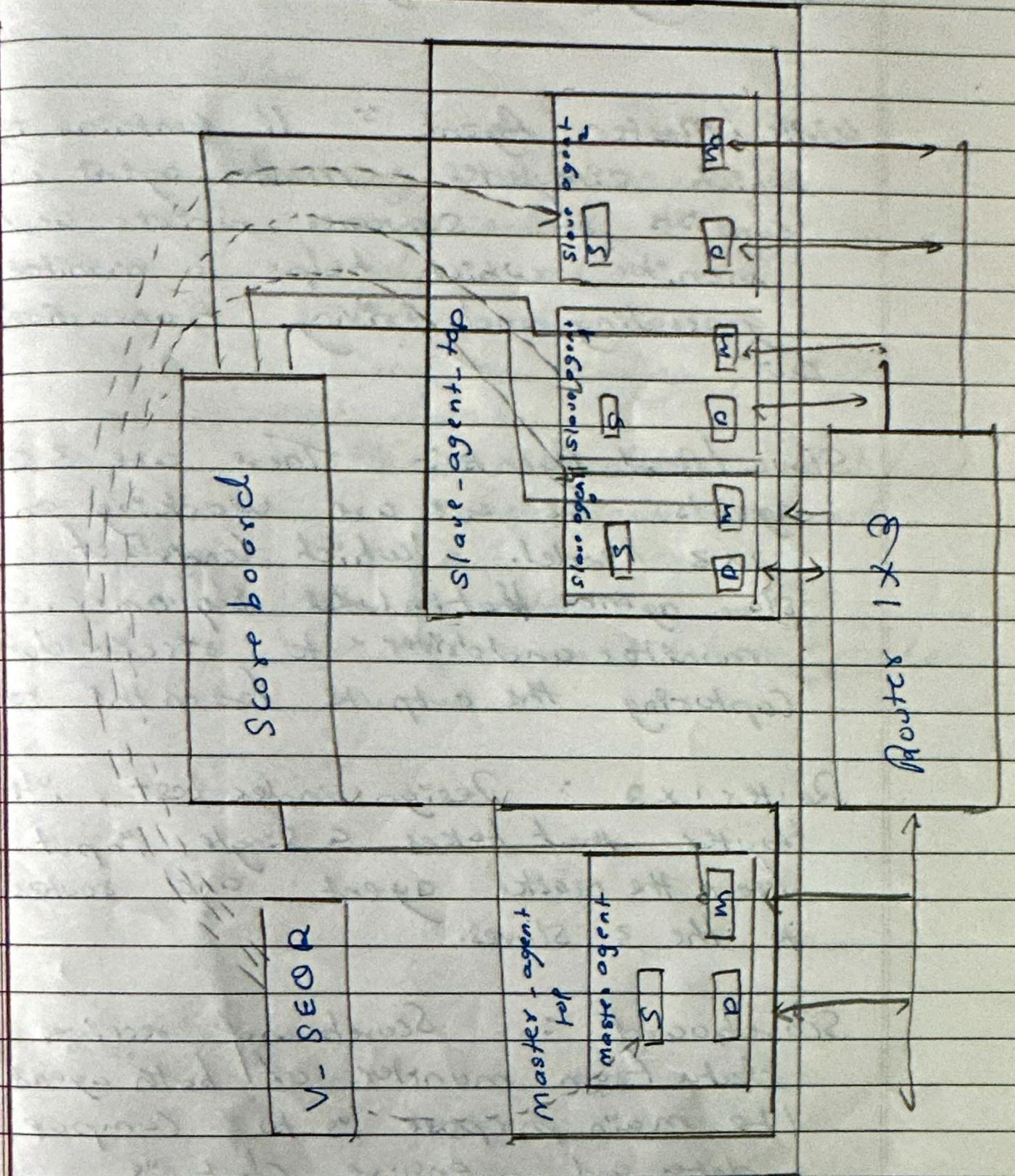
The douter asserts the vid-out_x signal when valid data appears on the vid-out_x output bus.

The packet receiver will then wait until it has enough space to hold the bytes of the packet.

The read-enb_x input signal can be asserted on the falling clock edge in which data are read from the data-out_x .

read-enb_x must be asserted within 30 clock cycles or resets the Atc

* TB Architecture.



The architecture consists of various main components working together to simulate and verify the design.

Write / Master Agent :- It contains top which simulates master agent which consists of sequences, drives and monitor, which helps in monitoring, generating and driving transactions to DUT.

Slave / Read Agents :- There are 3 Slave agents as we are working on 1×3 Model. which consists of slave agent that includes sequencer, monitors and driver to receive data capturing the outputs from the drivers.

Router 1×3 : Design under test, its a router that takes a single input from the master agent and routes it to the 3 slaves.

Scoreboard :- Scoreboard receives data from monitor of both agent. Its main purpose is to compare data and ensure that it's functioning correctly.

Virtual Sequence : It controls master & slave sequences. Generating test stimuli to load to master agent.

* Router Interface

clock - Active high clocking event

pkt valid - Detects arrival of new packet.

resetn - Low synchronous reset

data in - 8 bit Input bus.

read_enb_x - Signal for reading packet through output data bus.

vld_out_y - Signal that detects valid high # availability for destination network.

data out - 8 bit output bus

busy - Detects busy state.

error - Detects mismatch between packet parity.