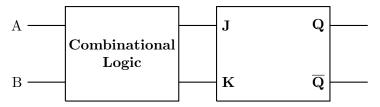
## Assignment 12

## ESC 201

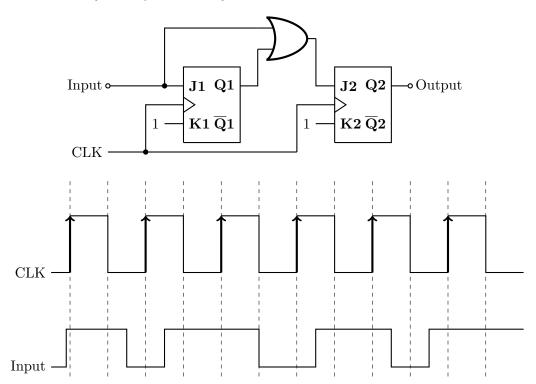
## Basic

1. Give a circuit realization of the combinatorial logic block shown below to obtain the following truth table. Use any 2-input gates.

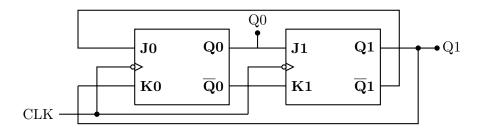
A	В	Q
0	0	$\overline{\mathrm{Q}}_n$
0	1	1
1	0	$Q_n$
1	1	0



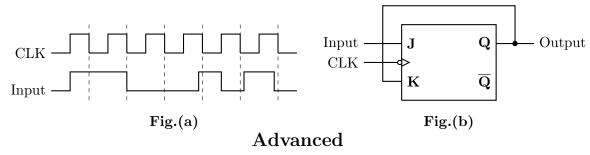
2. Write the characteristic tale of JK flip flop. The input waveform is shown below for the given circuit containing J-K flip flop. Draw the corresponding output waveform. Assume that all devices have no delay and  $\mathbf{Q2}$ =0 initially.



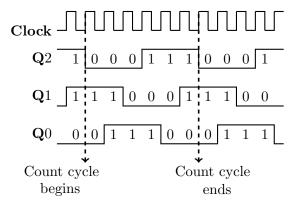
3. If initially Q0 = Q1 = 0, find the logic states of Q0 and Q1 immediately after 777<sup>th</sup> clock pulse.



4. The waveform of the clock as shown in **Fig.(a)** excites the circuit shown in **Fig.(b)**. Sketch the output waveform.



- 5. A sequential circuit has two JK flip-flops with outputs  $Q_1$ ,  $Q_2$  and one input X. The circuit is described by the following flip-flop input equations:  $J_1 = J_2 = X$ ,  $K_1 = \overline{Q}_2$  and  $K_2 = Q_1$ . Derive the next state equations for the circuit and draw the state transition table.
- 6. A sequential circuit contains two flip-flops  $T_1$  and  $T_2$ . The circuit has no external inputs. The only external outputs are the values of current state  $(Q_1 \text{ and } Q_2)$ . The flip-flop inputs are connected as:  $T_1 = Q_1 + Q_2$  and  $T_2 = \overline{Q}_1 + Q_2$ . What function does the circuit perform?
- 7. Design a sequential circuit with two D flip-flops A and B and one input x such that when x=0, the state of the circuit remains the same. When x=1, the circuit goes through the state transitions from 00 to 01, to 11, to 10 and back to 00, and repeats.
- 8. Design a synchronous counter with three positive edge triggered JK flip flops using K-maps for the three pair of iputs  $J_2$   $K_2$ ;  $J_1$   $K_1$  and  $J_0$   $K_0$  to produce three phase waveforms at the output of the three flip flops Q2, Q1 and Q0 respectively as shown. (States which do not arise should be treated as 'dont care' conditions).



9. Design a 3- bit synchronous counter which counts 0,3,6,1,4,7,2,5,0,3,.... using **JK** flip flops.