Assignment 13: MOSFET as a switch

(Solutions will be provided on 16th Nov.)

1. This problem is concerned with the design of a MOSFET switch which must satisfy a prescribed static discipline. The transistor has the following characteristics:

   On resistance: 100 to 500 ohms

   Threshold voltage: 1.8 to 2.6 V

   (These ranges reflect the normal manufacturing variances for a specific FET type)

The available voltage is 5V. For reasons of switching speed, the resistance RL between the drain and the power supply may not exceed 10k ohms. The static discipline is:

V_{OH} = 4.5 V V_{IH} = 3V

V_{IL} = 1.5 V V_{OL} 0.5 V

(a) What are the permissible ranges for RL that satisfy the static discipline

Sol: We use the switch-resistor model (SR) model:
MOSFET OFF => Vout = 5V (ok)
MOSFET ON => $V_{out} = {R_{ON}}/{(R_{ON} + R_L)} \times 5$ V which should be at least 0.5 (=V_{OL})
When R_{ON} is small and R_L is large, V_{out} will be small. So the worst case for V_{out} occurs when: R_{ON} is large and R_L is small. Since R_{ON} < 500, R_L should be at least 4.5 kohms or else V_{out} could exceed 0.5 V. Upper limit is of course 10k.

(b) What is the noise margin for a low input

Sol: The usual definition is simply 1.5-0.5 = 1V

Clarification: We can choose R_L according to our needs
However, we cannot choose R_{ON} or V_T. For such problems you must design R_L taking into account the worst possible values of R_{ON} and V_T. Imagine an adversary sitting inside the transistor trying to set the values of these parameter (R_{ON} and V_T) to ruin your day.

However, given the MOSFET specifications, the actual noise margin is higher. So let us choose R_L to be as large as possible (to ensure a small V_{out}). As before, the worst case R_{ON} value is 500 ohms so that Vout is at most $= 5\left({500}/{500 + 10000}\right) = 0.24$ (it will be smaller for larger values of R_{ON} but we cannot be wishful).

From the perspective of choosing RL, this is the lowest Vout (since we want a low Vout)
From the perspective of transistor, this is the highest Vout (the adversary inside the transistor will test all values of RON will come to this conclusion).

Similarly, a low input is guaranteed as long as $V_{GS} < V_T$, so the MOSFET switch will continue to work so long as the input voltage is less than 1.8 V. (worst value of V_T). Again, it could be higher for higher V_T but we cannot be too optimistic.

Now consider a communication channel: The MOSFET at the transmitter will produce a "low" voltage of 0.24 V in when ON. Add noise to it, and we can still have the MOSFET at the receiver end interpret the received voltage of 1.8 V as "low." So the noise margin is actually 1.8-0.24 = 1.56 V. Note that such calculations can only be done when V_T, R_L and R_{ON} are given.

(c) What is the noise margin for a high input

Sol: Again, the usual definition is 4.5-3 = 1.5V. But all input voltages higher than 2.6 V are always interpreted as "high". Similarly, the MOSFET always provides 5V at the output since R_{OFF} is infinite.
So a "high" voltage of 5V produced at the output can decay all the way up to 2.6 V and still be interpreted as "high" The noise margin is therefore: 5-2.6 = 2.4V

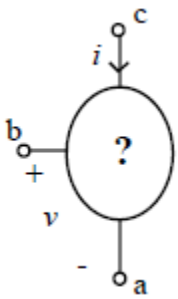
(d) Assume that n of these transistors are used to create a multiple-input NAND gate. What is the value of RL that maximizes *n*?

Sol: Recall the multi-input NAND gate circuit. Suppose the output is "low" which happens all inputs are "high." In this case, all the n MOSFETs will be ON, resulting in a series resistance of n x R_{ON}. So we have that $V_{out} = {nR_{ON}}/{(nR_{ON} + R_L)} \times 5$ V which should be at most 0.5 V to ensure static discipline. Clearly, we need the largest possible value of RL to ensure that V_{out} remains below 0.5. So RL should be 10k.

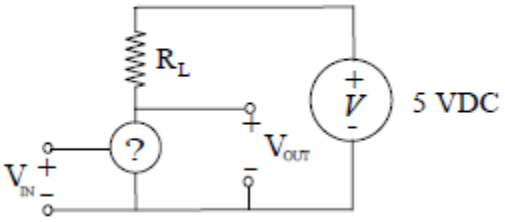
(e) What is the largest value of *n*?

Sol: So let us say that RL = 10k. Then for the worst case value of R_{ON}, we can only have n=2 (in which case V_{out} = 0.45 V). Note that a higher value of n may be realizable in practice if R_{ON} can be measured. But as a designer, one must always assume the worst case values.

2. A three terminal device shown has the characteristics indicated: when *v* is less than 3V, terminal c is connected to terminal a. When *v* is greater than 4 V, terminal c is isolated and I must be zero.
    a. Devise and sketch a circuit in which this device functions as a buffer. Label input and output terminals. Prepare a truth table showing values of the input and output voltages of your circuit



A buffer is a circuit which gives low for low input and high for a high input. The required circuit is:

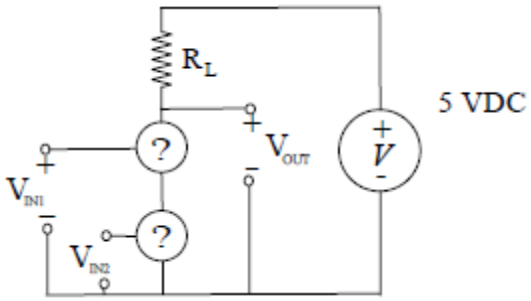


The required table is:

V_{in}	V_{out}
0-3 V	0 V
4-5 V	5 V

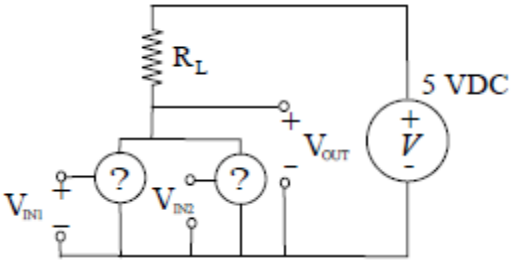
b. Using one or more of these devices, devise and sketch a two-input AND gate

Sol:



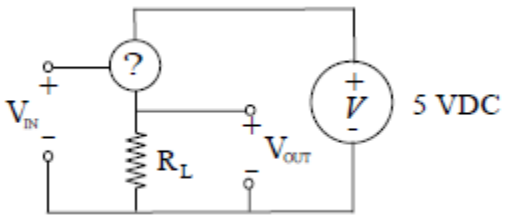
c. Repeat for a two-input OR gate

Sol:

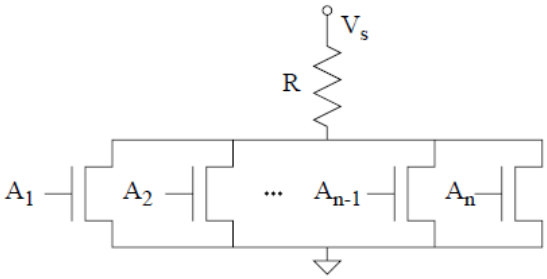


d. Can you use this devise to create an inverter? Explain.

Sol:



3. Consider the n-input NOR gate shown below. Assume that each transistor has an ON resistance of R_{ON}.
    a. For what set of inputs does the gate consume the maximum amount of power?
    b. Derive an expression for this worst case power
    c. What is the value of the worst case power for R=10k and R_{ON} = 0.5k, V_S = 5V?



Sol:
(a) Here, note that R is part of the gate. Most power is consumed when all gates are ON
(b) Worst case power is given by $V_S^2 \Big/ \frac{R_{ON}}{n} + R_L$ since all the MOSFETs will be in parallel. This expression is maximized when n is goes to infinity.
(c) Substitute to obtain 0.05n/(20n+1) which ranges from 2.43 (n=2) to 2.5 (n large) mW