Homework 6

READ INSTRUCTIONS CAREFULLY BEFORE YOU START THE HOMEWORK.

This homework is due on Sunday, Oct 4, 2020.

Homework must be submitted electronically through iLearn on https://ilearn.csumb.edu by 11:55 pm on the due date. Late homework will not be accepted.

Homework must be typed and in pdf format only. Any other formats will not be accepted. You must submit a single file for the entire homework. **Put your name in the document as well.** Your homework submission should present the problems in the original order and be properly labeled.

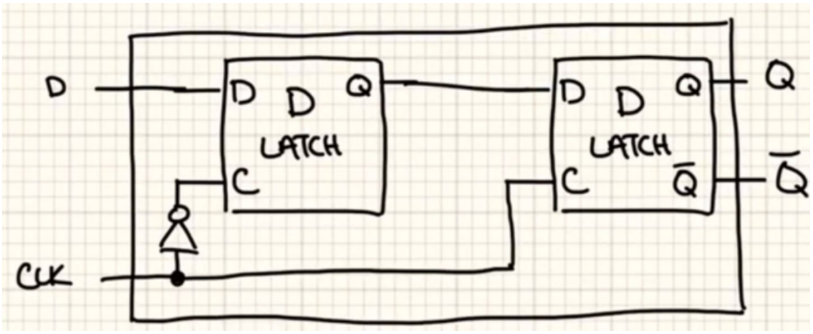
This homework is worth 15 points. Each part of a question carries equal weight unless specified otherwise.

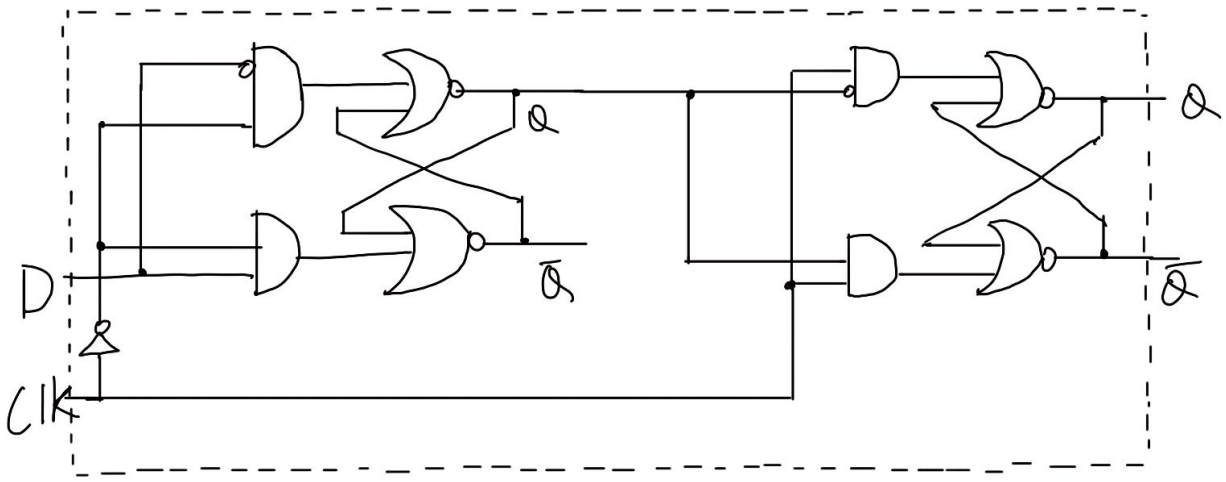
Name : ____Sahil Sinha_____

Exercise 1

In this exercise you will draw a gate level D Flip Flop. Show how you can connect the D Latches below together at the gate level to create a D Flip Flop.

- Draw the gate level of each D latch below
- Connect them together as shown to create a D Flip Flop
- Label all of the inputs and outputs

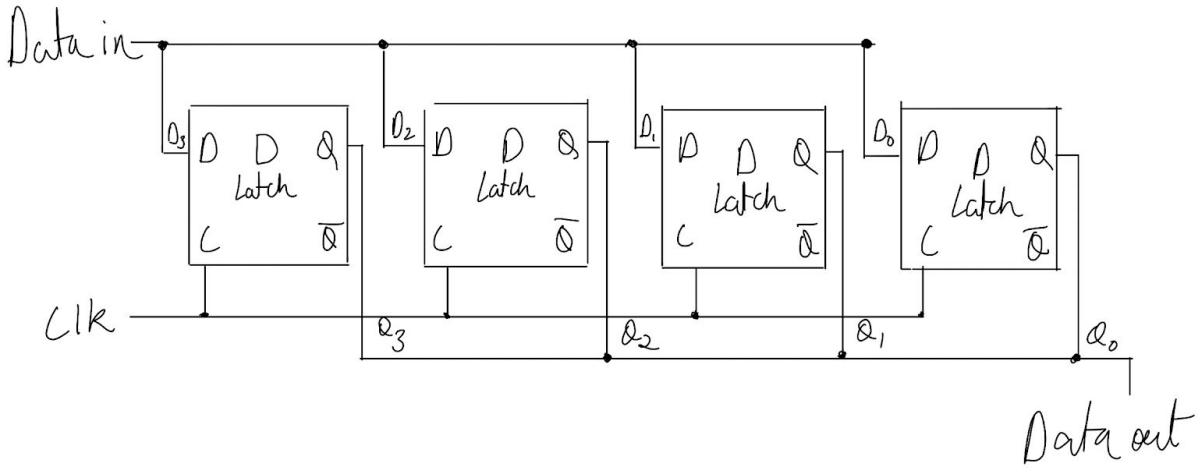




Exercise 2

Build a 4 bit register to store 4 bits of data. You will build this register using 4 D Flip-Flops. You will diagram this at the logic block level (**one block per flip-flop**). Here are your criteria:

- The register will take in data on a 4 bit bus labeled **DataIn**
- The register will update data on the 1 bit signal **CLK**
- The register will produce data on a 4 bit bus labeled **DataOut**
- Draw all of the above components for the register and label them clearly



Exercise 3

For the following clock diagram describing the interaction of **CLK** and **DataIn$_0$**, of a 1-bit Register, draw the **DataOut$_0$** signal.

- Draw the **DataOut$_0$** if CLK is positive edge triggered.
- Draw the **DataOut$_0$** if CLK is negative edge triggered.