Self- heating effects in SOI MOSFET transistor and Numerical Simulation Using Silvaco Software

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***Abstract*—In this paper we briefly present SOI MOSFET transistor and problems generated at high-temperature and self-heating effects, then we present simulation results we obtained using SILVACO TCAD tools relating to SOI n-MOSFET structures we have consider. We will also exhibit some simulation results we obtained relating to the influence of temperature variation on our structure, that having a direct impact on their drain current.**

***Index Terms*—SOI technology, SOI MOSFET, Self-heating effects, Silvaco Software.**

I. INTRODUCTION

Integrated circuits that are used in military, automobile, nuclear and well-logging industry require high temperature operation (above 150 °C). The excellent physical and electronic properties of silicon make it an important semiconductor material for high-temperature applications [1].

Several technologies have been explored as a possible choice for high-temperature operation. These technologies include CMOS [1], SOI [1], and GaAs [1].

The use of bulk CMOS device at high temperatures is limited by the presence of latch-up and high leakage current through the well junction.

Nowadays, SOI technology is considered to take the CMOS processing to its ultimate scalability. In order to highlight the qualities and also the defects of SOI technology. SOI devices have no latch-up and low leakage current due to the absence of the well .It is for these advantages that SOI technology is largely used at high temperatures applications.

We propose in this work to present, simulation results we obtained using SILVACO software for an SOI n-channel MOSFET with static biased.

II. SOI MOSFET TRANSISTOR

SOI (Silicon-On-Insulator) is initially invented for application in many special environments, such as radiation-hardened or high-voltage integrated circuits. It is only in recent years that SOI has emerged as a serious contender for low-power and high-performance applications [2]. SOI MOSFET is different from the traditional bulk MOSFET. For bulk MOSFET, the silicon channel region is built on the substrate directly. For SOI MOSFET, a buried oxide layer is formed on the bulk silicon substrate. On the top of the buried oxide layer there is a silicon thin film, where active MOS devices and circuits are located. The cross section of a basic n-type MOSFET on SOI is shown in Fig. 1 (a) and a photograph of a fabricated SOI MOSFET example is shown in Fig. 1 (b).

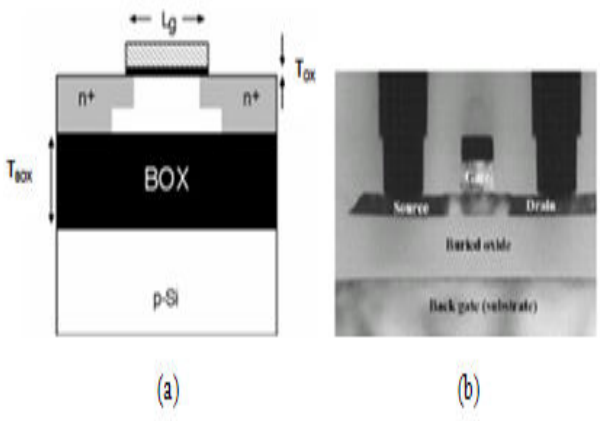

Fig. 1. (a) Structure of SOI MOSFET, (b) Photograph of real SOI MOSFET [3-4].

SOI MOSFET has many advantages over bulk MOSFET in device and circuit level. Because of the buried oxide (BOX) layer, the parasitic capacitances of SOI MOSFET devices are smaller than those of bulk MOSFET. Thus, the delays of digital CMOS circuit due to the junction capacitances can be reduced by using SOI MOSFET, which therefore increase the speed of the digital CMOS circuit. In another aspect, the power delay product of SOI CMOS circuit is much smaller as compared to the bulk counterpart, again owing to the smaller parasitic capacitances in SOI MOSFET as well as reduced leakage currents through BOX. So we can say that, SOI MOSFET technology has high speed and low-power

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properties. In device aspect, SOI MOSFET has no latch-up due to the buried oxide isolation and device isolation is much simpler for the SOI MOSFET as compared to the bulk MOSFET, which make SOI CMOS technology a higher device density and an easier device isolation structure.

Although these advantages of SOI technology are well known, the successful introduction of SOI technology for large-scale applications faces some key challenges across the entire spectra of material, process, manufacturing, devices, and designs. The SOI manufacturing processes are just becoming mature enough for mass production of low-cost, low-defect-density substrates. Another major concern is the control of silicon film thickness to accurately control the threshold of fully depleted devices.

SOI MOSFET can be further divided as partially depleted (PD) Fig. 2 (a) and fully depleted (FD) SOI device Fig. 2(b). Also, elements that have a thin SOI layer (normally <50 nm) and have all body areas under the channel depleted, are called fully depleted type SOI. Conversely, elements that have a thick SOI layer (normally >100 nm) and have some areas at the bottom of the body area that are not depleted, are called partial partially depleted SOI [5].

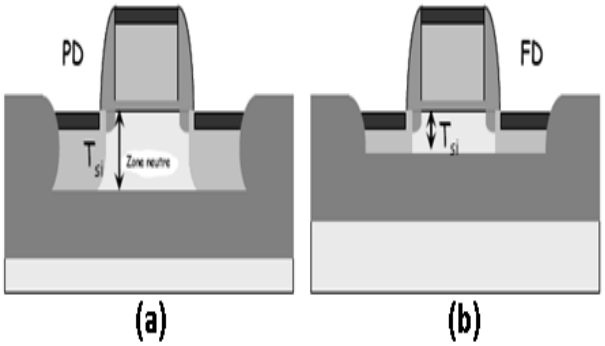

Fig. 2. (a) Structure of partially depleted SOI MOSFET, (b) Structure of fully depleted SOI MOSFET [6].

III. DEVICE SIMULATION

Numerical simulations of the SOI n MOSFET were performed by using the SILVACO TCAD tools. The different parameters of our structure are assumed as follows:

TABLE I. PARAMETERS OF SOI N MOSFET TRANSISTOR.

Symbol	Designation	Value
L_D,L_S,L_G	Drain length, Source length and Gate length	1[um]
L	Channel length	0.7[um]
T_{OX}	Gate oxide thickness	0.017[um]
Tsi	Silicon film thickness	0.2[um]
T_{BOX}	Buried oxide thickness	0.4[um]
	substrate thickness	1.2[um]
	Depth junction	0.52[um]
N_A	Substrate concentration	$1x10^{17}$[cm-3]
N_D	Drain and Source concentration	$1x10^{20}$ [cm-3]

The below structure is obtained using ATLAS device simulation using. The thickness of the silicon film is 0.2 um. This ensures that the channel is partially depleted.

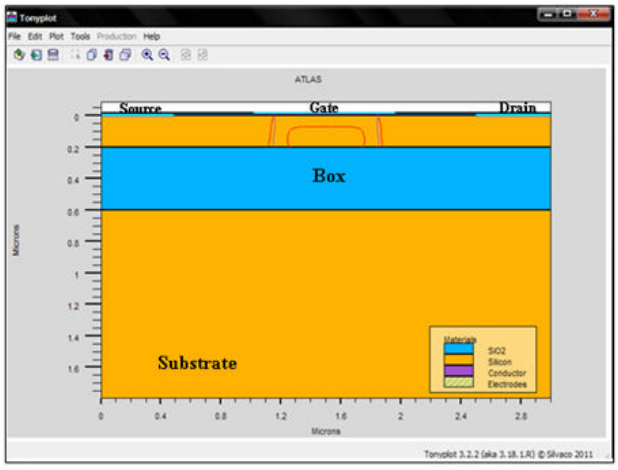

Fig. 3. Device structure of the n-MOSFET with effective channel length 0.7µm, channel doping is 1E17cm-3, drain and source doping concentration is 1E20cm-3, gate oxide thickness is 0.017um, Silicon film thickness 0.2µm.

IV. SELF-HEATING EFFECTS

During the operation of the MOSFET transistor, the electric power generates a quantity of heat per Joule effect. More the power will be raised; the temperature of the channel will increase.

However, the physical parameters such as mobility, the threshold voltage or the saturation speed are temperature dependent. These three parameters are related to the temperature by the following empirical relations (1), (2) and (3) [7]:

$$\mu_{eff} = \mu_{eff,Tamb}(T/T_{amb})^{-k1} \quad (1)$$

$$V_{th} = V_{theff,Tamb} - k_2(T-T_{amb}) \quad (2)$$

$$V_{sat} = V_{sateff,Tamb} - A_T[(T/T_{amb})/T_{amb}] \quad (3)$$

Where: $k_1 \in [1,5 ; 1,7]$, $k_2 \in [0,5 ; 4]$, $A_T = 3,3 \cdot 10^4$.

μ_{eff} ,Tamb , V_{theff} ,Tamb et V_{sateff} ,Tamb are respectively the effective mobility, the effective threshold voltage and the effective saturation speed at the ambient temperature, T_{amb}.

The reduction of the effective mobility is the restrictive factor dominating. When the temperature or the dissipated power increases, mobility decrease involving the decrease of the drain current I_{DS}. Thus, the dissipated power will be lower, which will involve the reduction in the temperature. A phenomenon self maintained is then set up connecting the temperature of the channel and I_{DS}.It is **Self-heating effects.** Consequently, I_{DS} - V_{DS} characteristics presents in saturation a decrease similar to the behavior of a negative resistance [7].

Generated heat is evacuated by the whole of the device according to the type of material and its thermal conductivity. This last quantity varies linearly according to the temperature

of the crystal. According to the values given to TABLE II for pure materials [7], the thermal conductivity of silicon is 100 times larger than that of SiO_2. This means that heat will be evacuated more easily by silicon than by the dioxide of silicon. This last act like a thermal insulator compared to silicon.

TABLE II. SOME TYPICAL VALUES OF THE THERMAL CONDUCTIVITY FOR THE PURE CRYSTAL AT 300 K [11]

Typical values of K at 300 K ($W.m^{-1}.K^{-1}$)	
Silicon	148
SiO_2	1.4
Aluminum	237
Copper	401

Generated heat is thus evacuated with difficulty in the case of a MOSFET comprising a buried oxide compared to its counterpart on massive silicon. This insulation involves the increase in the temperature in the channel. Consequently, the effects of **Self-heating effects** are more significant in the SOI MOSFET transistor.

Fig. 4 present the temperature distribution within a PDSOI n-MOSFET and the thin film's temperature appears to be higher than the external temperature by about 140 K.

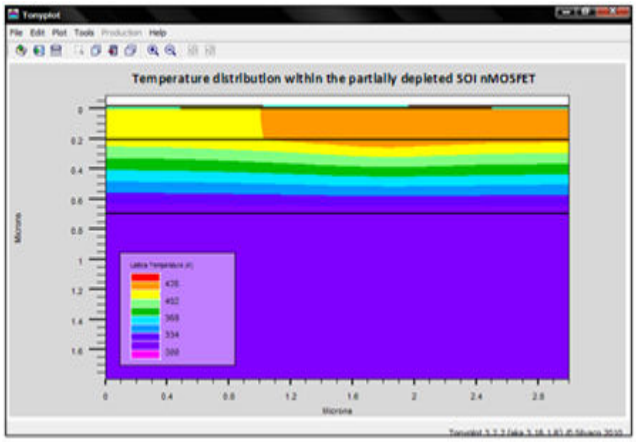

Fig. 4. Temperature distribution within a partially depleted SOI n MOSFET. The external temperature is 300 K.

V. SIMULATION RESULTS AND DISCUSSION

Fig. 5 and Fig. 6 illustrate respectively I_{DS}-V_{DS} characteristics for FD SOI n MOSFET transistor and PDSOI n MOSFET for gate bias of 3V.

The current drain I_{DS} decreases with increasing temperature. At high temperature, the channel mobility decreases. This reduction in mobility leads to a reduction of the drain current.

For PDSOI device, the Kink effect decreases for high temperatures (Fig. 5). Kink effect is one of the principal effects of the floating substrate, started by the accumulation of carriers produced by impact ionization in the silicon film. This effect is translated in PDSOI transistors by the increase of drain current and an electric noise in its saturation region.

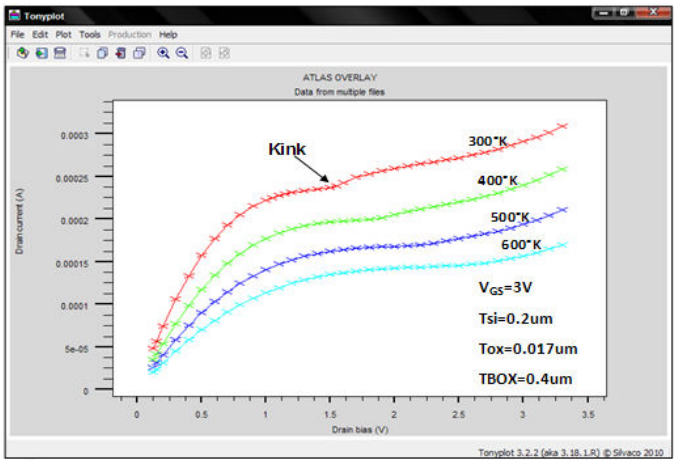

Fig. 5 . Simulated I_{DS}–V_{DS} plot for a partially depleted SOI n-MOSFET at operating temperatures of 300, 400,500 and 600 K.

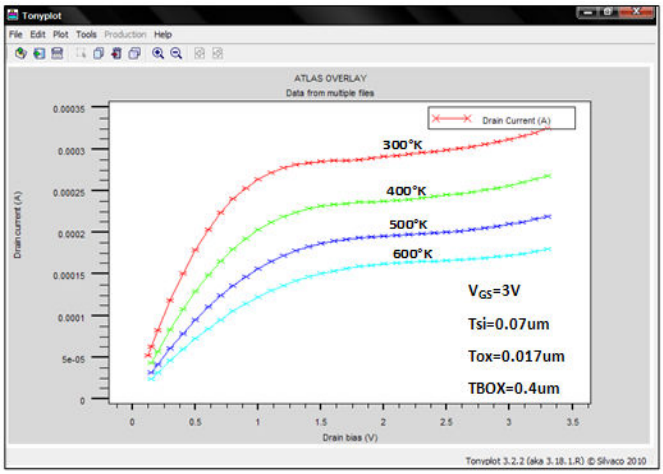

Fig. 6. Simulated I_{DS}–V_{DS} plot for a fully depleted SOI n-MOSFET at operating temperatures of 300, 400,500 and 600 K.

The dependence of the drain current I_{DS} with the temperature is influenced by the threshold voltage and the channel mobility $I_D(T) \approx \mu(T)[V_{GS}-V_{th}(T)]$:. The influences of the reduction of these two parameters in current are opposed.

The $[V_{GS}\_V_{th}(T)]$ term caused the drain current to increase with increasing temperature because the threshold voltage decreased with temperature. On the other hand, the $\mu(T)$ term caused the drain current to decrease with increasing temperature because at high temperatures, lattice scattering dominates and caused a reduction in the channel mobility. At high gate bias, the $\mu(T)$ term dominates while at low gate bias, the [VGS_Vth(T)] term dominates[1]. (Fig. 7 and Fig. 8).

Gate bias V_{GS} for which current I_{DS} does not vary according to the temperature, in a beach of temperature given is called $\mathbf{V_{GS}(ZTC)}$(Zero Temperature Coefficient).

In addition, we can see the advantage of SOI technology, which exhibit a ZTC points over a wide range of temperature up to 600 K. Shoucair was able to identify the ZTC bias point of bulk CMOS transistors in both the linear and the saturation regions up to only 200 °C [1].

Beyond that, the drain current is offset by a large amount with respect to the ZTC drain current. This is because at high temperature beyond 200 °C, the leakage current is comparable to the drain current which limits the device operation. The extended temperature range of SOI devices is due to the suppression of leakage current by the buried oxide between the active thin film and the substrate [1].

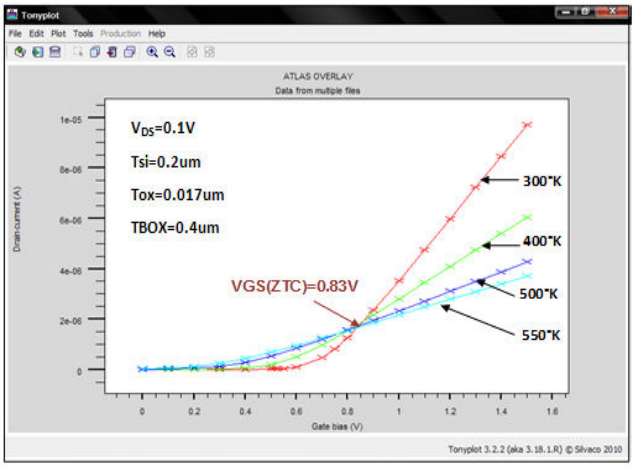

Fig. 7. Simulated I_{DS}–V_{GS} plot for a partially depleted SOI n-MOSFET at operating temperatures of 300, 400,500 and 600 K.

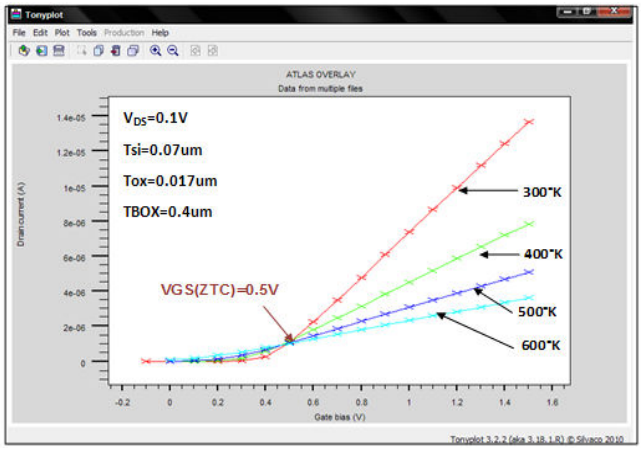

Fig. 8. Simulated I_{DS}–V_{GS} plot for a fully depleted SOI n-MOSFET at operating temperatures of 300, 400,500 and 600 K.

ZTC bias point exists in both linear and saturation regions of I_{DS} -V_{GS} characteristics according to the value of the V_{DS} biasing applied, which is well illustrated on the graph of Fig. 9.

In the short channel devices , the potential barrier to form the conduction channel depends by both the transversal field (controlled by the gate-to-source bias)and the longitudinal field (controlled by the drain-to-source bias), at high drain bias, we see a lower ZTC bias point, the potential barrier decreases leading to drain-induced-barrier- lowering (DIBL) that causes the threshold voltage to drop. Hence we see a lower ZTC bias point at high drain bias for a short channel SOI MOSFET.

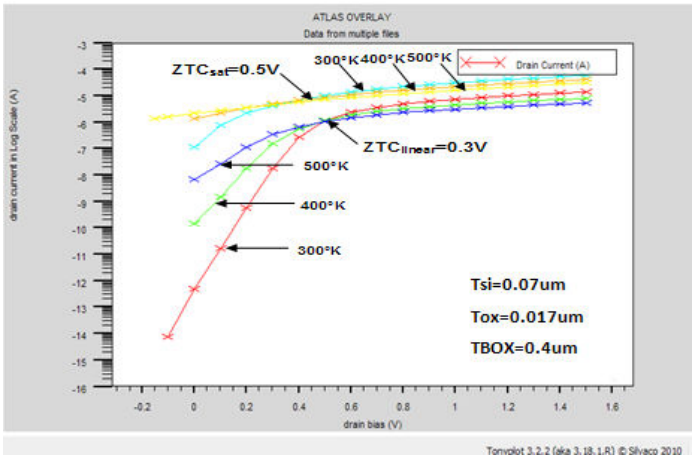

Fig. 9. Simulated I_{DS}–V_{GS} plot for a fully depleted SOI n-MOSFET: in the linear region **ZTC- linear** : V_{DS}=0.1V and the saturation region **ZTC- sat** :V_{DS}=2V.

VI. CONCLUSION

From the simulations results of the SOI n MOSFET structure worked via Atlas-SILVACO tool, we could note the following remarks:

The temperature is one of the essential parameters to be taken into account. Indeed the temperature makes it possible to modify the components performances and consequently circuits.

The use of CMOS devices on bulk substrate at high temperatures is limited by the presence of the latch-up and high leakage currents.

CMOS devices on SOI substrate functions at high temperatures. With this technology the latch-up is eliminated and the leakage current are unimportant, it is for these advantages that SOI technology is largely used at high temperatures applications.

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