

# Microprocessor

## Formative Assessment - II

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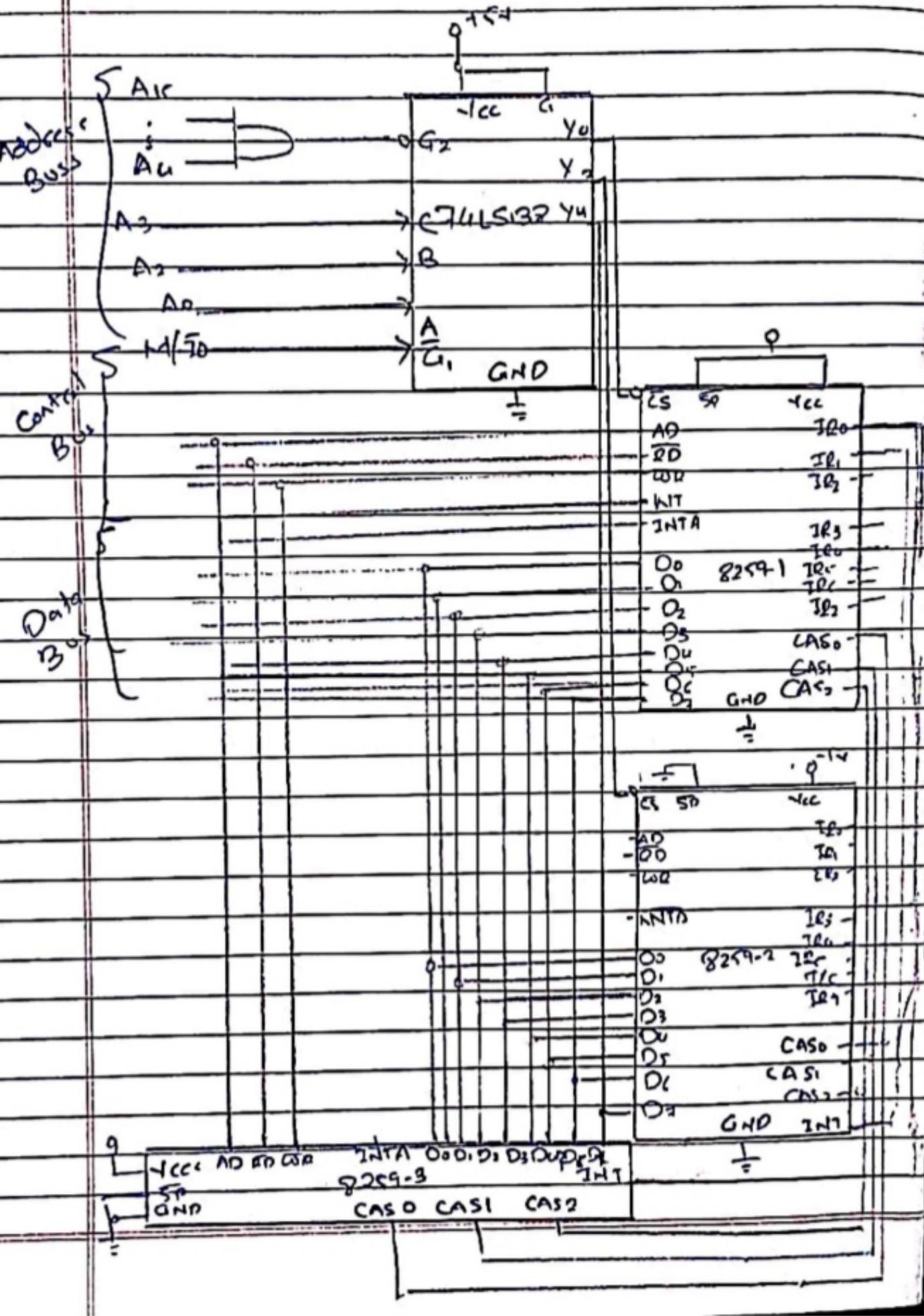
Q1.

Interface three 8259 - PIC with 8086 in Minimum mode & Explain master slave configuration in fully Nested mode.

Ans

The below Diagram shows that how an 8259 can be interfaced with the 8086 microprocessor system in minimum mode.

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Diagram



### Description:-

- 1) The 74151 3:8 address decoder will assert the CS input of the 8259 when on. If base address is FFF0H or FFF2H on the address bus.
- 2) The A.D input of the 8259A is used to select one of the two internal addressing in the device. A0 of the 8259A is connected to system line A1 so the system addresses for the two internal addresses are FFF0H & FFF2H.

- 3) The data lines of an 8259 are connected to the lower half of the system data bus; because the 8086 expects to receive interrupt types of these lower eight data lines.
- 4) RD & WR signals are connected to the system RD & WR lines
- 5) The interrupt request signal INT from the 8259 is connected to the INTR input of the 8086 & INTA on the 8259 A
- 6) The eight IR inputs are available for interrupt signals

### # Master Slave configuration :-

- 1) When the slave receives an interrupt signal on one of its IR inputs, it checks what condition & priority of the interrupt request, if the interrupt is unmasked. If its priority is higher than any other interrupt level being serviced in the slave then the slave will send an NT signal to the IP input of master.
- 2) If that IP input is enabled, the 8086 will go through its NIR interrupt producer & sends out two INTA pulses to both the master & the slave.

- 3) The slave ignores the first interrupt acknowledge pulse but the master outputs a 3-bit slave identification number on the CAS0 - CAS2 lines
- 4) If an interrupt signal is applied directly to one of the IR inputs of the master, the master will send the desired interrupt type of the 8086 when it receives the second INTA pulse from the 8086

Q. Design a 8086 based microprocessor system with the following specification

Ans: A) 8086 is working at 8 MHz.

\* Operating frequency - 8 MHz

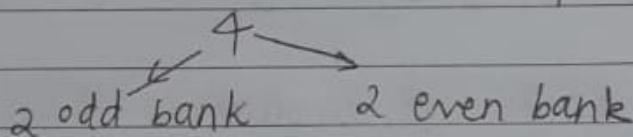
\* Crystal required frequency -  $8 \times 3 = 24 \text{ MHz}$

B) 128 kb Eprom using 32 KB  $\times$  8 chips

\* Available memory size - 32 kb

\* Required memory size = 128 kb

\* Required no of chips =  $128 / 32 \text{ kb} = 4$



\* 2 chip will be used as odd bank that will be selected by BHE.

\* Other 2 chip will be used as even bank that will be selected by AP.

Let  $n$  be the number of address lines

$$\text{SRAM Memory size} = 2^n$$

$$8 \text{ Kb} = 2^n$$

$$2^{13} = 2^n$$

$$n = 13$$

memory

\*  $A_13$  will be used for selecting even bank

+  $A_1 - A_{12}$  will be used for address lines

\* BHE will be used for selecting odd bank

## FA - 02 Microprocessor .

Let  $n$  be no of address lines.

\* SRAM memory Size = 2<sup>16</sup>

$$8k_B = 2^n$$

$$2^3 = 2^n$$

$$n = 13.$$

## Memory

## visible SRAM

8KB.

\* As will be used for selecting even bank.

\* A<sub>1</sub>-A<sub>3</sub> will be used as address lines.

\* BHE will be used for selecting odd bank.

→ Memory Mapping of SRAM ICs:-

A<sub>13</sub> A<sub>18</sub> A<sub>17</sub> A<sub>16</sub> A<sub>15</sub> A<sub>19</sub> A<sub>13</sub> A<sub>12</sub> A<sub>11</sub> A<sub>10</sub> A<sub>9</sub> A<sub>8</sub> A<sub>7</sub> A<sub>6</sub> A<sub>5</sub> A<sub>4</sub> A<sub>3</sub> A<sub>2</sub> A<sub>1</sub>

Starting add  
at ~~each~~ back

of even bark

of odd bank

of odd. bank

## Memory Mapping EEPROM ICs.

A<sub>19</sub> A<sub>18</sub> A<sub>17</sub> A<sub>16</sub> A<sub>15</sub> A<sub>14</sub> A<sub>13</sub> A<sub>12</sub> A<sub>11</sub> A<sub>10</sub> A<sub>9</sub> A<sub>8</sub> A<sub>7</sub> A<sub>6</sub> A<sub>5</sub> A<sub>4</sub> A<sub>3</sub> A<sub>2</sub> A<sub>1</sub> A<sub>0</sub>

1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 Starting address  
for EEPROM 1 even

1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 Last address of  
EEPROM 1 even

1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 Starting address  
of EEPROM 1 odd.

1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 starting address  
of EEPROM 2 even

1 Last add of  
EEPROM 2 even

1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 Starting address  
of EEPROM 2 odd.

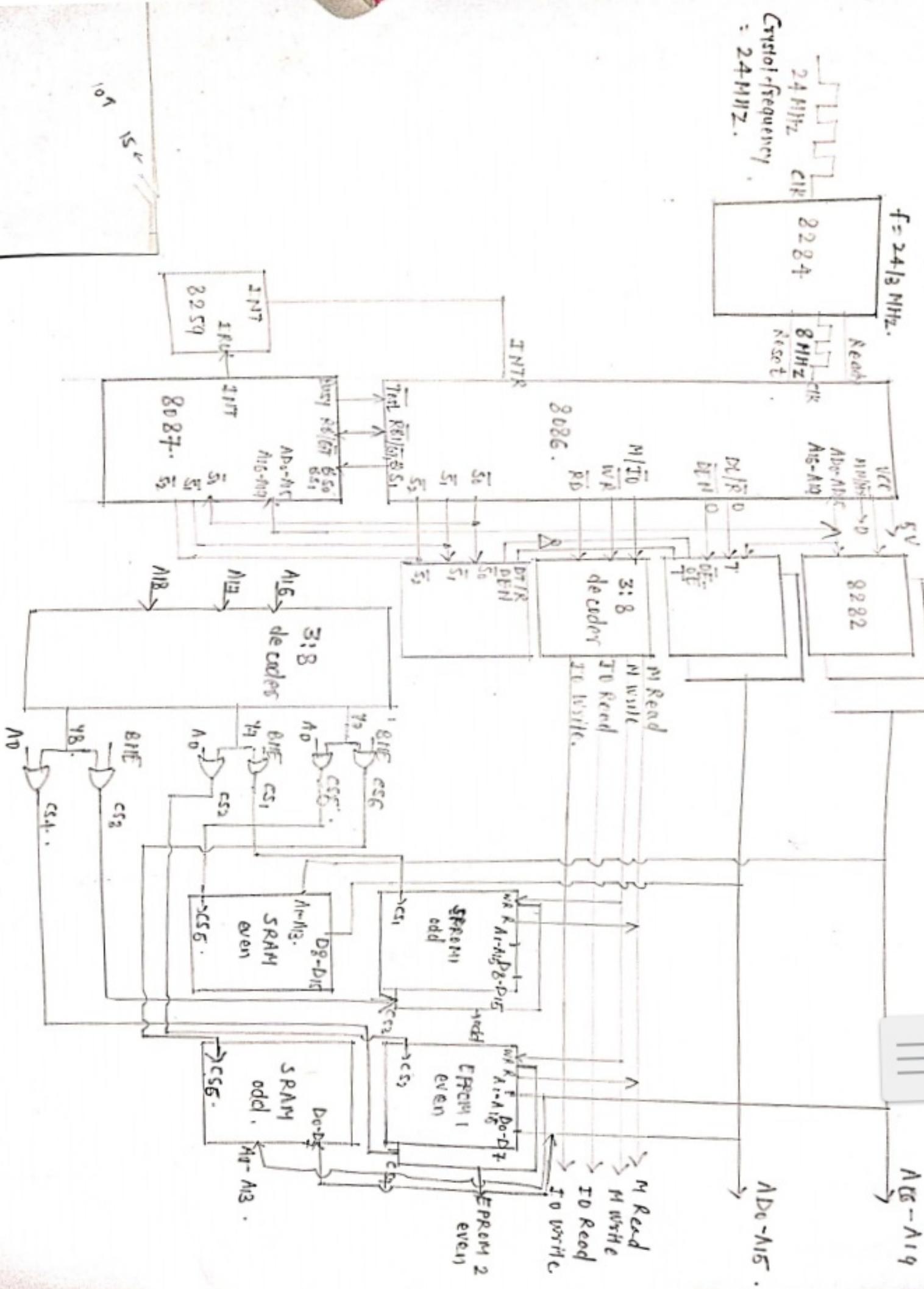
1 last address of  
EEPROM 2 odd.

\* We will use A<sub>16</sub>, A<sub>17</sub>, A<sub>18</sub> as de coders.

\* When A<sub>18</sub>, A<sub>17</sub>, A<sub>16</sub> is 0,0,0 SRAM will be Selected.

\* When A<sub>16</sub>, A<sub>17</sub>, A<sub>18</sub> is 110 then EEPROM 1 will be Selected.

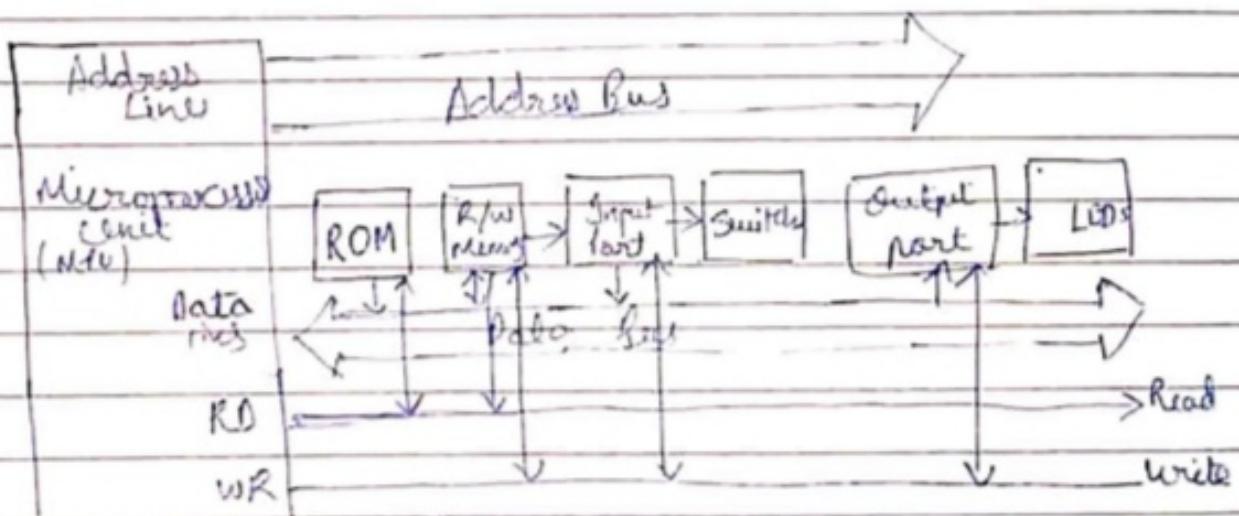
\* When A<sub>16</sub>, A<sub>17</sub>, A<sub>18</sub> is 111 then EEPROM 2 will be Selected.



Q.3 I/O Interfacing: There are various communication devices like, the keyboard, mouse, printer etc. So we need to interface the keyboard and other device with the microprocessor by using latches and buffers. This type is known as I/O interfacing.

In Memory Interfacing: 8 bit data line, 16 bit address line, Control Signals are connected to corresponding lines of memory IC.

In I/O Device Interfacing: 8 bit data line, Control & Signal are connected to corresponding lines of I/O devices.



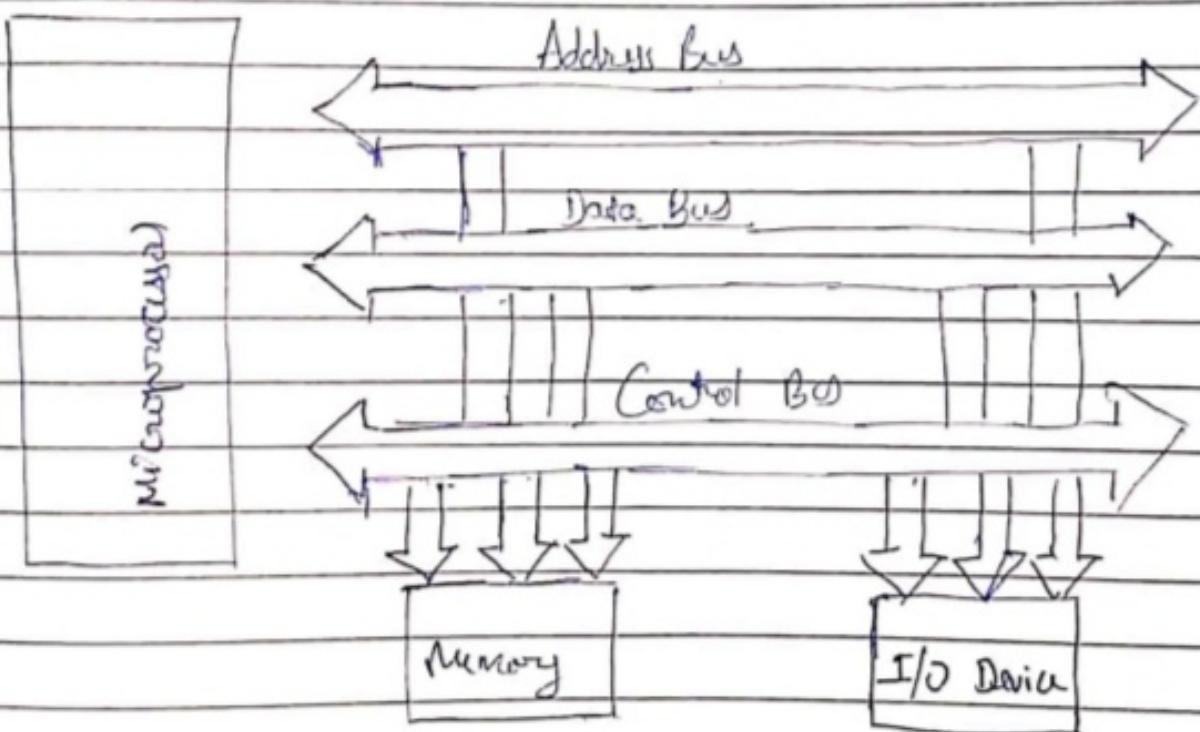
ways of Communication:-

Microprocessor can communicate in two ways with outside world:

1) Serial Communication Interface: In this type of communication, the interface gets

a single byte of data from the microprocessor and sends it bit by bit to the other system serially and vice-versa.

Parallel Communication Interface - In this type of communication, the interface get a byte of data from the microprocessor and sends it bit by bit to the other system in simultaneous parallel fashion and vice-versa.



Q9. List and describe the features of 80386 DX microprocessor & compare 8086 & 80386 microprocessor for their major features

Ans:- 80386 microprocessor is a 32-bit processor that holds the ability to carry out 32-bit operation. In one cycle it has (a) data & address 4GB (2<sup>32</sup>) of physical memory. Multitasking & protection capability are the two key characteristics of 80386 microprocessor. 80386 has internal dedicated hardware that facilitates multitasking.

We know 8086 is a 16-bit microprocessor & 80286 was an advancement of 8086 with some additional characteristics. But with the advance of technology, Intel introduced a 32-bit microprocessor where processing speed was twice that of the 80286 microprocessor. This was our 80386 microprocessor that was designed by Intel in October 1985 & was an upgraded version of the 80286 microprocessor.

features of 80386

- ① It's a 32-bit processor thus has 32-bit ALU
- ② 80386 has a data bus of 32-bit
- ③ It holds an address bus of 32-bit.

- (4) It supports physical memory addressability of 4TB & virtual memory addressability of 64TB.
- (5) 80386 supports a variety of operating clock frequencies, which are 15 MHz, 20 MHz, 25 MHz, & 33 MHz.
- (6) It offers 3 stages pipeline: fetch, decode & execute. As it supports simultaneous fetching, decoding & execution inside the system.

Q5. Segment descriptor are a part of segment table unit, used for translating a logical address to a linear address. Segment descriptors describe the memory segment referred to in the logical address.

fields:

Base address  $\rightarrow$  32 bit starting memory address

Segment limit  $\rightarrow$  20 bit length of segment

G  $\downarrow$  Granularity  $\rightarrow$  The limit is in units of bytes.

6 D = Default Operand  $\rightarrow$  clear, 16 bit, 32 bit

B = Big  $\rightarrow$  max offset size for a data segment  
32 bit

L = long  $\rightarrow$  "L" cannot be set at the same time

AVL = Available  $\rightarrow$  for software use.

P = Present  $\rightarrow$  If clear, exception is generated.

C = Conforming  $\rightarrow$  Are called less privileged level

E = Extend down  $\rightarrow$  a behaviour used for stack

R = Readable  $\rightarrow$  the segment may be executed

W = Writeable  $\rightarrow$  the data segment may be written in form.