Que) Write short notes on 8259A interrupt collector.

Ans) For applications where we require multiple interrupt sources, we need to use external devices called a programmable interrupt controlleres. By connecting PIC to the micro-processor we can increase the interrupt handling capacity of the micro-processor.

8259A programmable interrupt controller is commonly used priority interrupt controller.

Features of 8259A PIC ⇒

→ It is an LSI chip that manages 8 levels of interrupts i.e. It is used to implement 8 level interrupt system.
→ It can be cascaded in a master-slave configuration to handle upto 64 levels of interrupts.
→ It can identify the interrupting device.
→ The interrupt requests are individually maskable.
→ It does not require a clock signal.
→ The starting address of the vector number is programmable.
→ It can be used in buffered mode.
→ It can be used polled as well as interrupt mode.

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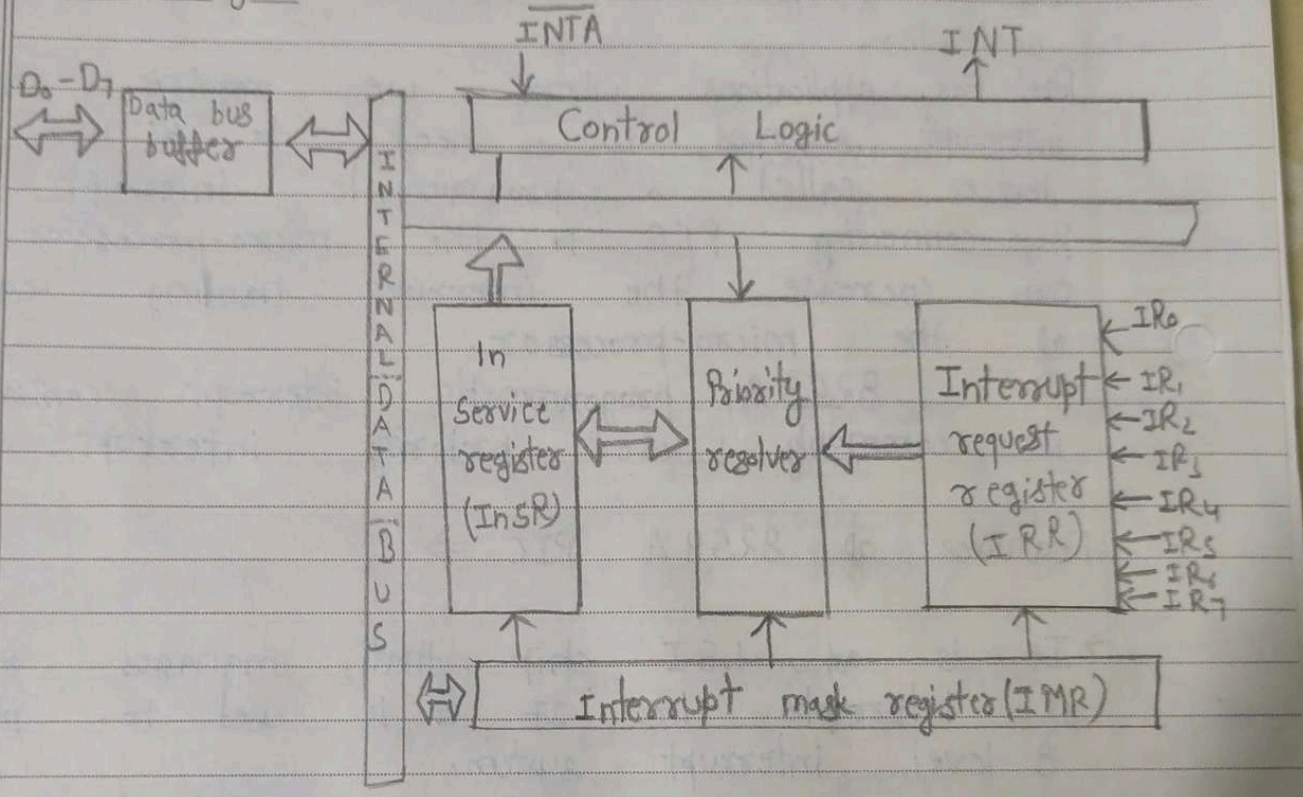
block diagram :-



Block diag. - 8259A PIC.

Que) Why 8253 programmable counter/timer is needed in a microprocessor system?

Ans) The 8253 programmable counter/timer is a versatile integrated circuit used in microprocessor system for various timing and counting operations. It provides multiple timer/counters that can be programmed to perform specific functions, making it a valuable component in many applications. Here are some reasons ~~why~~ why 8253 is needed in a microprocessor system.

1. Timing & synchronization: The 8253 allows precise timing and synchronization of events in a micro-processor system. It provides accurate timing measurement and generation of time delay, which are essential for controlling the timing of various operations in a system.

2. Real-time applications: Many micro-processor systems require real time functionality such as generating accurate periodic interrupts or generating accurate time depending signals.

3. Pulse generation: It can generate pulse of different frequencies and duty cycles. This capability is useful for generating clock signals, driving other components in the system.

4. Event counting: It can function as a counter to keep track of external events. It can count external signals and generate interrupts based on pre-defined conditions.

Overall, the 8253 programmable counter / timer is an essential component in a microprocessor system, providing precise timing, synchronization, event counting, pulse generation and other functions required in many applications.

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Que) Write short note on 8089 I/o processor.

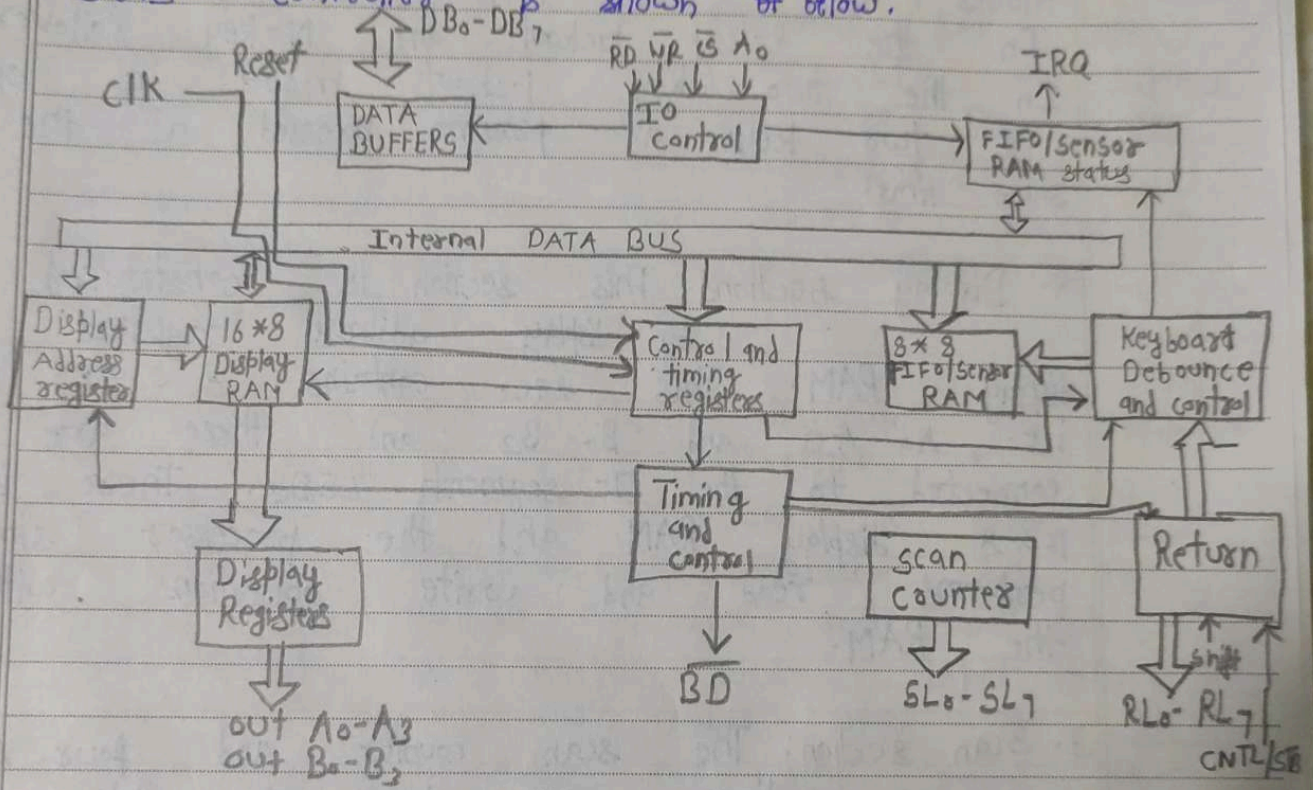
The intel 8089 I/o processor is contained in a 40-pin integrated circuit package. Within the 8089 are two independent units called channels. Each channel combine the general characteristics of a processor unit with these of a direct memory access controller.

The 8089 is designed to function as an IOP in a micro-processor / microcomputer system where the intel 8086 micro-processor is used as the CPU. The 8086 CPU initiates as I/o operation by building a message in memory that describes the function to be performed. The 8089 IOP reads the message from memory, carries out the operation, and notifies the CPU when it has finished.

The instruction set includes general data transfer instructions, basic arithmetic and logical operations, condition and unconditional branch operations, and subroutine call and return capabilities. The set also include operation, instructions to initiate DMA transfers and issue and interrupt request to the CPU. It provides efficient data transfer between any two components attached to the system bus to communicate with the IOP by enabling the channel attention lines. The select lines are used by the CPU to select one of two channels in the 8089.

Que.) Discuss the architecture of 8279 with diagram.

Ans) The functional block diagram of the intel 8279 controller is shown below:



Block diag. - 8279

Let us understand the operation of this architecture by considering its 4 separate sections.

1. keyboard section: this section is composed of return Buffer and keyboard Debounse and control. It holds the 8 return lines denoted by RL0 to RL7 that forms the column of the keyboard matrix. Shift and control / strobe

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are the two additional inputs provided to the provided to this unit. The two operating modes are 2-key lockout and N-key rollover. In the 2-key lockout and N-key rollover. In the two-key lockout mode of operation, if two keys are ~~present~~ pressed at the same time.

2. Display sections: This section is constituted by display address registers and display RAM. This sec. contains 8 o/p lines. i.e., $A_0 - A_3$ and $B_0 - B_3$ and these are connected to the 7-segment LEDs. There is a 16*8 display RAM and the processor simply performs read and write operations within the RAM.

3. Scan section: The scan counter and four scan lines are part of this section. there are two modes of scan counter namely, encode and decode. In encode mode, an binary counter will be obtained as the output of scan lines. In decode scan mode, internal decoded 1 out of 4 scan lines and thus can drive upto 4 displays.

4. CPU interface section: This section is composed of I/o control and data buffers along with timing and control registers. The timing

and control unit is also the part of this unit. This section is responsible for data transfer between 8279 and the CPU and hence consists of bidirectional data lines DB_0 to DB_7. There are two internal addresses whose specified value ie. either 0 or 1 makes the selection for either data buffer or control register.

Que.) Explain with a neat diagram the operation of the 8257 DMA controller.

Ans) Suppose any device which is connected to input-output port wants to transfer data to memory, first of all, it will send input-output port address and control signal, input-output read to input-output port, then it will send memory address and write signal to memory where data has to be transferred. In normal I/o technique, the processor become busy in checking whether any input-output operation is completed or not for next I/o operation.

Basic operations :-

HOLD - hold signal.
HLDA - Hold acknowledgment
DREQ - DMA request.
DACK - DMA acknowledgment.

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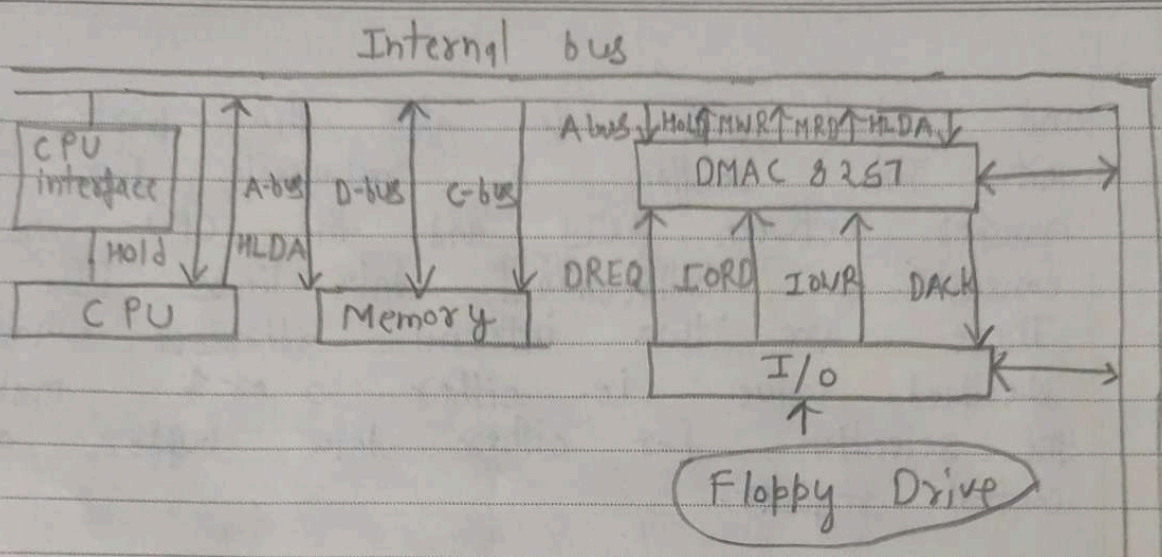

Suppose a floppy drive that is connected at input - output port wants to transfer data to memory, the following steps are performed.

* First of all the floopy drive will send a DMA request to the DMAC.
* Now the DMAC will send a hold signal to the CPU.
* After accepting the request, the cpu will send the HLDA to the DMAC.
* Now the DMAC will send a acknowlegment to the floopy drive which is connected at the I/o port.
* Now, with the help of I/o read and memory write signal the data is transferred from the floppy drive to the memory.

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Que.) Give the application of 8051 microcontroller?

Ans The 8051 microcontroller have many applications. Here are some of the most common applications of 8051 MC.

→ Embedded systems :- The 8051 microcontroller is commonly used in embadded systems, such as home automation systems, security systems, and industrial control system. Its low cost, small size and easy to programming make it a ideal choise for these applications.

→ Automative systems :- It is used as automative systems, such as engine control units, anti lock breaking systems and air-bags systems to control various functions and ensure safe and efficient operation.

→ Robotics :- It is also used to control the movement and operation of robots. It is commonly used to control the motors, sensors and other pheripherals of robots.

→ Communication systems :- It is used in communication systems, such as modems, routers and switches, to control the data transfer and communication protocols.

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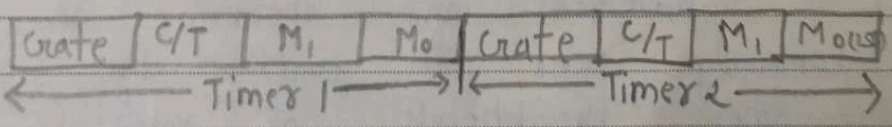
→ Medical devices :- It is used in medical devices such as, insulation pump, heart monitors and blood glucose meters, to control various functions to provide accurate and reliable result.

Que] Describe the following SFR of 8051 mc. 4
(i) TMOD (ii) TCON (iii) SCON (iv) DPTR.

Ans] The 8051 micro-controller special function registers acts as a control table that monitors and control the operations of the 8051 micro-controller.

(i) TMOD :- It stands for time mode, and as the name suggests, it is responsible for setting the mode of a timer among other things. It is an 8-bit register that is placed at the address 89H in the ROM space and is not bit addressable.



Structure of TMOD register - address 89H.

There are four modes that 8051 offers. We need to bits to set these modes -

M0	M1	selected mode
0	0	Mode 0
0	1	Mode 1
0	1	mode 2
1	1	Mode 3

(ii) TCON :- It stands for time control that is used by timers. It is used to send control signals for the functioning of the timer. It is bit addressable and is placed at the address 88H in the ROM. It is an 8-bit register which starts the timer and also contains the flag, which gets updated when the timer overflows.

TF_1 (MSB)	TR_1	TF_0	TR_0	IE_1	IT_1	IE0	ITO

Structure of TCON register.

(iii) SCON :- Using Serial control, most mc can communicate with peripherals using serial communication. To manage this asynchronous communication b/w devices, the SCON register is used.

SM0 (MSB)	SM_1	SM_2	REN	TB8	RB8	TI	RI (LSB)

SCON.7 SCON.6 SCON.5 SCON.4 SCON.3 SCON.2 SCON.1 SCON.0

Serial control register At B8H.

SM_2 enagles multiprocessor communication in modes 2 and 3. The ren bit is used to enable or disable reception. 9th bit is stored TB8 during transmitting data. 9th bit is stored in RB8 during recieving data.

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(iv) DPTR :- Data pointer is the 8051's only user accessable 16 bit register. DPTR is meant for pointing to data. It is used by the 8051 to access the external memory using the address indicated by DPTR. It is used to store 2-byte value.

Que.) What is timer counter interrupt? Also explain time modes of operation? (Or)

Ans) There are times when you need something to happen on time every time which becomes virtually impossible without using timer counter interrupts. These are similar to external interrupts, but instead of firing on an external event, they fire on timer. They are so called as they will interrupt the thread of execution after the current instruction completes, and run their codes, returning to the next instructions from where it left off when it is finished.

Different time mode operations :-

Mode 0 :- Both timer 1 and timer 0 in mode 0 operater, operate 8-bit counters time register is configured as a 13-bit register consisting of all 8-bits of TH1 and lower 5 bits of TL1

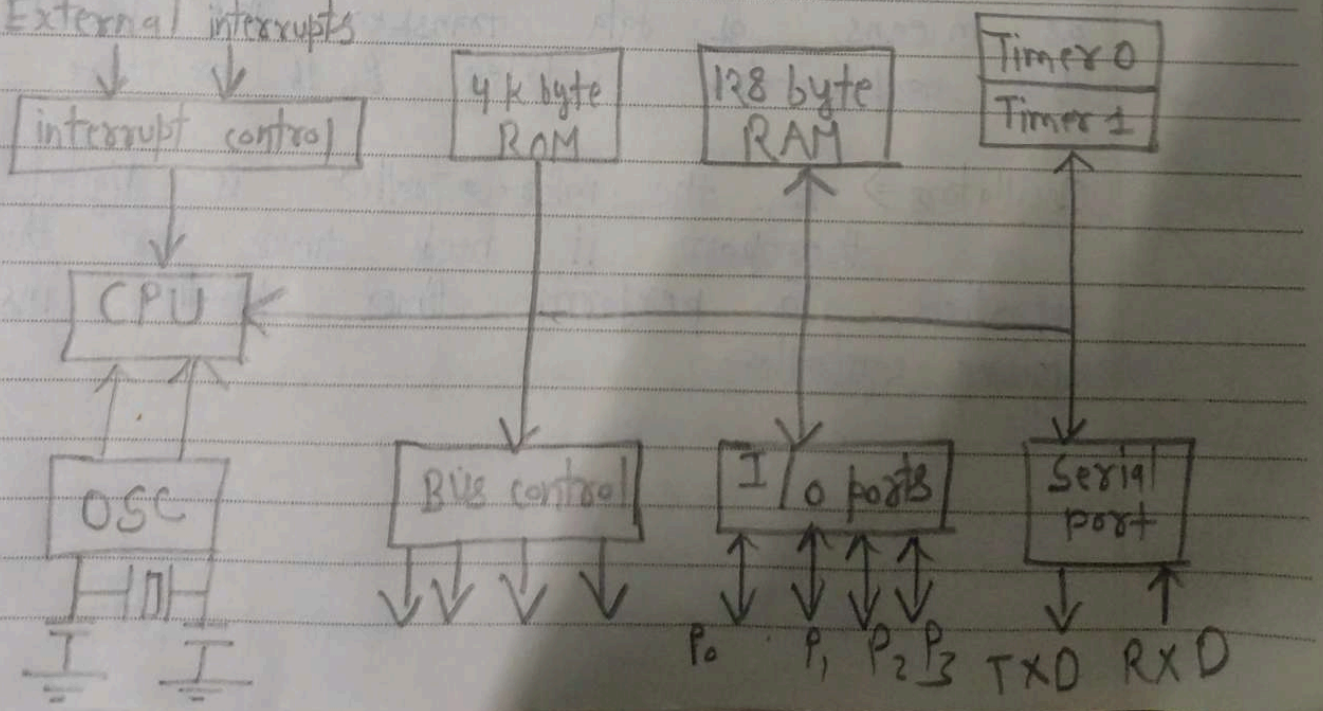
Mode 1 ⇒ It is a 16 bit mode and is commonly used mode. It functions in the same way as mode 0 except it uses 16 bits.

Mode 2 :- Both the timer registers are configured as 8-bit counters with automatic reload. overflow from TL1 sets TF1 and also reloads TL1 with the contents of TH1.

Mode 3 :- It is known as split timer mode. When timer 0 is placed in mode 3, it becomes two seperate 8-bit timers. Timer 0 is TL0 and timer 1 is TH0.

Que] Describe and explain the architecture of 8051 microcontroller.

Ans.



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CPU ⇒ It acts as a mind of any processing machine. It synchronizes and manages all processes that are carried out in micro-controller. User has no ~~cont~~ power to control CPU.

Interrupts ⇒ It is a subroutine call that given by the microcontroller when some other program with high priority is req. for acquiring the system buses.

Memory ⇒ For operation, microcontroller required a program. This program guids the microcontroller to perform the specific tasks. Any program required some on chip memory for the storage.

BUS ⇒ It is a group of wires which uses as a communication canal or acts as means of data transfer. The different bus configuration includes 8, 16 or more cables.

Oscillators ⇒ As the microcontroller is digital circuit, therefore it needs timer for their operations. To perform timer operation inside micro-controller.

SESSIONAL PAPERS

Q) Write instruction set of 8051.

Ans) The instructions of 8051 micro-controller can be classified into five different groups.

1. Data transfer instruction :- Data transfer related operations like move, swap, push, pop etc. are performed in this instruction set.

2. Arithmetic instruction :- Arithmetic operations like ADD or SUB etc. is are performed in this instruction set.

3. LOGical instruction :- Bit related operations are performed in this instruction set. Logical operations like OR, AND etc. are performed.

4 Branching instruction :- Call or jump operations are used in this instruction set.

eg) CJNE - compare and jump if not equal
JZ - jump if accumelator zero.

5. Bit-wise instruction :- Instruction performed after checking the bit related conditions.

eg) JB - jump if bit set.
JNB - jump if bit not set.