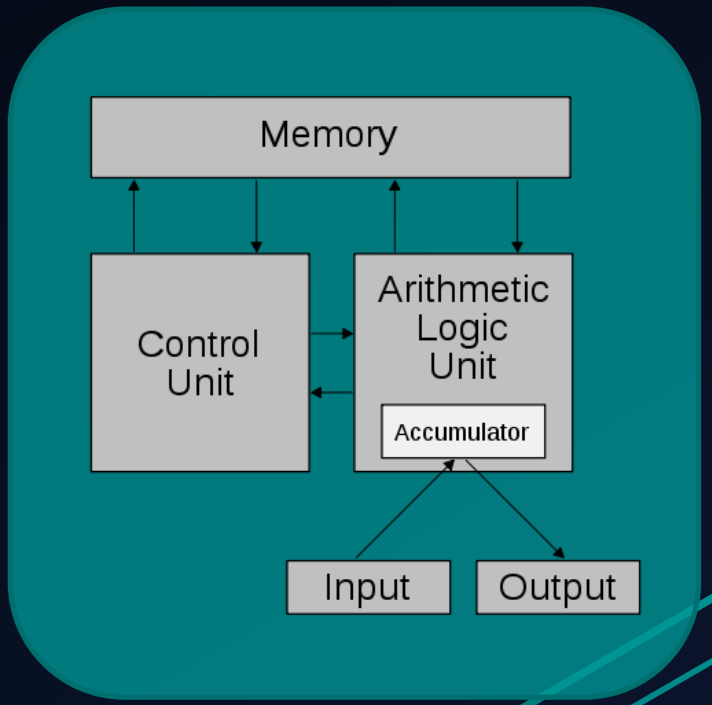
Development of 2 Bit ALU

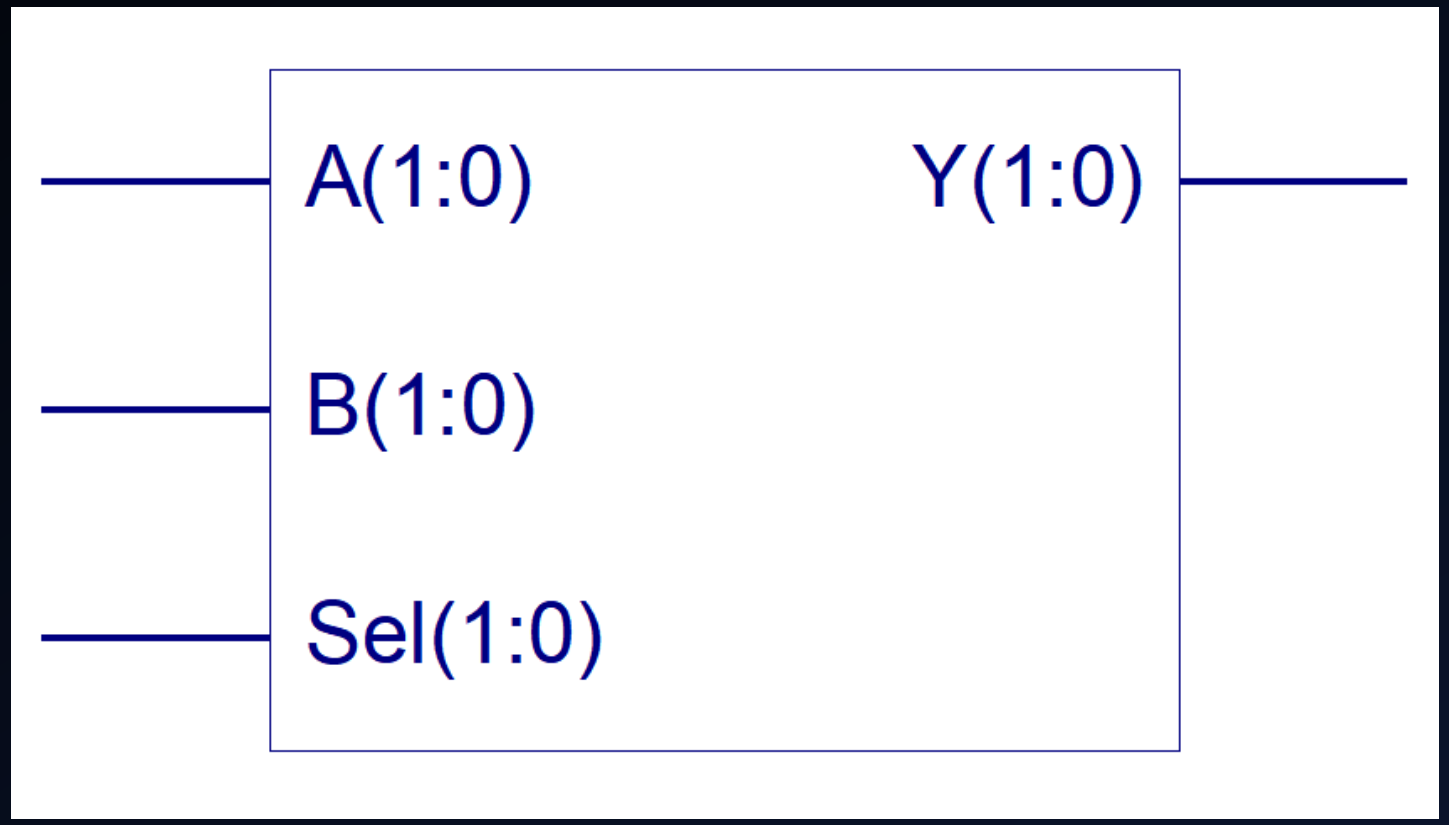
FOR PROCESS SIMULATION

Arithmetic Logic Unit

ARITHMETIC LOGIC UNIT (ALU) IS A VITAL COMPONENT OF ANY COMPUTING SYSTEM. IT IS A DIGITAL COMBINATIONAL CIRCUIT THAT PERFORMS THE REQUIRED ARITHMETIC AS WELL AS LOGICAL OPERATIONS ON THE OPERANDS. EARLIER VON NEUMANN PROPOSED FIRST ALU IN 1945 WHEN HE WAS WORKING ON EDVAC. CONVENTIONALLY ALU'S WERE DESIGNED USING BASIC LOGIC GATES SUCH AS AND, OR, NOT ETC. HOWEVER THESE GATES DISSIPATE SOME AMOUNT OF ENERGY DUE TO THE INFORMATION LOSS DURING THE OPERATION.



Block Diagram of the 2 Bit ALU



Synthesized in Xilinx ISE 8.1i

Progress so far…

We have synthesized the Logical Unit for the ALU, now there is The Arithmetic Unit to be constructed and synthesized. Here is the HDL code for Logical Unit

```
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22  use IEEE.STD_LOGIC_ARITH.ALL;
23  use IEEE.STD_LOGIC_UNSIGNED.ALL;
24  --library UNISIM;
25  --use UNISIM.VComponents.all;
26
27  entity ALU_2bit is
28      Port ( A : in  STD_LOGIC_VECTOR (1 downto 0);
29             B : in  STD_LOGIC_VECTOR (1 downto 0);
30             Y : out  STD_LOGIC_VECTOR (1 downto 0);
31             Sel : in  STD_LOGIC_VECTOR (1 downto 0));
32  end ALU_2bit;
33
34  architecture Behavioral of ALU_2bit is
35
36  begin
37
38  PROCESS(A,B,Sel)
39  BEGIN
40
41  CASE SEL IS
42  WHEN "00" =>
43           Y <= A AND B;
44  WHEN "01" =>
45           Y <= A OR B;
46  WHEN "10" =>
47           Y <= A NAND B;
48  WHEN "11" =>
49           Y <= A NOR B;
50  WHEN OTHERS =>
51           NULL;
52  END CASE;
53  END PROCESS;
54
55  end Behavioral;
56
```

Components required

- Quad 2-i/p AND Gates (7408)
- Quad 2-i/p OR Gates (7432)
- HEX Inverter / NOT Gates (7404)
- Dual 4 to 1 line MUX (74153)

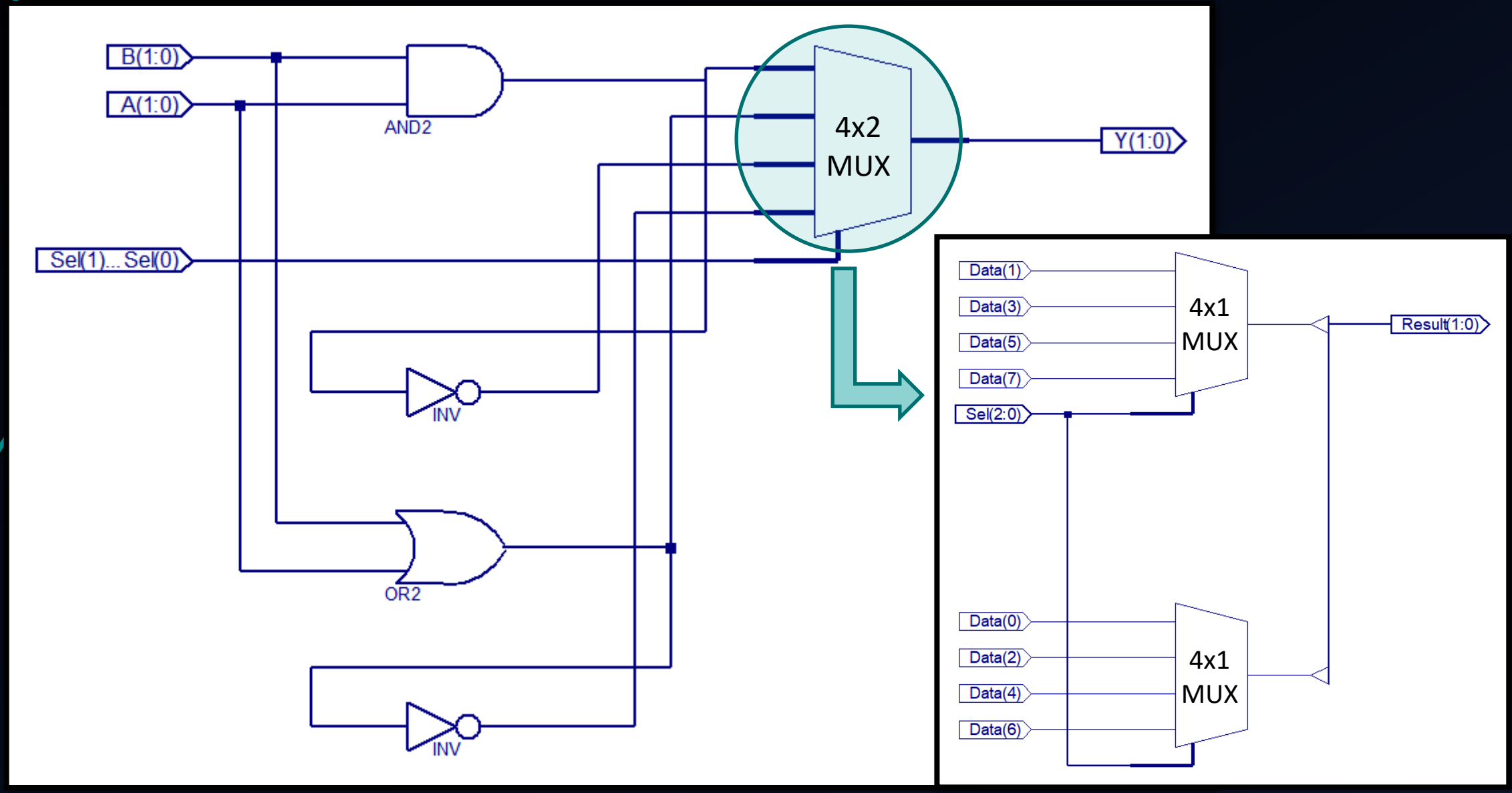
-There might more ICs be adding as for Arithmetic Operations

```
=========================================================
*                          Final Report
=========================================================
Final Results
RTL Top Level Output File Name     : ALU_2bit.ngr
Top Level Output File Name         : ALU_2bit
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : YES
Target Technology                  : Automotive CoolRunner2
Macro Preserve                     : YES
XOR Preserve                       : YES
wysiwyg                            : NO

Design Statistics
# IOs                              : 8

Cell Usage :
# BELS                             : 36
#      AND2                        : 10
#      INV                         : 14
#      OR2                         : 8
#      OR3                         : 4
# IO Buffers                       : 8
#      IBUF                        : 6
#      OBUF                        : 2
=========================================================
```

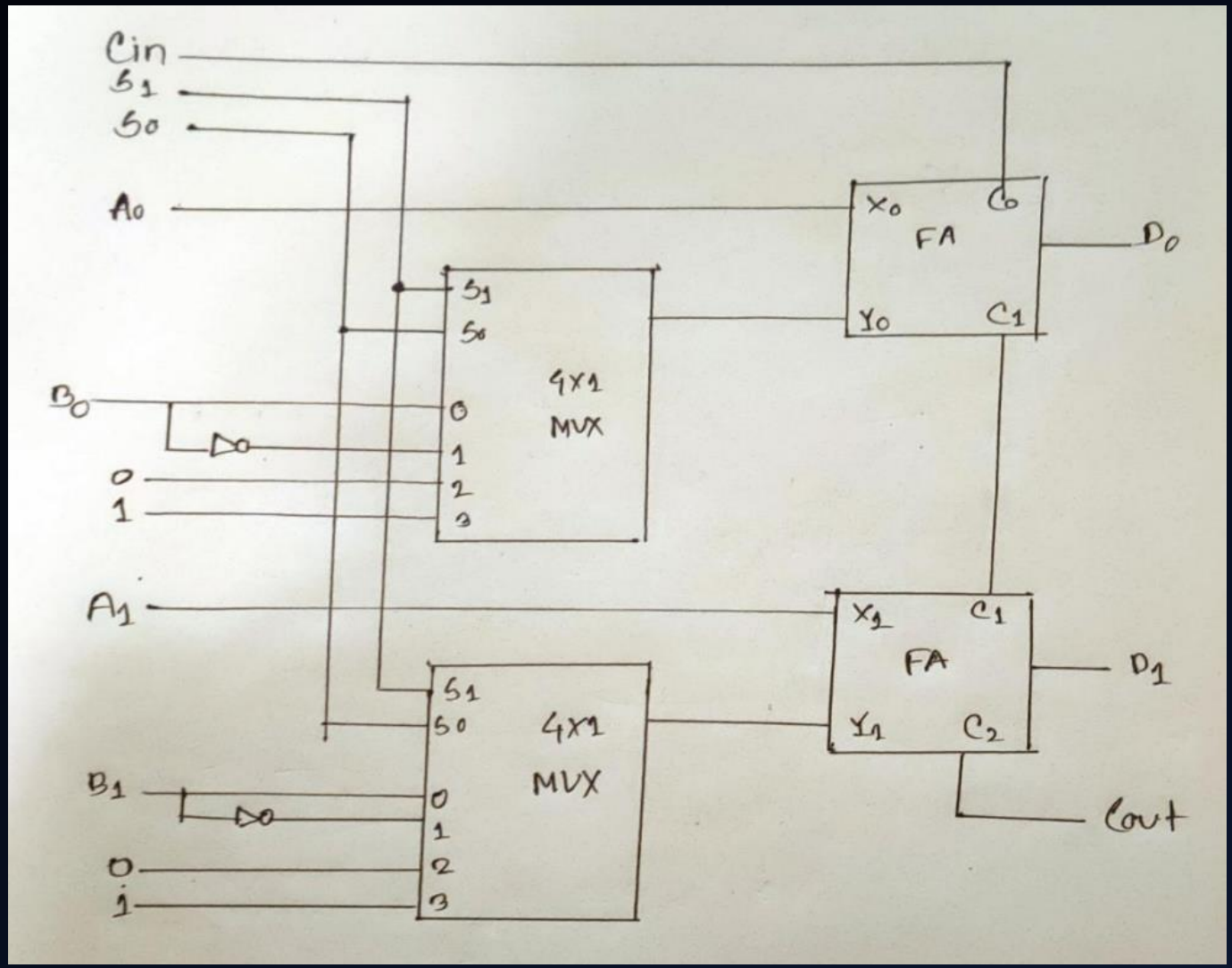
Circuit Diagram for Logical Unit



Working of the project

This ALU can perform AND, OR, NAND and NOR operations for now. We will be implementing Full Adder module to do Arithmetic Operations also. A rough circuit diagram can be seen on the next slide for Arithmetic Unit.

Circuit diagram for Arithmetic Unit



Truth Table

	A	B	S1	S0	Y
AND	00	00	0	0	00
OR	00	01	0	1	01
NAND	00	10	1	0	11
NOR	00	11	1	1	00
AND	01	00	0	0	00
OR	01	01	0	1	01
NAND	01	10	1	0	11
NOR	01	11	1	1	00
AND	10	00	0	0	00
OR	10	01	0	1	11
NAND	10	10	1	0	01
NOR	10	11	1	1	00
AND	11	00	0	0	00
OR	11	01	0	1	11
NAND	11	10	1	0	01
NOR	11	11	1	1	00

References

- www.bravelearn.com
- www.electronics-tutorials.ws
- www.knowelectronic.com
- www.circuitspedia.com