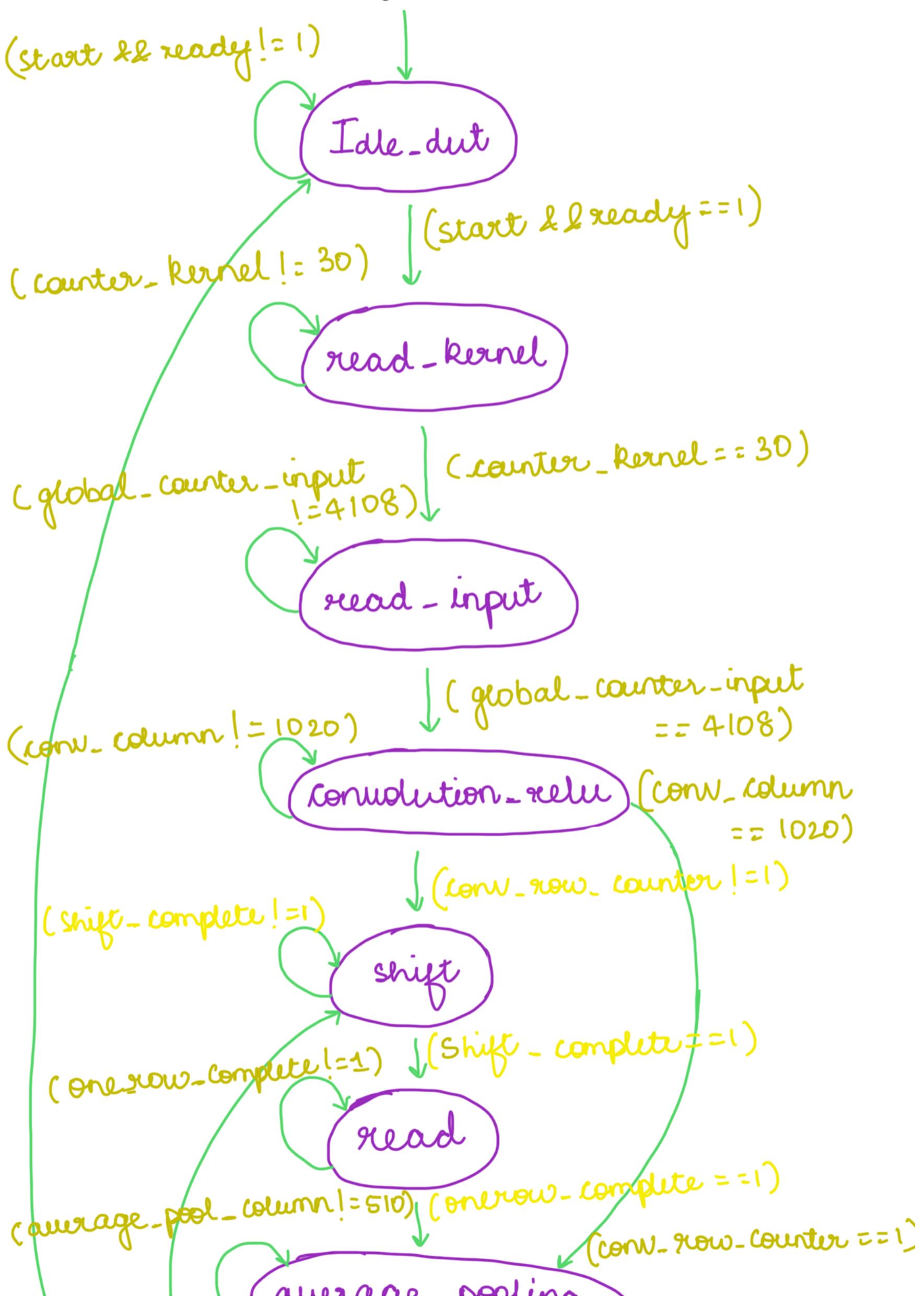
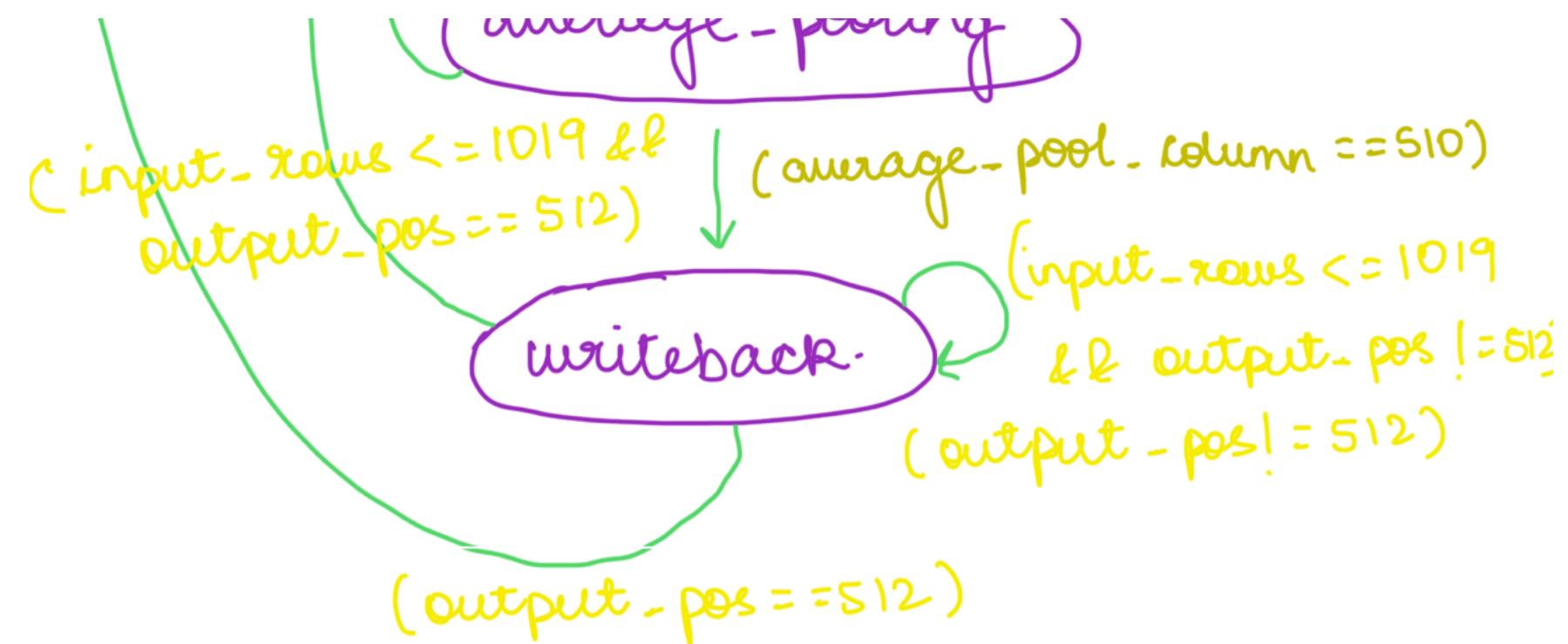


PROJECT REPORT (ECE 564)

Sahishna Mulagaleti

I) Finite State Diagram.





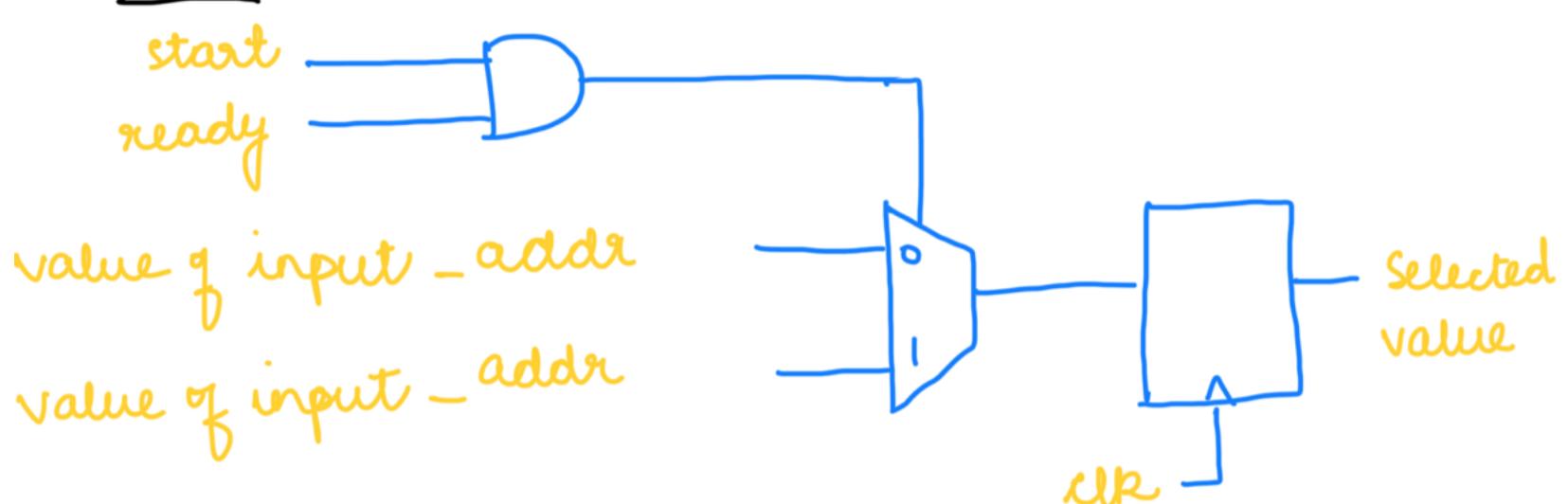
II) FSD States

- 1) idle-dut : Idle state of DUT when no operation is running.
- 2) read-kernel : To read and store the 16 elements of Kernel in a 4×4 matrix.
- 3) read-input : To read and store the first 4 rows of input (4×1024 inputs) from DRAM.
- 4) convolution-relu : To perform convolution of kernel and input and set relu conditions for each element.
- 5) shift : To shift up the elements of the 4×1024 input matrix to get rid of the first row.
- 6) read : To read the next set of 1024 inputs and store them in the last row of the 4×1024 input matrix.
- 7) average-pooling : To perform average pooling of 2 rows of the convolution-relu outputs.
- 8) writeback : To write the outputs of average pooling at the specified address.

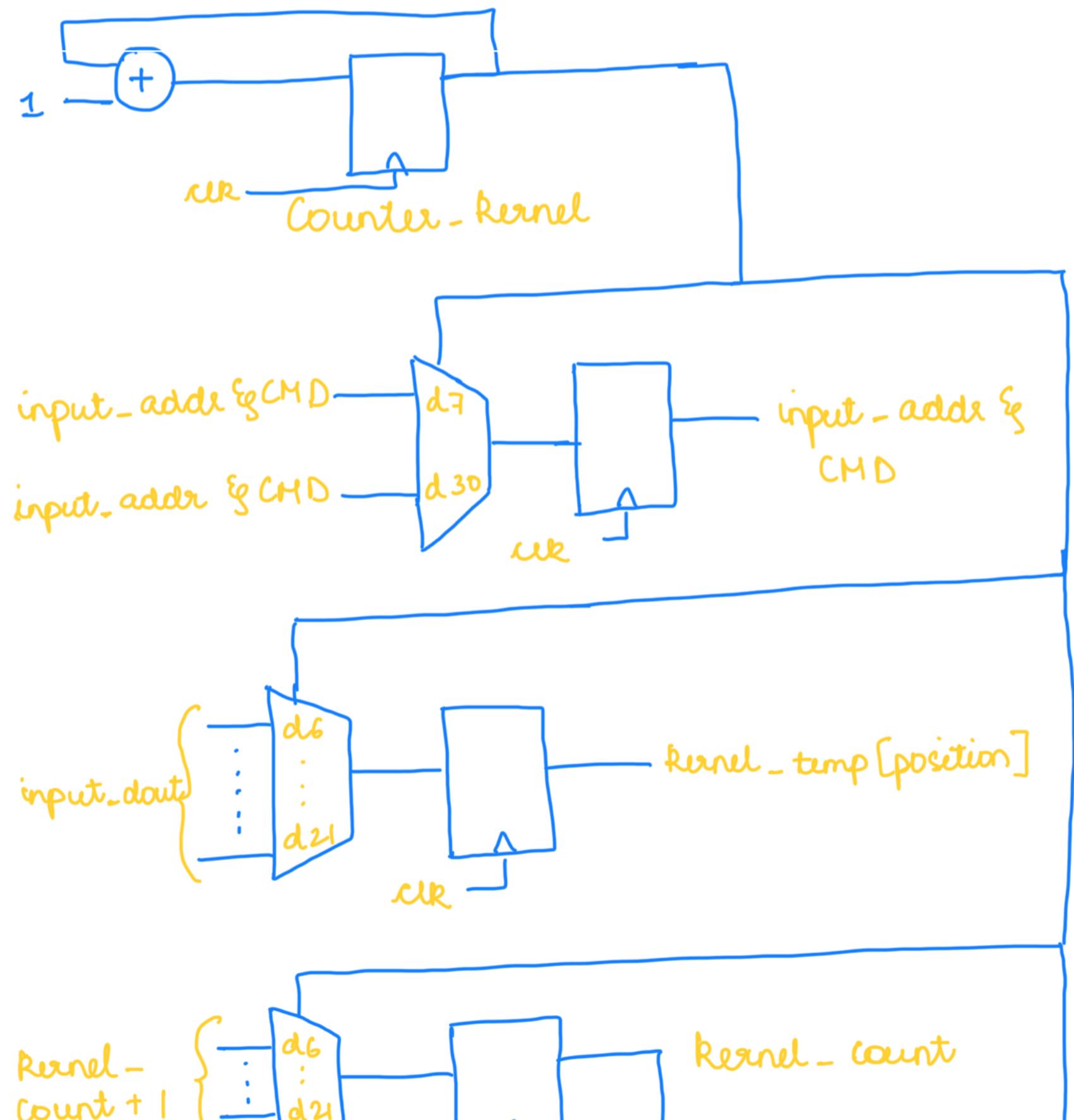
pointing back to UKHW w/ simpler answers.

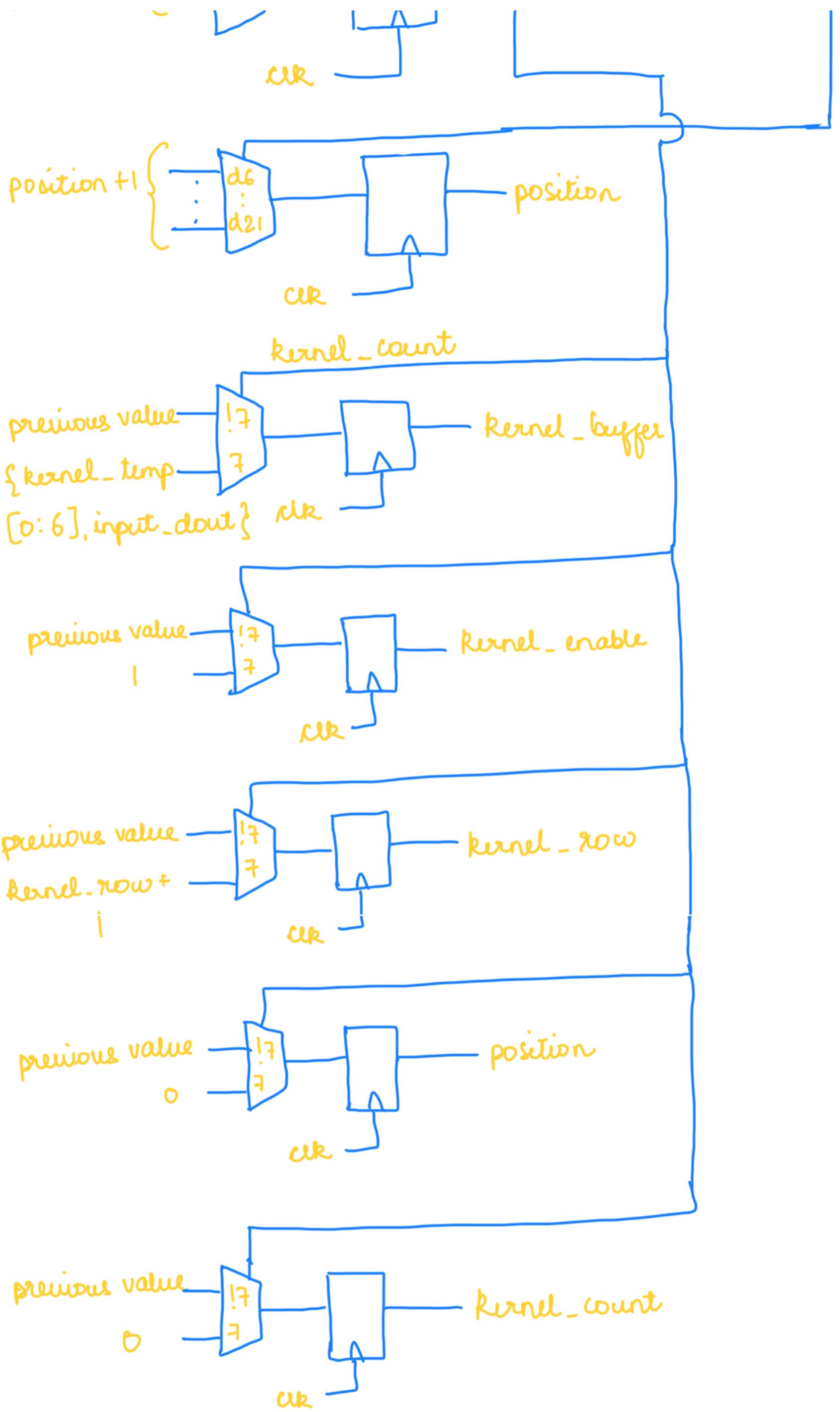
III) logic diagrams

i) Idle-dut state



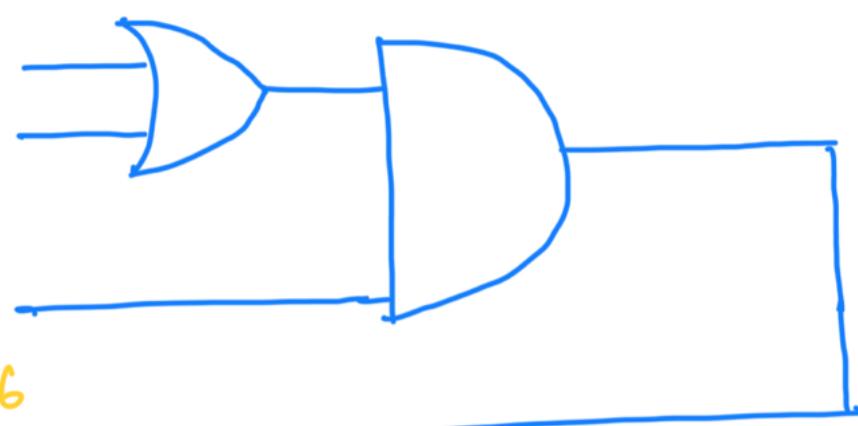
ii) Read-kernel state



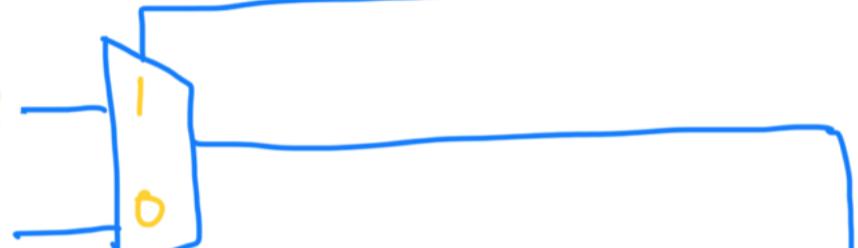


iii) read - input state

counter - input ≥ 7
global - counter -
input ≥ 1023
global - counter -
input ≤ 4096



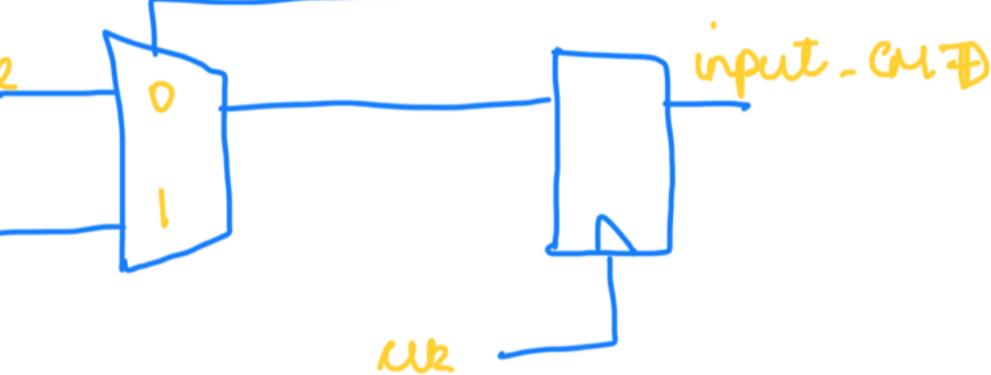
Address - counter = 7
Address - counter $\neq 7$



Address counter

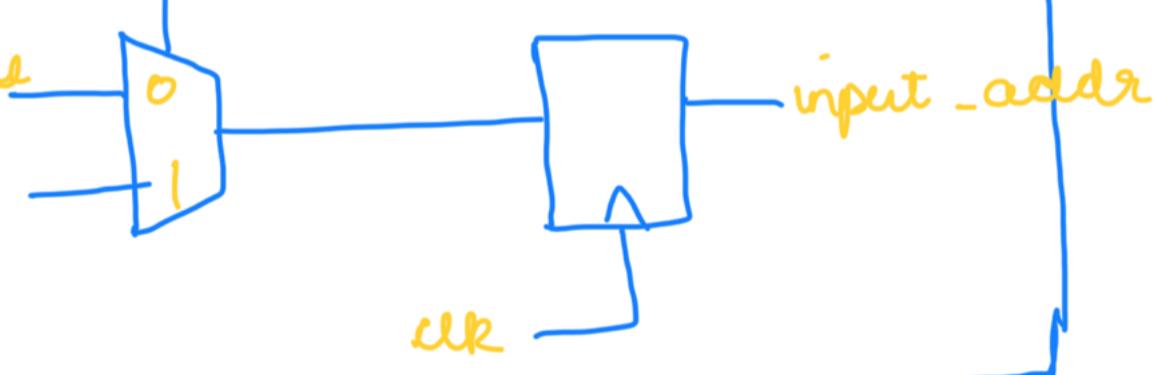
Previous value

1



Previous value

input - add
+ 8



Previous value

1



counter - input
+ 1

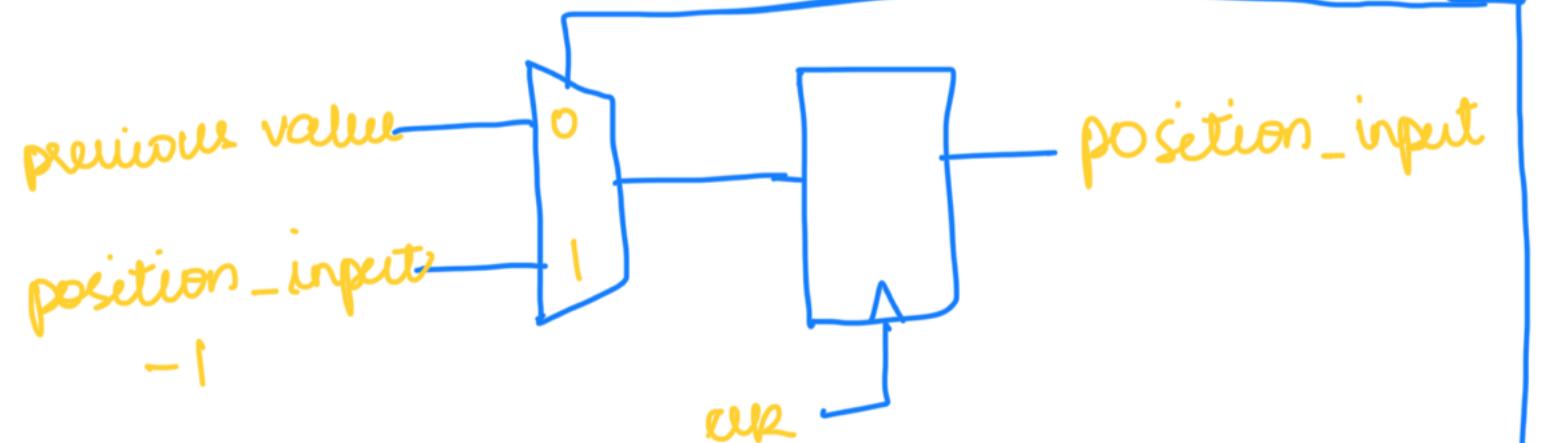
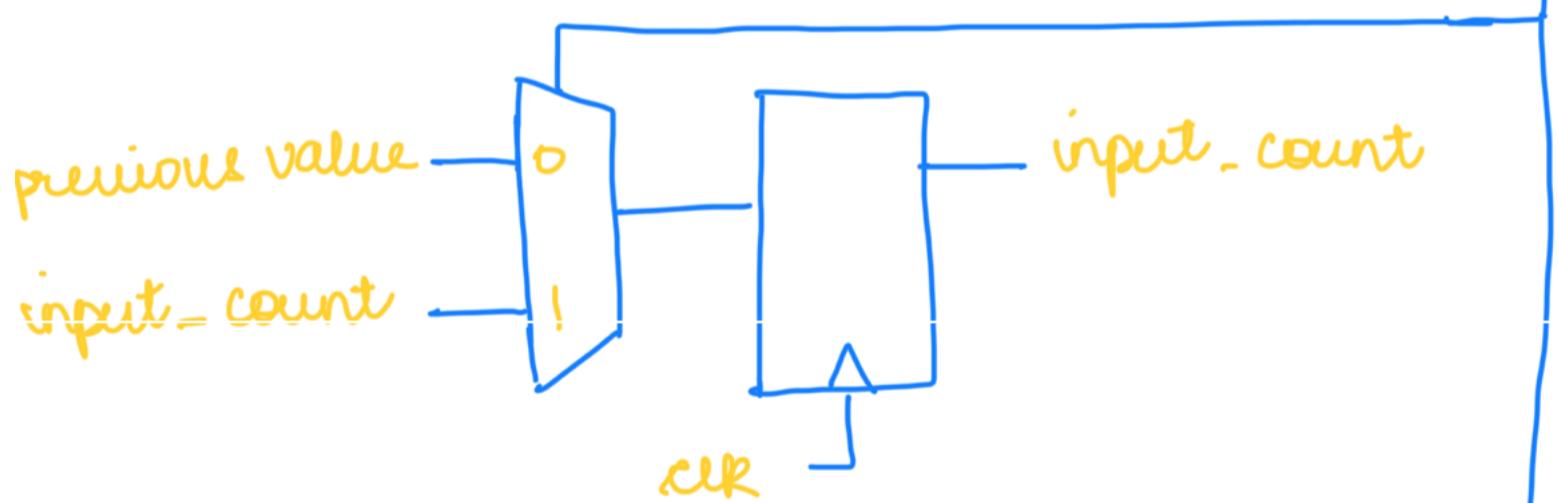
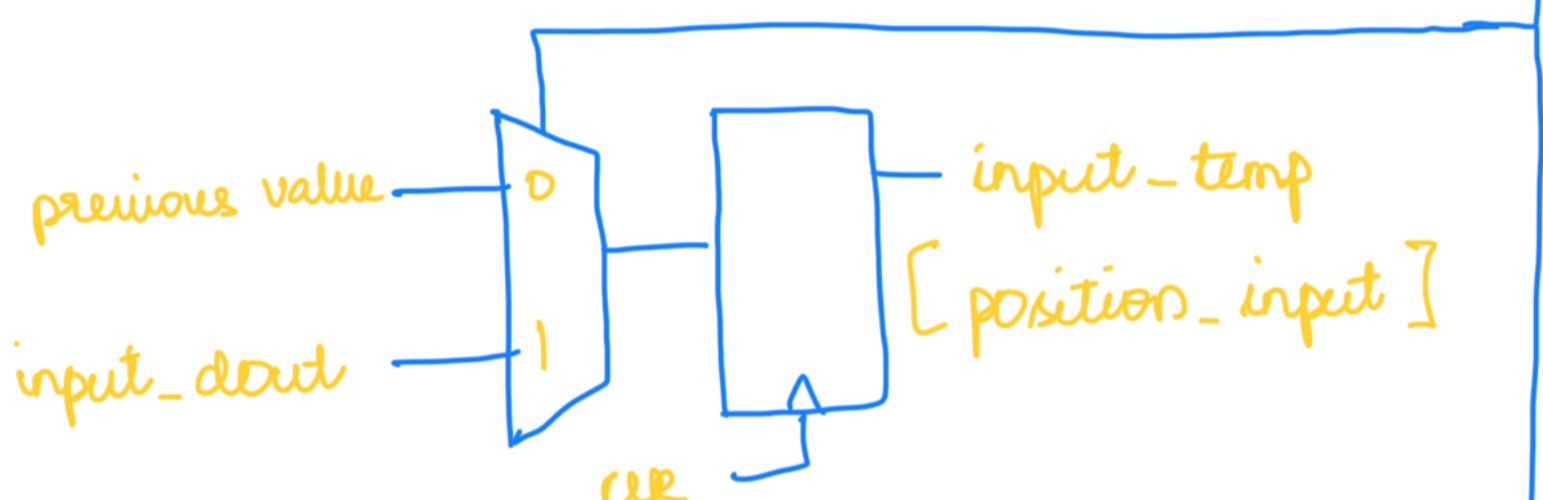
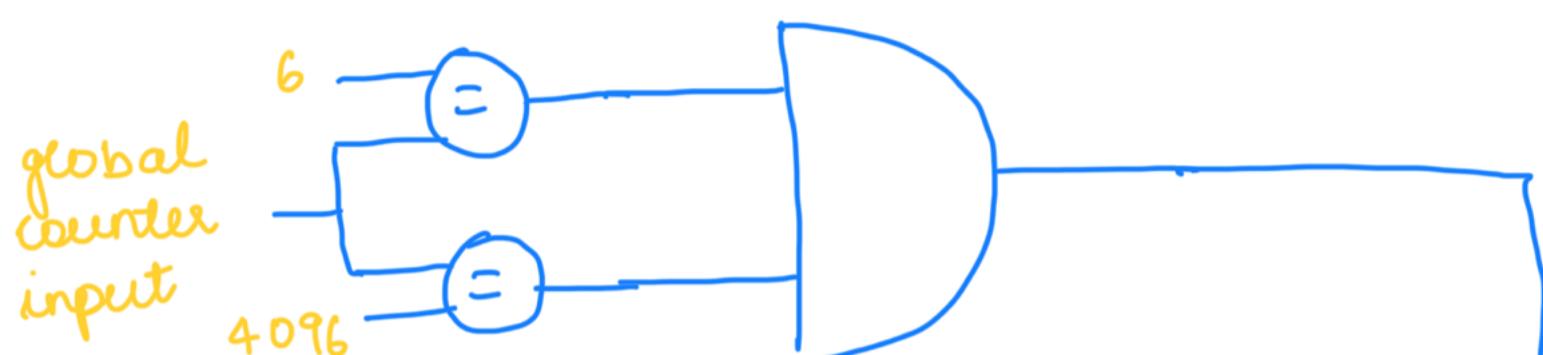
0

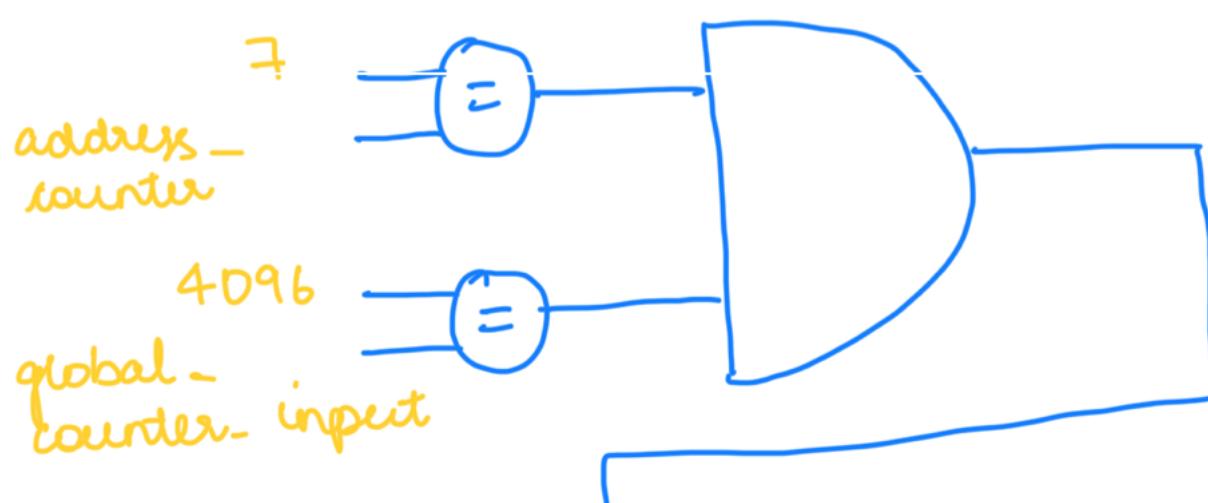
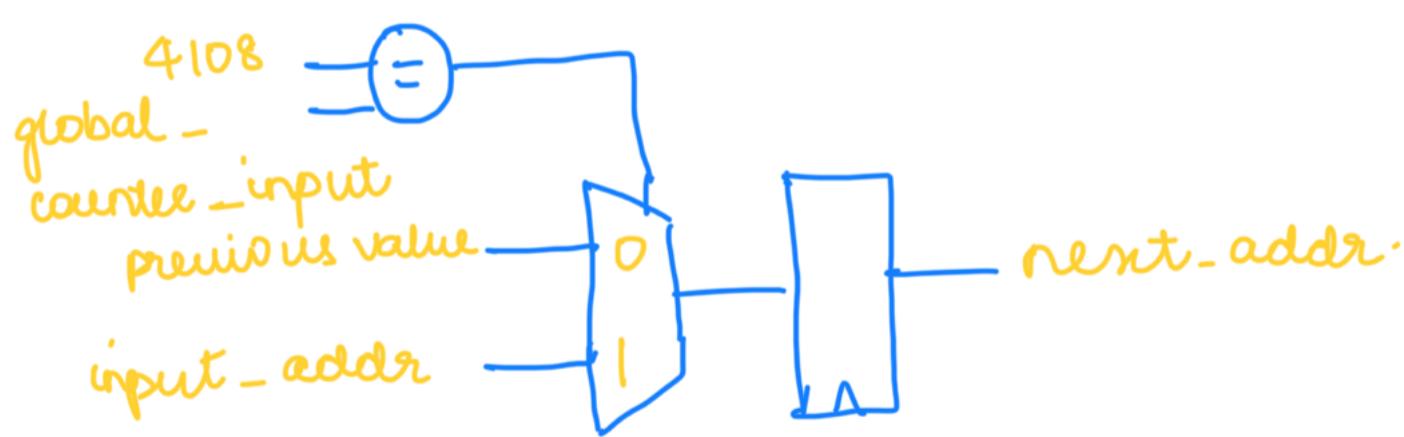
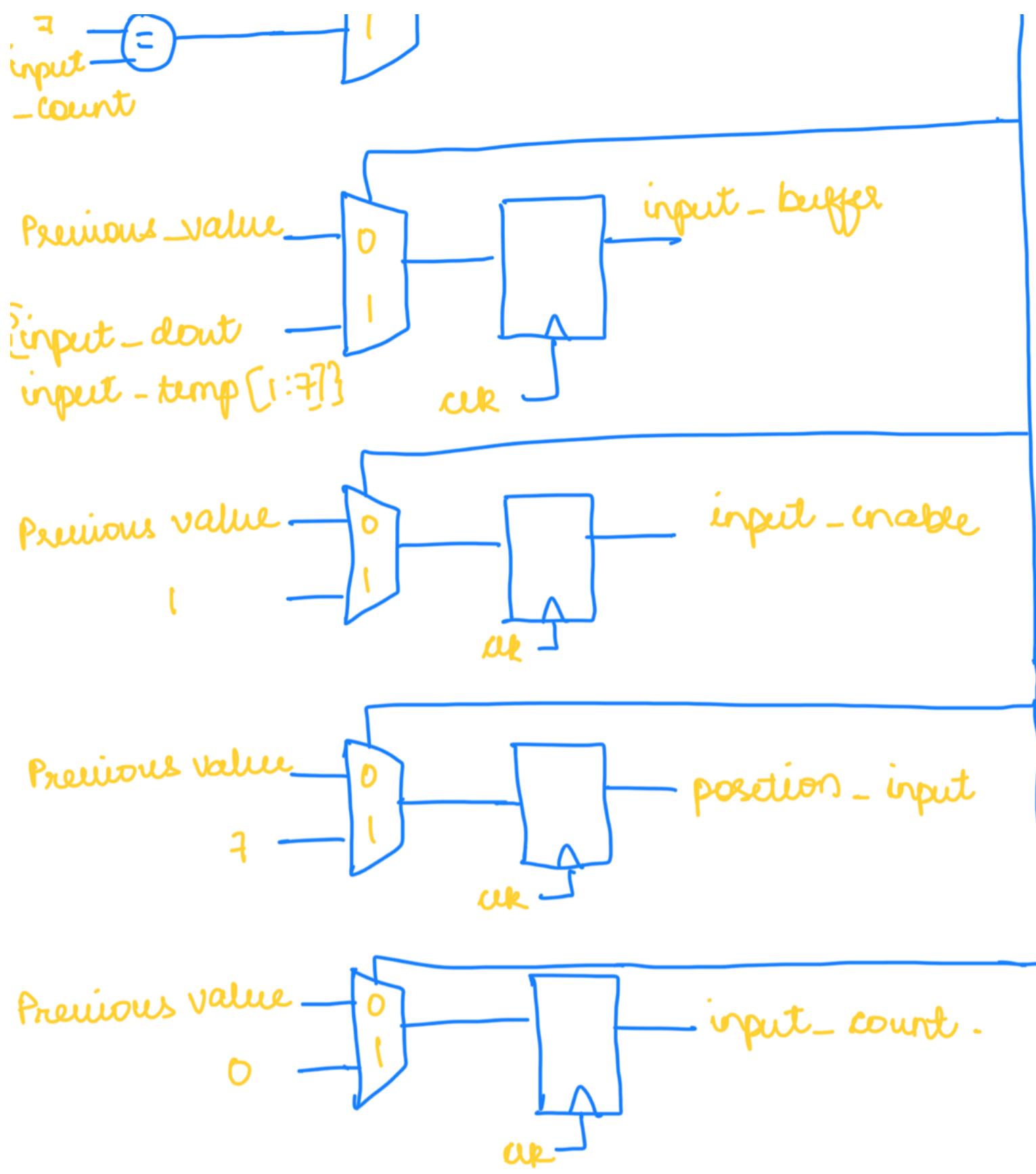


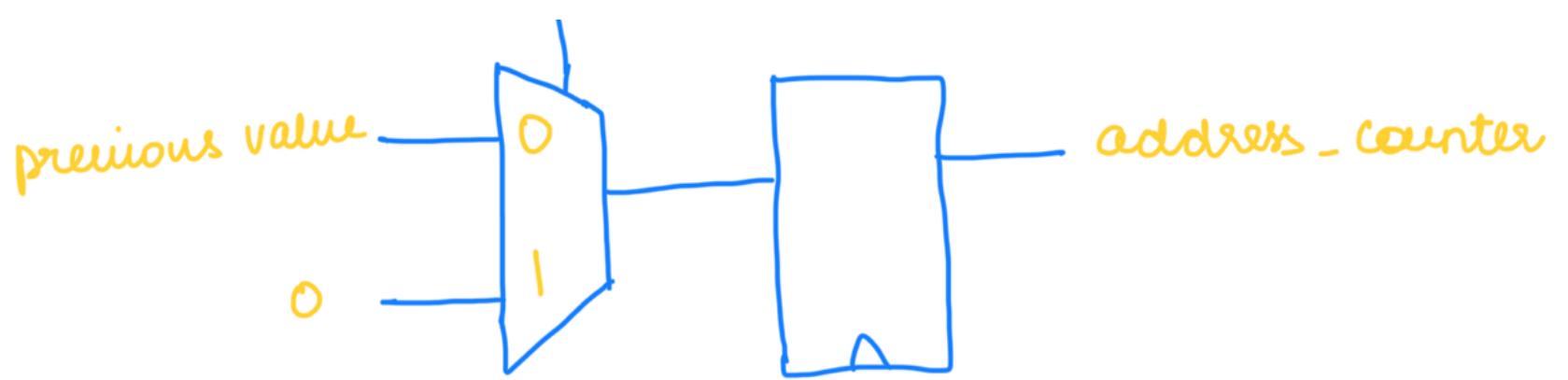
counter - input

1023

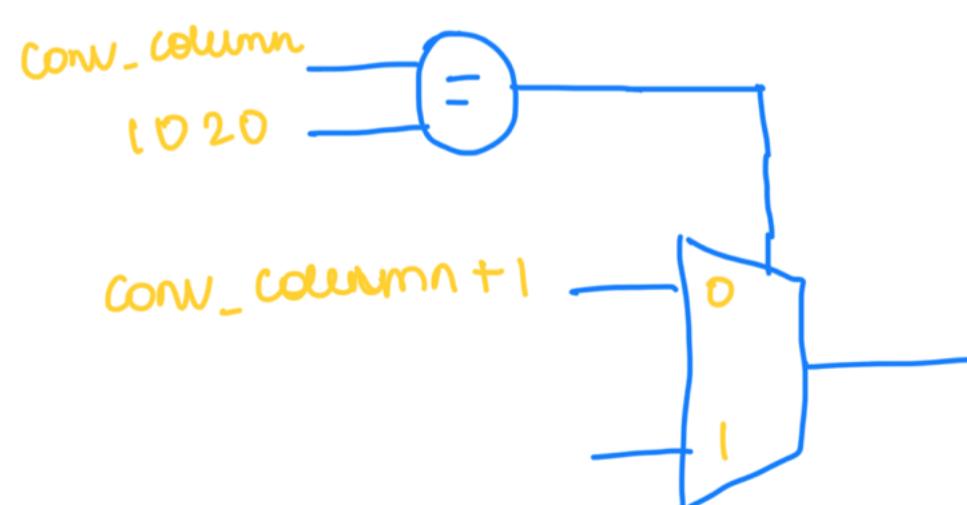
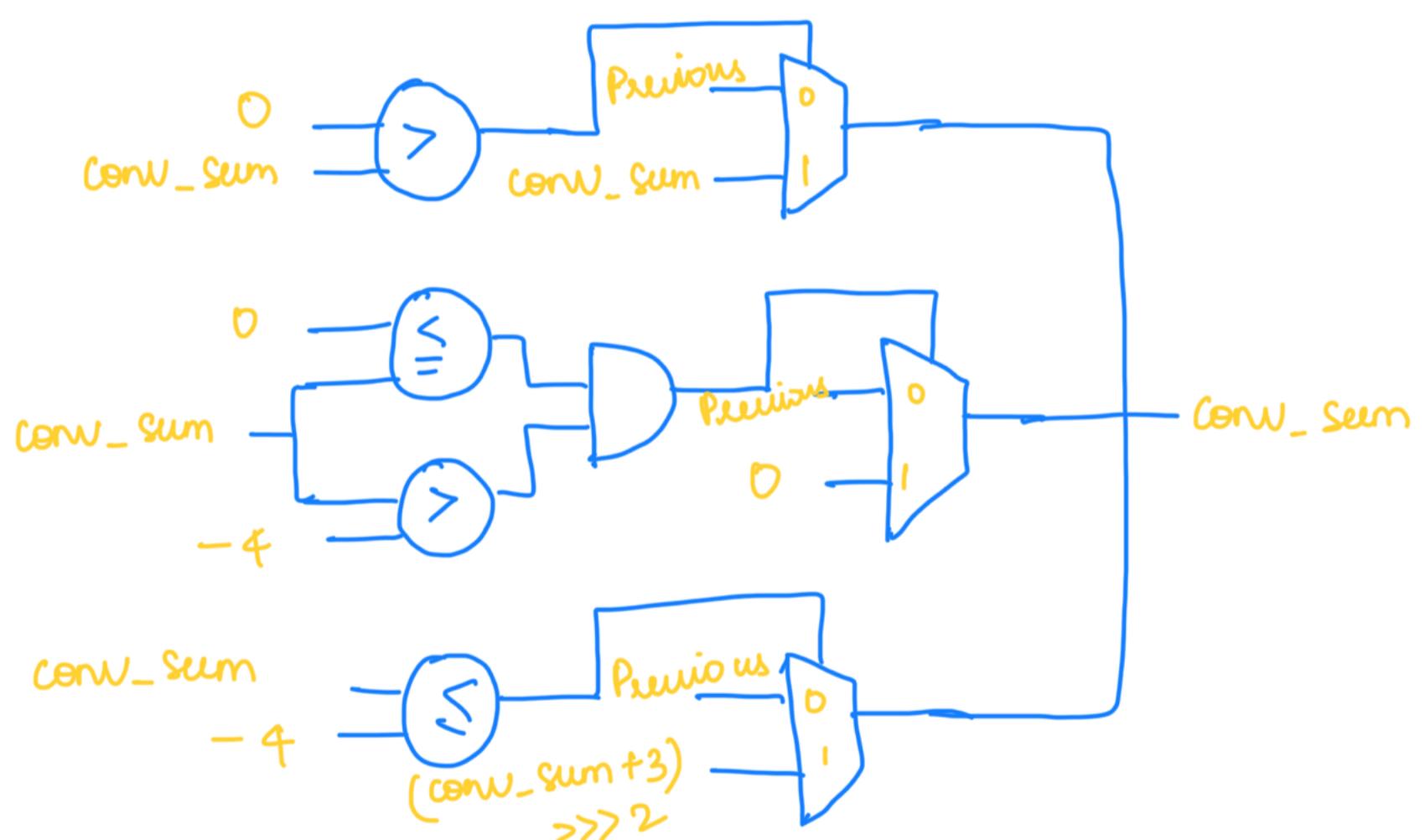
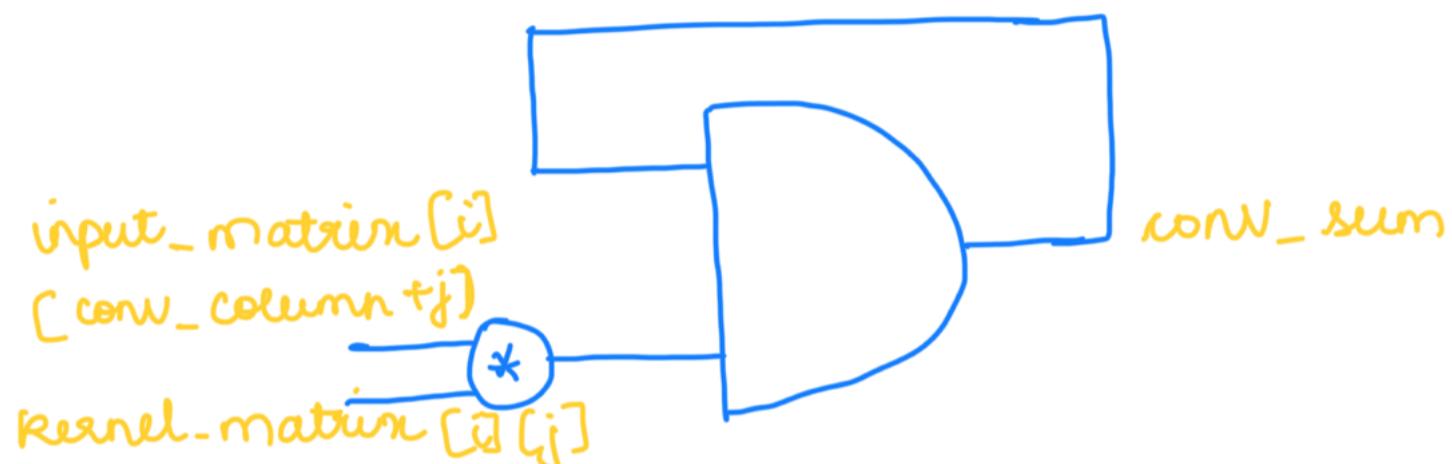
counter - input



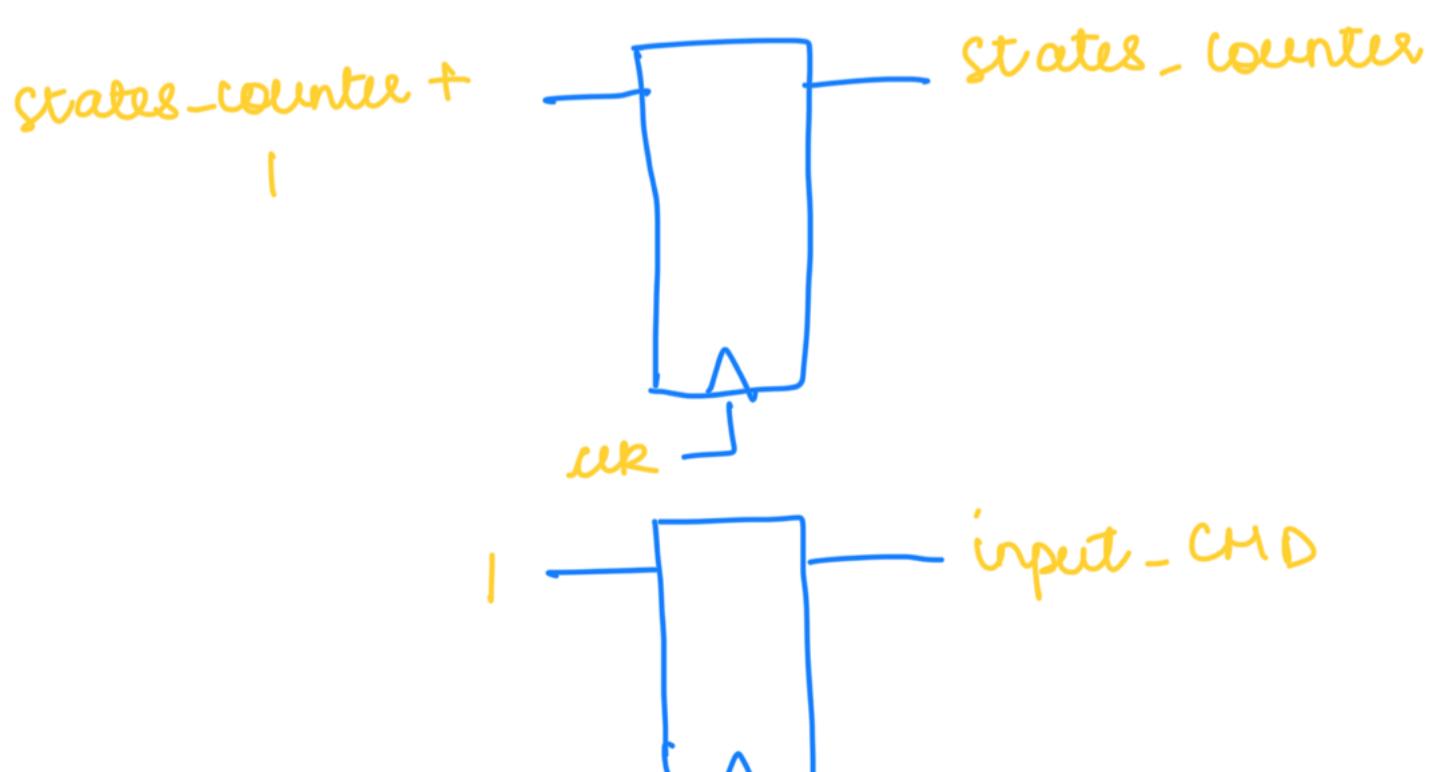
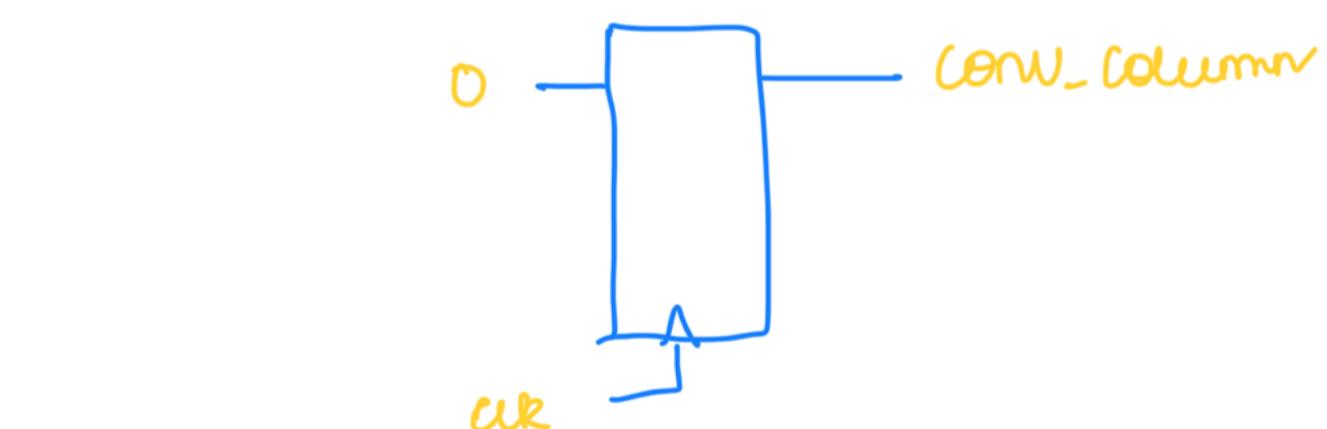
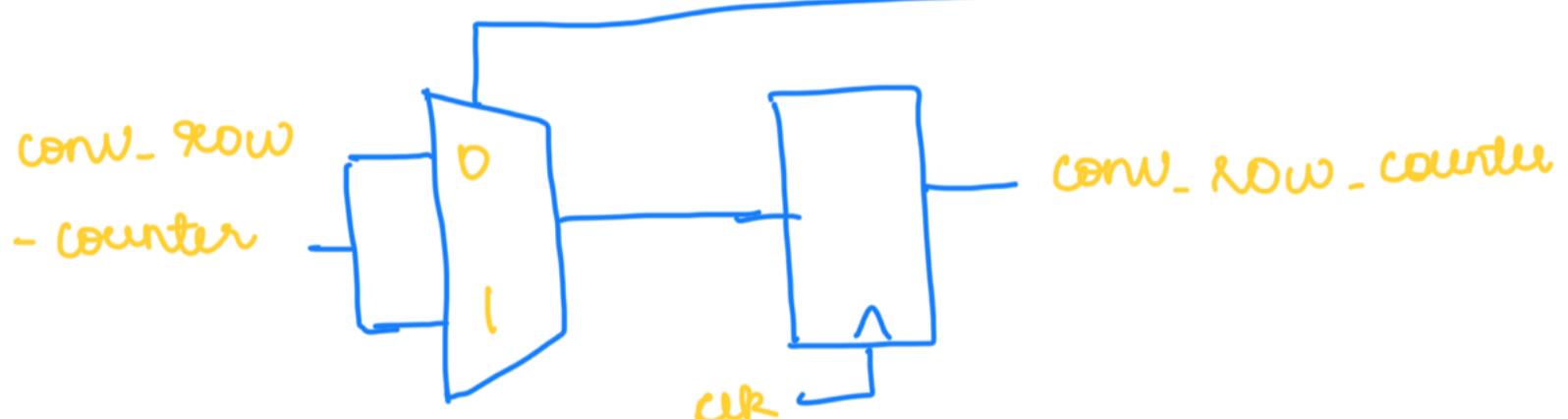
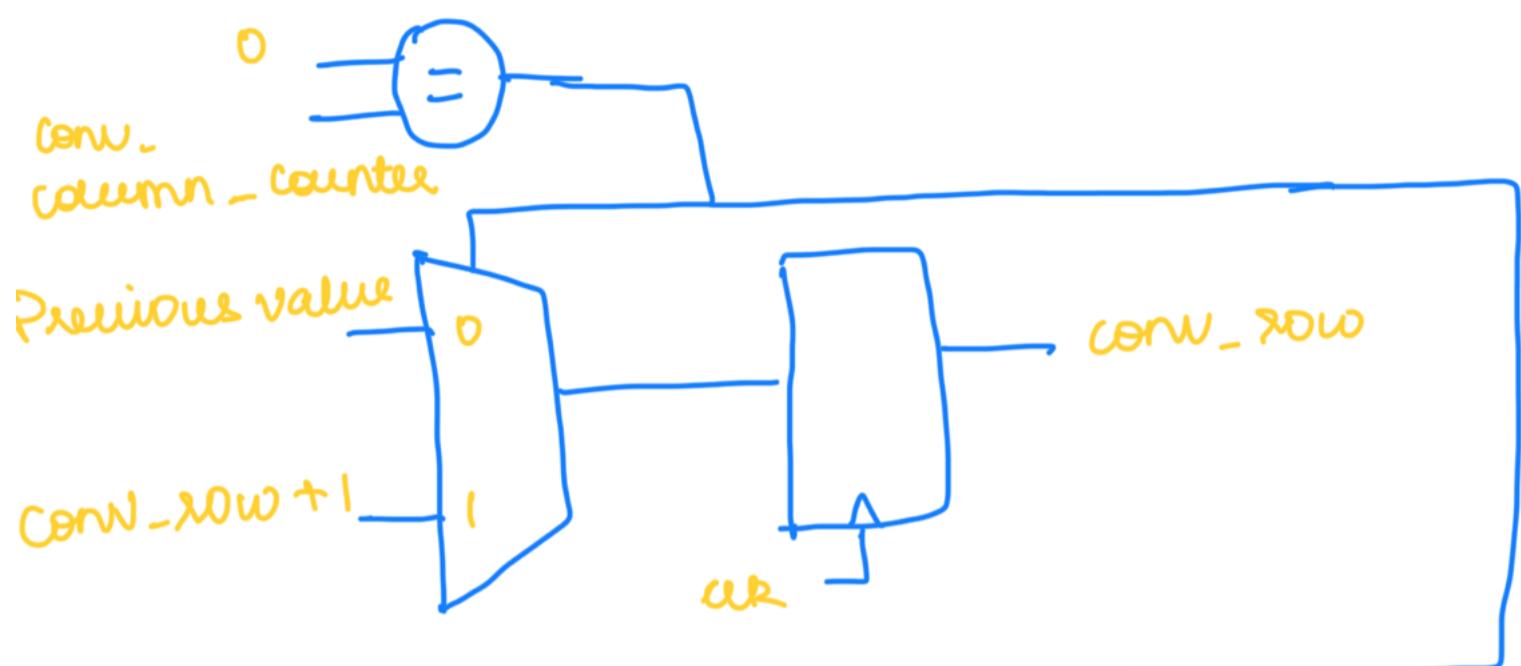


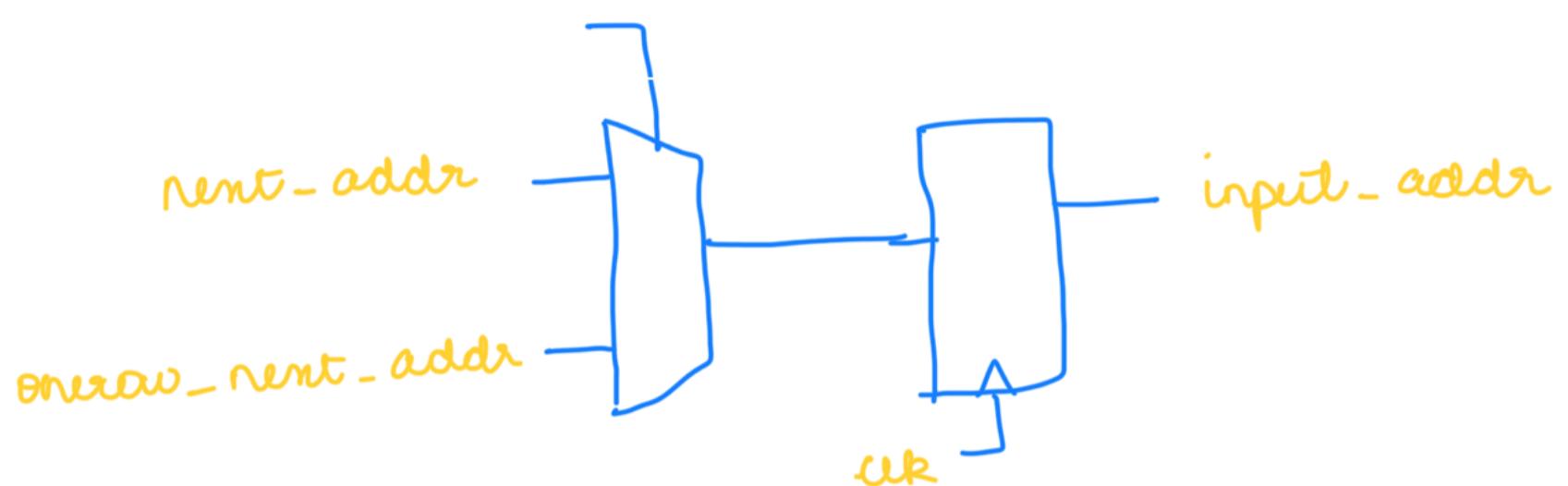
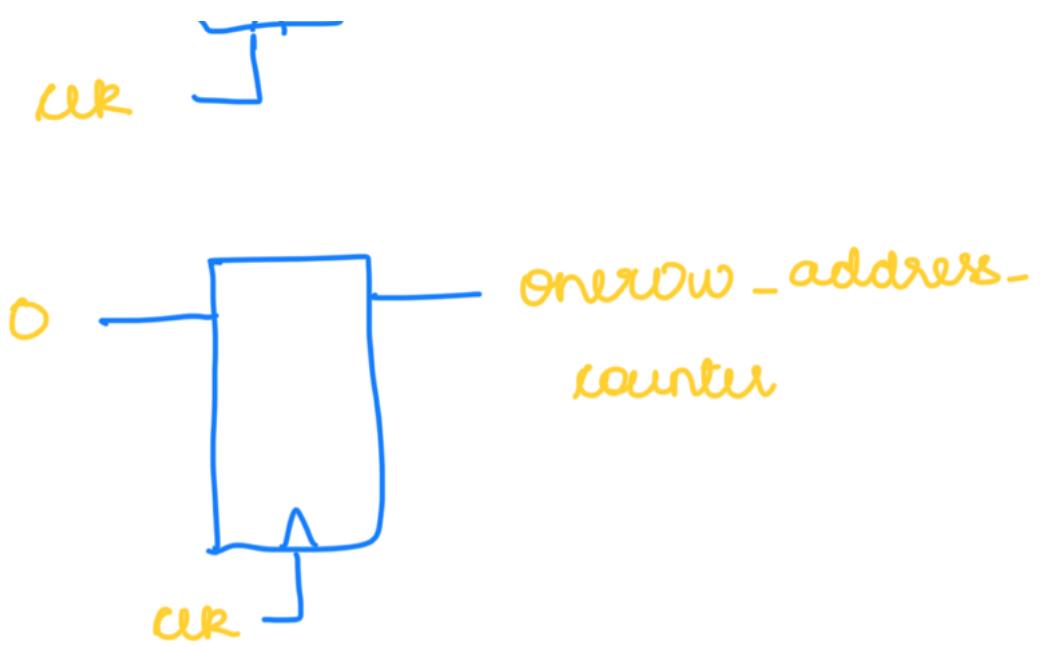


iv) Convolution_relu State



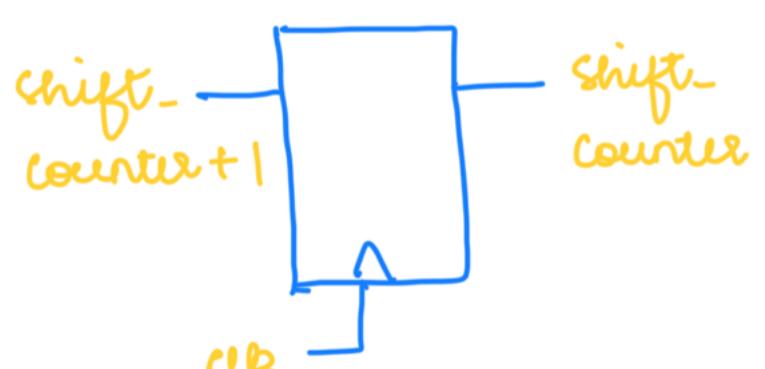
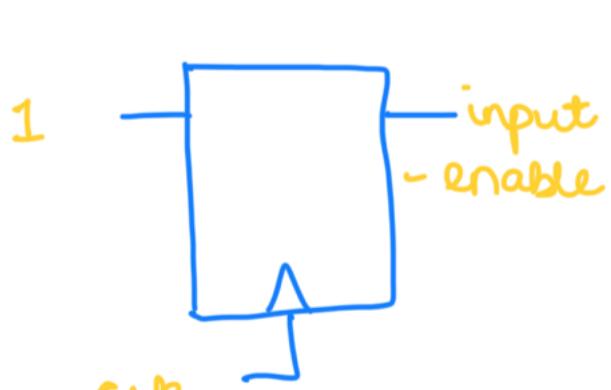
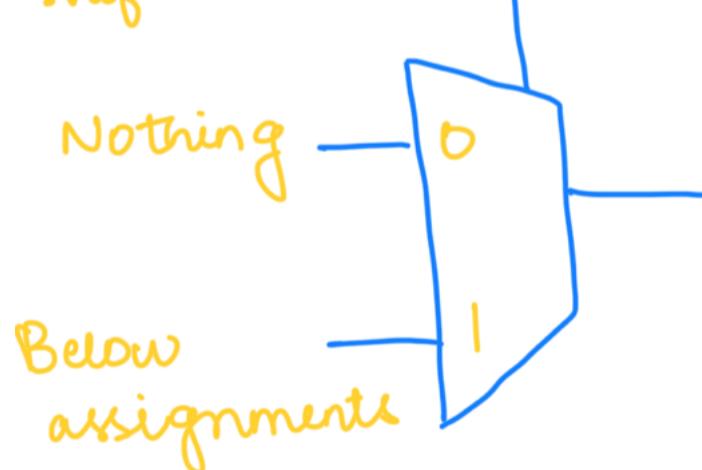
convolution_relu_matrix[conv_row]



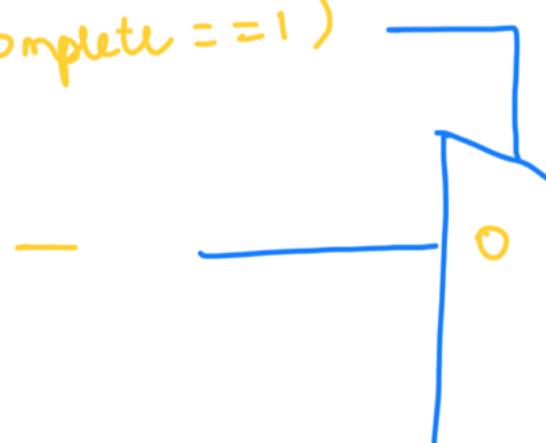


v) shift state

shift-counter? $\rightarrow 0$

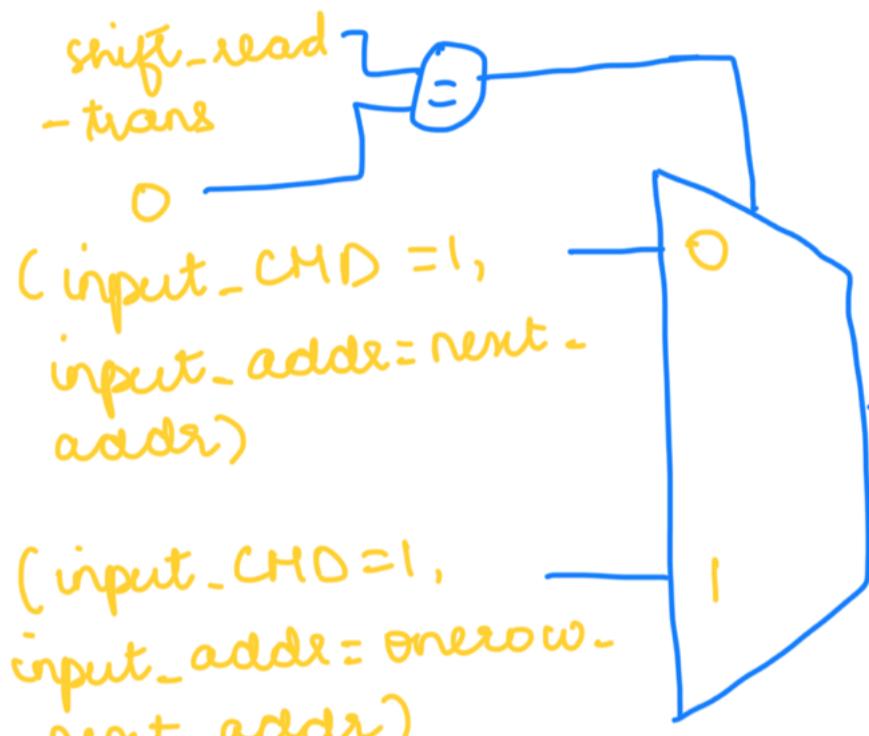


$(\text{shift-complete} == 1)$



Input register

$(\text{shift_counter} = 0,$
 $\text{onrow_pos} = 7, \text{input_CMD}$
 $= 1, \text{shift_read_trans}$
 $= \text{shift_read_trans} + 1,$
 $\text{input_enable} = 0)$

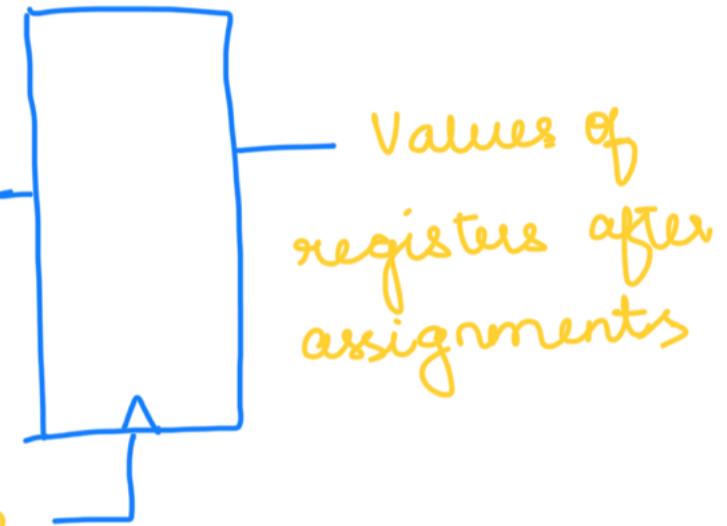


values after assignment

UR

$(\text{input_CMD} = 1,$
 $\text{input_addr} = \text{next_addr})$

$(\text{input_CMD} = 1,$
 $\text{input_addr} = \text{onrow_next_addr})$



Values of registers after assignments

UR

vi) read state

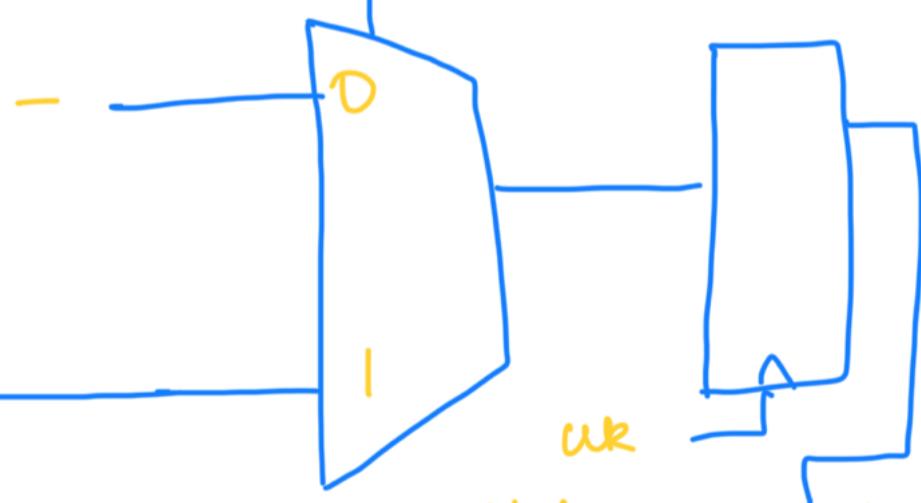
$\text{onrow_counter} \geq 0$
 $\text{onrow_counter} \leq 1023$



$\text{onrow_address_counter} = 20$

$\text{onrow_address_counter} + 1$

$(\text{input CMD} = 1,$
 $\text{input addr} + 8,$
 $\text{onrow_address_counter} = 0)$



Value of registers after assignments

$\text{onrow_counter} \geq 6$

$\text{onrow_counter} \leq 1031$

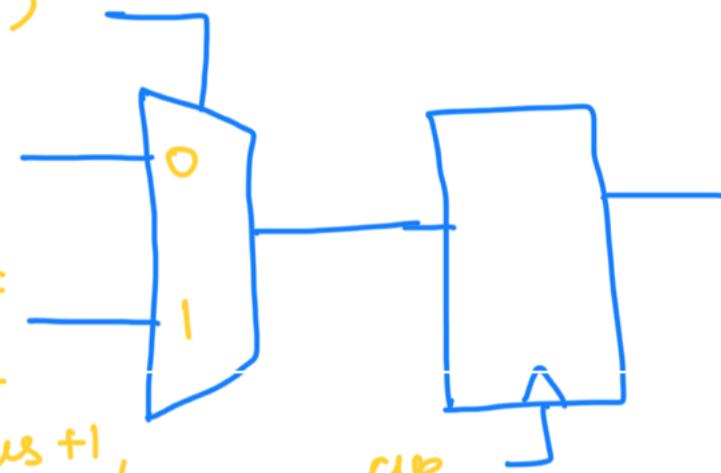


$(\text{input_Temp}[\text{onrow_pos}]$
 $= \text{input_dout}, \text{onrow_count} + 1,$
 $\text{onrow_count} = 7, \text{onrow_pos} - 1)$



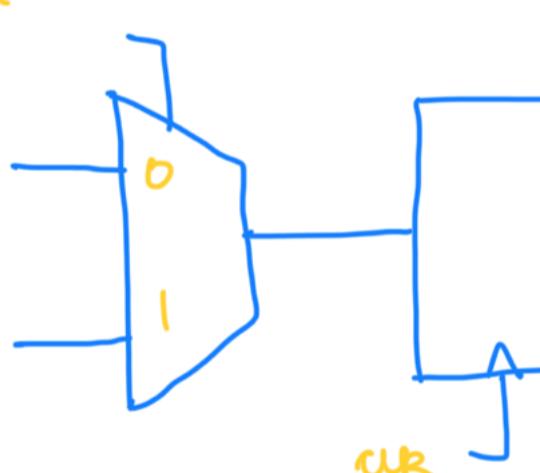

✓
 u_k
 Value of
registers
after assignment

input_buffer
 $= \{ \text{input_dout}, \text{input_temp}[1:7] \}$, $\text{input_enable} = 1$, $\text{onew_pos} = 0$, $\text{onew_count} = 0$
 $(\text{onew_complete} = z1)$

$\text{onew_counter} + 1$

 Value of
register after
assignments.
 $\text{onew_next_addr} = \text{input_addr}$, $\text{onew_counter} = 0$, $\text{input_rows} + 1$, $\text{onew_count} = 0$

vii) Average pooling state

$\text{average_pool_column} \leq 510$


 average-pool
 $[\text{average_pool}$
 $- \text{column}]$.

$(\text{average_pool_column} == 510)$

$\text{average_pool_column} + 1$

 Value of
register
after assignmen

$\text{states counter} \geq 2$

$\text{CMD} = 2$

$\text{addre} = 0$

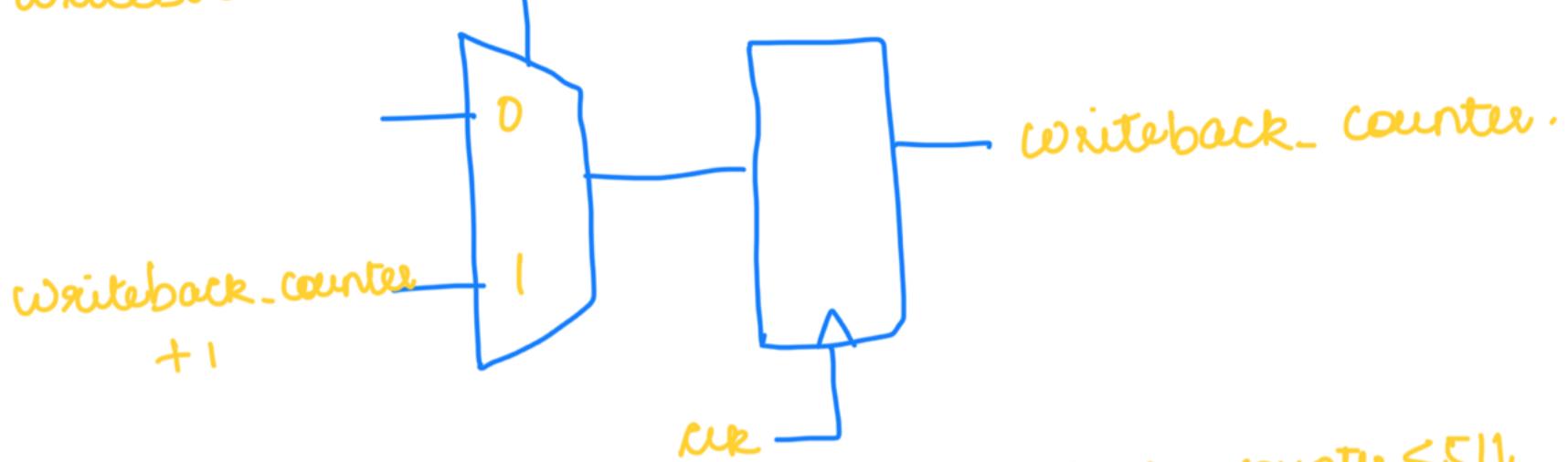
$\text{CMD} = 2$

writeback

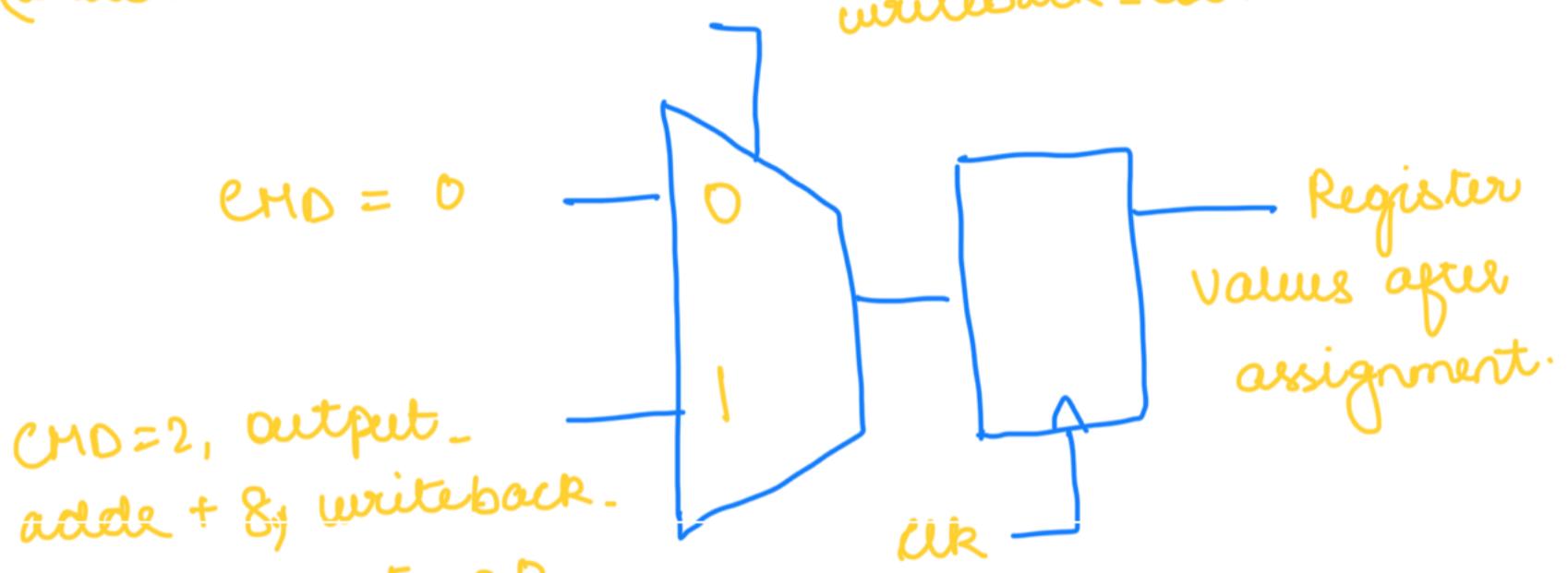
$\text{average_pool}[511] = 0$, $\text{average_pool_column} = 0$
 - next_addr $\text{average_pool}[511] = 0$, $\text{average_pool_column} = 0$
 $\text{average_pool_bufee} = \{ \text{average_pool} [\text{average_pool_pos} + 1] + \dots + \text{average_pool} [\text{average_pool_pos} + 0] \}$

viii) Writeback state

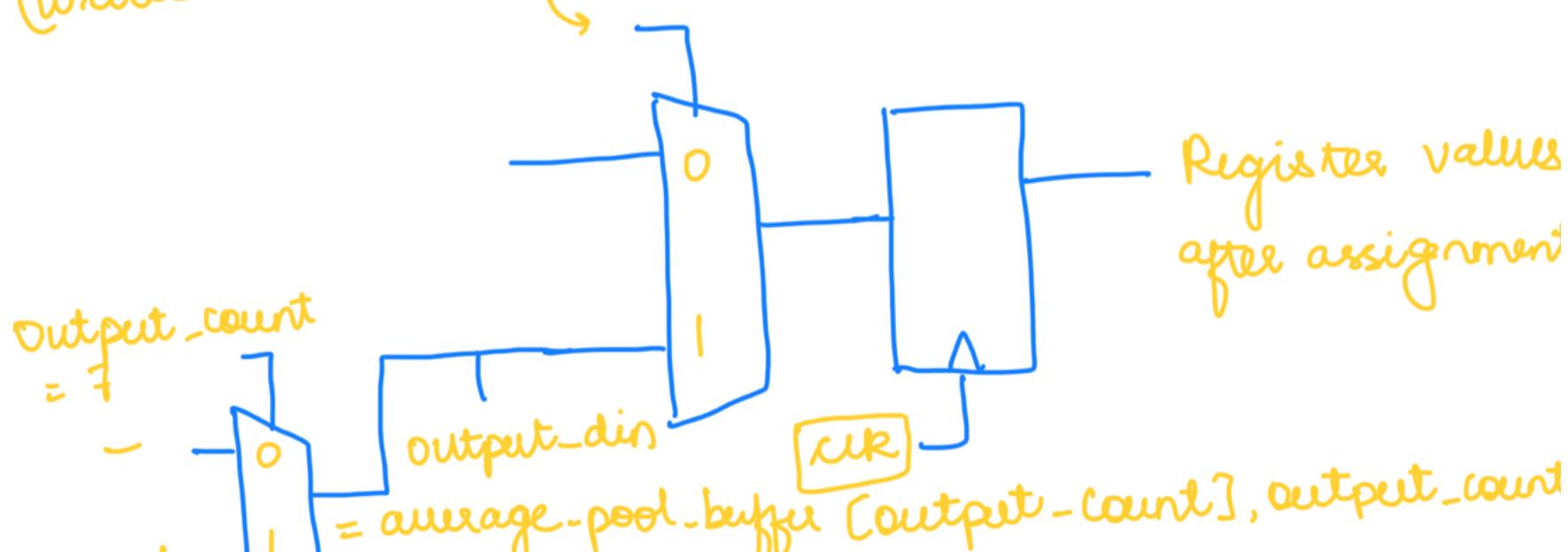
writeback_counter ≥ 600



(write back . address - counter == 7 & writeback - counter < 511 ,
writeback - counter == 511)



(writeback - counter ≥ 4 & output - pos < 512)



average - pool - buffer : {average - pool [average - pool - pos + 7] + ...
+ average - pool [average - pool - pos + 0]}, average - pool -
pos + 8

(output - pos == 512)



writeback_nent_addr
 $= \text{output_addr} + 8$,
 conv_row_counter = 0,
 conv_row = 0, output_pos
 $= 0$, writeback_counter = 0,
 writeback_address_counter = 0, clk
 output_count = 0, input_addr = oneRow_nent_addr,
 oneRow_address_counter = 0, input_CMD = 1, average_pool_pos = 1



Register values after assignment

IV) Reports

DCC_clock = 38

	timing_min_fast_holdcheck_tut1.rpt	timing_max_slow_holdfixed_tut1.rpt	timing_max_slow.rpt	cell_report_final.rpt
C:	> Users > sahis > AppData > Roaming > MobaXterm > slash > mx86_64b > RemoteFiles > 200260_2_1 >			timing_min_fast_holdcheck_tut1.rpt
17	Wire Load Model Mode: top			
18				
19	Startpoint: input_instance/row_reg[28]			
20	(rising edge-triggered flip-flop clocked by clk)			
21	Endpoint: input_instance/row_reg[28]			
22	(rising edge-triggered flip-flop clocked by clk)			
23	Path Group: clk			
24	Path Type: min			
25				
26	Point	Incr	Path	
27				
28	clock clk (rise edge)	0.0000	0.0000	
29	clock network delay (ideal)	0.0000	0.0000	
30	input_instance/row_reg[28]/CK (DFFR_X1)	0.0000 #	0.0000 r	
31	input_instance/row_reg[28]/Q (DFFR_X1)	0.0695	0.0695 r	
32	U312264/Z (XOR2_X1)	0.0177	0.0872 f	
33	input_instance/row_reg[28]/D (DFFR_X1)	0.0000	0.0872 f	
34	data arrival time		0.0872	
35				
36	clock clk (rise edge)	0.0000	0.0000	
37	clock network delay (ideal)	0.0000	0.0000	
38	clock uncertainty	0.0500	0.0500	
39	input_instance/row_reg[28]/CK (DFFR_X1)	0.0000	0.0500 r	
40	library hold time	0.0020	0.0520	
41	data required time		0.0520	
42				
43	data required time		0.0520	
44	data arrival time		-0.0872	
45				
46	slack (MET)		0.0352	
47				

	timing_min_fast_holdcheck_tut1.rpt	timing_max_slow_holdfixed_tut1.rpt	timing_max_slow.rpt	cell_report_final.rpt
C:	> Users > sahis > AppData > Roaming > MobaXterm > slash > mx86_64b > RemoteFiles > 200260_2_2 >			timing_max_slow_holdfixed_tut1.rpt
15	Wire Load Model Mode: top			
66	intadd_1/U7/CO (FA_X1)	0.5172	20.5195 f	
67	intadd_1/U6/CO (FA_X1)	0.5172	21.0367 f	
68	intadd_1/U5/CO (FA_X1)	0.5172	21.5540 f	
69	intadd_1/U4/CO (FA_X1)	0.5172	22.0712 f	
70	intadd_1/U3/CO (FA_X1)	0.5172	22.5885 f	
71	intadd_1/U2/S (FA_X1)	0.8395	23.4280 r	
72	U314104/ZN (NAND4_X1)	0.1182	23.5462 f	
73	U314105/ZN (NOR4_X1)	0.5735	24.1197 r	
74	U314106/ZN (NAND3_X1)	0.1754	24.2951 f	
75	U209581/ZN (OAI21_X2)	1.1133	25.4084 r	
76	U211534/ZN (INV_X4)	0.4794	25.8879 f	
77	U209549/ZN (INV_X1)	0.7422	26.6301 r	
78	U314170/ZN (AOI211_X1)	0.2914	26.9216 f	
79	U314171/ZN (AOI21_X1)	1.3673	28.2889 r	
80	U314172/ZN (INV_X2)	0.4284	28.7173 f	
81	U463488/ZN (INV_X1)	0.8416	29.5589 r	
82	U212877/ZN (INV_X4)	0.2983	29.8572 f	
83	U212853/ZN (INV_X1)	0.7878	30.6449 r	
84	U317092/ZN (OAI22_X1)	0.3085	30.9534 f	
85	convolution_relu_matrix reg[1][125][10]/D (DFF_X1)	0.0000	30.9534 f	

```

86 data arrival time                                30.9534
87
88 clock clk (rise edge)                          38.0000 38.0000
89 clock network delay (ideal)                   0.0000 38.0000
90 clock uncertainty                            -0.0500 37.9500
91 convolution_relu_matrix_reg[1][125][10]/CK (DFF_X1) 0.0000 37.9500 r
92 library setup time                           -0.4047 37.5453
93 data required time                           37.5453
94 -----
95 data required time                           37.5453
96 data arrival time                           -30.9534
97 -----
98 slack (MET)                                 6.5919
99

```

85580				cell_report_final.rpt
C: > Users > sahis > AppData > Roaming > MobaXterm > slash > mx86_64b > RemoteFiles > 200260_2_4 >				cell_report_final.rpt
785581	writeback_next_addr_reg[22]	DFFR_X1	NangateOpenCellLibrary_PDKv1_2_v2008_10_slow_nldm	
785582			5.5860 n	
785583				
785584	writeback_next_addr_reg[23]	DFFR_X1	NangateOpenCellLibrary_PDKv1_2_v2008_10_slow_nldm	
785585			5.5860 n	
785586				
785587	writeback_next_addr_reg[24]	DFFR_X1	NangateOpenCellLibrary_PDKv1_2_v2008_10_slow_nldm	
785588			5.5860 n	
785589				
785590	writeback_next_addr_reg[25]	DFFR_X1	NangateOpenCellLibrary_PDKv1_2_v2008_10_slow_nldm	
785591			5.5860 n	
785592				
785593	writeback_next_addr_reg[26]	DFFR_X1	NangateOpenCellLibrary_PDKv1_2_v2008_10_slow_nldm	
785594			5.5860 n	
785595				
785596	writeback_next_addr_reg[27]	DFFR_X1	NangateOpenCellLibrary_PDKv1_2_v2008_10_slow_nldm	
785597			5.5860 n	
785598				
785599	writeback_next_addr_reg[28]	DFFR_X1	NangateOpenCellLibrary_PDKv1_2_v2008_10_slow_nldm	
785600			5.5860 n	
785601				
785602	writeback_next_addr_reg[29]	DFFR_X1	NangateOpenCellLibrary_PDKv1_2_v2008_10_slow_nldm	
785603			5.5860 n	
785604				
785605	writeback_next_addr_reg[30]	DFFR_X1	NangateOpenCellLibrary_PDKv1_2_v2008_10_slow_nldm	
785606			5.5860 n	
785607				
785608	writeback_next_addr_reg[31]	DFFR_X1	NangateOpenCellLibrary_PDKv1_2_v2008_10_slow_nldm	
785609			5.5860 n	
785610				
785611	-----			
785612	Total 355769 cells		734251.7864	
785613	1			

85580				cell_report_final.rpt
C: > Users > sahis > AppData > Roaming > MobaXterm > slash > mx86_64b > RemoteFiles > 200260_2_3 >				timing_max_slow.rpt
17	Wire Load Model Mode: top			
76	U314106/ZN (NAND3_X1)		0.1754	24.2947 f
77	U209581/ZN (OAI21_X2)		1.1133	25.4080 r
78	U211534/ZN (INV_X4)		0.4794	25.8874 f
79	U209549/ZN (INV_X1)		0.7422	26.6297 r
80	U314170/ZN (AOI211_X1)		0.2914	26.9211 f
81	U314171/ZN (AOI21_X1)		1.3673	28.2885 r
82	U314172/ZN (INV_X2)		0.4284	28.7168 f
83	U463488/ZN (INV_X1)		0.8416	29.5585 r
84	U212877/ZN (INV_X4)		0.2983	29.8567 f
85	U212853/ZN (INV_X1)		0.7878	30.6445 r
86	U317092/ZN (OAI22_X1)		0.3085	30.9530 f
87	convolution_relu_matrix_reg[1][125][10]/D (DFF_X1)		0.0000	30.9530 f
88	data arrival time			30.9530
89	-----			
90	clock clk (rise edge)		38.0000	38.0000
91	clock network delay (ideal)		0.0000	38.0000
92	clock uncertainty		-0.0500	37.9500
93	convolution_relu_matrix_reg[1][125][10]/CK (DFF_X1)		0.0000	37.9500 r
94	library setup time		-0.4047	37.5453
95	data required time			37.5453
96	-----			
97	data required time			37.5453
98	data arrival time			-30.9530
99	-----			
100	slack (MET)			6.5924

