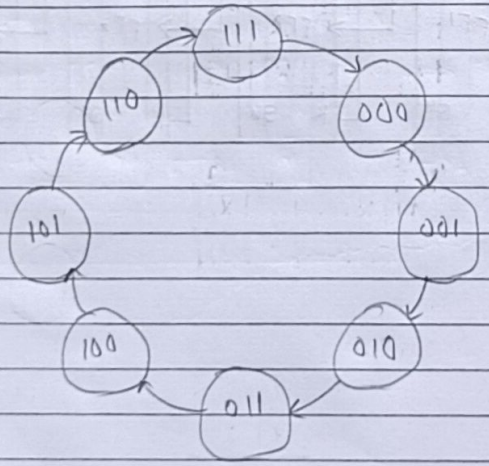
DESIGN OF SYNCHRONOUS COUNTERS

* PROCEDURE:-

1. Derive the state transition diagram
2. Draw state transition table
3. Choose flip-flop type for implementation & use exitation table to rempp next state functions.
4. Obtain the expression for input variables of the flipflop in terms of present state values.
5. Minimize them using K-Maps.
6. Implement the circuit.

(1) Synchronous 3-bit Up Counter. Using JK FF

step 1 - state transition diagram



step 2 & step 3:- (Exitation table)

PS			NS			Inputs					
Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	0	0	0	X	1	X	1	X	1

step 4 & step 5 - Obtaining the input expressions.

* J_0

Q_2 \ Q_1Q_0	00	01	11	10
0	1	X	X	1
1	1	X	X	1

$J_0 = 1$

* K_0

Q_2 \ Q_1Q_0	00	01	11	10
0	X	1	1	X
1	X	1	1	X

$K_0 = 1$

* J_1

Q_2 \ Q_1Q_0	00	01	11	10
0		1	X	X
1		1	X	X

$J_1 = Q_0$

* K_1

Q_2 \ Q_1Q_0	00	01	11	10
0	X	X	1	
1	X	X	1	

$K_1 = Q_0$

* T_2

Q_2 \ Q_1Q_0	00	01	11	10
0			1	
1	X	X	X	X

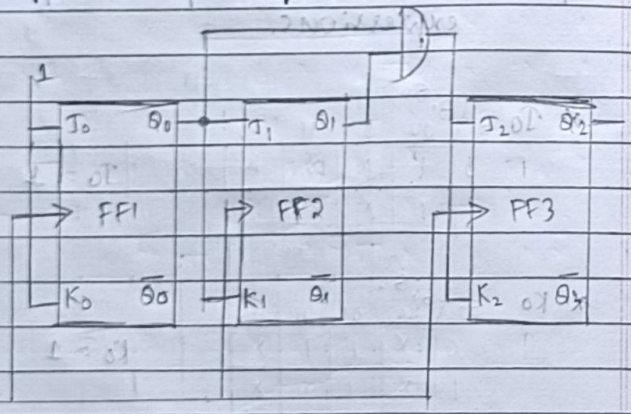
$T_2 = Q_1Q_0$

* K_2

Q_2 \ Q_1Q_0	00	01	11	10
0	X	X	X	X
1			1	

$K_2 = Q_1Q_0$

step 3 :- circuit implementation.



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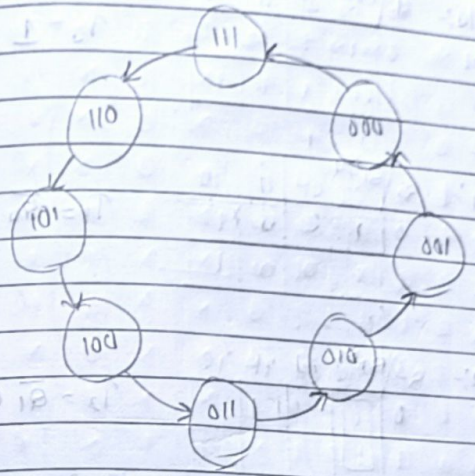
② Synchronous 3-bit Down Counter Using T-FF

step 1 :- state transition diagram



step 2 & step 3 :- Excitation Table

PS			NS			Input		
Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	T_2	T_1	T_0
0	0	0	1	1	1	1	1	1
0	0	1	0	0	0	0	0	1
0	1	0	0	0	1	0	1	1
0	1	1	0	1	0	0	0	1
1	0	0	0	1	1	1	1	1
1	0	1	1	0	0	0	0	1
1	1	0	1	0	1	0	1	1
1	1	1	1	1	0	0	0	1

step 4 & step 5 :- obtaining the input expressions.

* T_0 :-

Q_2 \ Q_1Q_0	00	01	11	10
0	1	1	1	1
1	1	1	1	1

$T_0 = 1$

* T_1 :-

Q_2 \ Q_1Q_0	00	01	11	10
0	1	0	0	1
1	1	0	0	1

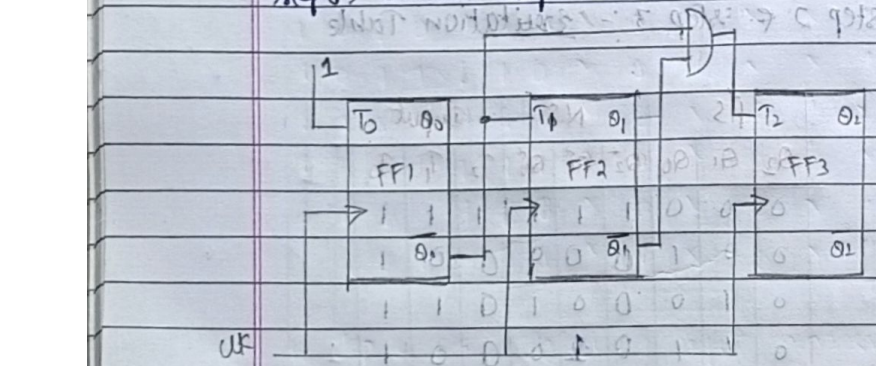
$T_1 = \bar{Q}_0$

* T_2 :-

Q_2 \ Q_1Q_0	00	01	11	10
0	1			
1	1			

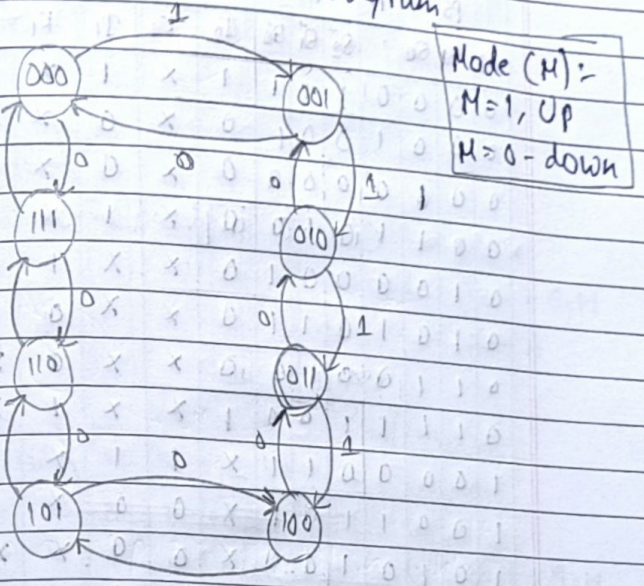
$T_2 = \bar{Q}_1 \bar{Q}_0$

step 6 :- circuit implementation



③ Synchronous 3-bit Up-down Counter Using JK-FF

step 1 :- state transition diagram



step 2 & step 3:-

PS			M	NS			Inputs					
Q_2	Q_1	Q_0		Q_2^+	Q_1^+	Q_0^+	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	1	1	1	1	x	1	x	1	x
0	0	0	1	0	0	1	0	x	0	x	1	x
0	0	1	0	0	0	0	0	x	0	x	x	1
0	0	1	1	0	1	0	0	x	1	x	x	1
0	1	0	0	0	0	1	0	x	x	1	1	x
0	1	0	1	0	1	1	0	x	x	0	1	x
0	1	1	0	0	1	0	0	x	x	0	x	1
0	1	1	1	1	0	0	1	x	x	1	x	1
1	0	0	0	0	1	1	x	1	1	x	1	x
1	0	0	1	1	0	1	x	0	0	x	1	x
1	0	1	0	1	0	0	x	0	0	x	x	1
1	0	1	1	1	1	0	x	0	1	x	x	1
1	1	0	0	1	0	1	x	0	x	1	1	x
1	1	0	1	1	1	1	x	0	x	0	1	x
1	1	1	0	1	1	0	x	0	x	0	x	1
1	1	1	1	0	0	0	x	1	x	1	x	1

step 4 & 5:- Obtaining input expressions.

* J_0

Q_2Q_1 \ Q_0M	00	01	11	10
00	1	1	x	x
01	1	1	x	x
11	1	1	x	x
10	1	1	x	x

$J_0 = 1$

* K_0

Q_2Q_1 \ Q_0M	00	01	11	10
00	x	x	1	1
01	x	x	1	1
11	x	x	1	1
10	x	x	1	1

$K_0 = 1$

* J_1

Q_2Q_1 \ Q_0M	00	01	11	10
00	1		1	
01	x	x	x	x
11	x	x	x	x
10	1		1	

$J_1 = Q_0\bar{M} + Q_0M$
$= Q_0 \odot M$

* K_1

Q_2Q_1 \ Q_0M	00	01	11	10
00	x	x	x	x
01	1		1	
11	1		1	
10	x	x	x	x

$K_1 = \bar{Q_0}\bar{M} + Q_0M$
$= Q_0 \odot M$

* J_2

Q_2Q_1 \ Q_0M	00	01	11	10
00	1			
01			1	
11	x	x	x	x
10	x	x	x	x

$J_2 = \bar{Q_1}\bar{Q_0}M$
$+ Q_1Q_0M$

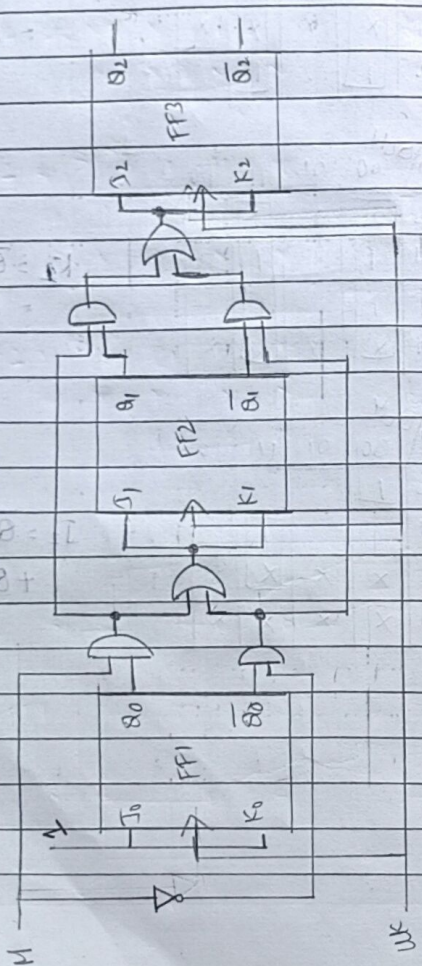
→

* K_2

Q_1Q_0 \ M	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11			1	
10	1			

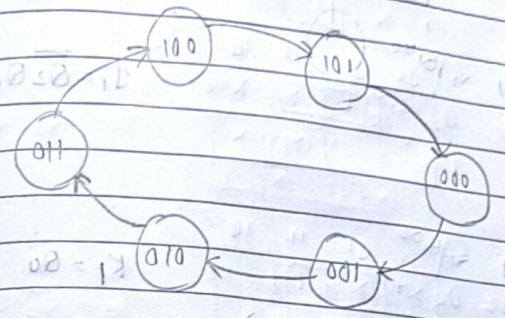
$K_2 = \bar{Q}_1\bar{Q}_0M + Q_1Q_0M$

* step 6:- Circuit implementation



④ Synchronous Mod-6 Counter Using JK-FF

step 1:- state transition diagram



step 2 & step 3

PS			NS			Inputs					
Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	0	0	0	X	1	0	X	X	1

step 4 & 5:- obtaining input expressions

* J_0

Q_2 \ Q_1Q_0	00	01	11	10
0	1	X	X	1
1	1	X	X	X

$J_0 = 1$

* K_0

Q_2 \ Q_1Q_0	00	01	11	10
0	X	1	1	X
1	X	1	X	X

$K_0 = 1$

* J_1

Q_2 \ Q_1Q_0	00	01	11	10
0		1	X	X
1			X	X

$J_1 = \overline{Q_2} Q_0$

* K_1

Q_2 \ Q_1Q_0	00	01	11	10
0	X	X	1	
1	X	X	X	X

$K_1 = Q_0$

* J_2

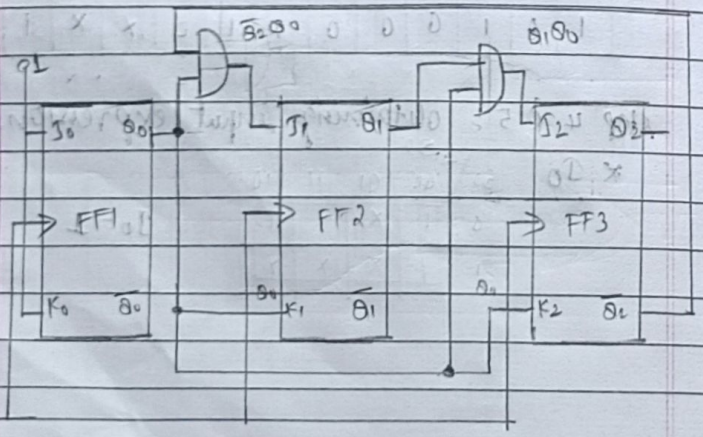
Q_2 \ Q_1Q_0	00	01	11	10
0			1	
1	X	X	X	X

$J_2 = Q_1 Q_0$

* K_2

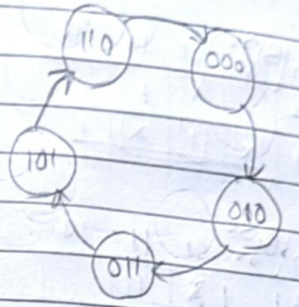
Q_2 \ Q_1Q_0	00	01	11	10
0	X	X	X	X
1		1	X	

$K_2 = Q_0$



(5) Design a synchronous counter that generates the sequence - 0, 2, 3, 5, 6, 0, ... using T-FF

Step 1 - State transition diagram



Step 2 & Step 3

PS			NS			Inputs		
Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	T_2	T_1	T_0
0	0	0	0	1	0	0	1	0
0	0	1	X	X	X	X	X	X
0	1	0	0	1	1	0	0	1
0	1	1	1	0	1	1	1	0
1	0	0	X	X	X	X	X	X
1	0	1	1	1	0	0	1	1
1	1	0	0	0	0	1	1	0
1	1	1	X	X	X	X	X	X

step 4 & step 5 - obtaining input expressions

* T_0

Q_2 \ Q_1Q_0	00	01	11	10
0		X		1
1	X	1	X	

$T_0 = \overline{Q_1} Q_0 + \overline{Q_2} Q_1 \overline{Q_0}$

* T_1

Q_2 \ Q_1Q_0	00	01	11	10
0	1	X	1	
1	X	1	X	1

$T_1 = Q_2 + \overline{Q_1} + Q_0$

* T_2

Q_2 \ Q_1Q_0	00	01	11	10
0		X	1	
1	X		X	1

$T_2 = \overline{Q_2} Q_0 + Q_2 Q_1$