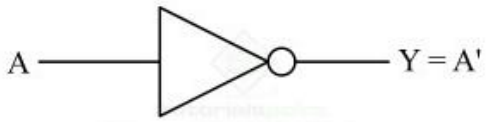
GATES USING 2X1 MULTIPLEXER

Basic logic gates are the building of Digital System Design. And using Multiplexer, we can realize these basic logic gates. A Multiplexer is a combinational circuit that has 2^n input lines and a single output line. Where n is a number of select lines. A Multiplexer is also known as Data Selector, it selects between 2^n input signals and forwards the selected input to a single output line.

NOT GATE

The NOT Gate is a basic logic gate that used in digital electronic circuits. The NOT gate has a single input and a single output. The output of the NOT gate is the logical inversion of its input. Hence, it is also called an inverter.

The standard logic symbol of the NOT gate has a triangle pointing to the right with a circle at its right end. The circle at right corner is referred to as an inversion bubble.

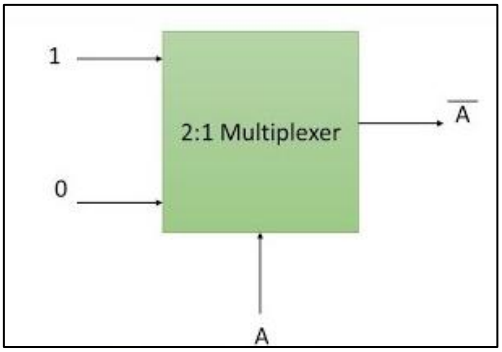


The NOT gate produces an output which is the complement or inversion of its input. For example, if we give a logic 0 at its input, it will provide a logic 1 at output. Similarly, when we give a logic 1 at input, it produces a logic 0 at output.

INPUT	OUTPUT (Y)
0	1
1	0

NOT Gate Using 2x1 MUX

The functional block diagram of a 2:1 multiplexer equivalent to the NOT gate is shown below.



There are two possible inputs, i.e. 0 and 1. We have applied 1 to the input line I_0 and 0 to the input line I_1. The input variable of the NOT gate is applied to the select line S of the MUX.

The operation of the 2:1 MUX as the NOT gate can be described as follows

- When the input to the select line is A = 0, then the multiplexer will transmit the 1 applied at the input line I_0 to the output line.
- When the input to the select line is A = 1, then the multiplexer will transmit the 0 applied at the input line I_1 to the output line.

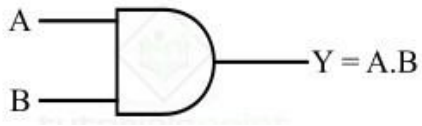
Hence, the output expression of the NOT gate using 2:1 MUX will be,

$$Y = A`. 1 + A . 0 = A`$$

AND GATE

AND Gate is a basic logic gate which may have two or more inputs, but only one output. The AND gate gives logic 0 state (LOW) as output if any one of its inputs is in the logic 0 state, otherwise, it gives a logic 1 states (HIGH) as output. Therefore, the output of the AND gate is HIGH or logic 1 state, only if all its inputs are HIGH or logic 1 state.

The logic symbol of a two input AND gate is shown below,

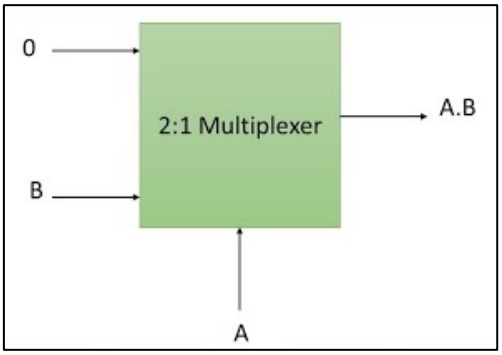


Where, the '.' (dot) symbol represents the AND operation. It is read as "Y is equal to A AND B". The operation of the AND gate can be understood with the help of its function table which is given below.

INPUT		OUTPUT
A	B	Y = A.B
0	0	0
0	1	0
1	0	0
1	1	1

AND Gate Using 2x1 MUX

The functional block diagram of a 2:1 multiplexer equivalent to the AND gate is shown below.



Here, the input line I_0 of MUX is set to logic 0 state. The input line I_1 of MUX is applied with B. The input variable A of the AND gate is used to control select line of MUX.

The operation of the 2:1 MUX as the AND gate can be described as follows

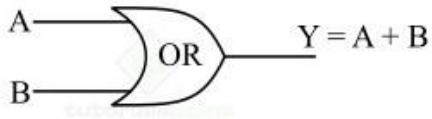
- When A = 0, the output of the MUX as AND gate is 0.
- When A = 1, the output of the MUX as AND gate is equal to B.

Hence, the output expression of the AND gate using 2:1 MUX will be,

$$Y = A`. B`. 0 + A1`. B . 0 + A . B`. 0 + A . B . 1 = AB$$

OR GATE

OR Gate is a basic logic gate that may accept two or more inputs, but gives only one output. The OR gate gives a HIGH or logic 1 state as output if any one of its inputs is in the HIGH or logic 1 state, otherwise, it gives a LOW or logic 0 state as output. Hence, the output of the OR gate is LOW or logic 0 state, only if all its inputs are LOW or logic 0 state. The logic symbol of a two input OR gate is shown below

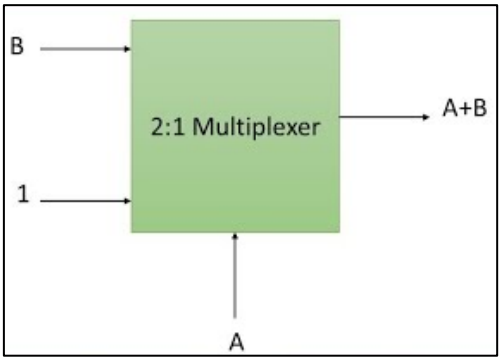


Where, the + symbol represents the OR operation. It is read as Y is equal to A OR B. The operation of the OR gate can be analyzed with the help of its function table given below

INPUT		OUTPUT
A	B	Y = A+B
0	0	0
0	1	1
1	0	1
1	1	1

OR Gate Using 2x1 Mux

The functional block diagram of a 2:1 multiplexer operating as a two input OR gate is shown below.



Here, the input line I_1 of MUX is set to logic 1 state. The input line I_0 of MUX is applied with B. The input variable A of the OR gate is used to control select line of MUX.

The operation of the 2:1 MUX as the OR gate can be described as follows −

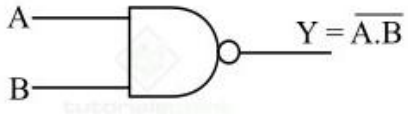
- When A = 0, the output of the MUX as OR gate is equal to B.
- When A = 1, the output of the MUX as OR gate is equal to logic 1.

Hence, the output expression of the AND gate using 2:1 MUX will be,

$$Y = A`. B`. 0 + A1`. B . 1 + A . B`. 1 + A . B . 1 = A + B$$

NAND GATE

The NAND gate is the logic gate whose output is LOW when all its inputs are high, and its output is HIGH, when any of its inputs is LOW. Therefore, the operation of the NAND gate is opposite that of the AND gate. The logic symbol of a two input NAND gate is shown below

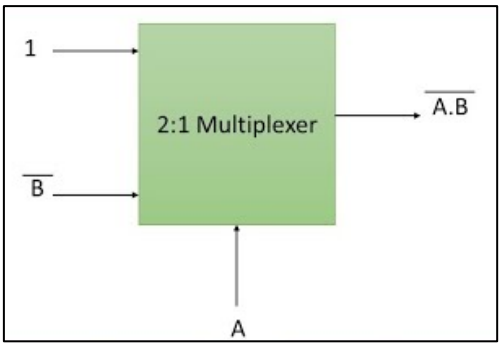


For the NAND gate, if A and B are the input variables and Y is the output variable. It is read as "Y is equal to A.B whole bar". The operation of the NAND gate for different possible combinations of inputs can be analyzed with the help its truth table which is given below

INPUT		OUTPUT
A	B	Y = (A.B)`
0	0	1
0	1	1
1	0	1
1	1	0

NAND Gate Using 2x1 Mux

The functional block diagram of a 2:1 multiplexer operating as a two input NAND gate is shown below



Here, the input line I_0 of the 2:1 MUX is set to logic 1 state and the input line I_1 of MUX is applied with B`. The input variable A of the NAND gate is used to control select line of MUX.

The operation of the 2:1 MUX as the NAND gate can be described as follows

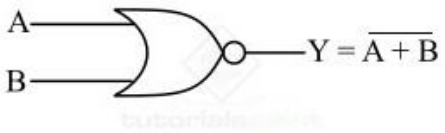
- When A = 0, the output of the MUX as NAND gate is 1.
- When A = 1, the output of the MUX as NAND gate is equal to B`.

Hence, the output expression of the NAND gate using 2:1 MUX will be,

$$Y = A`. B`. 1 + A1`. B . 1 + A . B`. 1 + A . B . 0 = (AB)`$$

NOR GATE

The NOR gate is a logic gate whose output is HIGH, only when all its inputs are LOW, and it gives an output LOW, even if any of its inputs becomes HIGH. Therefore, the operation of the NOR gate is opposite that of the OR gate. The logic symbol of a two input NOR gate is shown below,

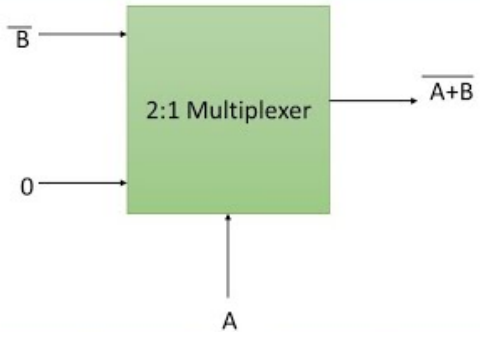


For a NOR gate, if A and B are the input variables and Y is the output variable. It is read as "Y is equal to A plus B whole bar". We can analyze the operation of the NOR gate for different possible combinations of inputs by its truth table which is given below,

INPUT		OUTPUT
A	B	Y = A+B
0	0	1
0	1	0
1	0	0
1	1	0

NOR Gate Using 2x1 Mux

The functional block diagram of a 2:1 multiplexer operating as a two input NOR gate is shown below,



Here, the input line I_0 of the MUX is applied with B` and he input line I_1 of the MUX is set to logic 0 state. The input variable A of the NOR gate is used to control select line of MUX.

The operation of the 2:1 MUX as the NOR gate can be described as follows −

- When A = 0, the output of the MUX as NOR gate is equal to B`.
- When A = 1, the output of the MUX as NOR gate is equal to logic 0.

Hence, the output expression of the NOR gate using 2:1 MUX will be,

$$Y = A`. B`. 1 + A1`. B . 0 + A . B`. 0 + A . B . 0 = (A + B)`$$

EX-OR GATE

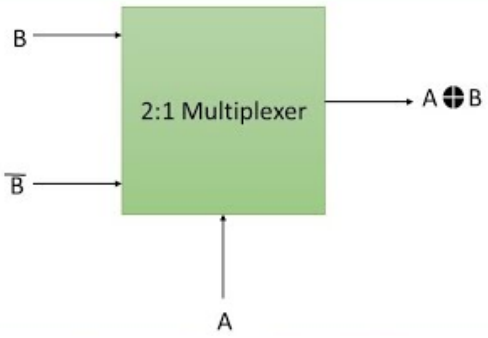
The EX-OR gate is a logic gate whose output is HIGH, only when all its inputs are DIFFERENT, and it gives an output LOW when inputs are SAME. The logic symbol of a two input EX-OR gate is shown below,

For a EX-OR gate, if A and B are the input variables and Y is the output variable. It is read as "Y is equal to A EX-OR B". We can analyze the operation of the EX-OR gate for different possible combinations of inputs by its truth table which is given below,

INPUT		OUTPUT
A	B	Y = A+B
0	0	0
0	1	1
1	0	1
1	1	0

EX-OR Gate Using 2x1 Mux

The functional block diagram of a 2:1 multiplexer operating as a two input EX-OR gate is shown below,



Here, the input line I_0 of the MUX is applied with B and the input line I_1 of the MUX is applied with B`. The input variable A of the EX-OR gate is used to control select line of MUX.

The operation of the 2:1 MUX as the OR gate can be described as follows −

- When A = 0, the output of the MUX as OR gate is equal to B.
- When A = 1, the output of the MUX as OR gate is equal to logic B`.

Hence, the output expression of the AND gate using 2:1 MUX will be,

$$Y = A`. B`. 0 + A1`. B . 1 + A . B`. 1 + A . B . 0 = (A \text{ xor } B)$$

EX-NOR GATE

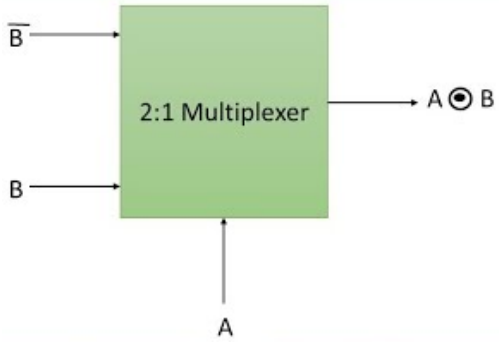
The EX-NOR gate is a logic gate whose output is HIGH, only when all its inputs are SAME, and it gives an output LOW when inputs are DIFFERENT. The logic symbol of a two input EX-NOR gate is shown below,

For a EX-NOR gate, if A and B are the input variables and Y is the output variable. It is read as "Y is equal to A EX-NOR B". We can analyze the operation of the EX-NOR gate for different possible combinations of inputs by its truth table which is given below,

INPUT		OUTPUT
A	B	Y = A+B
0	0	1
0	1	0
1	0	0
1	1	1

EX-NOR Gate Using 2x1 Mux

The functional block diagram of a 2:1 multiplexer operating as a two input EX-NOR gate is shown below,



Here, the input line I_0 of the MUX is applied with B` and the input line I_1 of the MUX is applied with B. The input variable A of the EX-NOR gate is used to control select line of MUX.

The operation of the 2:1 MUX as the OR gate can be described as follows −

- When A = 0, the output of the MUX as OR gate is equal to B`.
- When A = 1, the output of the MUX as OR gate is equal to logic B.

Hence, the output expression of the AND gate using 2:1 MUX will be,

$$Y = A`. B`. 1 + A1`. B . 0 + A . B`. 0 + A . B . 1 = (A \text{ xnor } B)$$