Class : BE 6

Roll. No : 42260

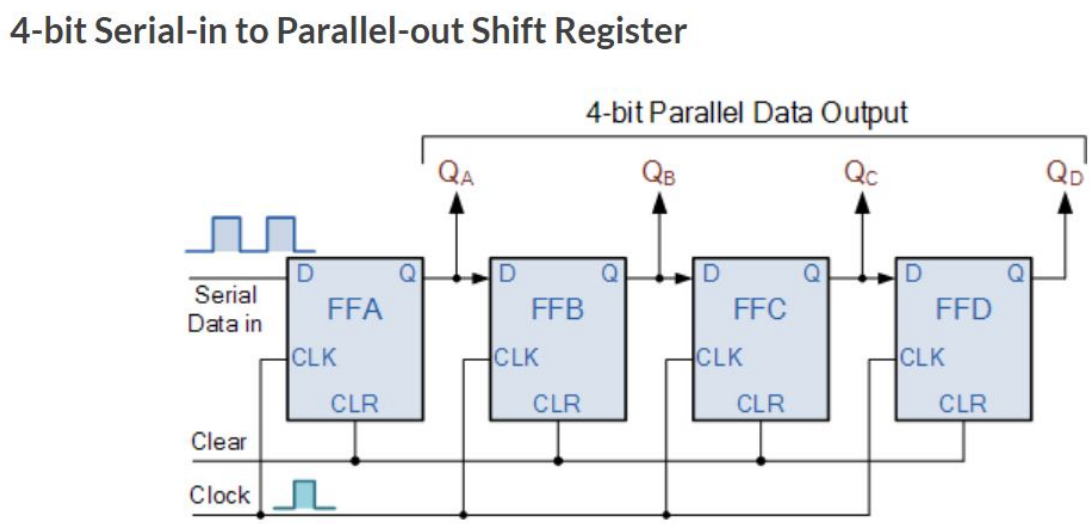
Assignment No. : 2

Assignment Name : Universal Shift Register

Date Of Performance : 27/9/21

Assignment: Write a VHDL Program to Model a Universal Shift Register. Synthesize the model for the target PLD. Simulate the model using a TestBench. Implement it on the target PLD

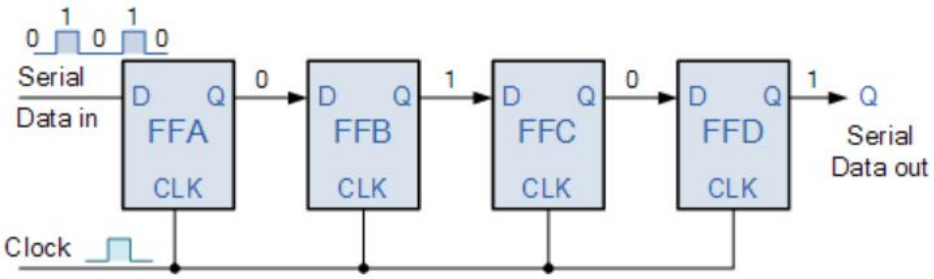
Block Diagram:



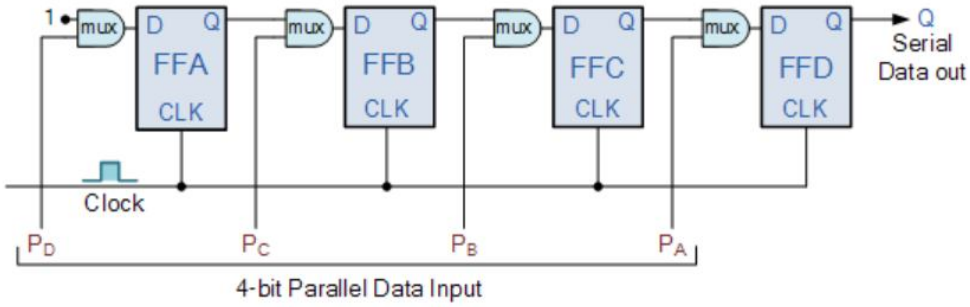
Truth Table:

Clock Pulse No	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	0	0	0	0

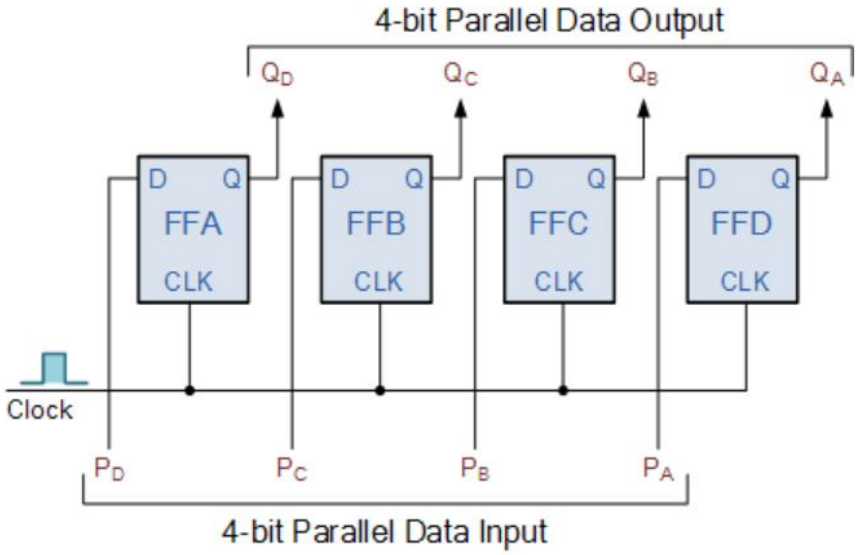
4-bit Serial-in to Serial-out Shift Register



4-bit Parallel-in to Serial-out Shift Register



4-bit Parallel-in to Parallel-out Shift Register

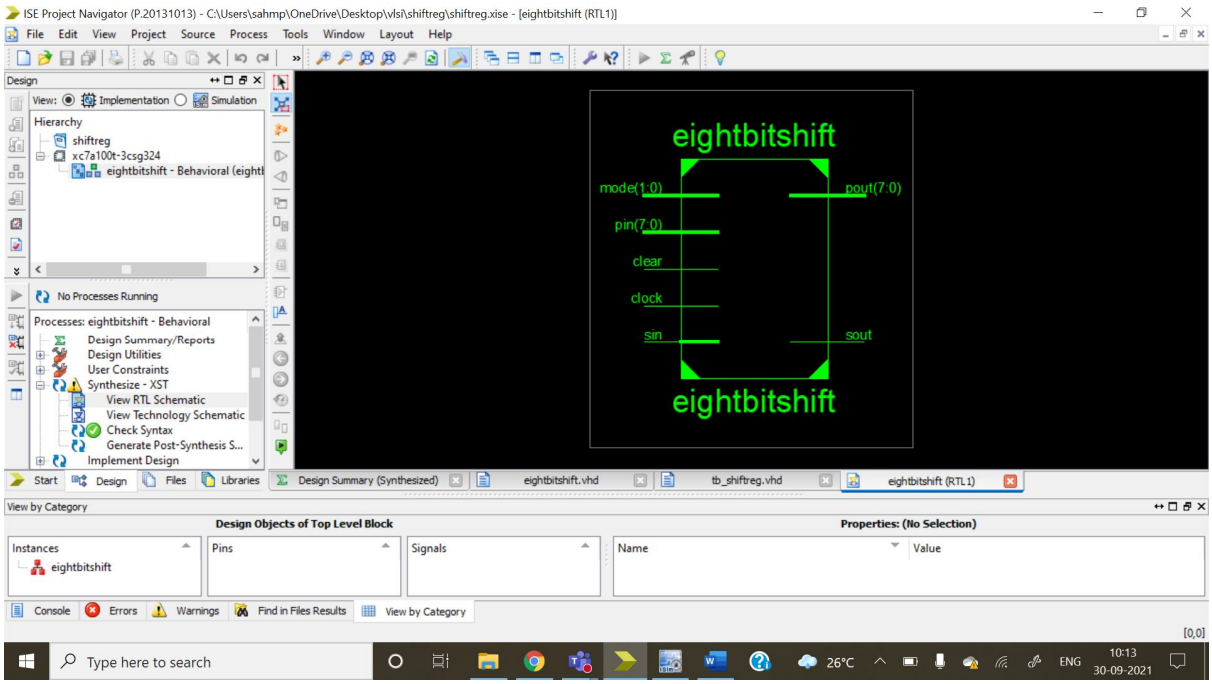


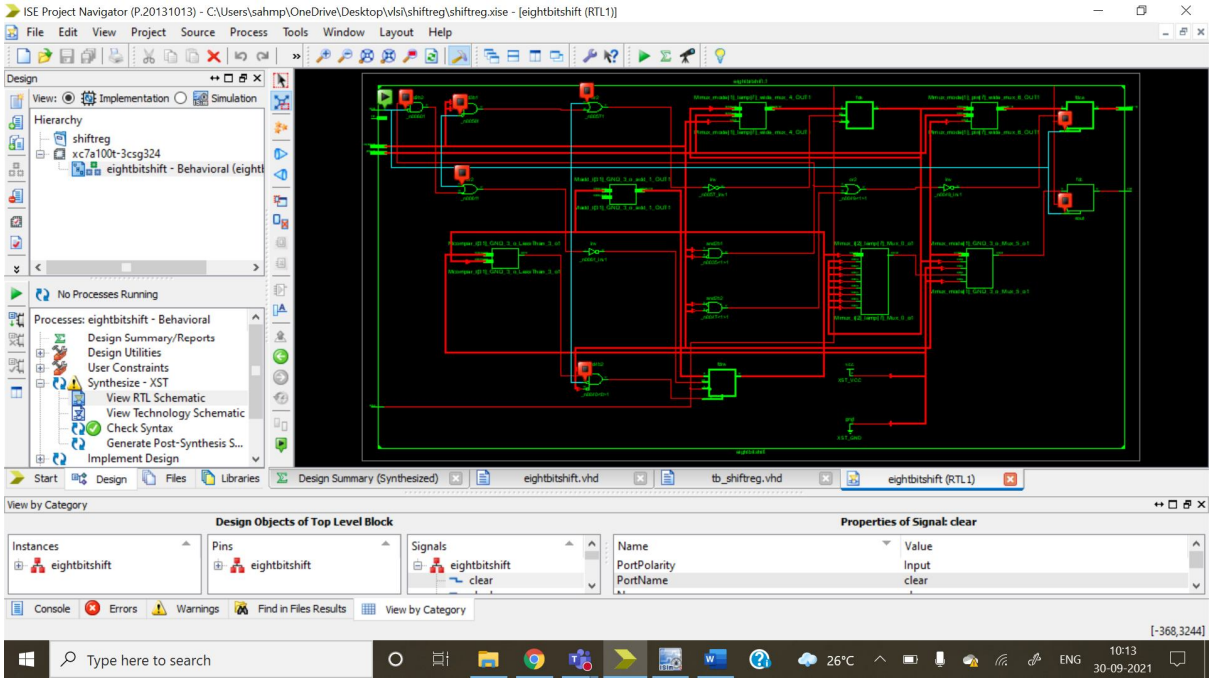
Main VHDL Program:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity eightbitshift is
port (clock, sin, clear : in std_logic;
mode : in std_logic_vector(1 downto 0);
pin : in std_logic_vector(7 downto 0);
pout : out std_logic_vector(7 downto 0);
sout : out std_logic);
end eightbitshift;

architecture Behavioral of eightbitshift is
signal temp: std_logic_vector(7 downto 0);
signal i:integer:=0;
begin

process (clock, clear)

begin

if (clear='1') then --active high reset

sout<='0';
pout <= (others => '0');

--elsif (clock'event and clock='1') then
elsif rising_edge(clock) then

case mode is
when "00"=> --siso
```

```
temp (6 downto 0) <= temp(7 downto 1);
temp(7) <= sin;
sout <= temp(0);
when "01"=> --sipo
temp (6 downto 0) <= temp(7 downto 1);
temp(7) <= sin;
pout <= temp;
sout <= '0';
when "10"=> --piso
temp <= pin;
sout <= temp(i);
i <= i + 1;
if (i >= 7) then
i <= 0;
end if;
when others=> --pipo
pout <= pin;
sout <= '0';
end case;
end if;

end process;

end Behavioral;
```

RTL Schematic:


ISE Project Navigator (P.20131013) - C:\Users\sahmp\OneDrive\Desktop\vlsi\shiftreg\shiftreg.xise - [eightbitshift (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
shiftreg
xc7a100t-3csg324
eightbitshift - Behavioral (eightb
No Processes Running
Processes: eightbitshift - Behavioral
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis S...
Implement Design
eightbitshift
mode(1:0)
pin(7:0)
clear
clock
sin
pout(7:0)
sout
eightbitshift
Start Design Files Libraries
Design Summary (Synthesized)
eightbitshift.vhd
tb_shiftreg.vhd
eightbitshift (RTL1)
View by Category
Design Objects of Top Level Block
Properties: (No Selection)
Instances
eightbitshift
Pins
Signals
Name
Value
Console Errors Warnings Find in Files Results View by Category
[0,0]
Type here to search
26°C
ENG
10:13
30-09-2021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Start Design Files Libraries
Design Summary (Synthesized)
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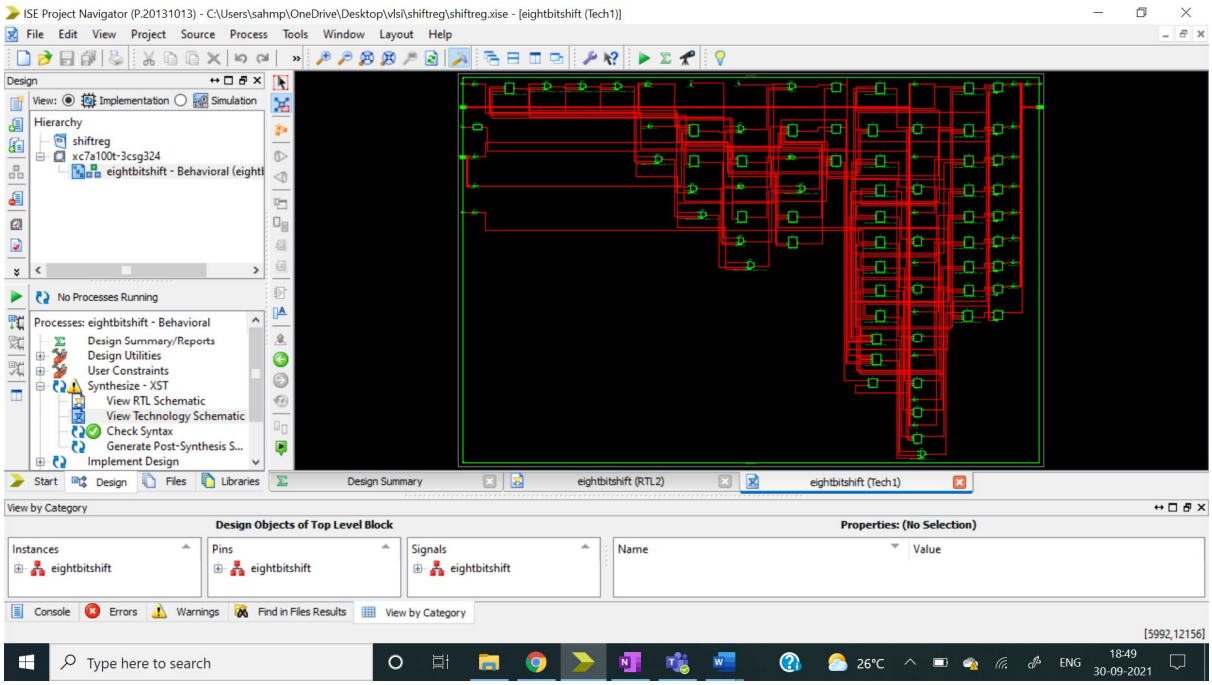
tb_shiftreg.vhd
eightbitshift (RTL1)
View by Category
Design Objects of Top Level Block
Properties of Signal: clear
Instances
eightbitshift
Pins
eightbitshift
Signals
eightbitshift
clear
Name
Value
PortPolarity
Input
PortName
clear
Console Errors Warnings Find in Files Results View by Category
[-368,3244]
Type here to search
26°C
ENG
10:13
30-09-2021

Technology Schematic:



Synthesis Report

a) Device Utilisation Summary

Top Level Output File Name : eightbitshift.ngc

Primitive and Black Box Usage:

BELS : 47
GND : 1
INV : 1
LUT1 : 2
LUT2 : 1
LUT3 : 19
LUT4 : 2
LUT5 : 1
LUT6 : 4
MUXCY : 11
MUXF7 : 1
VCC : 1
XORCY : 3
FlipFlops/Latches : 20
FD : 3
FDC : 1
FDCE : 8
FDE : 8
Clock Buffers : 1
BUFGP : 1
IO Buffers : 21

```
#      IBUF                : 12
#      OBUF                : 9

Device utilization summary:
---------------------------

Selected Device : 7a100tcsg324-3


Slice Logic Utilization:
 Number of Slice Registers:          20  out of  126800     0%
 Number of Slice LUTs:               30  out of  63400     0%
    Number used as Logic:            30  out of  63400     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    31
   Number with an unused Flip Flop:     11  out of    31    35%
   Number with an unused LUT:           1  out of    31     3%
   Number of fully used LUT-FF pairs:   19  out of    31    61%
   Number of unique control sets:       4

IO Utilization:
 Number of IOs:                  22
 Number of bonded IOBs:              22  out of    210    10%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:           1  out of    32     3%
```

b) Timing Report

```
NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clock                              | BUFGP                  | 20    |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design
```

Timing Summary:

Speed Grade: -3

Minimum period: 1.968ns (Maximum Frequency: 508.027MHz)
Minimum input arrival time before clock: 1.375ns
Maximum output required time after clock: 0.640ns
Maximum combinational path delay: No path found

Timing Details:

All values displayed in nanoseconds (ns)

Testbench Program:

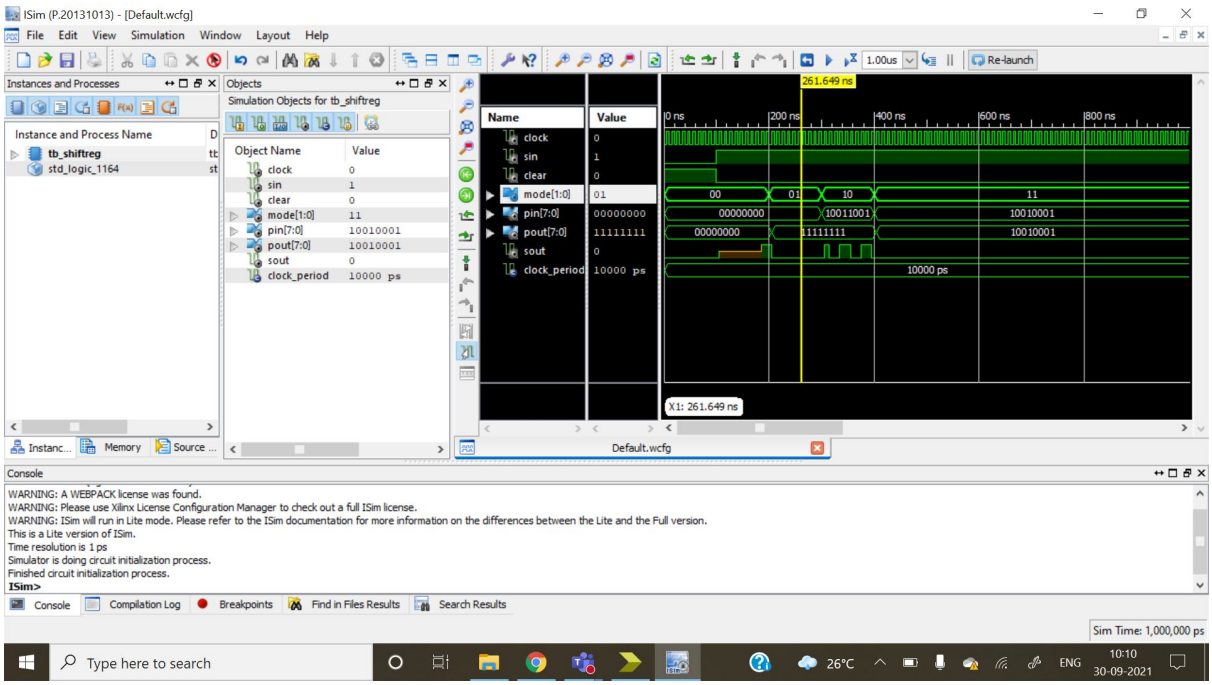
```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;

ENTITY tb_shiftreg IS
END tb_shiftreg;

ARCHITECTURE behavior OF tb_shiftreg IS

  -- Component Declaration for the Unit Under Test (UUT)

  COMPONENT eightbitshift
  PORT(
      clock : IN  std_logic;
      sin : IN  std_logic;
      clear : IN  std_logic;
```

```
        mode : IN  std_logic_vector(1 downto 0);
        pin : IN  std_logic_vector(7 downto 0);
        pout : OUT  std_logic_vector(7 downto 0);
        sout : OUT  std_logic
       );
    END COMPONENT;


   --Inputs
   signal clock : std_logic := '0';
   signal sin : std_logic := '0';
   signal clear : std_logic := '0';
   signal mode : std_logic_vector(1 downto 0) := (others => '0');
   signal pin : std_logic_vector(7 downto 0) := (others => '0');

            --Outputs
   signal pout : std_logic_vector(7 downto 0);
   signal sout : std_logic;

   -- Clock period definitions
   constant clock_period : time := 10 ns;

BEGIN

            -- Instantiate the Unit Under Test (UUT)
   uut: eightbitshift PORT MAP (
        clock => clock,
        sin => sin,
        clear => clear,
        mode => mode,
        pin => pin,
```

```
        pout => pout,
        sout => sout
       );

  -- Clock process definitions
  clock_process :process
  begin
                clock <= '0';
                wait for clock_period/2;
                clock <= '1';
                wait for clock_period/2;
  end process;

  -- Stimulus process
  stim_proc: process
  begin
    -- hold reset state for 100 ns.
clear<='1';
wait for 100 ns;
clear<='0';
mode<="00";--siso
sin<='1';
wait for 100 ns;
mode<="01";--sipo
sin<='1';
wait for 100 ns;
mode<="10";--piso
pin<="10011001";
wait for 100 ns;
mode<="11";--pipo
pin<="10010001";
```

```
wait for 100 ns;

      -- insert stimulus here

    wait;

  end process;


END;
```

Isim Waveforms:



Pin Locking Report: Attached separately

Conclusion:

Thus we have :

1) Modeled a universal shift register using Behavioral Modeling Style.

2) Observed following Schematics : RTL & Technology Schematics generated Post-Synthesis.

3) Interpreted Device Utilisation Summary in terms of LUTs , SLICES , IOBs , Multiplexers & D FFs used out of the available device resources.

4) Interpreted the TIMING Report in terms of Maximum combinational delay as indicative of the Maximum Operating Frequency .

5) Written a TESTBENCH to verify the functionality of universal shift register & verified the functionality as per the TRUTH-TABLE ,by observing ISIM Waveforms.

6) Used PlanAhead Editor for pin-locking.

7) Prototyped the FPGA XC3S250EPQ208-5 to realize universal shift register & verified its operation by giving suitable input combinations