Class: BE – 6

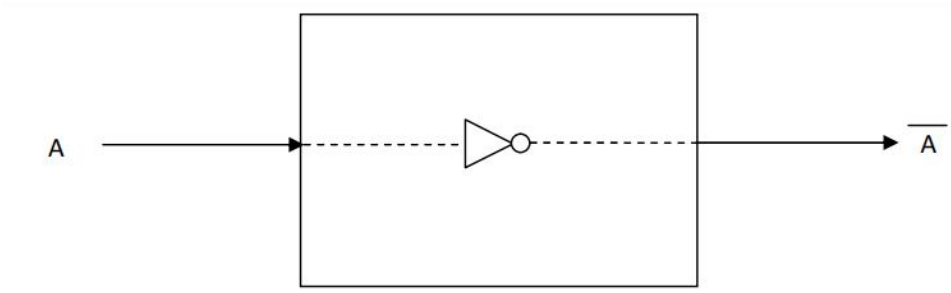
Roll. No: 42260

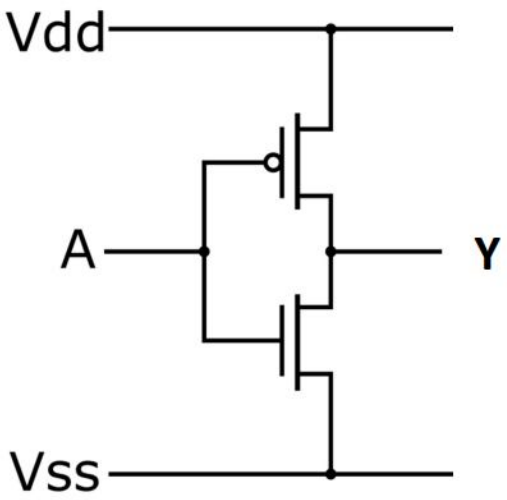
Assignment No.: 5

Assignment Name: CMOS Inverter

Date Of Performance: 18/10/2021

Block Diagram:



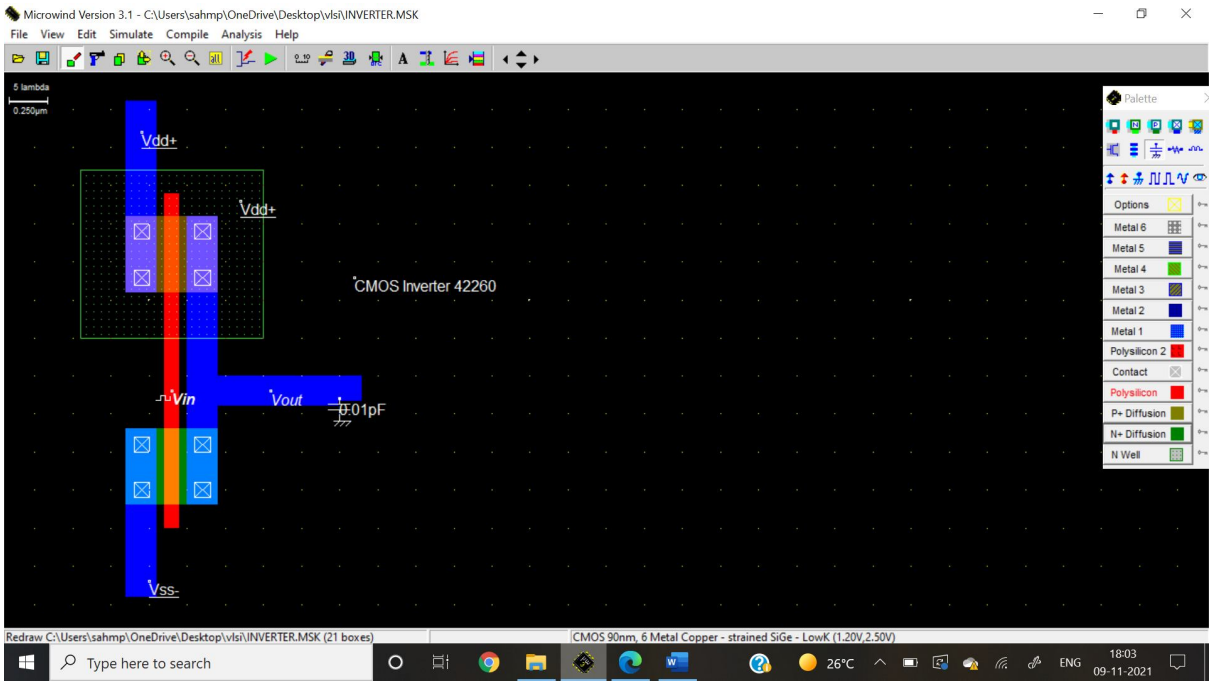


Truth-Table:

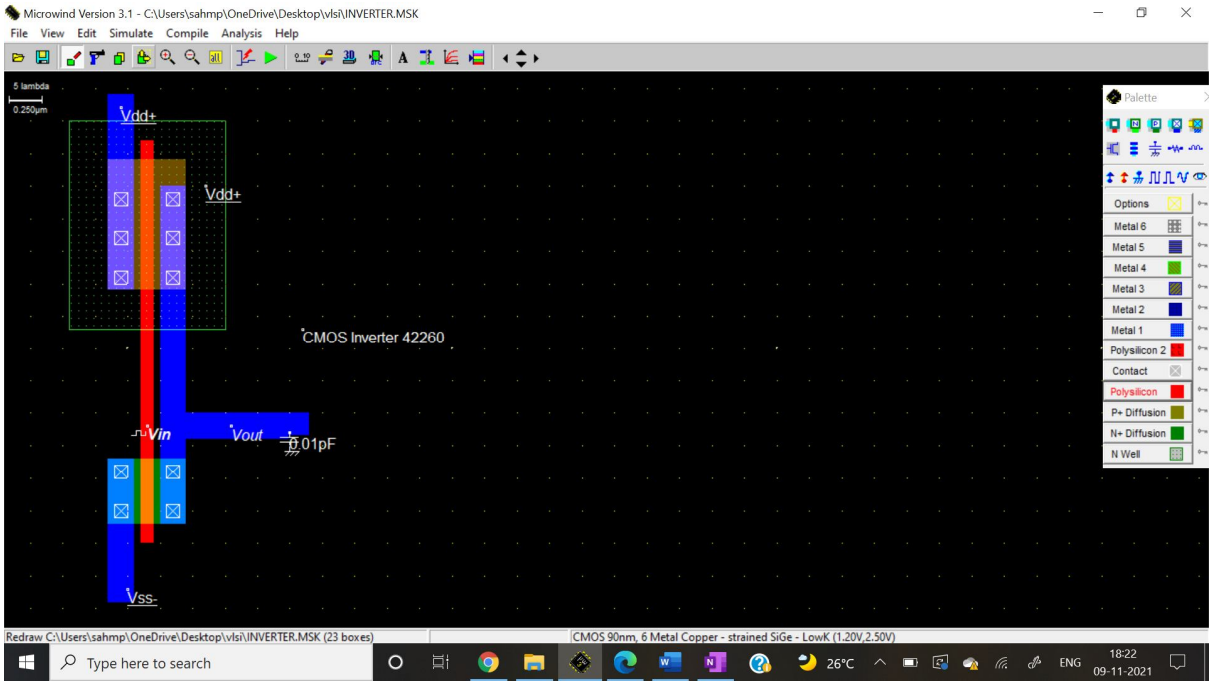
INPUTS (s)	OUTPUT (s)
A	$\overline{A}$

Layout:

Asymmetric



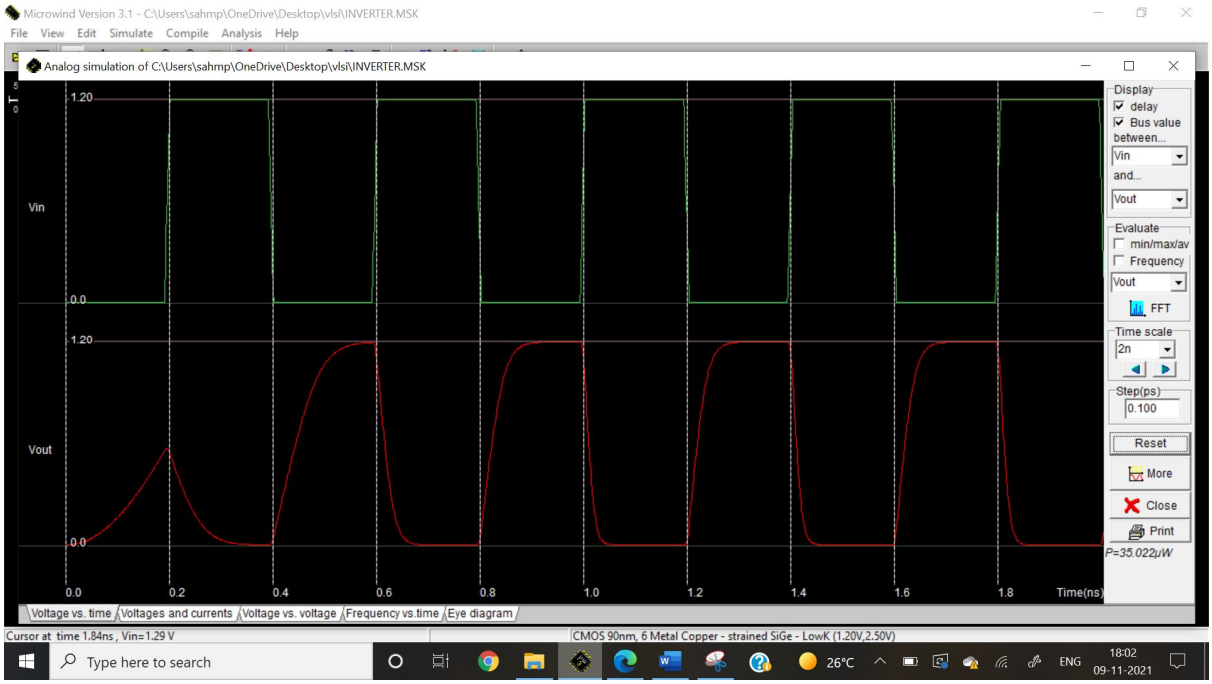
Symmetric



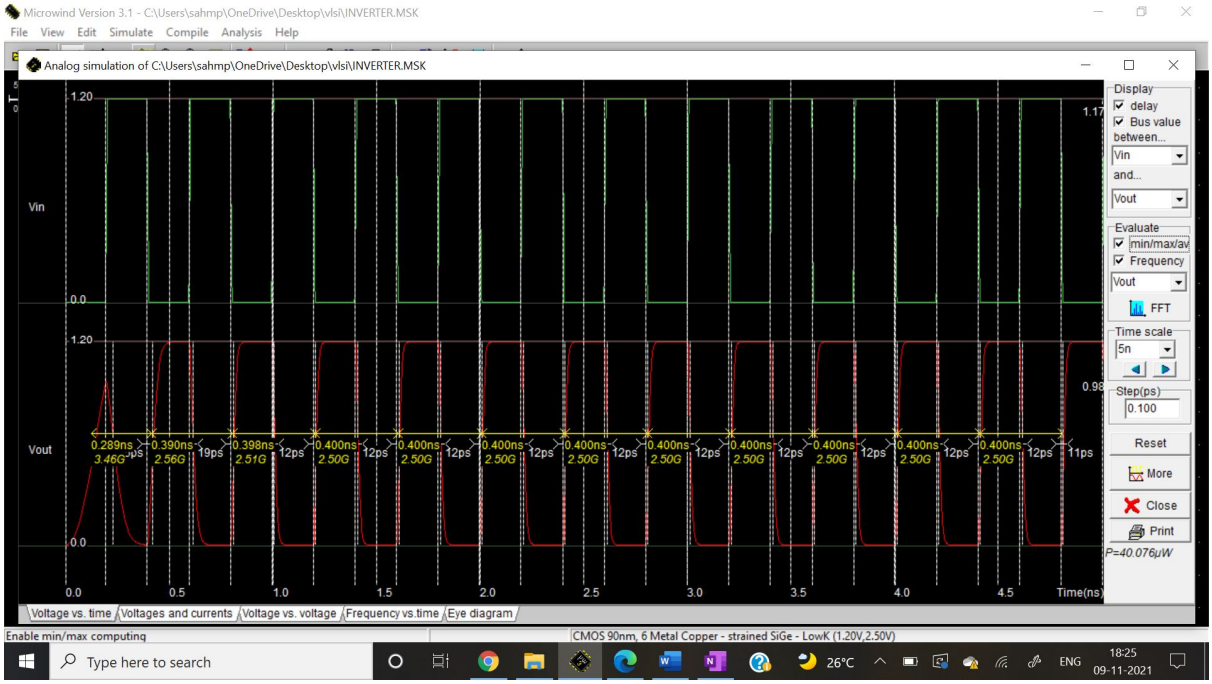
Waveforms:

a) Vin , Vout

Asymmetric

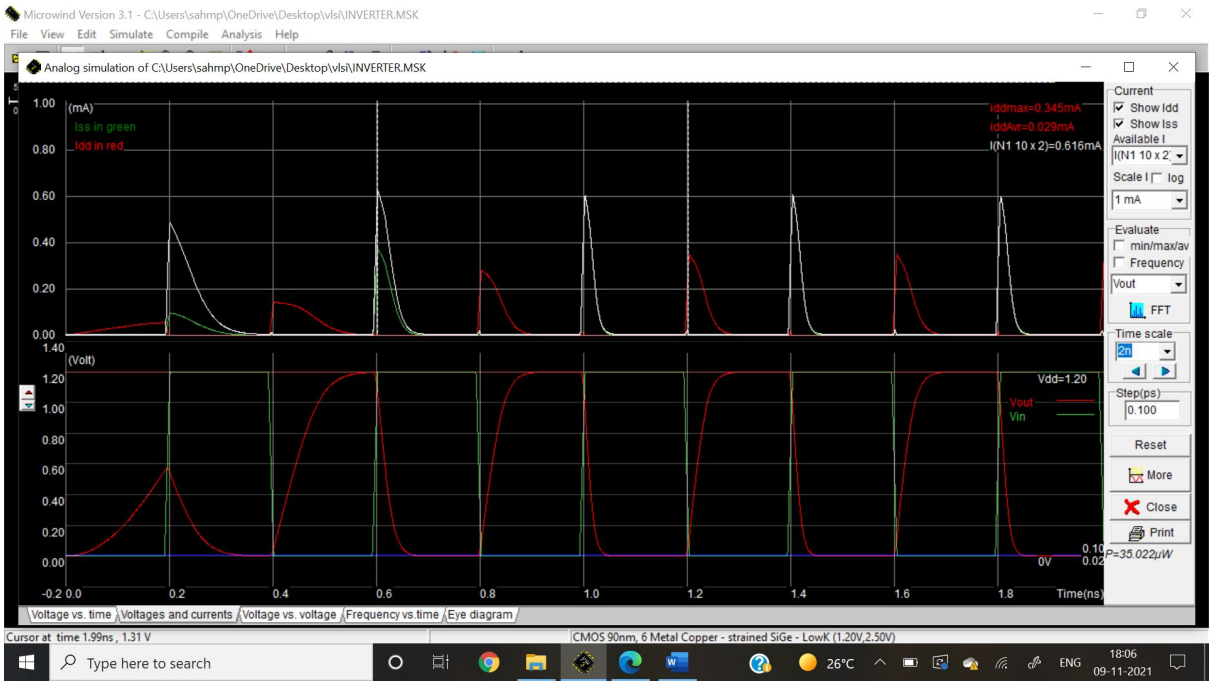

Microwind Version 3.1 - C:\Users\sahmp\OneDrive\Desktop\vlsi\INVERTER.MSK
File View Edit Simulate Compile Analysis Help
Analog simulation of C:\Users\sahmp\OneDrive\Desktop\vlsi\INVERTER.MSK
Vin
Vout
1.20
0.0
Time(ns)
Display
delay
Bus value between...
Vin
and...
Vout
Evaluate
min/max/av
Frequency
FFT
Time scale
2n
Step(ps)
0.100
Reset
More
Close
Print
P=35.022µW
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
Eye diagram
Cursor at time 1.84ns , Vin=1.29 V
CMOS 90nm, 6 Metal Copper - strained SiGe - LowK (1.20V,2.50V)
Type here to search
26°C
ENG
18:02
09-11-2021

Symmetric

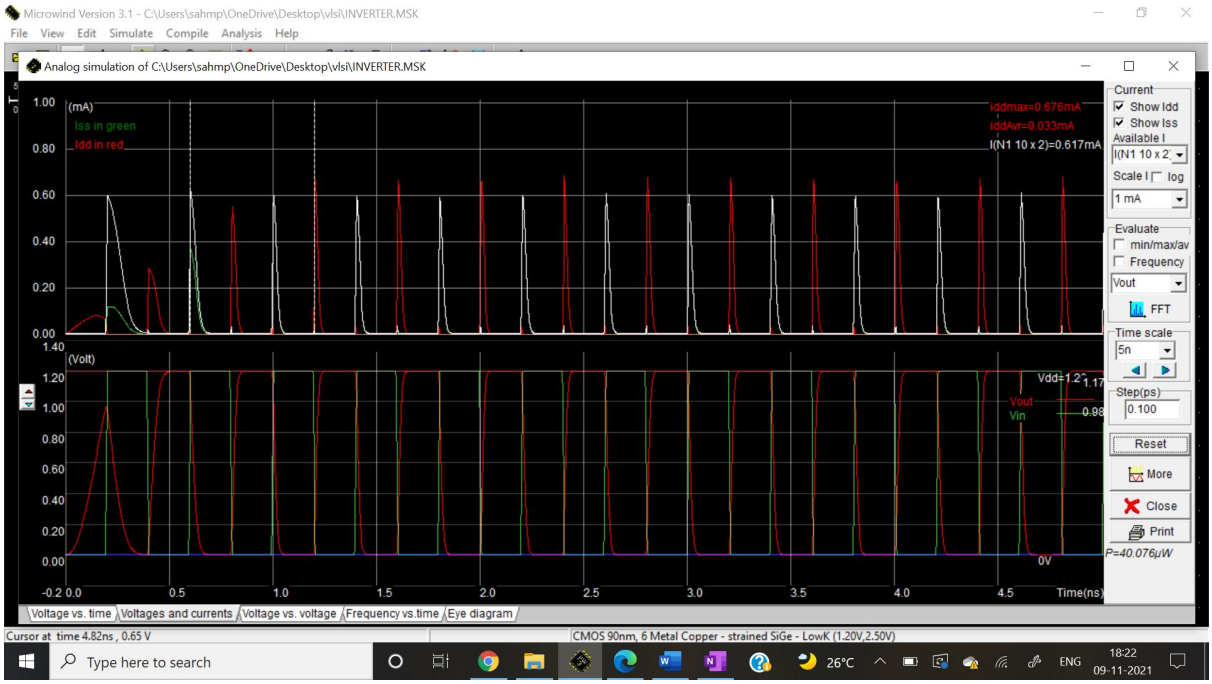

Microwind Version 3.1 - C:\Users\sahmp\OneDrive\Desktop\vlsi\INVERTER.MSK
File View Edit Simulate Compile Analysis Help
Analog simulation of C:\Users\sahmp\OneDrive\Desktop\vlsi\INVERTER.MSK
Vin
Vout
1.20
0.0
1.17
0.98
0.289ns 3.46G
0.390ns 2.56G
19ps
0.398ns 2.51G
12ps
0.400ns 2.50G
11ps
Time(ns)
Display
delay
Bus value between...
Vin
and...
Vout
Evaluate
min/max/av
Frequency
FFT
Time scale
5n
Step(ps)
0.100
Reset
More
Close
Print
P=40.076µW
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
Eye diagram
Enable min/max computing
CMOS 90nm, 6 Metal Copper - strained SiGe - LowK (1.20V,2.50V)
Type here to search
26°C
ENG
18:25
09-11-2021

b) Vout , Iout

Asymmetric



Symmetric



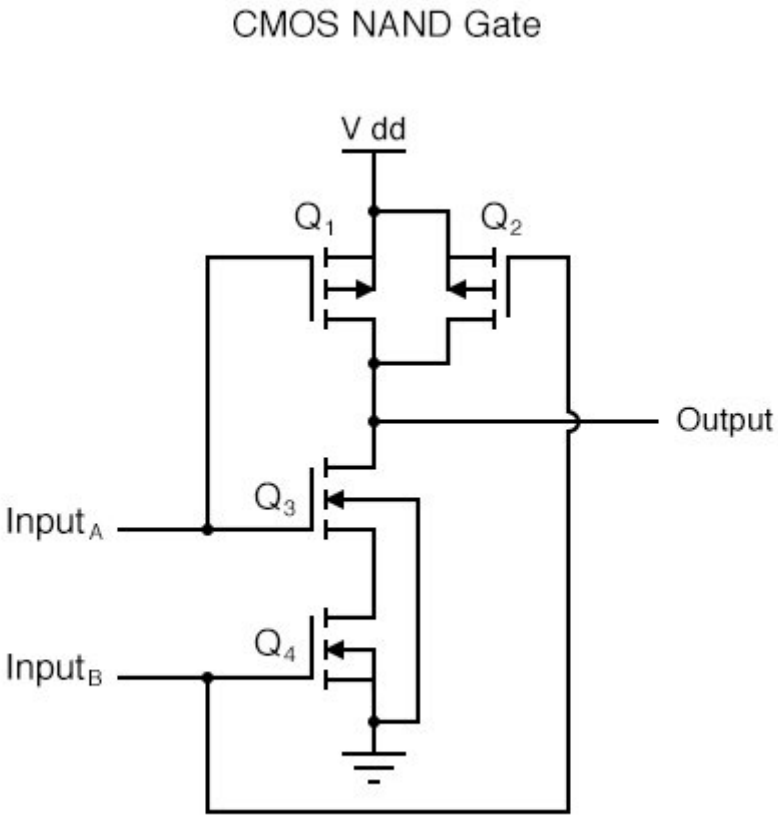
Performance Analysis:

Pdynamic	40.076uW
fmax	2.5GHz

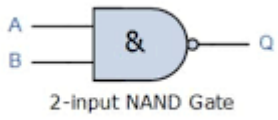
Assignment Name: NAND GATE

Date Of Performance: 8/11/2021

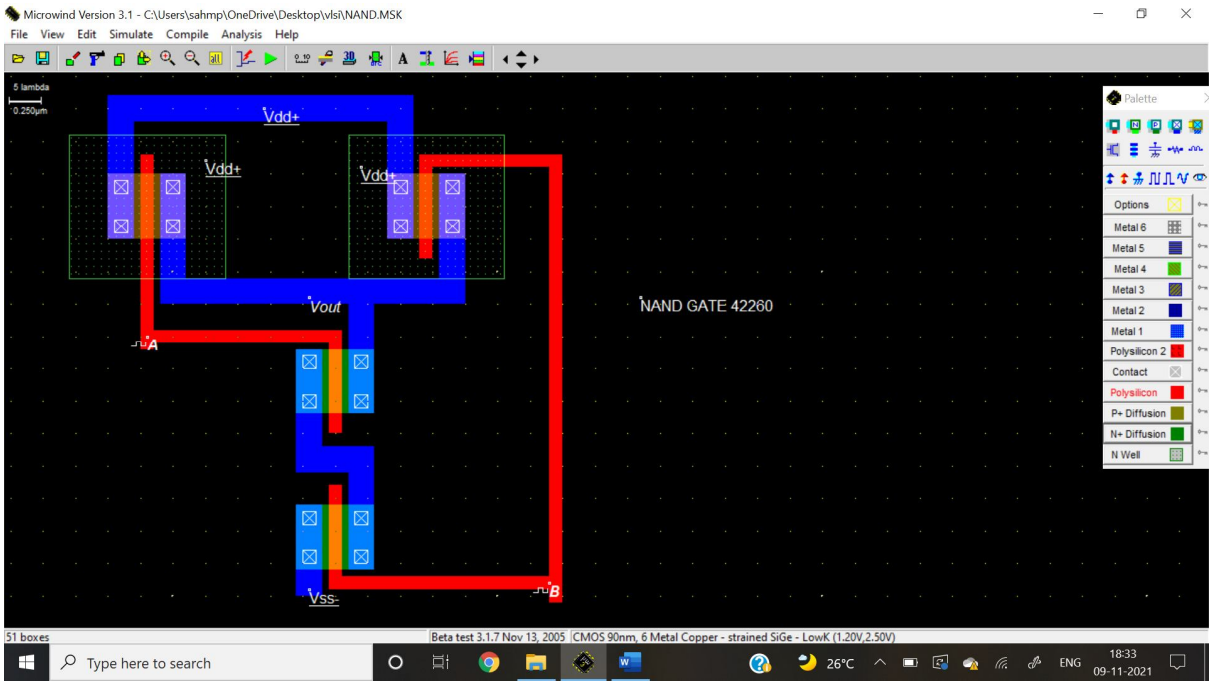
Block Diagram:



Truth-Table:

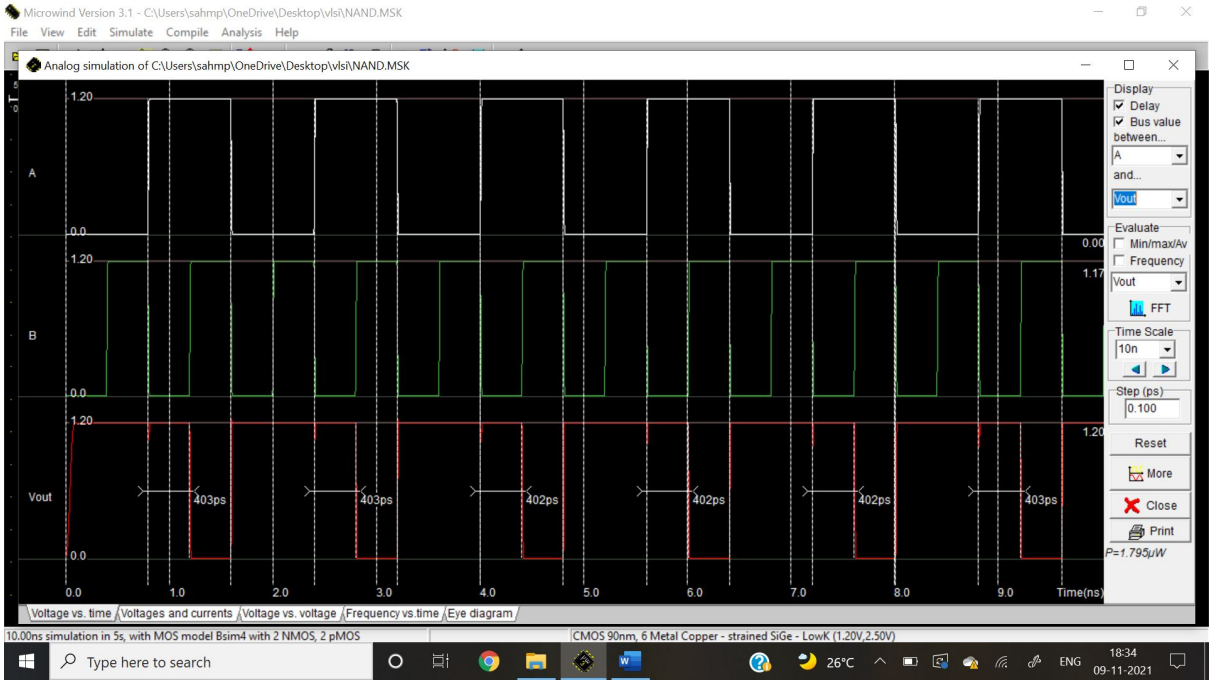
Symbol	Truth Table		
 2-input NAND Gate	A	B	Q
	0	0	1
	0	1	1
	1	0	1
	1	1	0
Boolean Expression Q = A NAND B			

Layout:

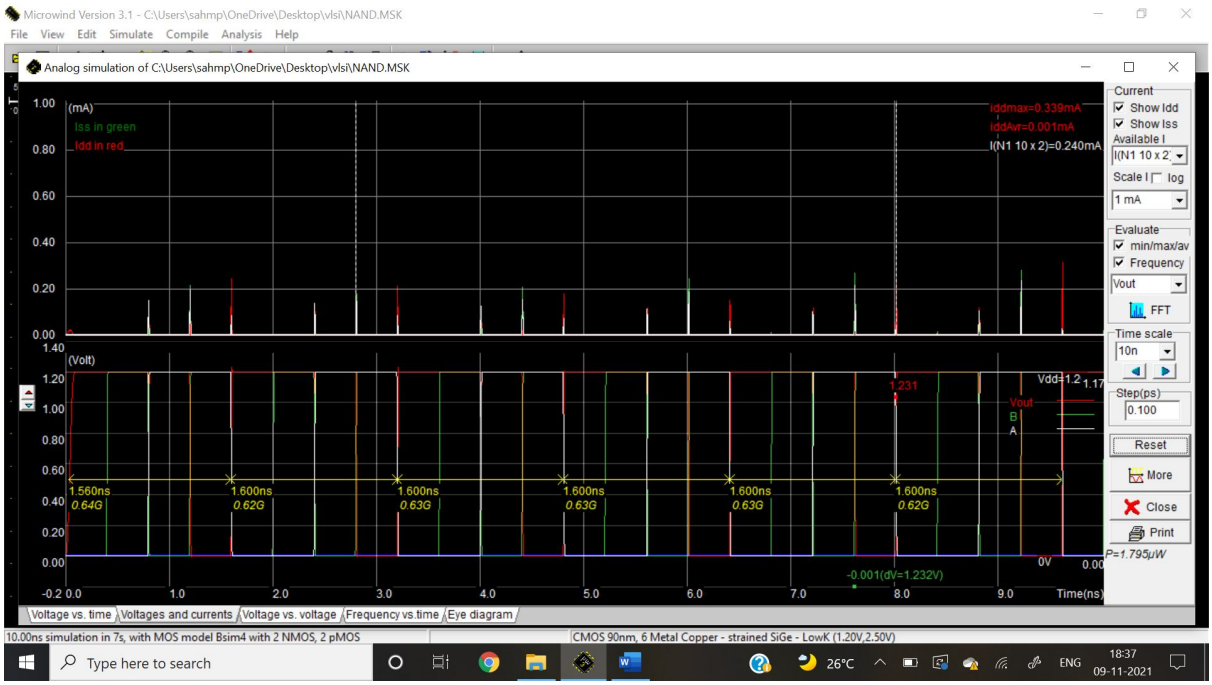


Waveforms:

a) Vin , Vout



b) Vout , Iout



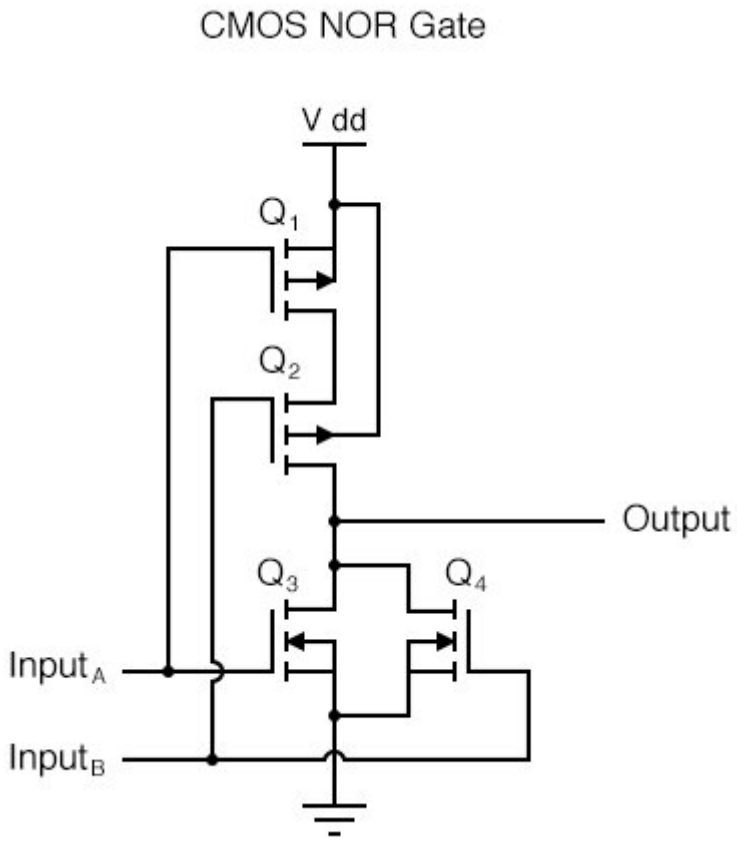
Performance Analysis:

Pdynamic	1.795uW
Fmax	0.63GHz

Assignment Name: NOR GATE

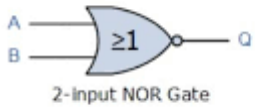
Date Of Performance: 8/11/2021

Block Diagram:

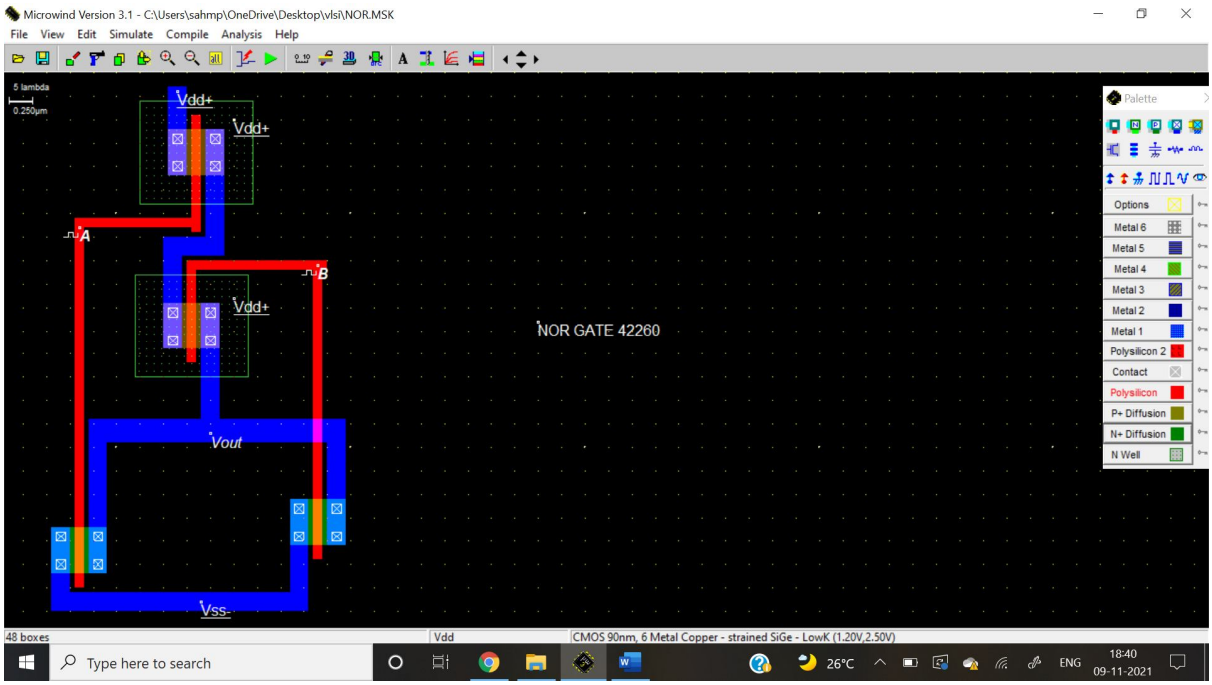


Truth-Table:

Symbol	Truth Table		
	A	B	Q
	0	0	1
	0	1	0
	1	0	0
	1	1	0
Boolean Expression Q = A NOR B			

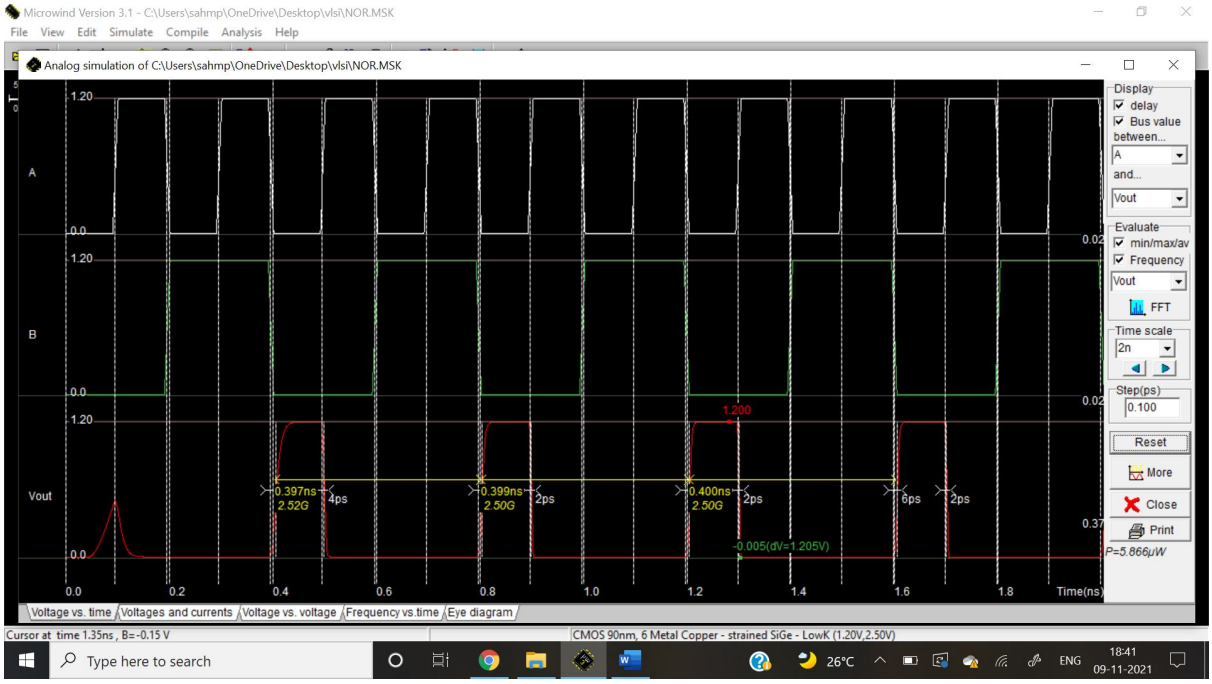


Layout:

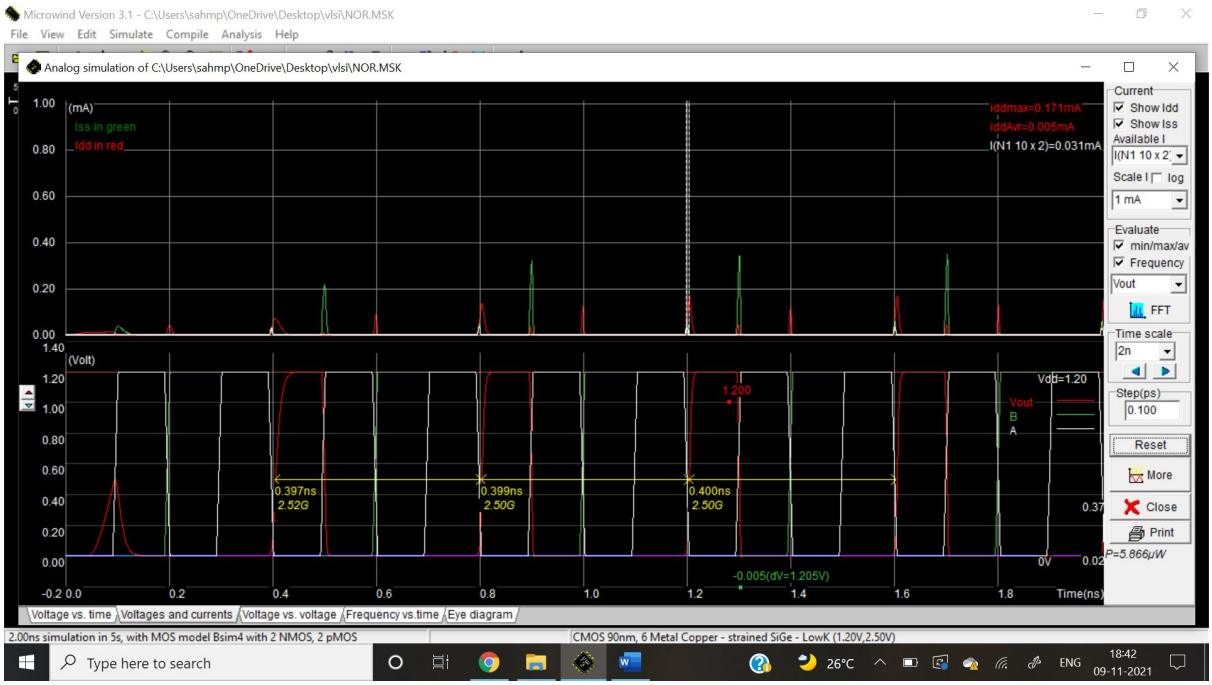


Waveforms:

a) Vin , Vout



b) Vout , Iout



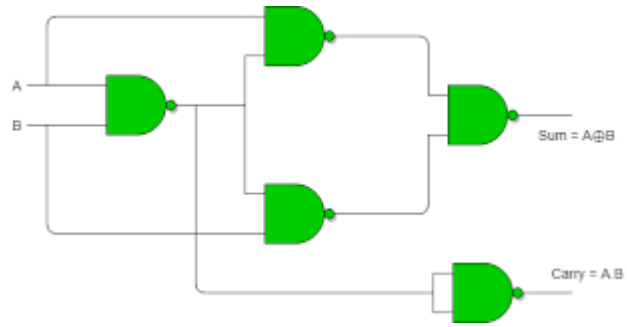
Performance Analysis:

Pdynamic	5.866uW
fmax	2.5GHz

Assignment Name: HALF ADDER

Date Of Performance: 8/11/2021

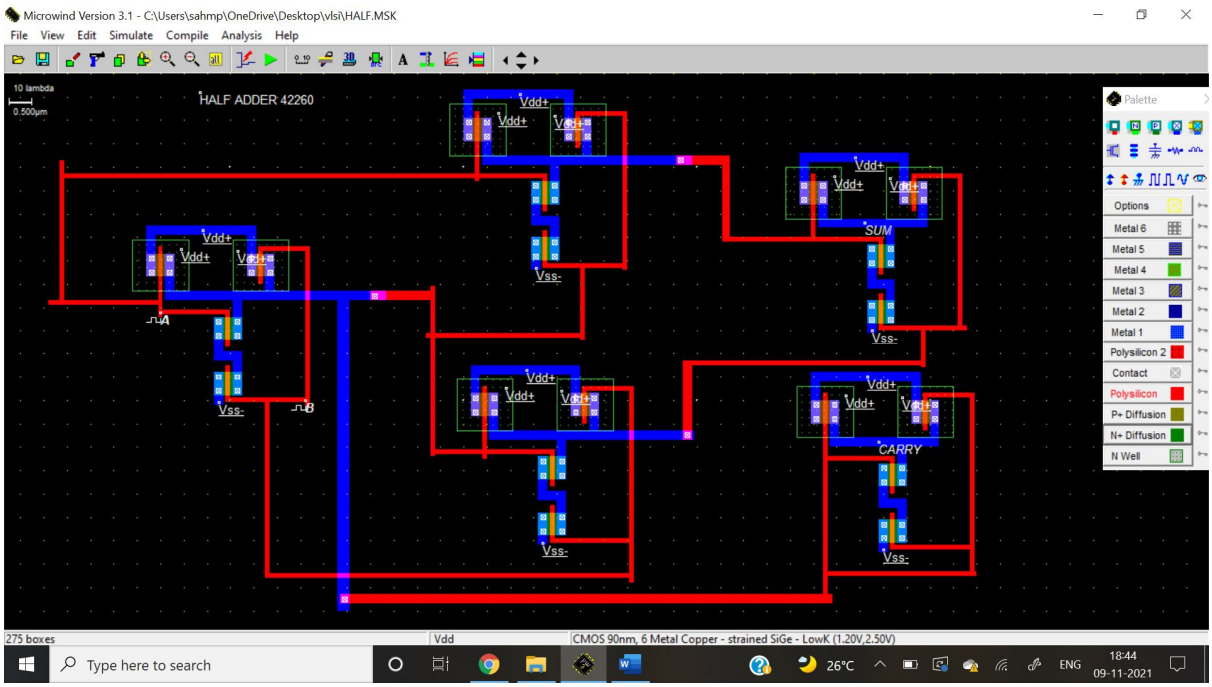
Block Diagram:



Truth-Table:

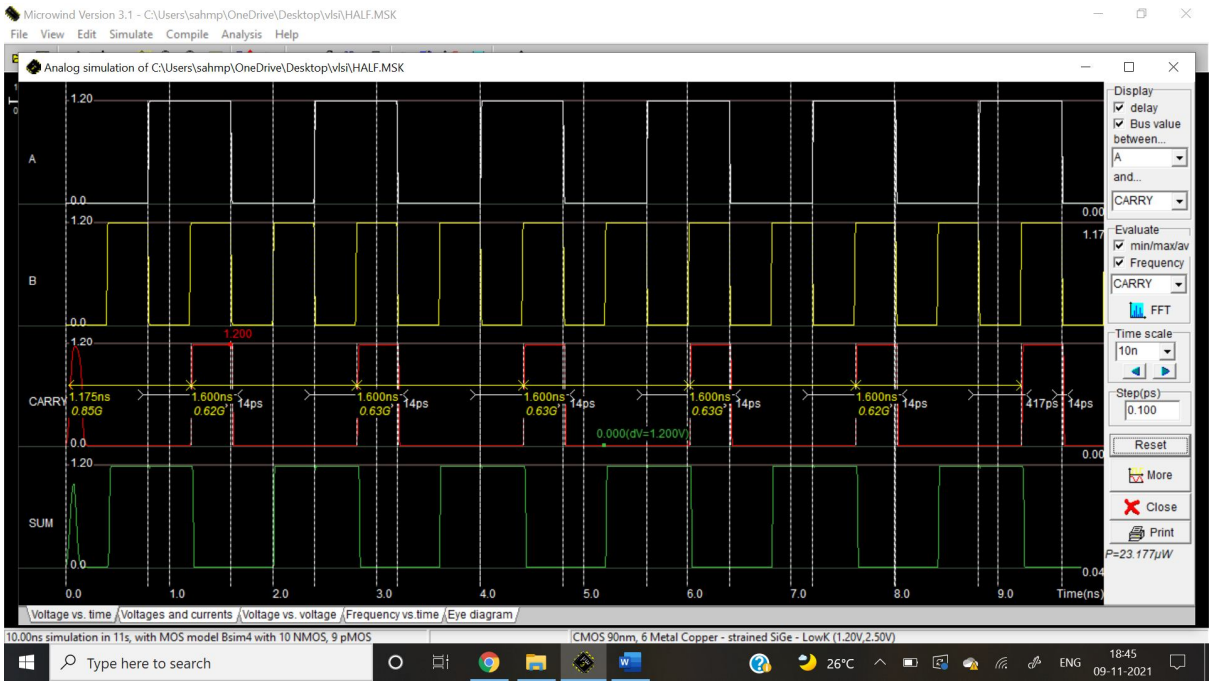
Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Layout:

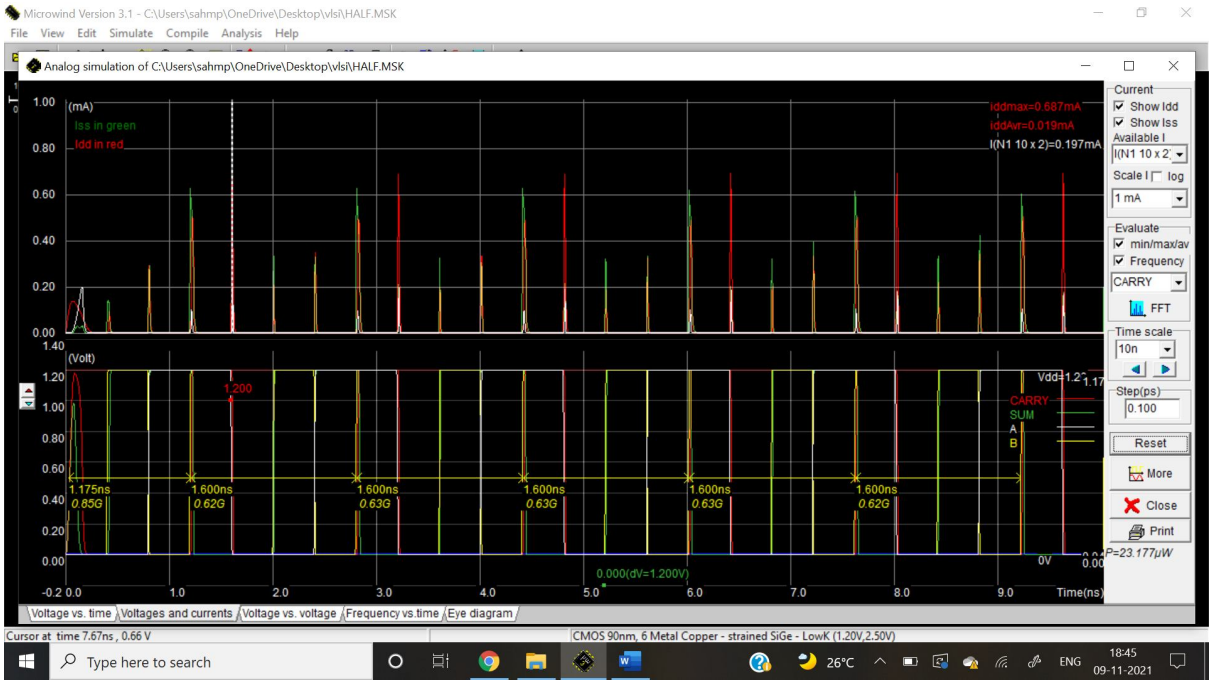


Waveforms:

a) Vin , Vout



b) Vout , Iout



Performance Analysis:

Pdynamic	23.177uW
fmax	0.63GHz

Conclusions:

Thus, we have:

1) Drawn the LAYOUT for CMOS Inverter, NAND GATE, NOR GATE AND HALF ADDER using 90 nm & 120 nm Foundry.

2) Simulated the LAYOUT to observe waveforms & verified its functionality as per TRUTH-TABLE.

3) Noted the values of Pdynamic for floating Load.

4) Appreciated the validity of the mathematical model : Pdynamic = CL * (Vdd)2*fclk by Doubling & Halving the values of CL& fclk

5) Found a reduction in Pdynamic by using a better Foundry i.e. 90 nm instead of 120 nm

6) Learnt that the presence of spikes in O / P waveform at Switching instants indicate the inability of the MOSFETs to switch at GHz frequencies.

7) Learnt that the using a better Foundry enables the MOSFETs the inability of the MOSFETs to switch at Higher GHz frequencies ,as proved by the removal of Spikes at the O/P.