Class : BE 6

Roll. No : 42260

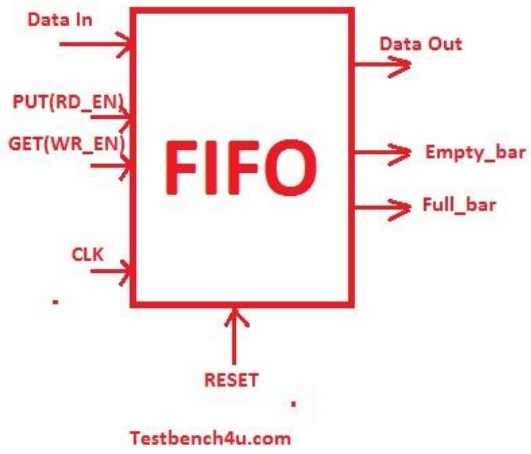
Assignment No. : 3

Assignment Name : FIFO memory

Date Of Performance : 4/10/21

Assignment: Write a VHDL Program to Model a FIFO memory. Synthesize the model for the target PLD. Simulate the model using a TestBench. Implement it on the target PLD

Block Diagram:



Main VHDL Program:

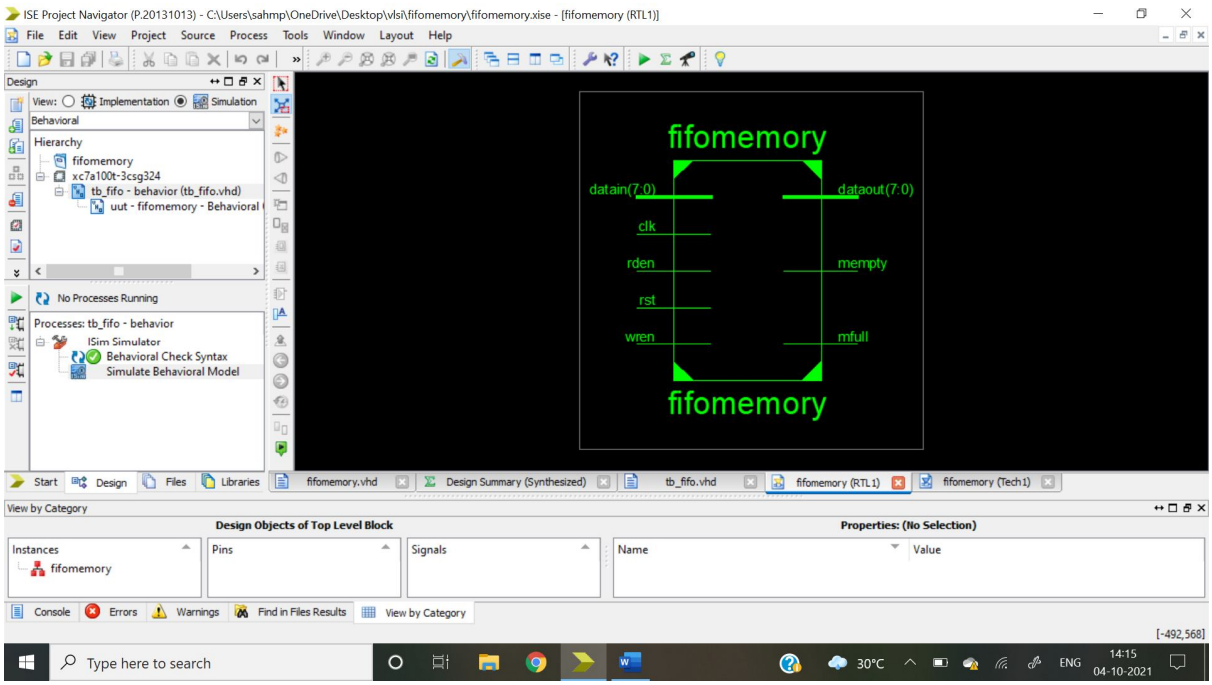
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
```

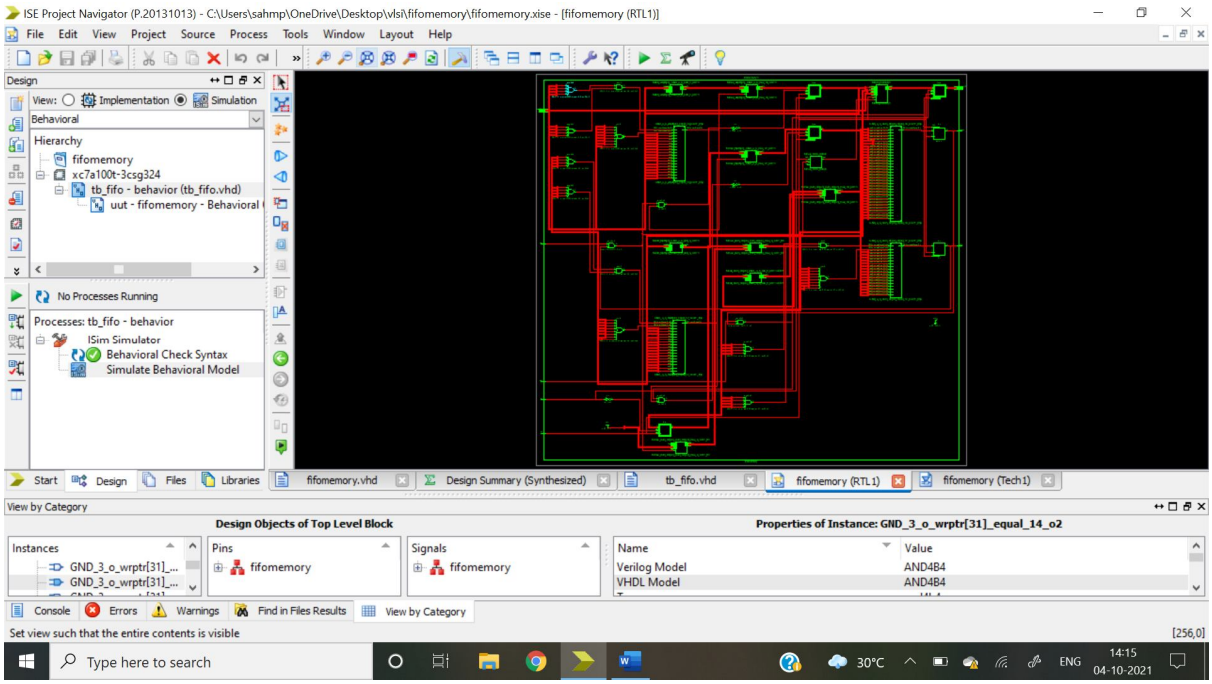
```
--use UNISIM.VComponents.all;

entity fifomemory is
   Port ( datain : in  STD_LOGIC_VECTOR (7 downto 0);
          clk : in  STD_LOGIC;
          rst : in  STD_LOGIC;
          wren : in  STD_LOGIC;
          rden : in  STD_LOGIC;
          dataout : out  STD_LOGIC_VECTOR (7 downto 0);
          mfull : out  STD_LOGIC;
          mempty : out  STD_LOGIC);
end fifomemory;

architecture Behavioral of fifomemory is
signal depth : integer := 16;
type memory_type is array (0 to depth-1) of STD_LOGIC_VECTOR(7 downto 0); --width
signal memory : memory_type := (others =>(others => '0'));
signal rdptr : integer := 0;
signal wrptr : integer := 0;
signal empty : std_logic:='0';
signal full : std_logic:='0';

begin --concurrent
mempty <= empty;
mfull <= full;
process(clk,rst) --sequential
variable num_ele : integer :=0;
            begin
            if (rst ='1') then
                        dataout <= "00000000";
                        empty<='1';
```

```
            full<='0';
            rdptr<=0;
            wrptr<=0;
elsif (rising_edge (clk)) then

            if (wren = '1' and full = '0') then
            memory(wrptr) <= datain;
            wrptr <= wrptr+1;
            num_ele := num_ele+1;
            end if;

            if (rden='1' and empty='0') then
            dataout <= memory(rdptr);
            rdptr <= rdptr+1;
            num_ele := num_ele-1;
            end if;

            if (rdptr = depth) then
            rdptr<=0;
            end if;

            if (wrptr = depth) then
            wrptr<=0;
            end if;

            if (num_ele = 0) then
                        empty <= '1';
            else
                        empty <= '0';
            end if;
```

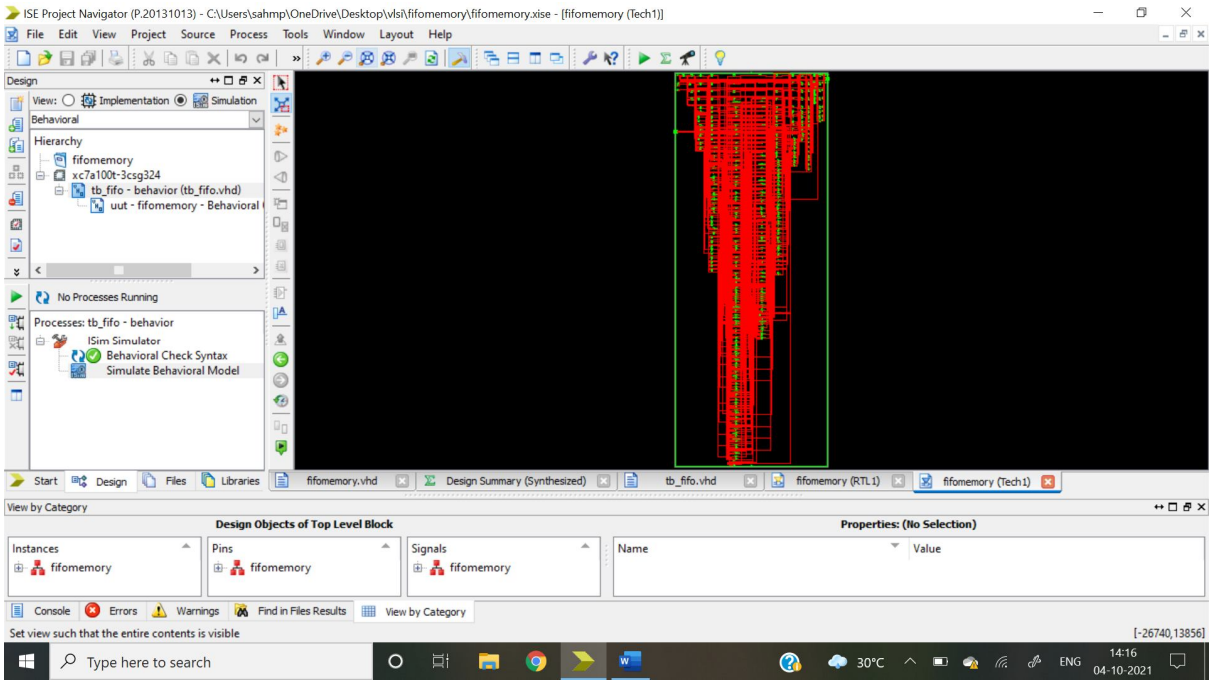
```
                if (num_ele = depth) then
                        full <= '1';
                else
                        full <= '0';
                end if;


        end if;
end process;
end Behavioral;
```

RTL Schematic:





Technology Schematic:



Synthesis Report

a) Device Utilisation Summary

Top Level Output File Name : fifomemory.ngc

Primitive and Black Box Usage:

```
------------------------------
# BELS                  : 284
#      GND              : 1
#      INV              : 34
#      LUT1             : 39
#      LUT2             : 4
#      LUT3             : 2
#      LUT4             : 32
#      LUT5             : 2
#      LUT6             : 25
#      MUXCY            : 70
#      VCC              : 1
#      XORCY            : 74
# FlipFlops/Latches     : 52
#      FDC              : 1
#      FDCE             : 18
#      FDE              : 32
#      FDP              : 1
# RAMS                  : 3
#      RAM32M           : 1
#      RAM32X1D         : 2
# Clock Buffers         : 1
#      BUFGP            : 1
# IO Buffers            : 21
#      IBUF             : 11
#      OBUF             : 10
```

Device utilization summary:

```
---------------------------
```

Selected Device : 7a100tcsg324-3

Slice Logic Utilization:

```
 Number of Slice Registers:          52  out of  126800     0%
 Number of Slice LUTs:              146  out of  63400     0%
   Number used as Logic:            138  out of  63400     0%
   Number used as Memory:             8  out of  19000     0%
     Number used as RAM:              8
```

Slice Logic Distribution:

```
 Number of LUT Flip Flop pairs used:   151
```

Number with an unused Flip Flop: 99 out of 151 65%
Number with an unused LUT: 5 out of 151 3%
Number of fully used LUT-FF pairs: 47 out of 151 31%
Number of unique control sets: 5

IO Utilization:
Number of IOs: 22
Number of bonded IOBs: 22 out of 210 10%

Specific Feature Utilization:
Number of BUFG/BUFGCTRLs: 1 out of 32 3%

b) Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 55    |
-----------------------------------+------------------------+-------+
```

Asynchronous Control Signals Information:

```
----------------------------------------
```

No asynchronous control signals found in this design

Timing Summary:

```
---------------
```

Speed Grade: -3

Minimum period: 4.796ns (Maximum Frequency: 208.507MHz)
Minimum input arrival time before clock: 4.578ns
Maximum output required time after clock: 0.748ns
Maximum combinational path delay: No path found

Timing Details:

```
---------------
```

All values displayed in nanoseconds (ns)

Testbench Program:

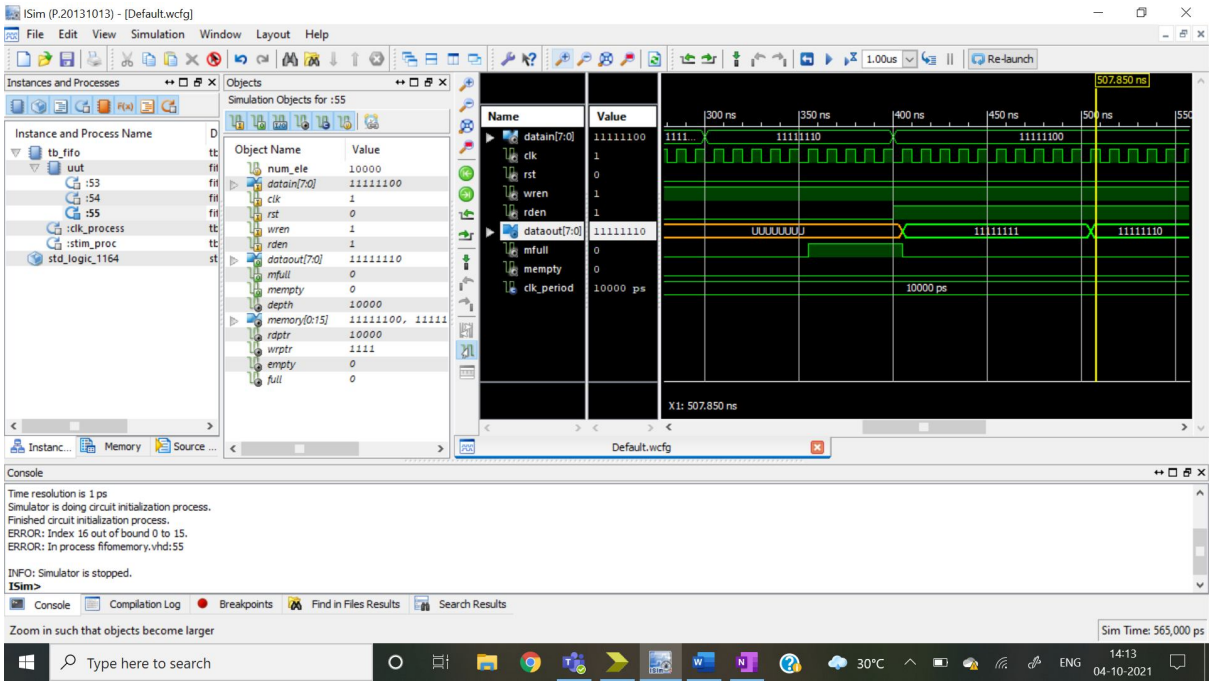
```
LIBRARY ieee;

USE ieee.std_logic_1164.ALL;
```

```
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;

ENTITY tb_fifo IS
END tb_fifo;

ARCHITECTURE behavior OF tb_fifo IS

   -- Component Declaration for the Unit Under Test (UUT)

   COMPONENT fifomemory
   PORT(
        datain : IN  std_logic_vector(7 downto 0);
        clk : IN  std_logic;
        rst : IN  std_logic;
        wren : IN  std_logic;
        rden : IN  std_logic;
        dataout : OUT  std_logic_vector(7 downto 0);
        mfull : OUT  std_logic;
        mempty : OUT  std_logic
       );
   END COMPONENT;


  --Inputs
  signal datain : std_logic_vector(7 downto 0) := (others => '0');
  signal clk : std_logic := '0';
  signal rst : std_logic := '0';
  signal wren : std_logic := '0';
```

```
  signal rden : std_logic := '0';

          --Outputs
  signal dataout : std_logic_vector(7 downto 0);
  signal mfull : std_logic;
  signal mempty : std_logic;

  -- Clock period definitions
  constant clk_period : time := 10 ns;

BEGIN

          -- Instantiate the Unit Under Test (UUT)
  uut: fifomemory PORT MAP (
       datain => datain,
       clk => clk,
       rst => rst,
       wren => wren,
       rden => rden,
       dataout => dataout,
       mfull => mfull,
       mempty => mempty
      );

  -- Clock process definitions
  clk_process :process
  begin
                    clk <= '0';
                    wait for clk_period/2;
                    clk <= '1';
                    wait for clk_period/2;
```

```
  end process;
   -- Stimulus process
  stim_proc: process
  begin
    -- hold reset state for 100 ns.
    wait for 100 ns;

    wait for clk_period*10;

    -- insert stimulus here
                    datain<="11111111";
                    wren<='1';
                    wait for 100 ns;
                    datain<="11111110";
                    wren<='1';
                    wait for 100 ns;
                    rden<='1';
                    datain<="11111100";
                    wren<='1';
                    wait for 100 ns;
                    rden<='1';
    wait;
  end process;

END;
```

Isim Waveforms:



Pin Locking Report: Attached separately

Conclusion:

Thus we have :

1) Modeled a FIFO memory using Behavioral Modeling Style.

2) Observed following Schematics : RTL & Technology Schematics generated Post-Synthesis.

3) Interpreted Device Utilisation Summary in terms of LUTs , SLICES , IOBs , Multiplexers & D FFs used out of the available device resources.

4) Interpreted the TIMING Report in terms of Maximum combinational delay as indicative of the Maximum Operating Frequency .

5) Written a TESTBENCH to verify the functionality of FIFO memory & verified the functionality as per the TRUTH-TABLE ,by observing ISIM Waveforms.

6) Used PlanAhead Editor for pin-locking.

7) Prototyped the FPGA XC3S250EPQ208-5 to realize FIFO memory & verified its operation by giving suitable input combinations