Class : BE 6

Roll. No : 42260

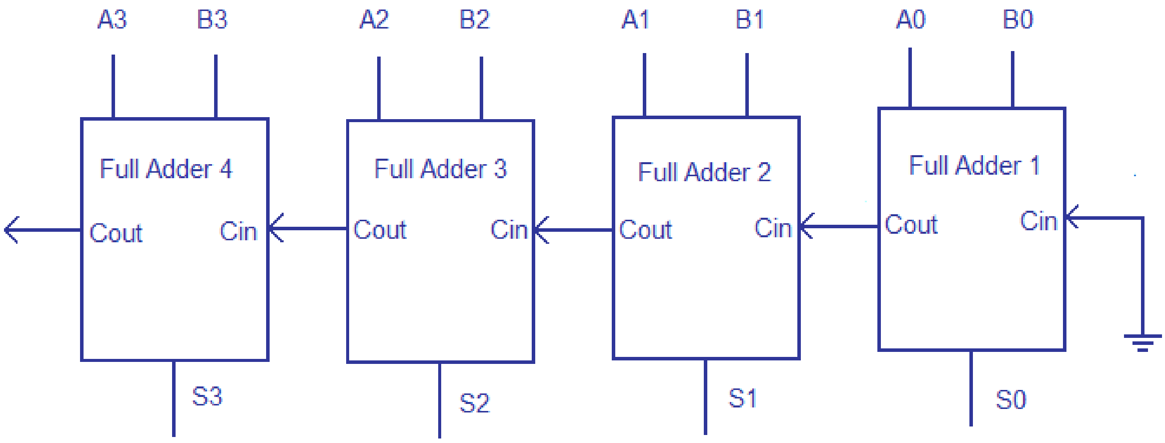
Assignment No. : 1

Assignment Name : 4 bit ripple carry adder

Date Of Performance : 25/8/21

Assignment: Write a VHDL Program to Model a 4 bit ripple carry adder. Synthesize the model for the target PLD. Simulate the model using a TestBench. Implement it on the target PLD

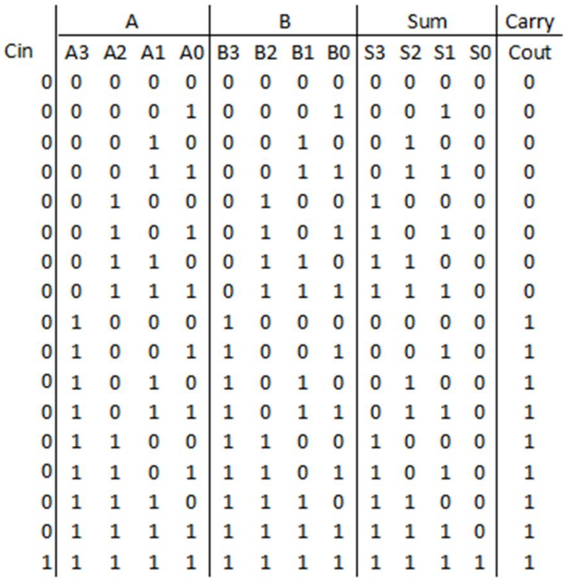
Block Diagram:



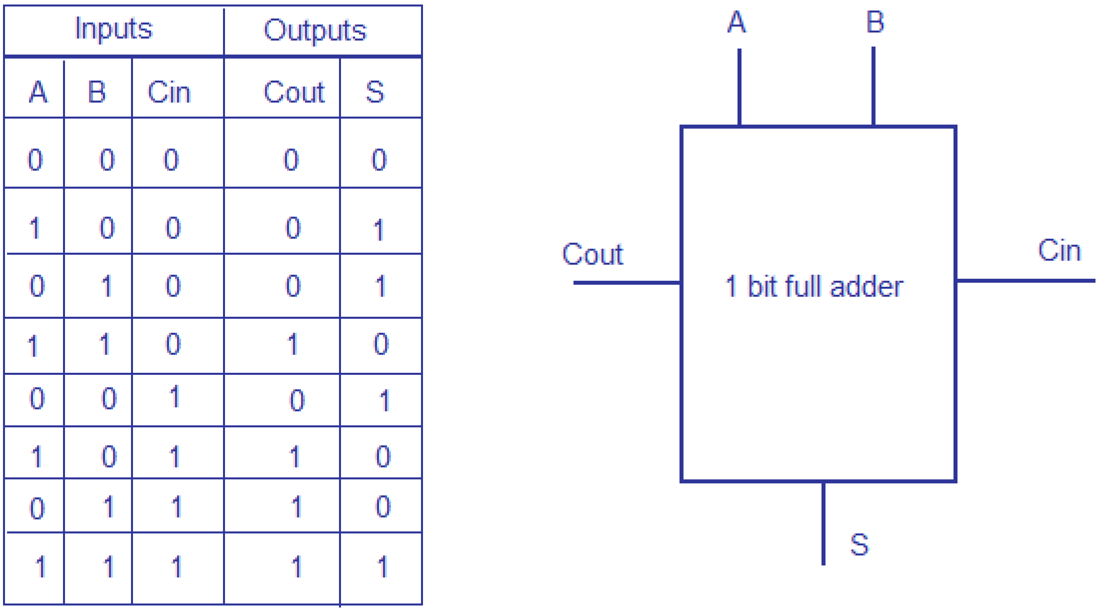
4 bit ripple carry adder

www.circuitstoday.com

Truth Table:



	A				B				Sum				Carry
Cin	A3	A2	A1	A0	B3	B2	B1	B0	S3	S2	S1	S0	Cout
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	1	0	0	1	0	0
0	0	0	1	0	0	0	1	0	0	1	0	0	0
0	0	0	1	1	0	0	1	1	0	1	1	0	0
0	0	1	0	0	0	1	0	0	1	0	0	0	0
0	0	1	0	1	0	1	0	1	1	0	1	0	0
0	0	1	1	0	0	1	1	0	1	1	0	0	0
0	0	1	1	1	0	1	1	1	1	1	1	0	0
0	1	0	0	0	1	0	0	0	0	0	0	0	1
0	1	0	0	1	1	0	0	1	0	0	1	0	1
0	1	0	1	0	1	0	1	0	0	1	0	0	1
0	1	0	1	1	1	0	1	1	0	1	1	0	1
0	1	1	0	0	1	1	0	0	1	0	0	0	1
0	1	1	0	1	1	1	0	1	1	0	1	0	1
0	1	1	1	0	1	1	1	0	1	1	0	0	1
0	1	1	1	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1



Inputs			Outputs	
A	B	Cin	Cout	S
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

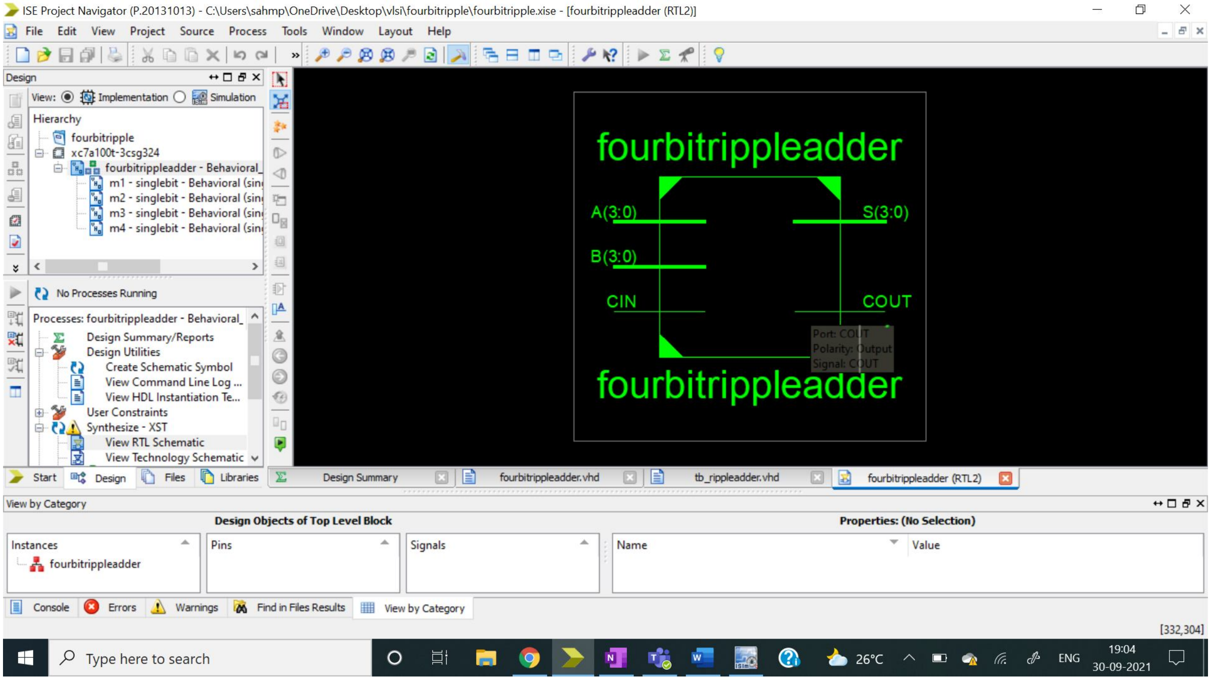
1 bit full adder truth table & schematic

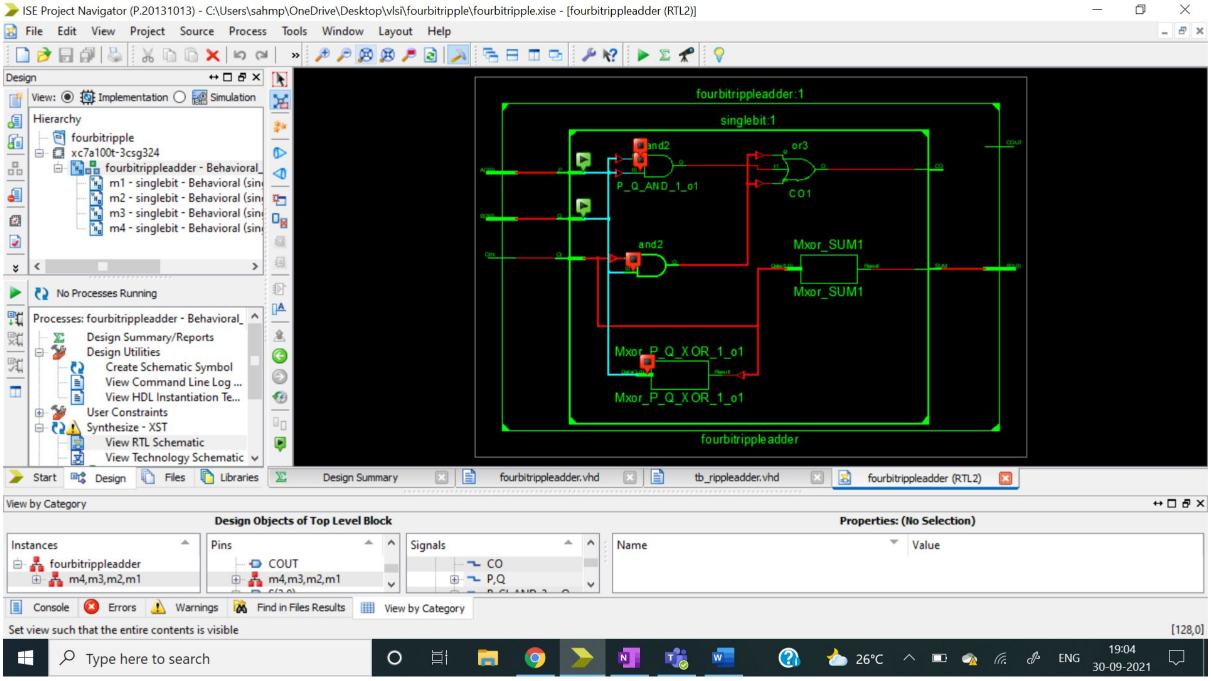
Main VHDL Program:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity singlebit is
   Port ( P : in  STD_LOGIC;
          Q : in  STD_LOGIC;
          CI : in  STD_LOGIC;
          SUM : out  STD_LOGIC;
          CO : out  STD_LOGIC);
end singlebit;

architecture Behavioral of singlebit is

begin

SUM <= ((P XOR Q) XOR CI);
```

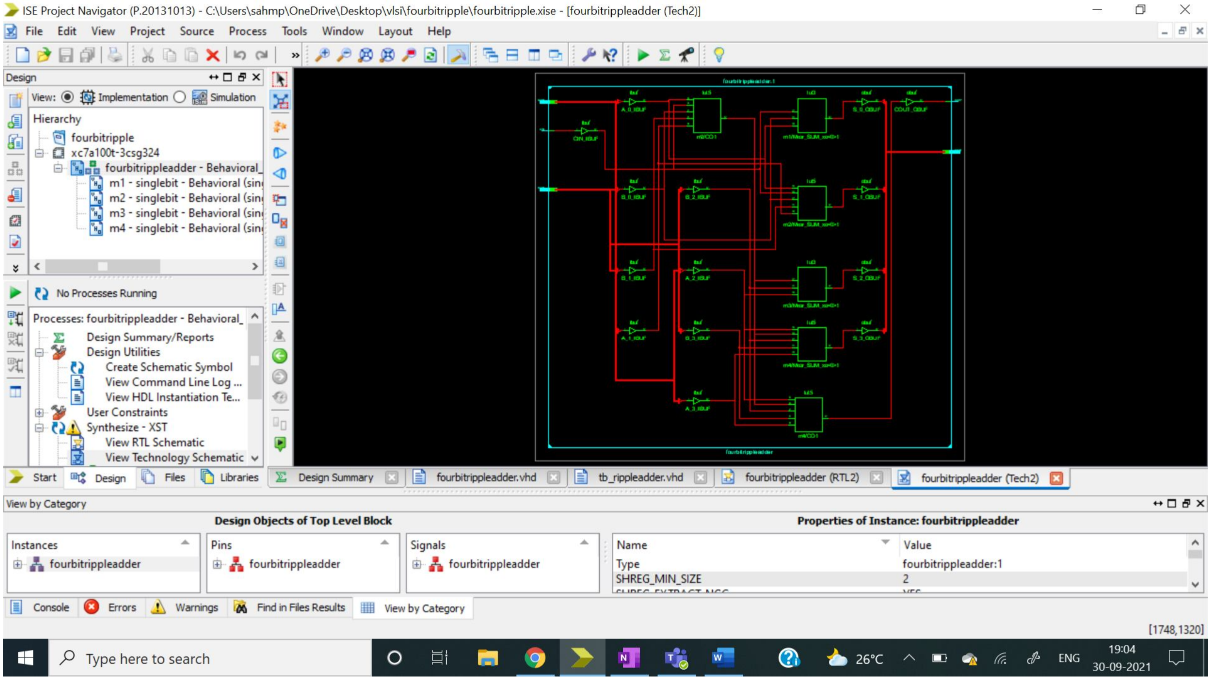
```
CO <= (P AND Q) OR (Q AND CI) OR (P AND CI);


end Behavioral;


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity fourbitrippleadder is
PORT( A : IN  std_logic_vector(3 downto 0);
                B : IN  std_logic_vector(3 downto 0);
                CIN : IN  std_logic;
                COUT : OUT  std_logic;
                S : OUT  std_logic_vector(3 downto 0));
--    Port ( A0 : in  STD_LOGIC;
--           A1 : in  STD_LOGIC;
--           A2 : in  STD_LOGIC;
--           A3 : in  STD_LOGIC;
--           B0 : in  STD_LOGIC;
--           B1 : in  STD_LOGIC;
--           B2 : in  STD_LOGIC;
--           B3 : in  STD_LOGIC;
--        CIN : in  STD_LOGIC;
--        COUT : out  STD_LOGIC;
--        S0 : out  STD_LOGIC;
--        S1 : out  STD_LOGIC;
--        S2 : out  STD_LOGIC;
--        S3 : out  STD_LOGIC);
end fourbitrippleadder;

architecture Behavioral_Sampreeti of fourbitrippleadder is


component singlebit
  Port ( P : in  STD_LOGIC;
      Q : in  STD_LOGIC;
                           CI : in  STD_LOGIC;
      SUM : out  STD_LOGIC;
      CO : out  STD_LOGIC);
end COMPONENT;




signal TEMP0,TEMP1,TEMP2:STD_LOGIC;
begin


m1: singlebit port map(A(0),B(0),CIN,S(0),TEMP0);
m2: singlebit port map(A(1),B(1),TEMP0,S(1),TEMP1);
m3: singlebit port map(A(2),B(2),TEMP1,S(2),TEMP2);
m4: singlebit port map(A(3),B(3),TEMP2,S(3),COUT);

end Behavioral_Sampreeti;
```

RTL Schematic:


ISE Project Navigator (P.20131013) - C:\Users\sahmp\OneDrive\Desktop\vlsi\fourbitripple\fourbitripple.xise - [fourbitrippleadder (RTL2)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
fourbitripple
xc7a100t-3csg324
fourbitrippleadder - Behavioral
m1 - singlebit - Behavioral
m2 - singlebit - Behavioral
m3 - singlebit - Behavioral
m4 - singlebit - Behavioral
No Processes Running
Processes: fourbitrippleadder - Behavioral
Design Summary/Reports
Design Utilities
Create Schematic Symbol
View Command Line Log ...
View HDL Instantiation Te...
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
fourbitrippleadder
A(3:0)
B(3:0)
CIN
S(3:0)
COUT
Port: COUT
Polarity: Output
Signal: COUT
fourbitrippleadder
Start Design Files Libraries
Design Summary
fourbitrippleadder.vhd
tb_rippleadder.vhd
fourbitrippleadder (RTL2)
View by Category
Design Objects of Top Level Block
Properties: (No Selection)
Instances
fourbitrippleadder
Pins
Signals
Name
Value
Console Errors Warnings Find in Files Results View by Category
[332,304]
Type here to search
26°C
ENG
19:04
30-09-2021


ISE Project Navigator (P.20131013) - C:\Users\sahmp\OneDrive\Desktop\vlsi\fourbitripple\fourbitripple.xise - [fourbitrippleadder (RTL2)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
fourbitripple
xc7a100t-3csg324
fourbitrippleadder - Behavioral
m1 - singlebit - Behavioral
m2 - singlebit - Behavioral
m3 - singlebit - Behavioral
m4 - singlebit - Behavioral
No Processes Running
Processes: fourbitrippleadder - Behavioral
Design Summary/Reports
Design Utilities
Create Schematic Symbol
View Command Line Log ...
View HDL Instantiation Te...
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
fourbitrippleadder:1
singlebit:1
and2
P_Q_AND_1_o1
or3
CO1
and2
Mxor_SUM1
Mxor_SUM1
Mxor_P_Q_XOR_1_o1
Mxor_P_Q_XOR_1_o1
fourbitrippleadder
Start Design Files Libraries
Design Summary
fourbitrippleadder.vhd
tb_rippleadder.vhd
fourbitrippleadder (RTL2)
View by Category
Design Objects of Top Level Block
Properties: (No Selection)
Instances
fourbitrippleadder
m4,m3,m2,m1
Pins
COUT
m4,m3,m2,m1
Signals
CO
P,Q
Name
Value
Console Errors Warnings Find in Files Results View by Category
Set view such that the entire contents is visible
[128,0]
Type here to search
26°C
ENG
19:04
30-09-2021

Technology Schematic:


ISE Project Navigator (P.20131013) - C:\Users\sahmp\OneDrive\Desktop\vlsi\fourbitripple\fourbitripple.xise - [fourbitrippleadder (Tech2)]
File
Edit
View
Project
Source
Process
Tools
Window
Layout
Help
Design
View: ● Implementation ○ Simulation
Hierarchy
fourbitripple
xc7a100t-3csg324
fourbitrippleadder - Behavioral
m1 - singlebit - Behavioral (sin
m2 - singlebit - Behavioral (sin
m3 - singlebit - Behavioral (sin
m4 - singlebit - Behavioral (sin
No Processes Running
Processes: fourbitrippleadder - Behavioral
Design Summary/Reports
Design Utilities
Create Schematic Symbol
View Command Line Log ...
View HDL Instantiation Te...
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Start
Design
Files
Libraries
Design Summary
fourbitrippleadder.vhd
tb_rippleadder.vhd
fourbitrippleadder (RTL2)
fourbitrippleadder (Tech2)
View by Category
Design Objects of Top Level Block
Properties of Instance: fourbitrippleadder
Instances
fourbitrippleadder
Pins
fourbitrippleadder
Signals
fourbitrippleadder
Name
Value
Type
fourbitrippleadder:1
SHREG_MIN_SIZE
2
Console
Errors
Warnings
Find in Files Results
View by Category
[1748,1320]
Type here to search
26°C
ENG
19:04
30-09-2021

Synthesis Report

a) Device Utilisation Summary

```
Top Level Output File Name        : fourbitrippleadder.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                          : 6
#      LUT3                      : 2
#      LUT5                      : 4
# IO Buffers                      : 14
#      IBUF                     : 9
#      OBUF                       : 5

Device utilization summary:
---------------------------

Selected Device : 7a100tcsg324-3


Slice Logic Utilization:
 Number of Slice LUTs:              6  out of  63400     0%
    Number used as Logic:            6  out of  63400     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:      6
   Number with an unused Flip Flop:       6  out of      6   100%
   Number with an unused LUT:           0  out of      6     0%
   Number of fully used LUT-FF pairs:     0  out of      6     0%
   Number of unique control sets:        0

IO Utilization:
 Number of IOs:                        14
 Number of bonded IOBs:               14  out of    210     6%

Specific Feature Utilization:
```

b) Timing Report

```
NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
No clock signals found in this design

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 1.551ns

Timing Details:
---------------
All values displayed in nanoseconds (ns)
```

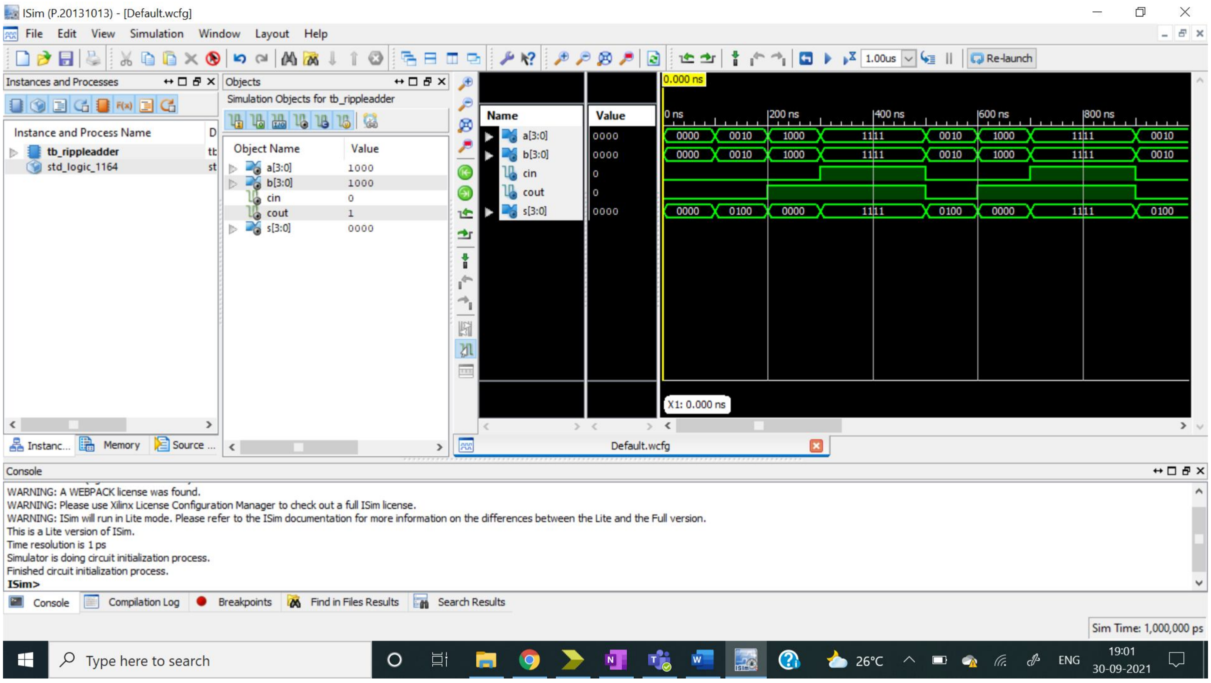
Testbench Program:

```
LIBRARY ieee;

USE ieee.std_logic_1164.ALL;


-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values
```

```
--USE ieee.numeric_std.ALL;

ENTITY tb_rippleadder IS
END tb_rippleadder;

ARCHITECTURE behavior OF tb_rippleadder IS

   -- Component Declaration for the Unit Under Test (UUT)

   COMPONENT fourbitrippleadder
   PORT(
        A : IN  std_logic_vector(3 downto 0);
        B : IN  std_logic_vector(3 downto 0);
        CIN : IN  std_logic;
        COUT : OUT  std_logic;
        S : OUT  std_logic_vector(3 downto 0)
       );
   END COMPONENT;


  --Inputs
  signal A : std_logic_vector(3 downto 0) := (others => '0');
  signal B : std_logic_vector(3 downto 0) := (others => '0');
  signal CIN : std_logic := '0';

         --Outputs
  signal COUT : std_logic;
  signal S : std_logic_vector(3 downto 0);
  -- No clocks detected in port list. Replace <clock> below with
  -- appropriate port name
  --constant <clock>_period : time := 10 ns;

BEGIN

		-- Instantiate the Unit Under Test (UUT)
  uut: fourbitrippleadder PORT MAP (
         A => A,
         B => B,
         CIN => CIN,
         COUT => COUT,
         S => S
       );

  -- Clock process definitions
--   <clock>_process :process
--   begin
--			<clock> <= '0';
--			wait for <clock>_period/2;
--			<clock> <= '1';
--			wait for <clock>_period/2;
--   end process;


  -- Stimulus process
  stim_proc: process
  begin
    -- hold reset state for 100 ns.
    wait for 100 ns;

   A<="0010";
		B<="0010";
```

```
           CIN <='0';


            wait for 100 ns;
           A<="1000";
           B<="1000";
           CIN <='0';


            wait for 100 ns;
           A<="1111";
           B<="1111";
           CIN <='1';


            wait for 100 ns;
    -- insert stimulus here


  end process;


END;
```

Isim Waveforms:



ISim (P.20131013) - [Default.wcfg]

Simulation Objects for tb_rippleadder

Object Name	Value
a[3:0]	1000
b[3:0]	1000
cin	0
cout	1
s[3:0]	0000

Name	Value
a[3:0]	0000
b[3:0]	0000
cin	0
cout	0
s[3:0]	0000

```
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>
```

Sim Time: 1,000,000 ps

Conclusion:

Thus we have :

1) Modeled a 4 bit ripple carry adder using Behavioral Modeling Style.

2) Observed following Schematics : RTL & Technology Schematics generated Post-Synthesis.

3) Interpreted Device Utilisation Summary in terms of LUTs , SLICES , IOBs , Multiplexers & D FFs used out of the available device resources.

4) Interpreted the TIMING Report in terms of Maximum combinational delay as indicative of the Maximum Operating Frequency .

5) Written a TESTBENCH to verify the functionality of 4 bit ripple carry adder & verified the functionality as per the TRUTH-TABLE ,by observing ISIM Waveforms.

6) Prototyped the FPGA XC3S250EPQ208-5 to realize 4 bit ripple carry adder & verified its operation by giving suitable input combinations