Class : BE 6

Roll. No : 42260

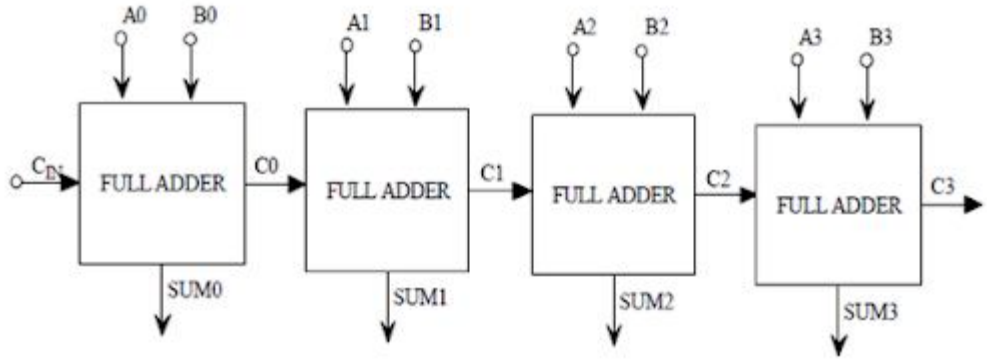
Assignment No. : 1

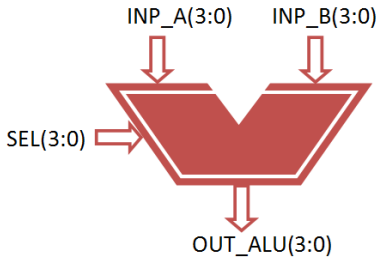
Assignment Name : 4 bit ALU

Date Of Performance : 20/9/21

Assignment: Write a VHDL Program to Model a 4 bit ALU. Synthesize the model for the target PLD. Simulate the model using a TestBench. Implement it on the target PLD

Block Diagram:





Truth Table:

Selection Input			Operation Performed
0	0	0	A + B
0	0	1	A - B
0	1	0	A - 1
0	1	1	A + 1
1	0	0	A and B
1	0	1	A or B
1	1	0	not A
1	1	1	A xor B

Main VHDL Program:

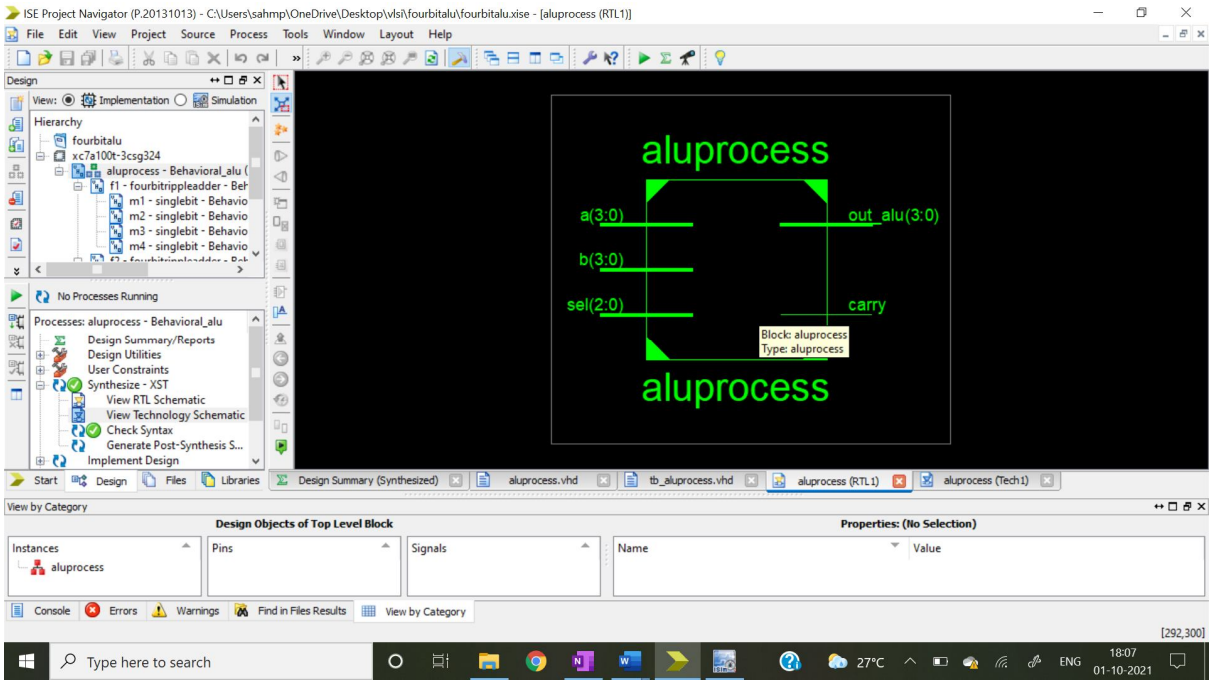
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity singlebit is
   Port ( P : in  STD_LOGIC;
          Q : in  STD_LOGIC;
          CI : in  STD_LOGIC;
          SUM : out  STD_LOGIC;
          CO : out  STD_LOGIC);
end singlebit;
architecture Behavioral_single of singlebit is
begin
SUM <= ((P XOR Q) XOR CI);
CO <= (P AND Q) OR (Q AND CI) OR (P AND CI);
end Behavioral_single;

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity fourbitrippleadder is
PORT( X : IN  std_logic_vector(3 downto 0);
                     Y : IN  std_logic_vector(3 downto 0);
                     CIN : IN  std_logic;
                     COUT : OUT  std_logic;
                     S : OUT  std_logic_vector(3 downto 0));

end fourbitrippleadder;

architecture Behavioral_Sampreeti of fourbitrippleadder is

component singlebit
```

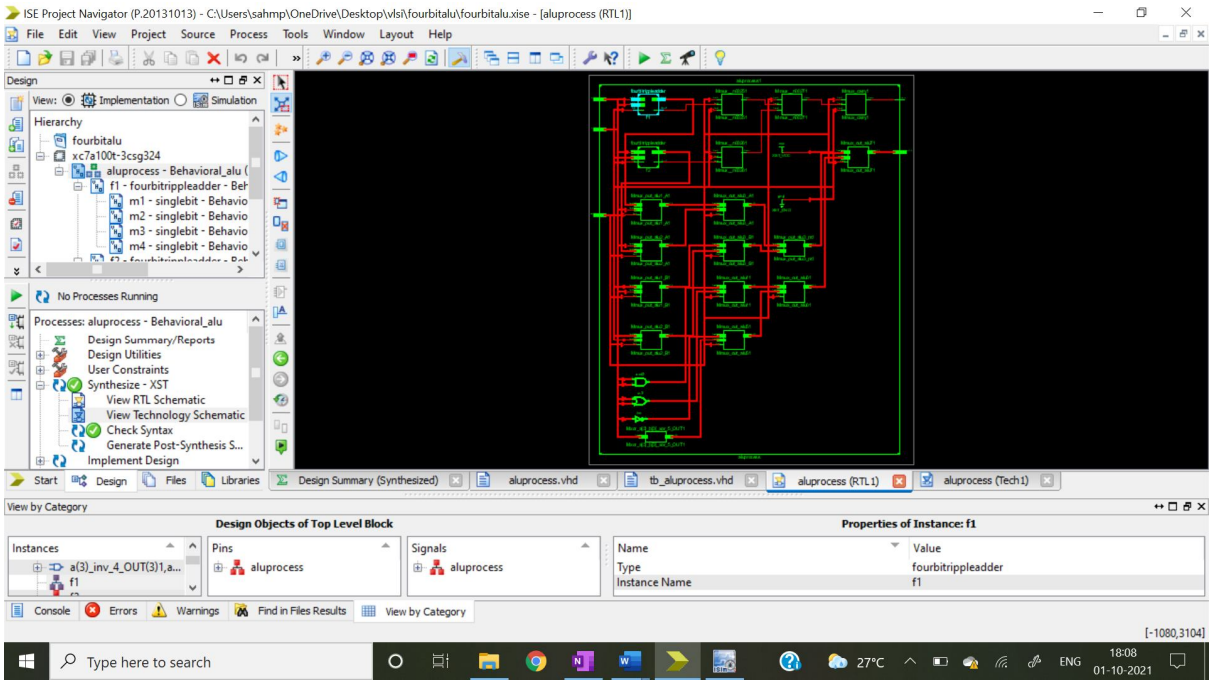
```
   Port ( P : in  STD_LOGIC;
          Q : in  STD_LOGIC;
                                CI : in  STD_LOGIC;
          SUM : out  STD_LOGIC;
          CO : out  STD_LOGIC);
end COMPONENT;



signal TEMP0,TEMP1,TEMP2:STD_LOGIC;
begin

m1: singlebit port map(X(0),Y(0),CIN,S(0),TEMP0);
m2: singlebit port map(X(1),Y(1),TEMP0,S(1),TEMP1);
m3: singlebit port map(X(2),Y(2),TEMP1,S(2),TEMP2);
m4: singlebit port map(X(3),Y(3),TEMP2,S(3),COUT);

end Behavioral_Sampreeti;

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_unsigned.ALL;



entity aluprocess is
 Port ( a : in STD_LOGIC_VECTOR(3 downto 0);
 b : in STD_LOGIC_VECTOR(3 downto 0);
 sel : in STD_LOGIC_VECTOR (2 downto 0);
 out_alu : out STD_LOGIC_VECTOR (3 downto 0);
 carry : out STD_logic);
end aluprocess;
```

```
architecture Behavioral_alu of aluprocess is

component fourbitrippleadder
PORT( X : IN  std_logic_vector(3 downto 0);
                Y : IN  std_logic_vector(3 downto 0);
                CIN : IN  std_logic;
                COUT : OUT  std_logic;
                S : OUT  std_logic_vector(3 downto 0));
end component;

signal hold1: std_logic_vector(3 downto 0);
signal hold2: std_logic_vector(3 downto 0);
signal carry1: std_logic;
signal carry2: std_logic;

begin

f1: fourbitrippleadder port map(a,b,'0',carry1,hold1);
f2: fourbitrippleadder port map(a,"0001",'0',carry2,hold2);
with sel select out_alu <=
                                hold1 when "000" ,
                                a - b when "001" ,
                        a - 1 when "010" ,
                                hold2 when "011" ,
                        a and b when "100" ,
        a or b when "101" ,
                        not a when "110" ,
                        a xor b when "111" ;
with sel select carry <=
                        carry1 when "000" ,
```

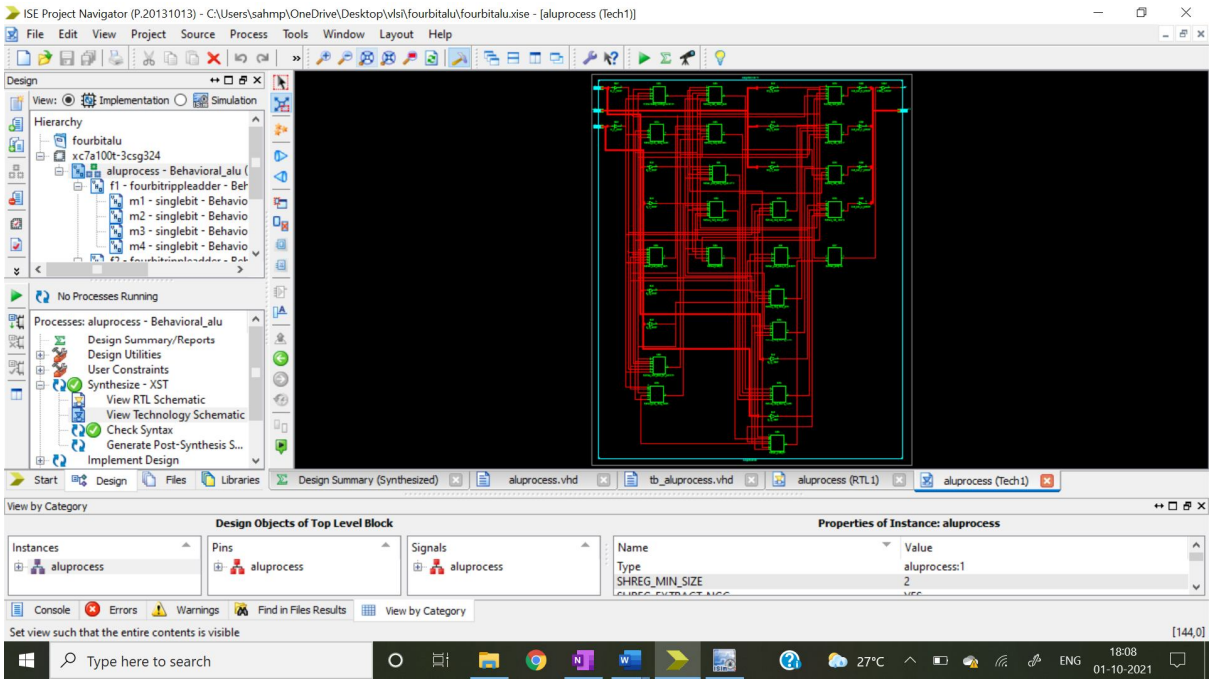
```
                    '0' when "001" ,
                '0' when "010" ,
                    carry2 when "011" ,
                '0' when "100" ,
        '0' when "101" ,
                '0' when "110" ,
                '0' when "111" ;


end Behavioral_alu;
```

RTL Schematic:





Technology Schematic:



Synthesis Report

a) Device Utilisation Summary

Top Level Output File Name : aluprocess.ngc

Primitive and Black Box Usage:

BELS : 21

```
#      LUT2                : 1
#      LUT3                : 2
#      LUT4                : 6
#      LUT5                : 4
#      LUT6                : 8
# IO Buffers                 : 16
#      IBUF                : 11
#      OBUF                : 5

Device utilization summary:
---------------------------

Selected Device : 7a100tcsg324-3


Slice Logic Utilization:
 Number of Slice LUTs:                21  out of  63400     0%
   Number used as Logic:              21  out of  63400     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    21
  Number with an unused Flip Flop:     21  out of     21   100%
  Number with an unused LUT:           0  out of     21     0%
  Number of fully used LUT-FF pairs:    0  out of     21     0%
  Number of unique control sets:        0

IO Utilization:
 Number of IOs:                   16
 Number of bonded IOBs:               16  out of    210     7%

Specific Feature Utilization:
```

b) Timing Report

```
NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
No clock signals found in this design

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
```

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 3.022ns

Timing Details:

All values displayed in nanoseconds (ns)

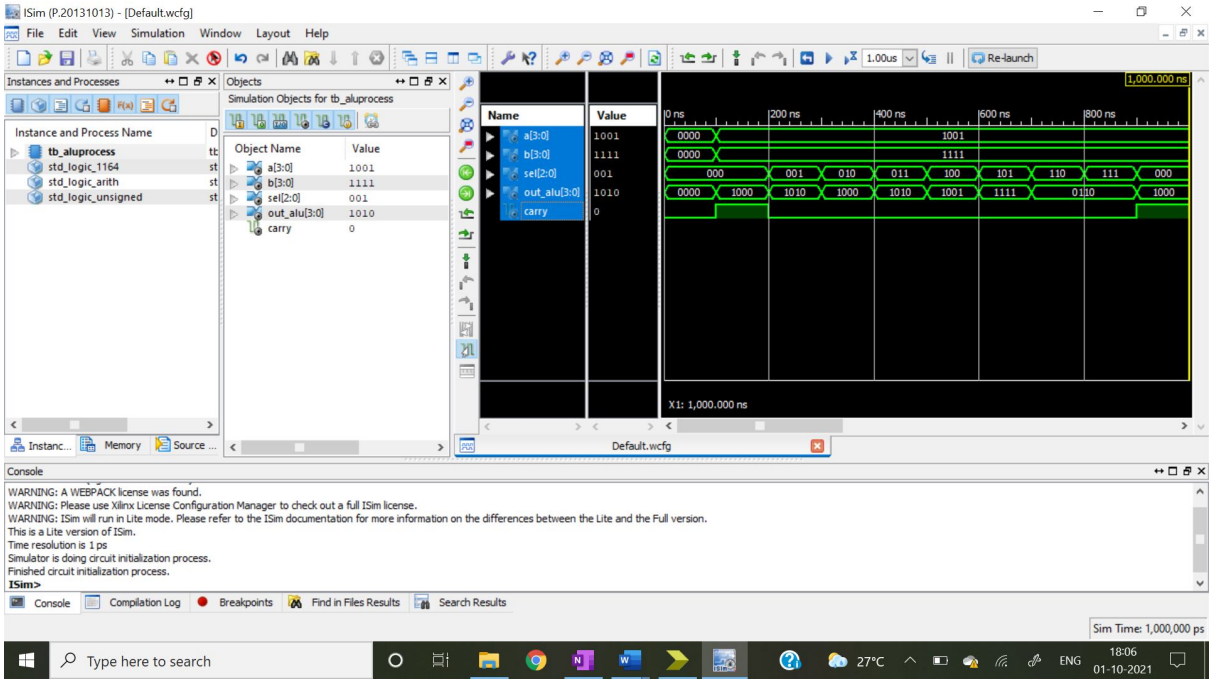
Testbench Program:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
use IEEE.STD_LOGIC_unsigned.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;

ENTITY tb_aluprocess IS
END tb_aluprocess;

ARCHITECTURE behavior OF tb_aluprocess IS

  -- Component Declaration for the Unit Under Test (UUT)

  COMPONENT aluprocess
  PORT(
      a : IN  std_logic_vector(3 downto 0);
      b : IN  std_logic_vector(3 downto 0);
      sel : IN  std_logic_vector(2 downto 0);
      out_alu : OUT  std_logic_vector(3 downto 0);
      carry : OUT  std_logic
     );
```

```
   END COMPONENT;


  --Inputs
  signal a : std_logic_vector(3 downto 0) := (others => '0');
  signal b : std_logic_vector(3 downto 0) := (others => '0');
  signal sel : std_logic_vector(2 downto 0) := (others => '0');

          --Outputs
  signal out_alu : std_logic_vector(3 downto 0);
  signal carry : std_logic;
  -- No clocks detected in port list. Replace <clock> below with
  -- appropriate port name

--   constant <clock>_period : time := 10 ns;

BEGIN

          -- Instantiate the Unit Under Test (UUT)
  uut: aluprocess PORT MAP (
        a => a,
        b => b,
        sel => sel,
        out_alu => out_alu,
        carry => carry
       );

  -- Clock process definitions
--   <clock>_process :process
--   begin
--                     <clock> <= '0';
```

```
--                      wait for <clock>_period/2;
--                      <clock> <= '1';
--                      wait for <clock>_period/2;
--   end process;
   -- Stimulus process
  stim_proc: process
  begin
     -- hold reset state for 100 ns.
     wait for 100 ns;

 a <= "1001";
 b <= "1111";
 sel <= "000";
 wait for 100 ns;
 sel <= "001";
 wait for 100 ns;
 sel <= "010";
 wait for 100 ns;
 sel <= "011";
 wait for 100 ns;
 sel <= "100";
 wait for 100 ns;
 sel <= "101";
 wait for 100 ns;
 sel <= "110";
 wait for 100 ns;
 sel <= "111";
 end process;



END;
```

Isim Waveforms:



Pin Locking Report: Attached separately

Conclusion:

Thus we have :

1) Modeled a 4 bit ALU using Behavioral Modeling Style.

2) Observed following Schematics : RTL & Technology Schematics generated Post-Synthesis.

3) Interpreted Device Utilisation Summary in terms of LUTs , SLICES , IOBs , Multiplexers & D FFs used out of the available device resources.

4) Interpreted the TIMING Report in terms of Maximum combinational delay as indicative of the Maximum Operating Frequency .

5) Written a TESTBENCH to verify the functionality of 4 bit ALU & verified the functionality as per the TRUTH-TABLE ,by observing ISIM Waveforms.

6) Used PlanAhead Editor for pin-locking.

7) Prototyped the FPGA XC3S250EPQ208-5 to realize 4 bit ALU & verified its operation by giving suitable input combinations