Class : BE 6

Roll. No : 42260

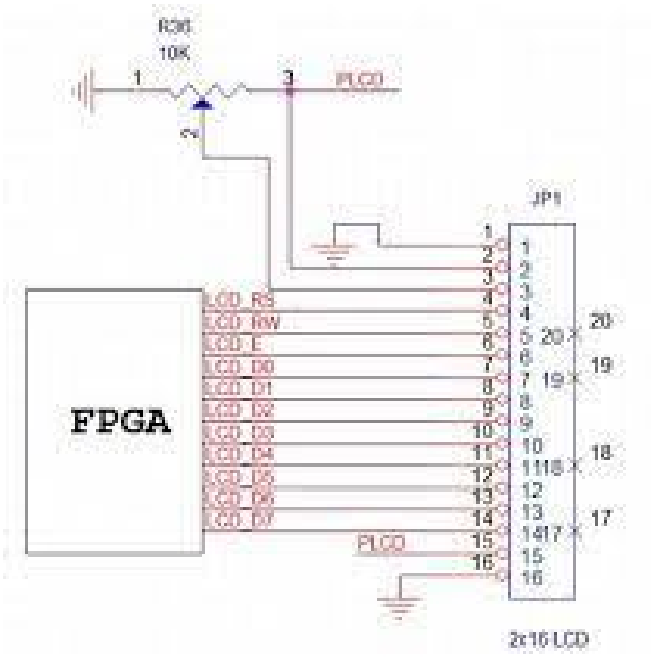
Assignment No. : 4

Assignment Name : Functional simulation of LCD Interfacing

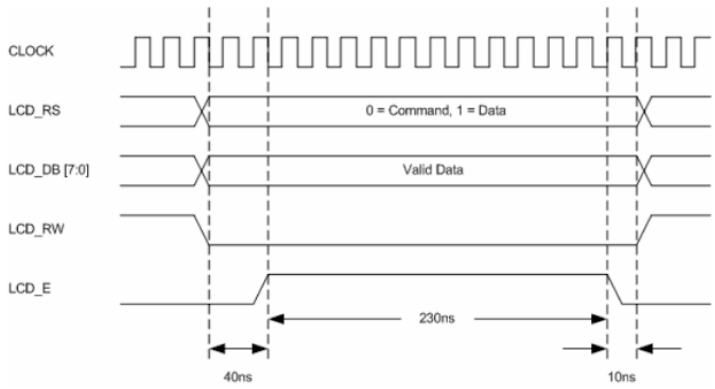
Date Of Performance : 11/10/21

Assignment: Write a VHDL Program to Model a functional simulation of LCD. Synthesize the model for the target PLD. Simulate the model using a TestBench. Implement it on the target PLD

Block Diagram:



Truth Table:

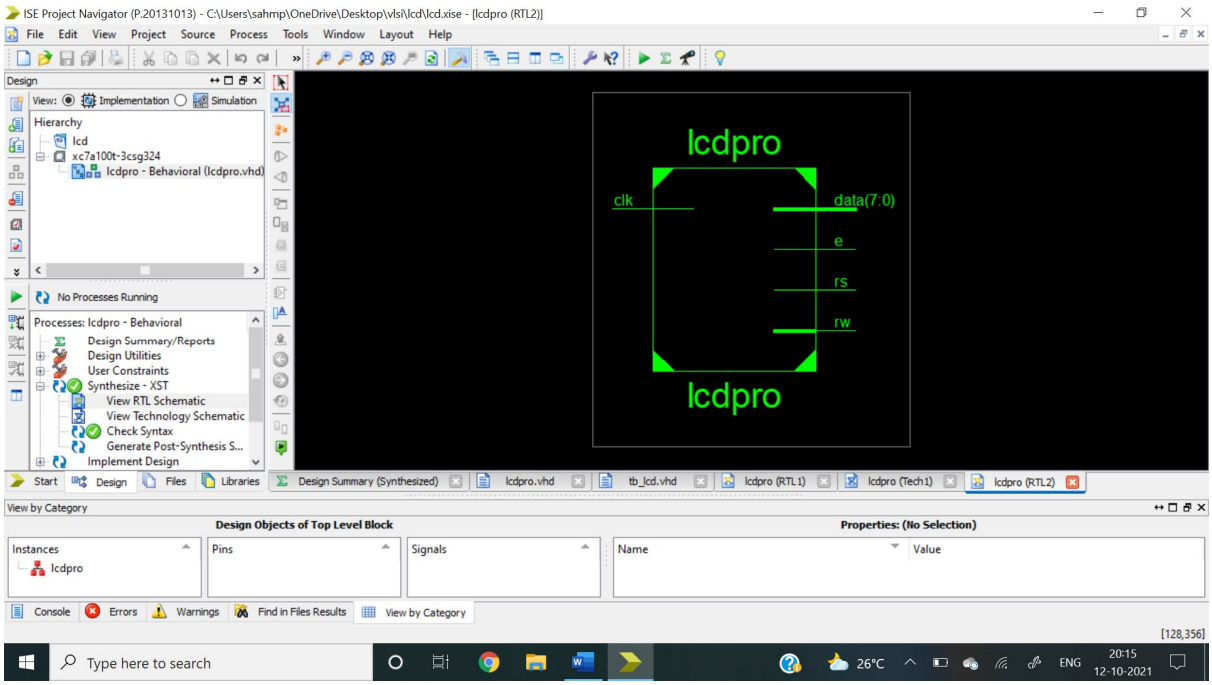


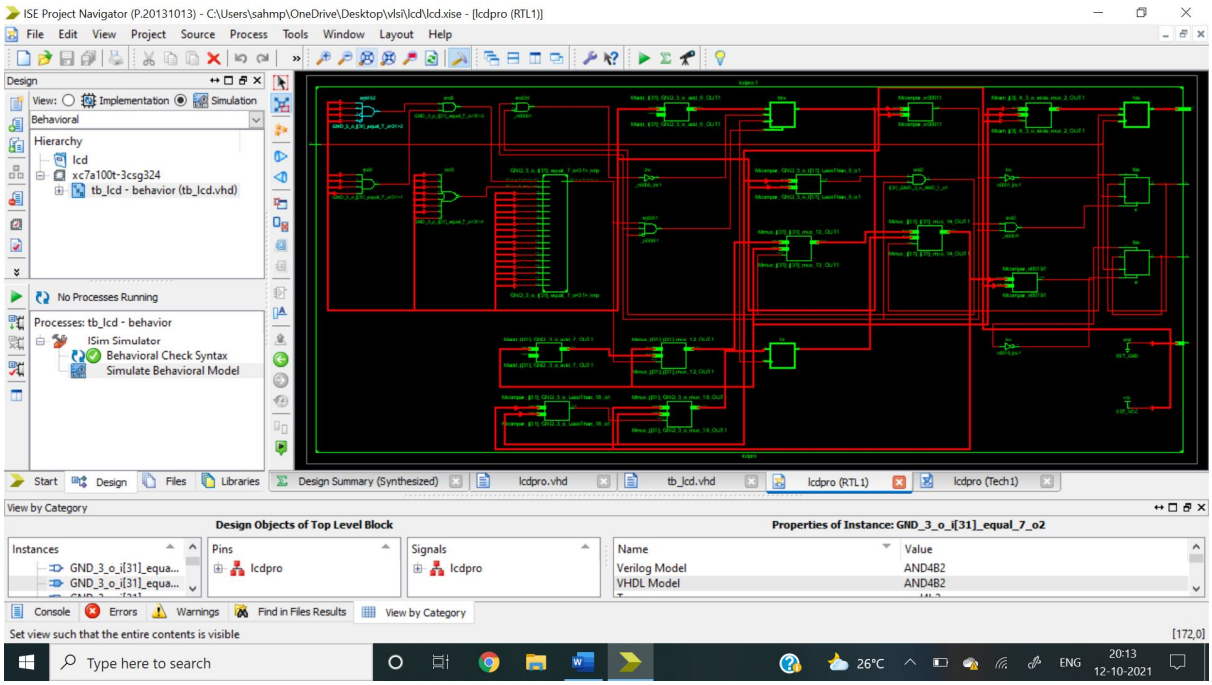
Main VHDL Program:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity lcdpro is
   Port ( clk : in  STD_LOGIC;
          rs : out  STD_LOGIC;
          e : out  STD_LOGIC;
          rw : out  STD_LOGIC;
          data : out  STD_LOGIC_VECTOR (7 downto 0));
end lcdpro;

architecture Behavioral of lcdpro is
constant N: integer :=9;
type arr is array (1 to N) of STD_LOGIC_VECTOR (7 downto 0);
constant datas: arr:=(X"36",X"0c",X"06",X"01",X"C0",x"54",x"45",x"43",x"48");
begin
rw<='0';--write
process(clk)
variable i: integer :=0;
variable j: integer :=1;
begin
```

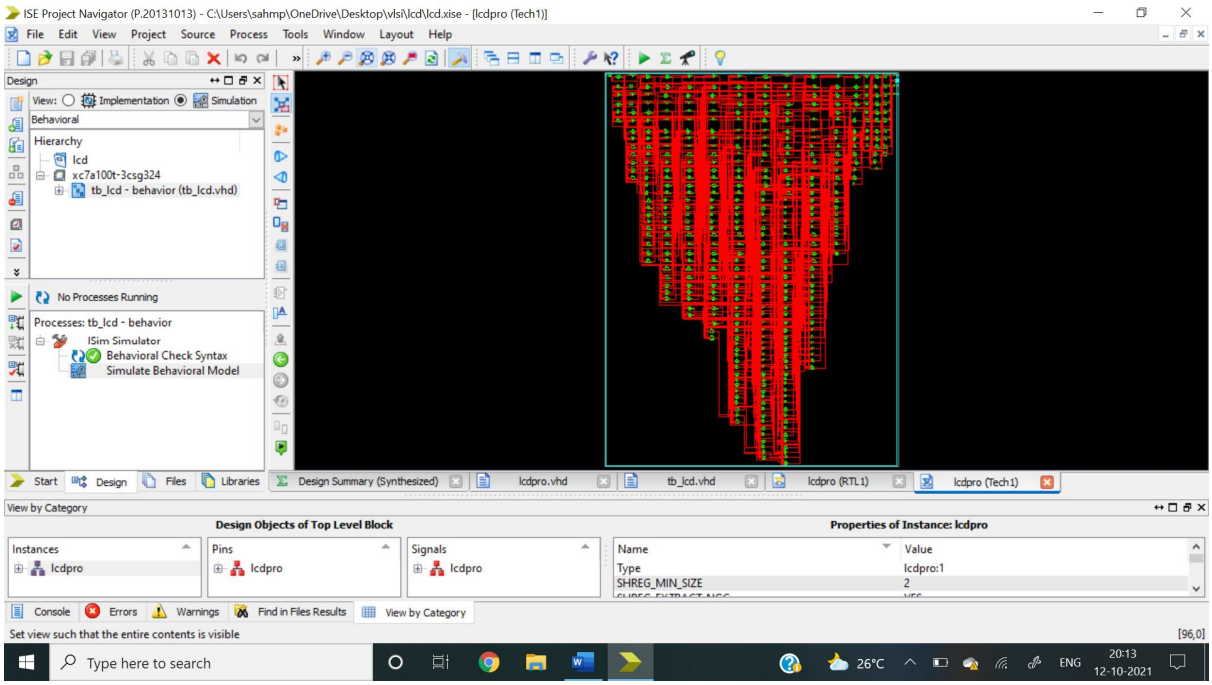
```
if(clk'event and clk='1') then

if i<=100000 then
i:=i+1;
e<='1';
data<=datas(j)(7 downto 0);
elsif i>100000 and i<200000 then
i:=i+1;
e<='0';
elsif i=200000 then
j:=j+1;
i:=0;
end if;

if j<=5 then
rs<='0';
elsif j>5 then
rs<='1';
end if;

if j>N then
j:=6;
end if;

end if;

end process;

end Behavioral;
```

RTL Schematic:





Technology Schematic:



Synthesis Report

a) Device Utilisation Summary

Top Level Output File Name : lcdpro.ngc

Primitive and Black Box Usage:

BELS : 327
GND : 1
INV : 5
LUT1 : 62
LUT2 : 11
LUT3 : 6
LUT4 : 37
LUT5 : 23
LUT6 : 26
MUXCY : 91
VCC : 1
XORCY : 64
FlipFlops/Latches : 74
FD : 32
FDE : 8
FDR : 1
FDRE : 32
FDS : 1
Clock Buffers : 1
BUFGP : 1
IO Buffers : 11
OBUF : 11

Device utilization summary:

Selected Device : 7a100tcsg324-3

Slice Logic Utilization:
Number of Slice Registers: 74 out of 126800 0%
Number of Slice LUTs: 170 out of 63400 0%
Number used as Logic: 170 out of 63400 0%

Slice Logic Distribution:
Number of LUT Flip Flop pairs used: 190
Number with an unused Flip Flop: 116 out of 190 61%
Number with an unused LUT: 20 out of 190 10%
Number of fully used LUT-FF pairs: 54 out of 190 28%
Number of unique control sets: 5

IO Utilization:
Number of IOs: 12
Number of bonded IOBs: 12 out of 210 5%

Specific Feature Utilization:
Number of BUFG/BUFGCTRLs: 1 out of 32 3%

b) Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

Clock Signal	Clock buffer(FF name)	Load
clk	BUFGP	74

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: 4.788ns (Maximum Frequency: 208.851MHz)
Minimum input arrival time before clock: No path found
Maximum output required time after clock: 0.645ns
Maximum combinational path delay: No path found

Timing Details:

All values displayed in nanoseconds (ns)

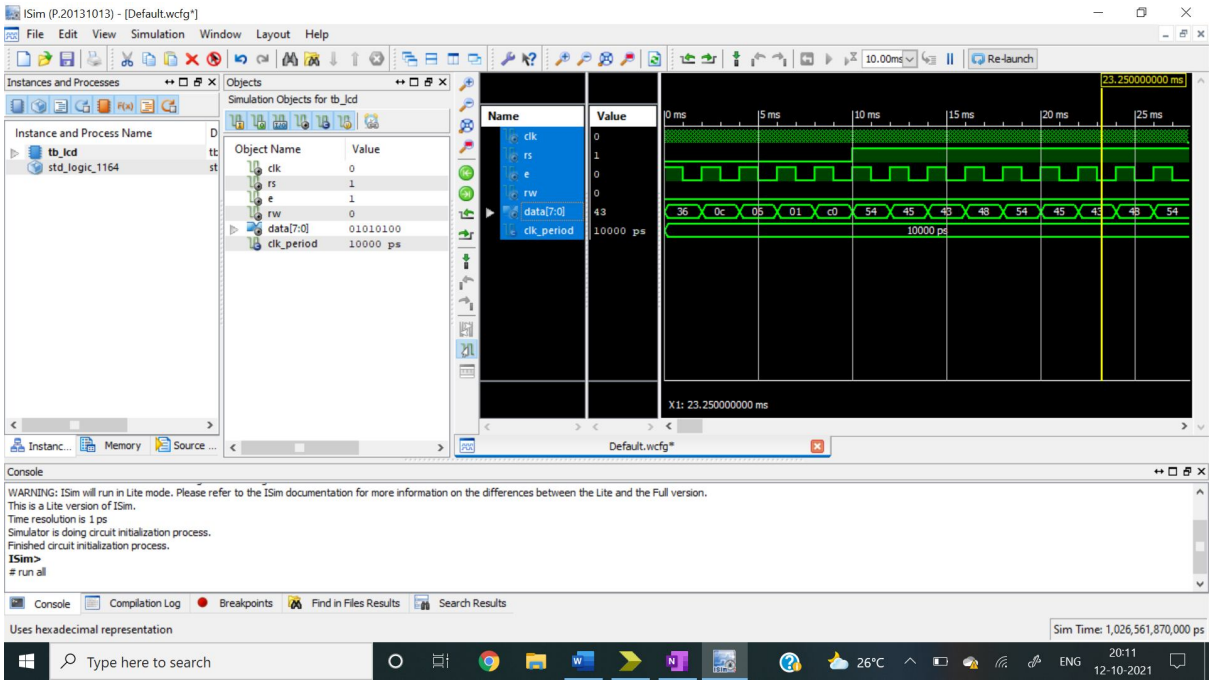
Testbench Program:

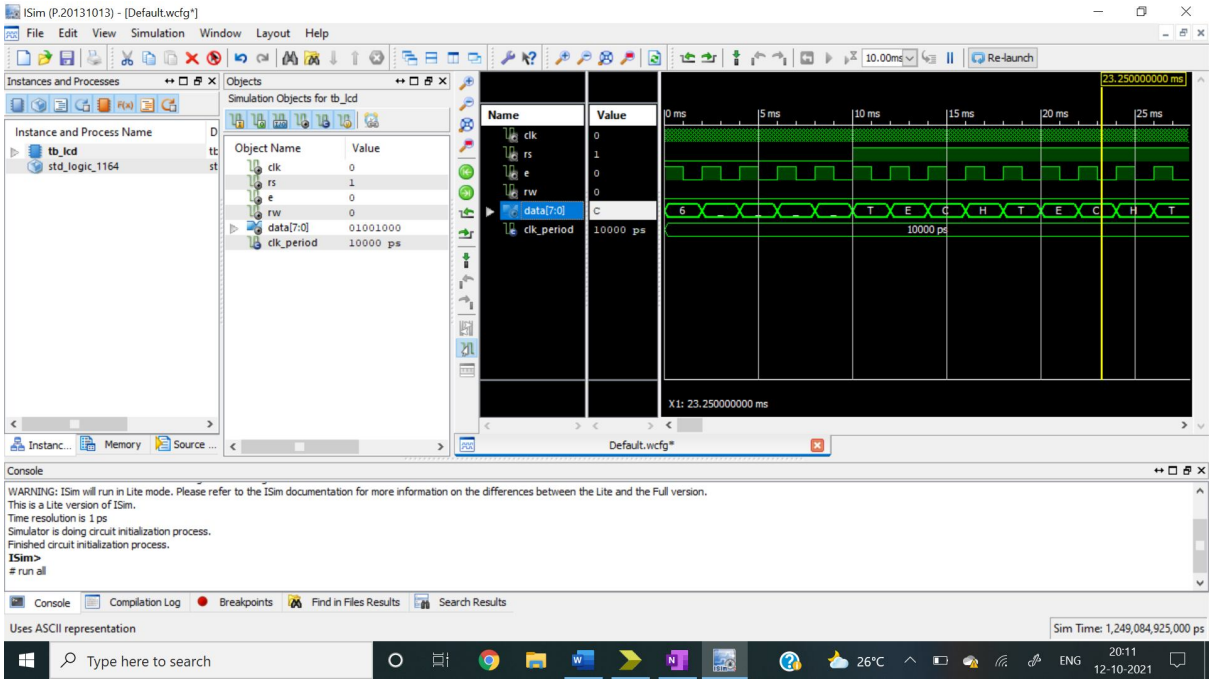
```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;

ENTITY tb_lcd IS
END tb_lcd;

ARCHITECTURE behavior OF tb_lcd IS

  -- Component Declaration for the Unit Under Test (UUT)

  COMPONENT lcdpro
  PORT(
      clk : IN  std_logic;
      rs : OUT  std_logic;
      e : OUT  std_logic;
      rw : OUT  std_logic;
      data : OUT  std_logic_vector(7 downto 0)
     );
  END COMPONENT;
```

```
  --Inputs
  signal clk : std_logic := '0';

          --Outputs
  signal rs : std_logic;
  signal e : std_logic;
  signal rw : std_logic;
  signal data : std_logic_vector(7 downto 0);

  -- Clock period definitions
  constant clk_period : time := 10 ns;

BEGIN

          -- Instantiate the Unit Under Test (UUT)
  uut: lcdpro PORT MAP (
       clk => clk,
       rs => rs,
       e => e,
       rw => rw,
       data => data
      );

  -- Clock process definitions
  clk_process :process
  begin
                    clk <= '0';
                    wait for clk_period/2;
                    clk <= '1';
```

```
                wait for clk_period/2;
  end process;


  -- Stimulus process
  stim_proc: process
  begin
    -- hold reset state for 100 ns.
    wait for 100 ns;

    wait for clk_period*10;

    -- insert stimulus here

    wait;
  end process;

END;
```

Isim Waveforms:





Pin Locking Report:

PlanAhead Generated physical constraints

NET "clk_12Mhz" LOC = P80;

NET "rst" LOC = P204;

NET "lcd_rs" LOC = P48;

NET "lcd_en" LOC = P49;

NET "lcd_data[0]" LOC = P47;

```
NET "lcd_data[1]" LOC = P41;

NET "lcd_data[2]" LOC = P39;

NET "lcd_data[3]" LOC = P35;

NET "lcd_data[4]" LOC = P33;

NET "lcd_data[5]" LOC = P31;

NET "lcd_data[6]" LOC = P29;

NET "lcd_data[7]" LOC = P24;
```

Conclusion:

Thus we have :

1) Modeled a functional simulation of LCD using Behavioral Modeling Style.

2) Observed following Schematics : RTL & Technology Schematics generated Post-Synthesis.

3) Interpreted Device Utilisation Summary in terms of LUTs , SLICES , IOBs , Multiplexers & D FFs used out of the available device resources.

4) Interpreted the TIMING Report in terms of Maximum combinational delay as indicative of the Maximum Operating Frequency .

5) Written a TESTBENCH to verify the functionality of functional simulation of LCD & verified the functionality as per the TRUTH-TABLE ,by observing ISIM Waveforms.

6) Used PlanAhead Editor for pin-locking.

7) Prototyped the FPGA XC3S250EPQ208-5 to realize functional simulation of LCD & verified its operation by giving suitable input combinations