Project 2 Report Team 8

Platform: modelsim on Windows10 64-bit

Members & Team Work

王雋文	1/3	Implement tag comparator and read/write of cache, Revise CPU
林威利	1/3	Implement state change, Revise CPU, Write report
莊明宇	1/3	Add halting signals to pipeline registers, Revise CPU

How do you implement this project and cache controller in detail

Module CPU:

Replace data memory with data cache, adding the input/output of data cache to the input/output of whole CPU module.

Module dcache_top:

Tag comparator and read/write of cache

Compare the tags from the request and from the cached data to set the hit bit. When read hit occurs, check the offset and take the right word out of the block; when write hit occurs, also check the offset and write the word to the correct place of the block.

Controller

STATE_IDLE:

If a request arrives and hit bit is set to 0 (miss), go to STATE_MISS, otherwise stay in STATE_IDLE and wait for next request.

STATE_MISS:

If the dirty bit of corresponding block is set, set the mem_enable, mem_write and write_back bits and go to STATE_WRITEBACK. Otherwise, set the mem_enable bit but not mem_write and write_back bits and go to STATE_READMISS.

STATE_READMISS:

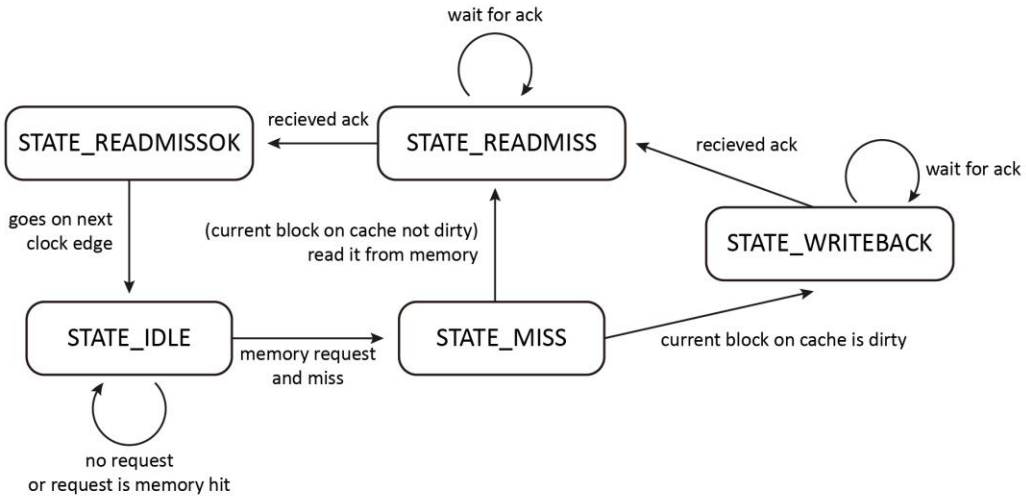
After receiving ack from memory, remove the mem_enable bit and set the cache_we bit and go to STATE_READMISSOK. Otherwise, stay in STATE_READMISS and wait for ack from memory.

STATE_READMISSOK:

Remove the cache_we bit and go back to STATE_IDLE.

STATE_WRITEBACK:

After receiving ack from memory, remove the mem_write and write_back bits and go to STATE_READMISS. Otherwise, stay in STATE_WRITEBACK and wait for ack from memory.



Modules PC, IF/ID, ID/EX, EX/MEM, MEM/WB

If stall signal is received, the pipeline registers, as well as PC, outputs the same values without receiving the new input values.

Problems and Solutions of the Project

Trivial Bugs

Celebrate X’mas and enjoy the festival.