Shiv Nadar University Chennai

End Semester Examinations 2022-2023 Even

Question Paper

Name of the Program: Common to B.Tech. AI & DS., B.Tech. CSE (IoT) and B.Tech. CSE (CS)		Semester: II
Course Code & Name: **CS1004 COMPUTER ORGANIZATION AND ARCHITECTURE**		
Regulation 2021		
Time: 3 Hours	Answer All Questions	Maximum: 100 Marks

Q.No.		Questions	Marks	CO	KL
1	a	Draw the structure of basic processor and memory interconnection.	2	CO1	KL2
2	a	Let us assume a register contains the word "SHIVNADAR". How this word is represented in memory using Big Endian and Little Endian format.	2	CO1	KL3
3	a	Given an n-bit number, write down the range of following number system: a. 1's Complement b. 2's Complement	2	CO2	KL2
4	a	What could be the value of bias to be added to the actual exponent in IEEE 754 single precision representation if a. Exponent=5 b. Exponent=9	2	CO2	KL3
5	a	Consider a system with two levels of cache memory L1 and L2. Write down the worst-case average access time of cache memory if the data required by the CPU is not present in both L1 and L2?	2	CO3	KL2
6	a	A CPU generates a virtual address to access data from the main memory. How is this virtual address translated into physical address?	2	CO3	KL3
7	a	Expand: a. USB b. PCI c. HDMI d. Wi-Fi	2	CO4	KL2
8	a	Define interrupt and list its types.	2	CO4	KL2
9	a	Provide the structure of 5 stage pipelining to execute a set of instruction?	2	CO5	KL2
10	a	How do you overcome the problem of data hazard?	2	CO5	KL3
11	a	Briefly discuss the following addressing modes with example: a. Immediate b. Direct c. Register d. Indirect e. Auto Increment	5	CO1	KL2
12	a	Design a Carry Look ahead adder circuit to add the given two 4-bit numbers. Derive the expression to calculate all carry generated for each stage.	5	CO2	KL3

13	a	Draw the structure of memory hierarchy and compare the performance of memory system with respect to cost, speed, and size.	5	CO3	KL2
14	a	Consider a pipeline having 4 phases with duration 65, 55, 90 and 85ns. Given latch delay is 15 ns. Calculate the following: a. Pipeline cycle execution time b. Non-pipeline execution time c. Speed up ratio	5	CO4	KL3
15	a	Perform floating point addition for the given number 0.512 and 312×10^{-3} and represent the results in IEEE 754 single precision form.	5	CO2	KL3
	b	Write an assembly language program to calculate the given expression. $Y=A*X^2+B*X+C$	5	CO1	KL3
16	a	State the need of virtual memory? How virtual memory is implemented using the hardware component called MMU? How virtual address is translated into physical address using page table?	10	CO3	KL3
17	a	Consider a 2-way set associative mapped cache of size 16 KB with block size 256 bytes. The size of the main memory is 128 KB. Find Number of bits in tag?	5	CO3	KL3
	b	Let the main memory access time be 1200ns and cache access time be 100ns. The average memory access time does not exceed 120ns. Calculate the hit ratio?	5	CO3	KL3
18	a	Discuss the mechanism used to transfer date between main memory and the IO devices without the involvement of CPU during data transfer?	10	CO5	KL2
19	a	Define hazard. What are the hazards that may occur during instruction execution? Describe the techniques for handling data and control hazards in pipelining?	10	CO4	KL2
20	a	Define Superscalar processor. Illustrate how multiple instructions are issued to the pipelining execution using such processor?	10	CO4	KL2

KL – Bloom's Taxonomy Levels
(KL1: Remembering, KL2: Understanding, KL3: Applying, KL4: Analyzing, KL5: Evaluating, KL6: Creating)
CO – Course Outcomes
