Shiv Nadar University Chennai

End Semester Examinations 2023-2024 Even

Question Paper

Name of the Program: Common to B.Tech. AI & DS, B.Tech. CSE (IoT), B.Tech. CSE (CS)		Semester: II
Course Code & Name: CS1004 COMPUTER ORGANIZATION AND ARCHITECTURE		
Regulation 2021		
Time: 3 Hours	Answer All Questions	Maximum:100 Marks

Questions		Marks	CO	KL
1	a. Draw the memory hierarchy model used in modern computers. Name the memory technology used at each level of the hierarchy.? b. Which mapping is usually preferred for L1 cache. Explain the reason for the same.? c. Explain with an example on how the following replacement mechanism works in a 4-line cache: i) Least Recently Used, and ii) Least Frequently Used. Which one is more optimal.? Support your choice with a maximum of three to four sentences.	15 (4 + 3 + 8)	CO3	KL4
2	a. Explain how the memory management unit is implemented in address translation.? b. Consider a computer system with a 2-level cache hierarchy. The L1 cache has a hit rate of 85%, and the access time is 1 ns. The L2 cache has a hit rate of 70%, and the access time is 5 ns. If the miss penalty to access main memory is 100 ns, what is the average memory access time (AMAT) for this system? (Note: miss penalty here includes main memory access time as well) c. You are designing a 4-way set associative cache for a computer system. The cache has a total capacity of 16 KB, and each cache line is 32 bytes long. The system also has main memory with a capacity of 256 KB which is byte addressable. Calculate the following: i. The number of sets in the cache and the number of bits needed for set-index. ii. The number of bits needed for the tag and byte-offset. iii. The total physical address size.	15 (6 + 4 + 5)	CO3	KL3
3	a. Given two numbers 11010 and 00111. Multiply them using booths algorithms by demonstrating all the steps. Draw the basic hardware structure for implementing the booths algorithm. b. P1, P2, P3, ….., P8 are the partial products obtained in multiplying two 8-bit numbers. Show how these can be reduced using carry-save adder (CSA) tree. Give the equation for computing the CSA tree depth in n-bit multiplication. c. Represent the smallest and the largest number in IEEE 754 single precision system.	15 (6 + 7 + 2)	CO2	KL4
4	a) What is called as overflow condition in 2's complement Arithmetic.? How do you differentiate between a carry and overflow in 2's complement arithmetic. b) Two processors A and B have clock frequencies of 700 MHz and 900 MHz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster and justify. c) Explain the purpose of the following in a processor: i) Stack Pointer, ii) Program Counter, and iii) Accumulator. d) Assuming 3-bit number system, represent all possible positive and negative binary numbers along with their decimal equivalents using the following methods: i. Signed Magnitude ii. 1's Complement iii. 2's Complement Also, mention the major disadvantage (if any) in each of the above systems.	15 (3 + 4+ 3 + 5)	CO1	KL3

5	a) How does data transfer occur between the main memory and I/O devices without requiring the CPU's direct participation during the process? Give explanation with suitable diagram. b) Explain different modes of operation in a DMA controller.	15 (10 + 5)	CO4	KL2
6	Consider a pipelined processor with a four-stage pipeline (Instruction Fetch, Instruction Decode, Execute, Write Back) and no forwarding mechanism. The following code snippet is from a program running on this processor: 1. ADD R3, R1, R2 2. MUL R6, R1, R4 3. AND R5, R3, R4 4. AND R6, R1, R2 5. OR R1, R3, R6 6. SUB R4, R1, R6 7. ADD R2, R4, R3 8. SUB R3, R5, R6 a) Identify all possible RAW, WAR, and WAW hazards present in the code snippet. (Clue: In the instruction ADD R3, R1, R2, the contents of R1 and R2 gets added and the result is stored in R3). b) Discuss the impact of these hazards on the pipeline and propose potential solutions to mitigate their effects, considering the absence of a forwarding mechanism in the pipelined processor. c) Calculate the number of clock cycles it would take to execute the code snippet if there were no hazards and the processor's clock cycle time was 1 ns.	15 (6 + 6 + 3)	CO5	KL5
7	a) How does a superscalar processor execute multiple instructions at a time? b) A non-pipelined single cycle processor operating at 100 MHz is converted into a synchronous pipelined processor with five stages requiring 2.5 ns, 1.5 ns, 2 ns, 1.5 ns, 1.5 ns, and 2.5 ns respectively. The delay of the latches is 0.5 ns. Find the speedup of the pipeline processor for 1000 instructions.	5 (2 + 3)	CO5	KL3
8	Draw and explain how the peripherals are interfaced with the processor via an I/O bus. What is the function of a PCI?	5	CO4	KL2

KL – Bloom's Taxonomy Levels
(KL1: Remembering, KL2: Understanding, KL3: Applying, KL4: Analyzing, KL5: Evaluating, KL6: Creating)
CO – Course Outcomes
