CS2610: Computer Organization and Architecture Lab

January-May 2023 Semester

Verilog Programming Assignment 8

Date: 10th April, 2023

Structural description method is to be used.

1. Design ALU that includes the following circuits:
    a. 8-bit integer adder/subtractor
    b. 8-bit unsigned integer multiplier
    c. 8-bit signed integer multiplier
    d. 12-bit floating-point adder
    e. 12-bit floating-point multiplier
    f. 8-bit comparator with output of zero for the same input operands

The ALU takes a 3-bit opcode and 2 operands as input, and produces the result of the operation specified by the opcode on the two input operands. The opcodes and the corresponding operations are as follows:

Opcode	Operation
000	No operation
001	8-bit integer addition
010	8-bit integer subtraction
011	8-bit unsigned integer multiplication
100	8-bit signed integer multiplication
101	12-bit floating-point addition
110	12-bit floating-point multiplication
111	8-bit comparison

2. Design the input and output interface for ALU. Each of the two input operands of the ALU needs to be sent as input to the arithmetic circuit specified by the opcode. The output of an arithmetic circuit specified by the opcode needs to be given as the output of the ALU.

3. Design a 12-bit register file that contains 8 registers, two read ports and one write port. Positive-edge triggered D flip-flops are to be used to build a register.

4. Execute each of the instructions given below independently, using the ALU and Register File. The contents of the source operand registers need to be read from the Register file and given as input to the arithmetic circuit specified by the opcode. The output from the arithmetic circuit specified by the code needs to be written into the destination operand register.

ADD R2, R0, R1

SUB R3, R0, R1

MUL R4, R0, R1

IMUL R4, R0, R1

FADD R7, R5, R6

FMUL R7, R5, R6

CMP R2, R0, R1