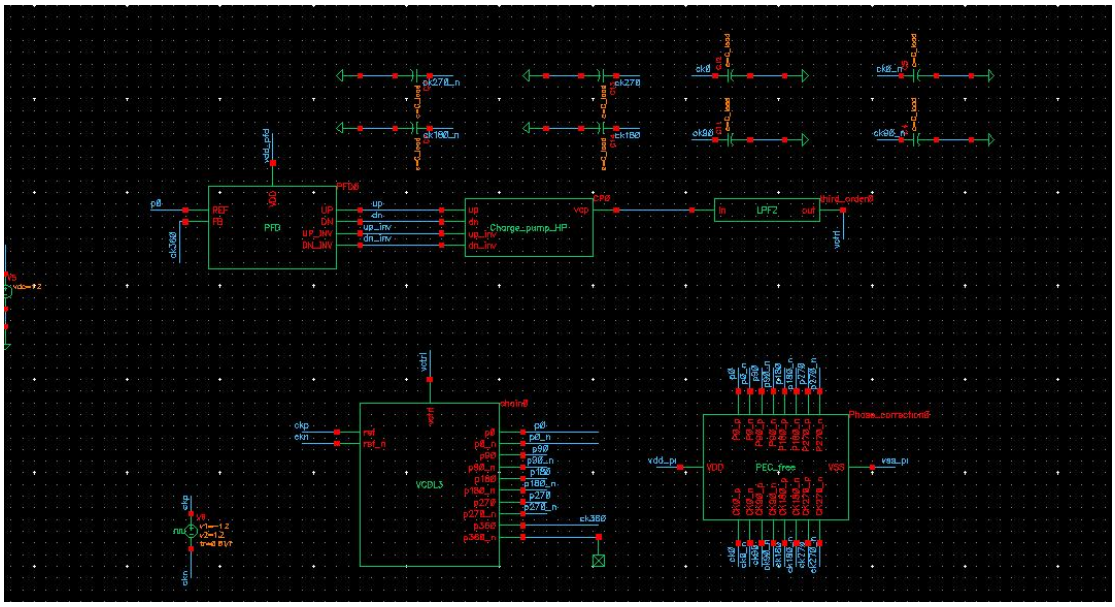
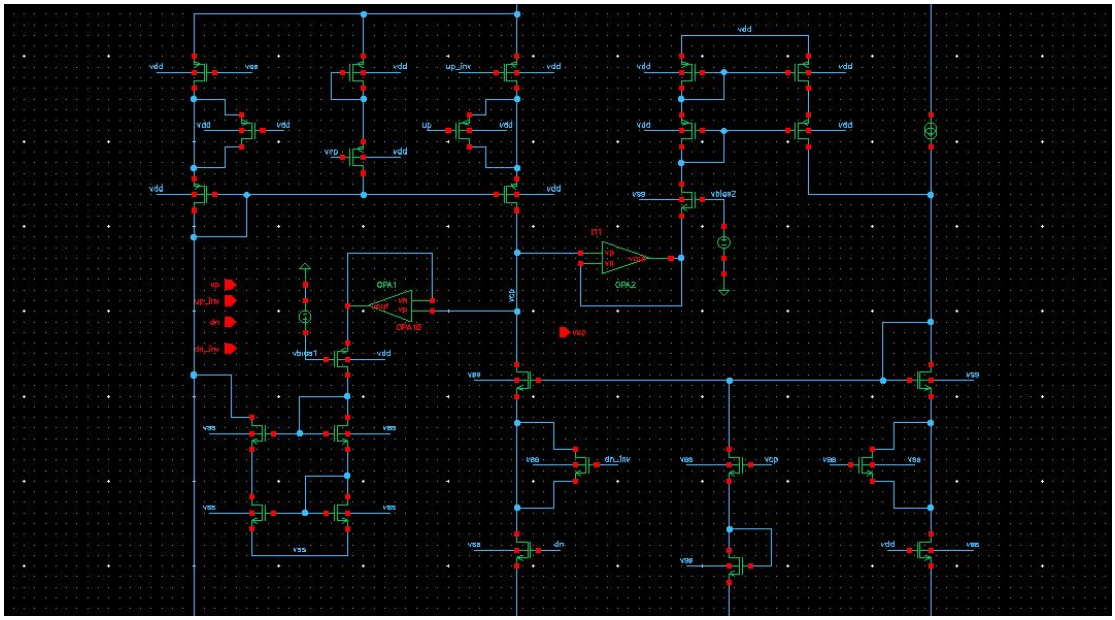
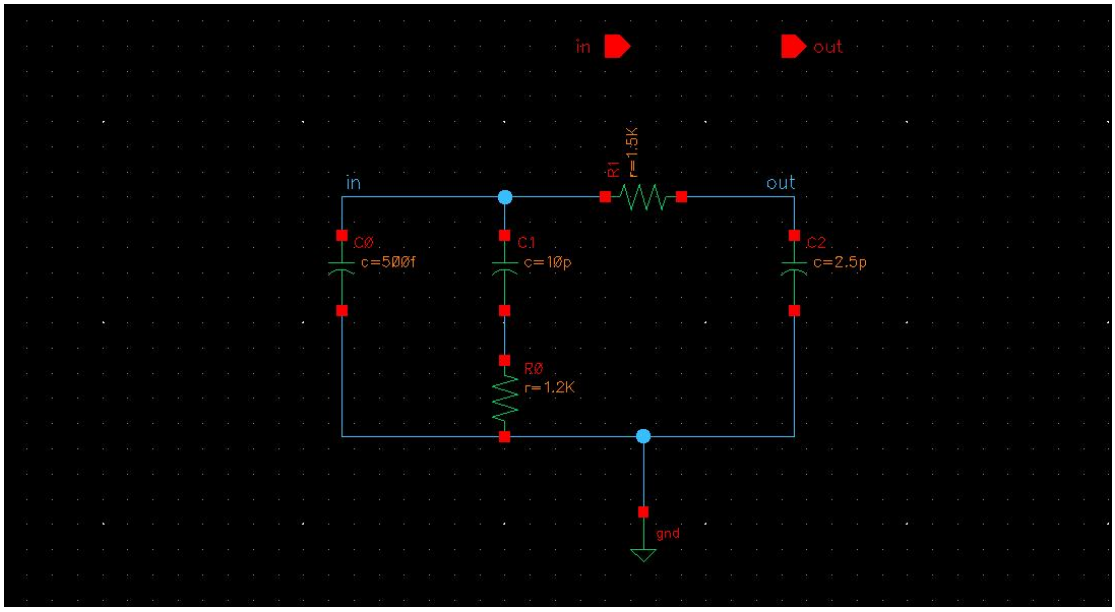
Quadrature clock generator -Brief work done report:



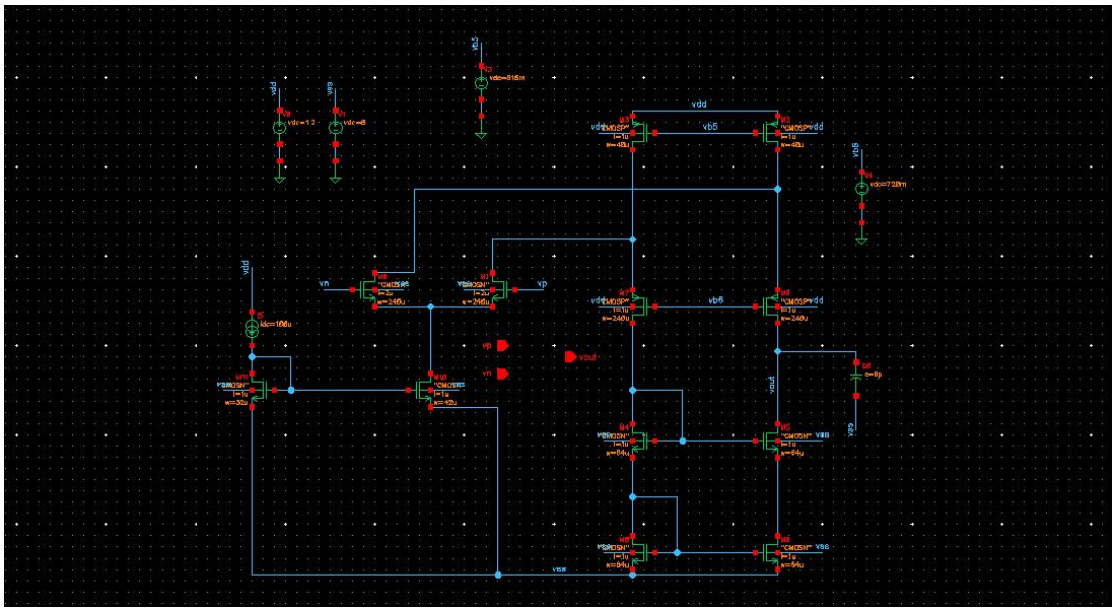
DLL architecture



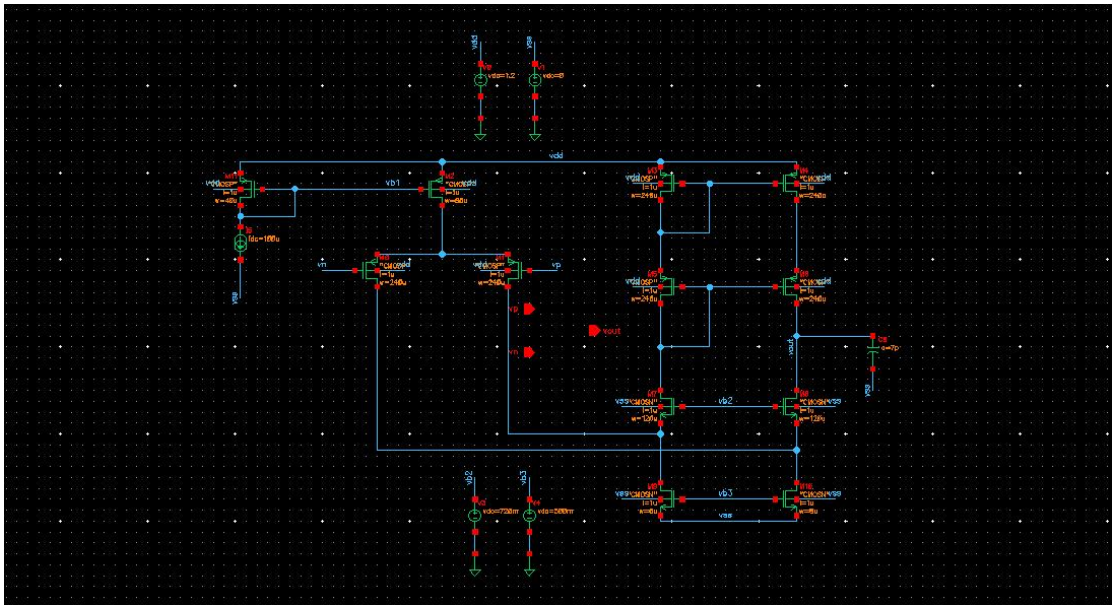
Charge pump with current mismatch detection circuit



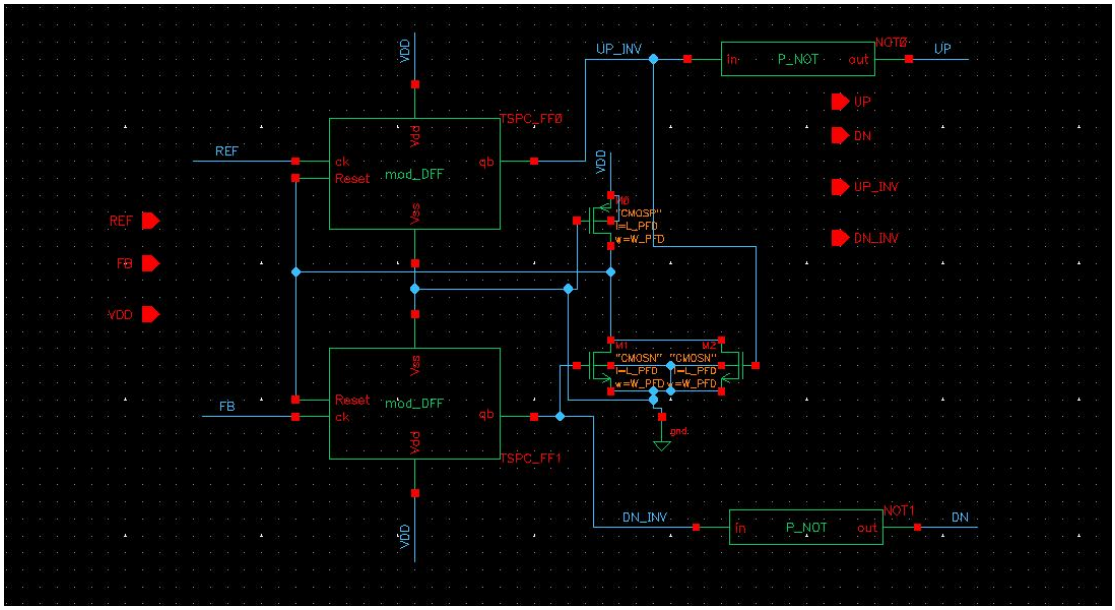
Third order loop filter



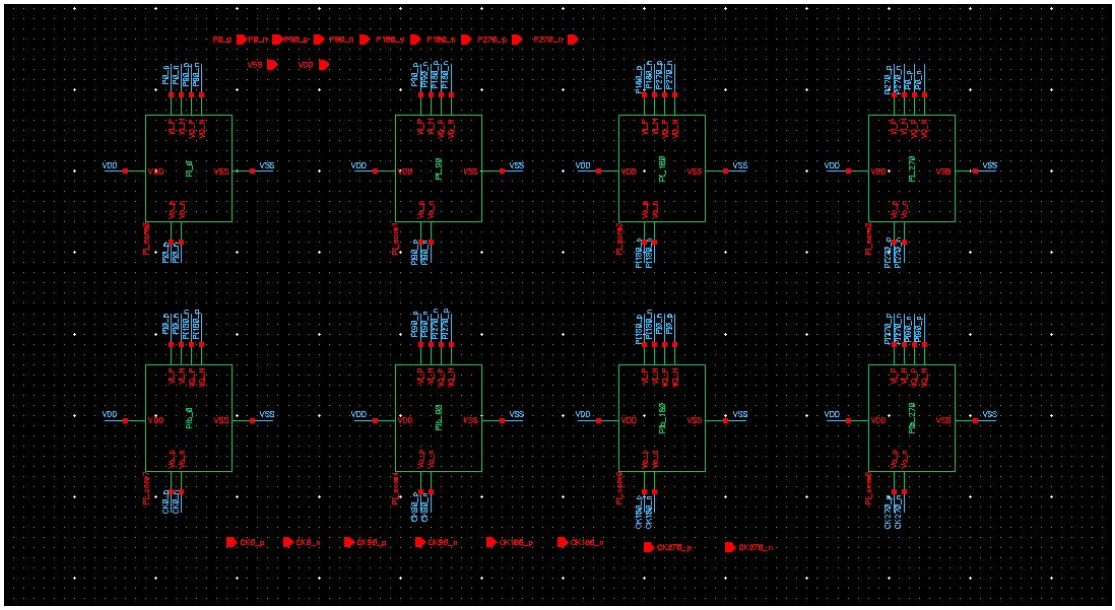
Folded cascode op-amp1 used in CMDC



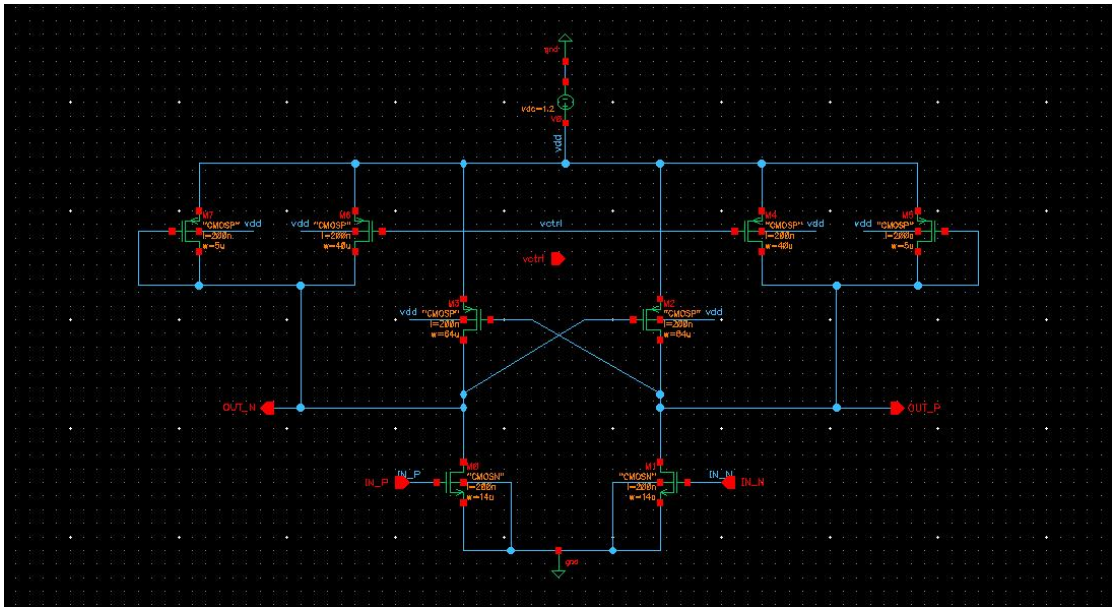
Folded cascode op-amp2 used in CMDC



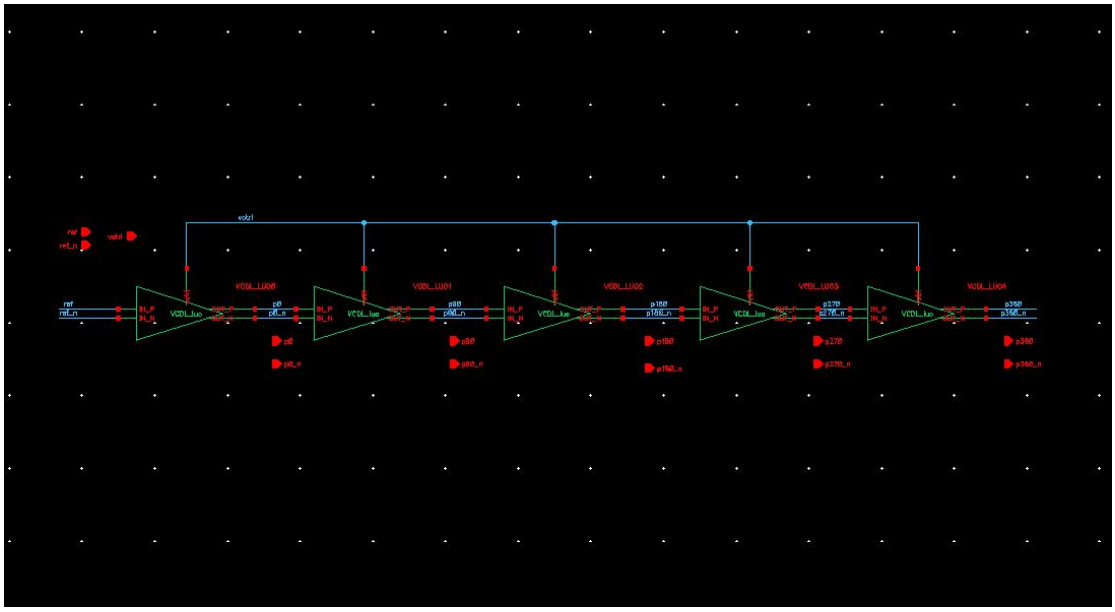
PFD circuit



Simple differential buffer based analog PI connected in zig-zag architecture

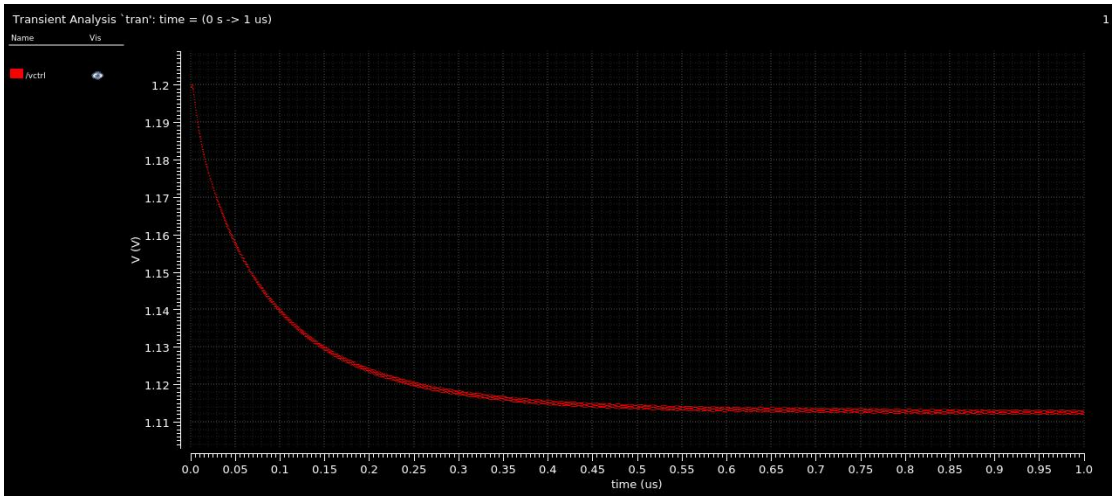


Single voltage-controlled delay line cell

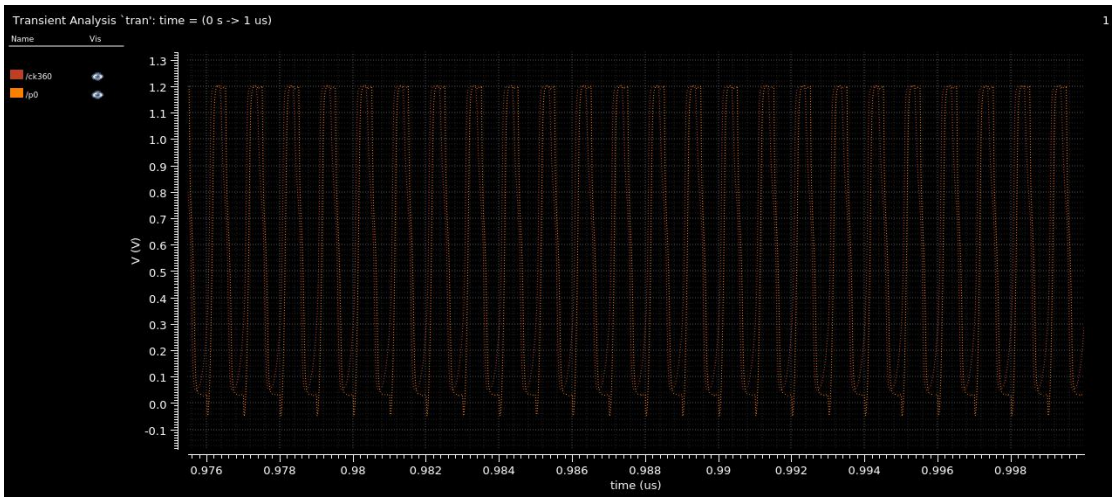


VCDL chain of five

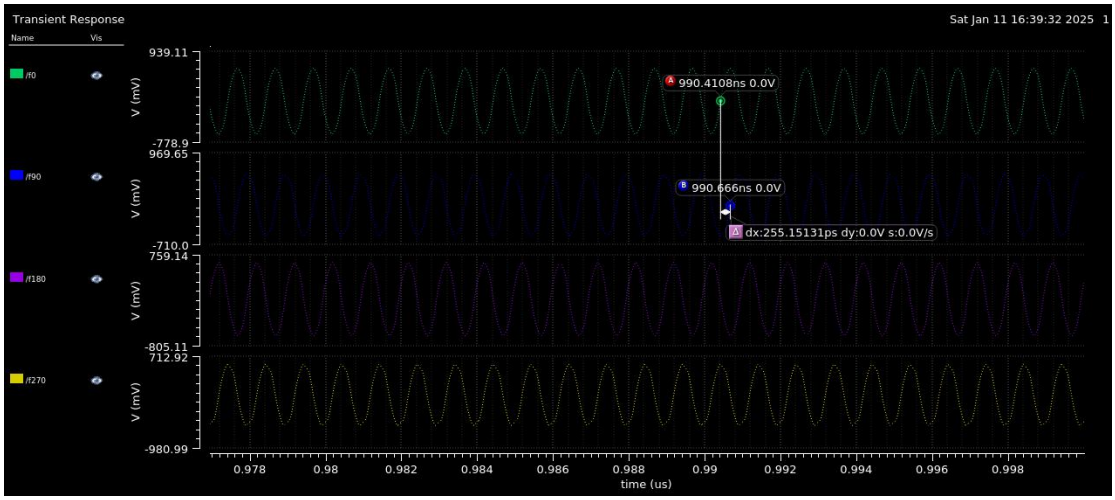
Performance evaluation:



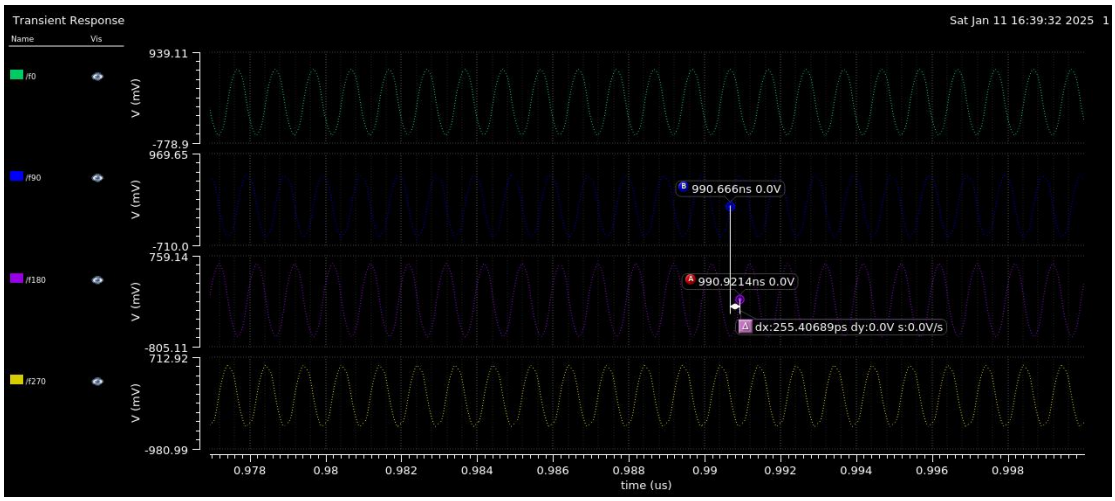
Control voltage showing locking of DLL at ~0.5 ms



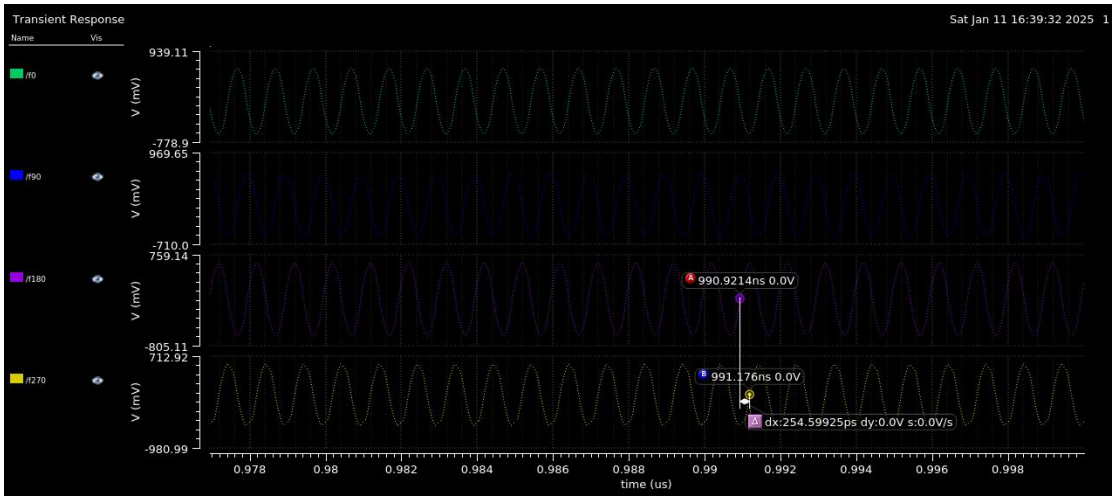
Phase 0, Phase 360 used as reference and feedback signals in locked condition.



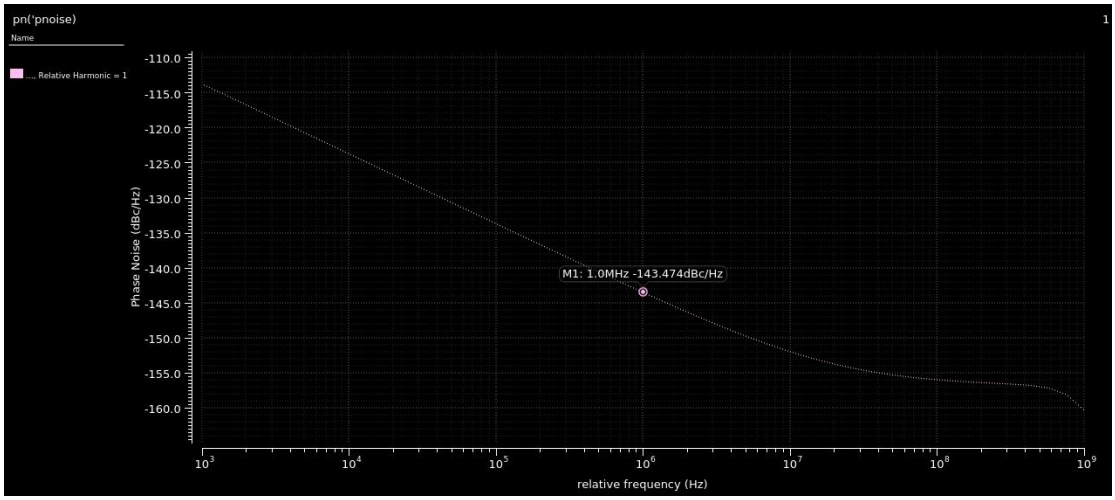
Phase difference of **91.8º** achieved between ck0 and ck90



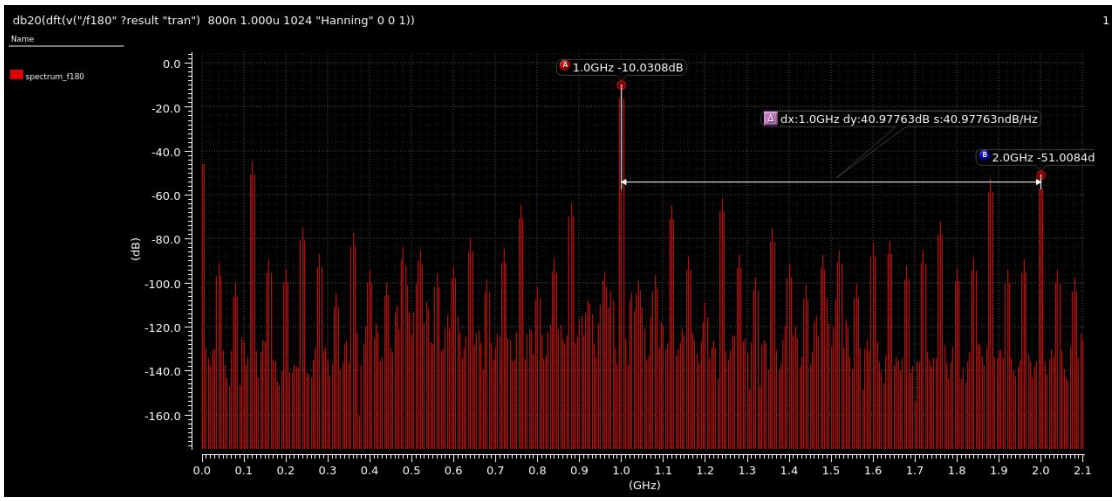
Phase difference of **91.8º** achieved between ck90 and ck180



Phase difference of **91.6º** achieved between ck180 and ck270

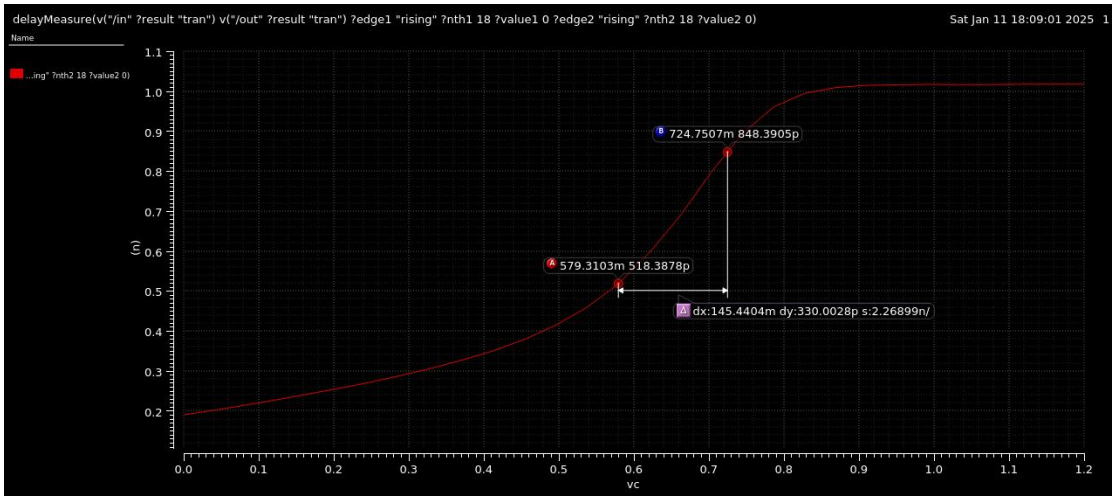


Phase Noise of **144dBc/Hz** achieved at 1MHz offset

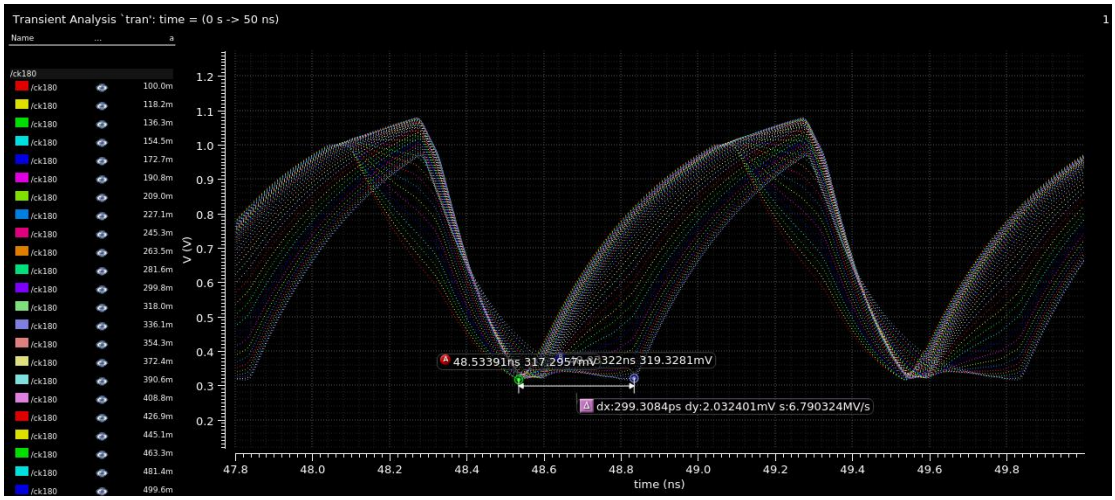


Spurs of -41 dBc achieved

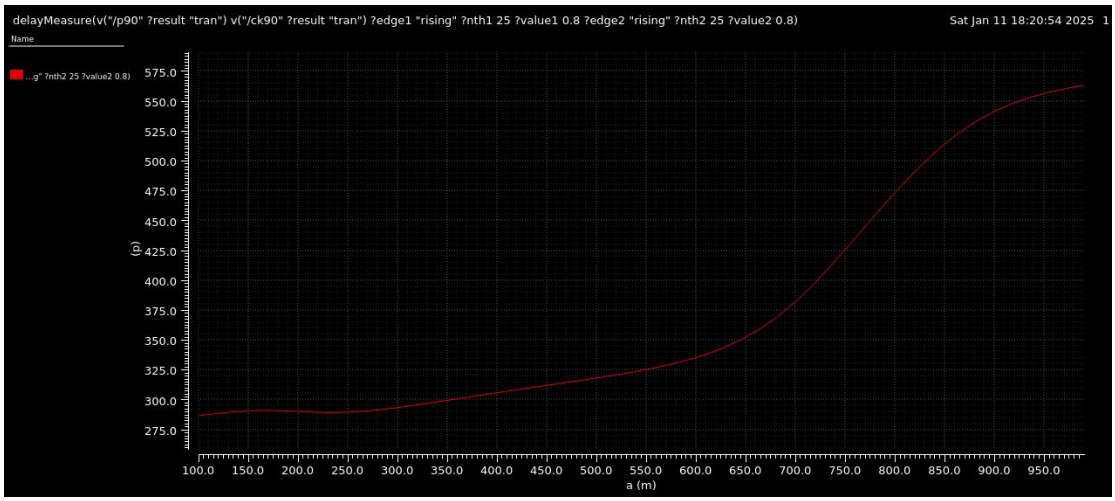
Performance evaluation of sub-blocks:



VCDL delay vs. Control voltage



Interpolation done by PI from a=0.1 to 0.99



PI phase vs weight curve