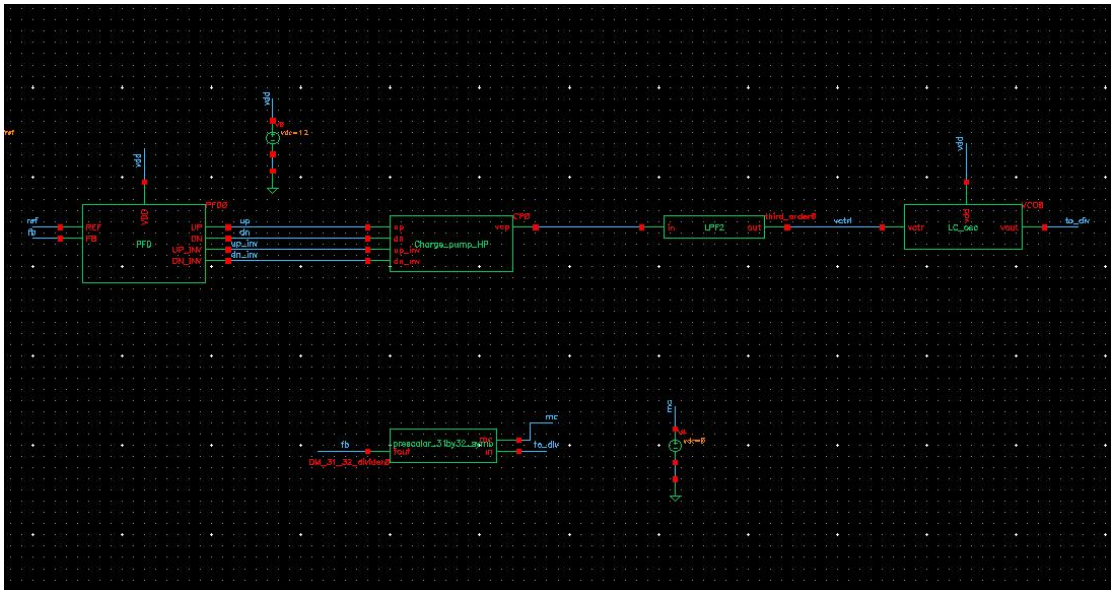
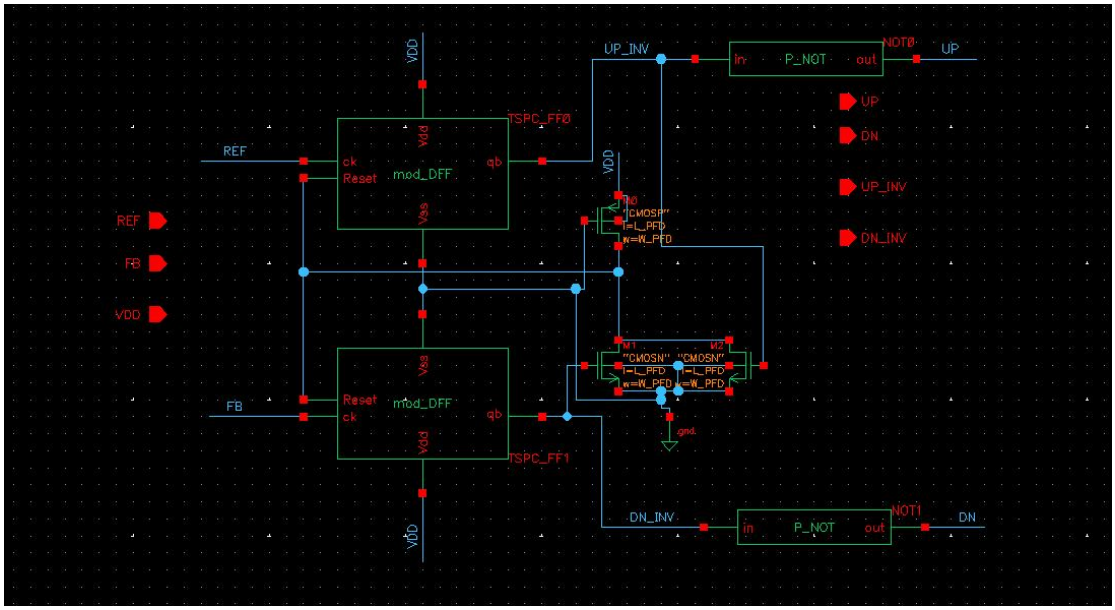
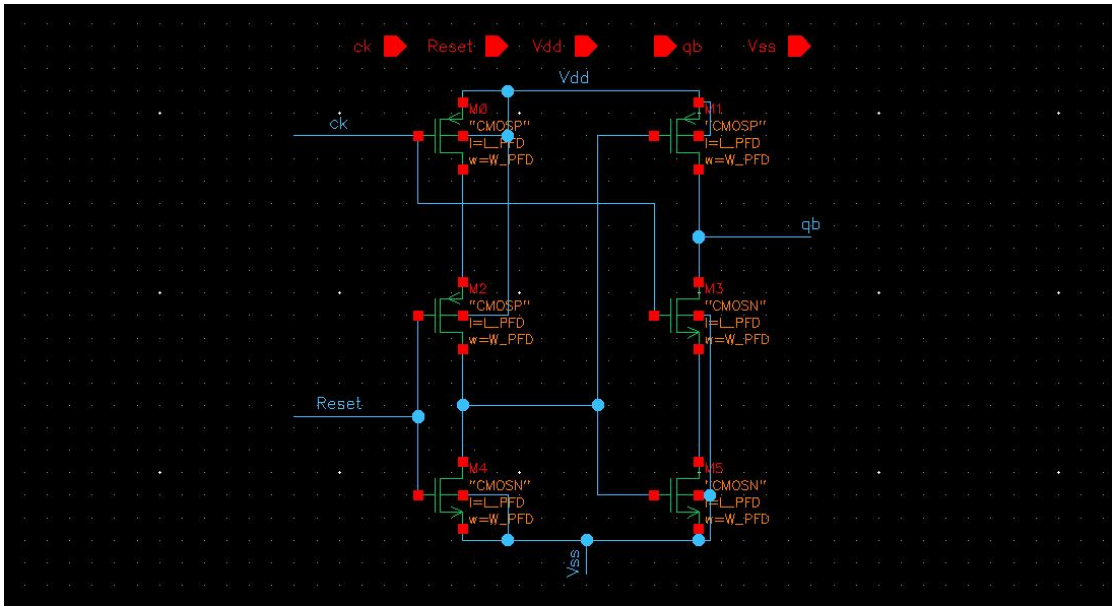
3.2 GHz PLL - Brief work done report



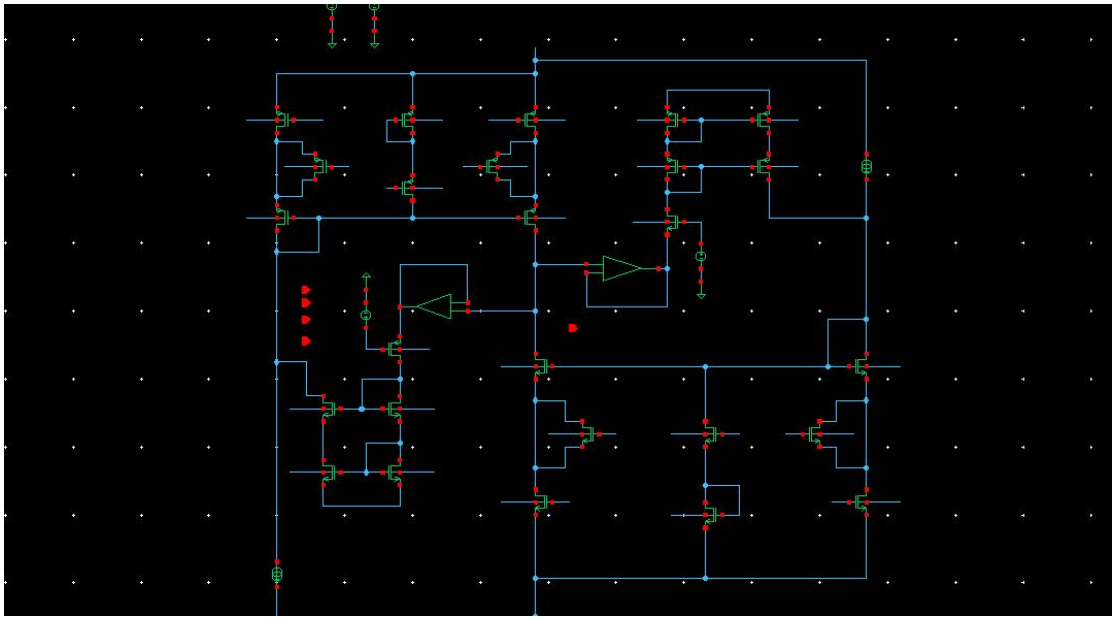
Architecture of PLL



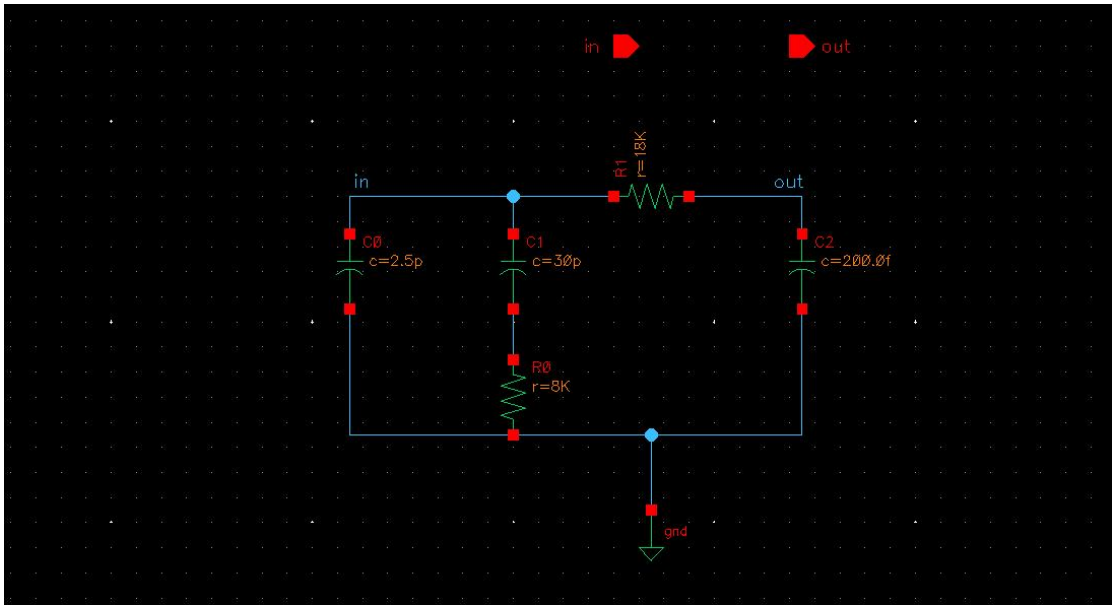
PFD



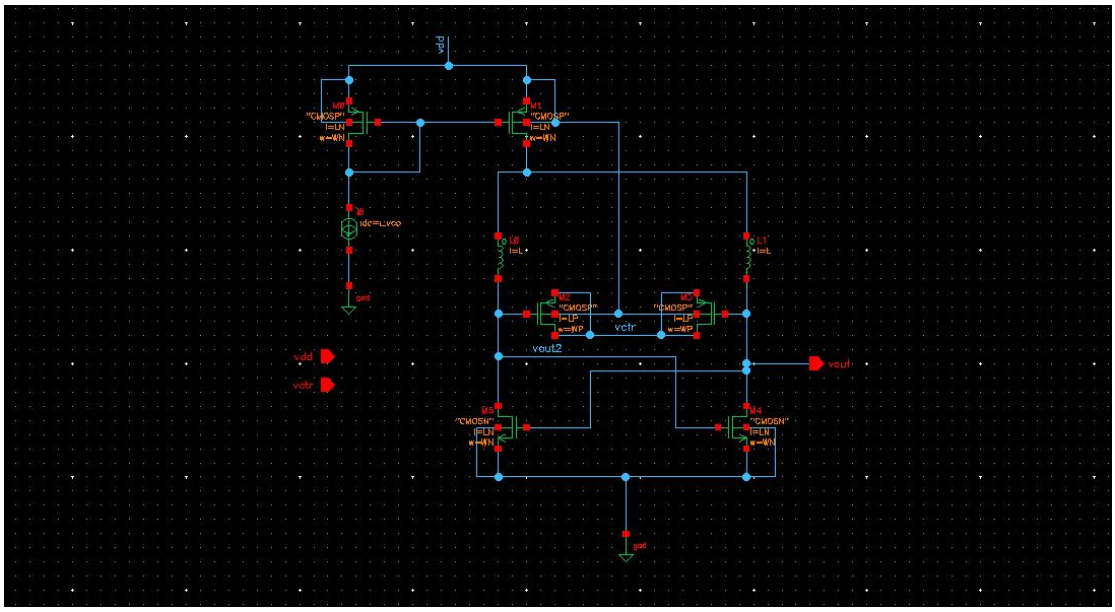
Modified D Flip-Flop



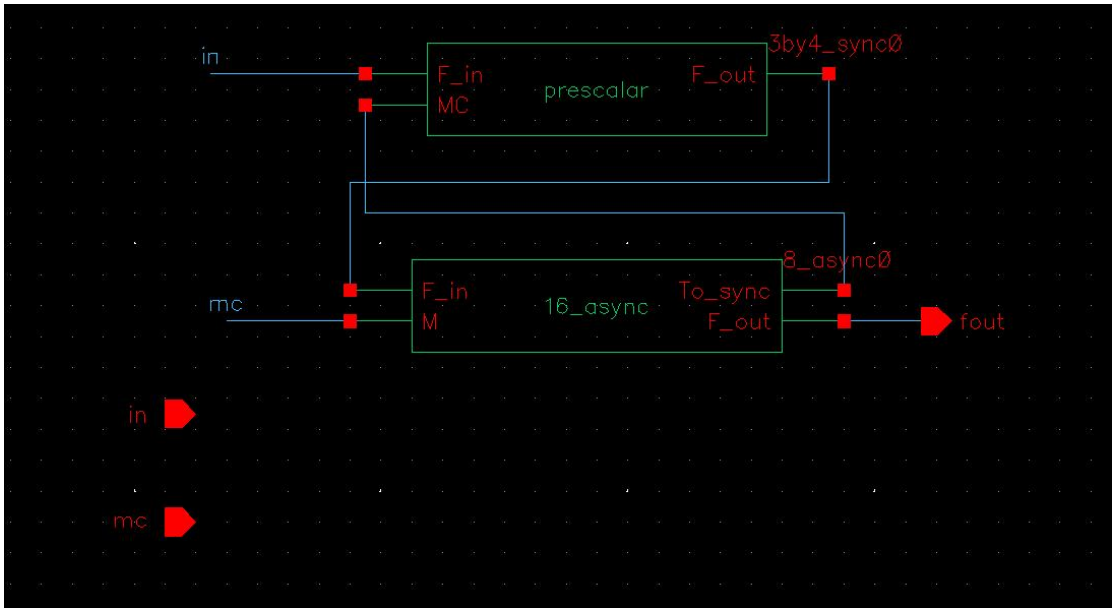
Charge pump



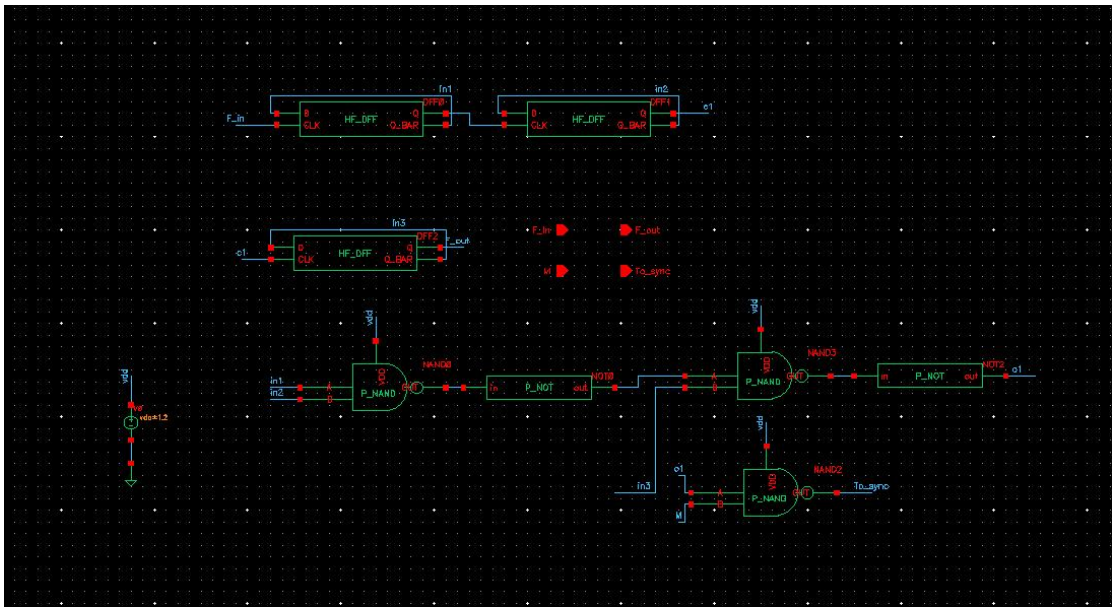
Third-order loop filter



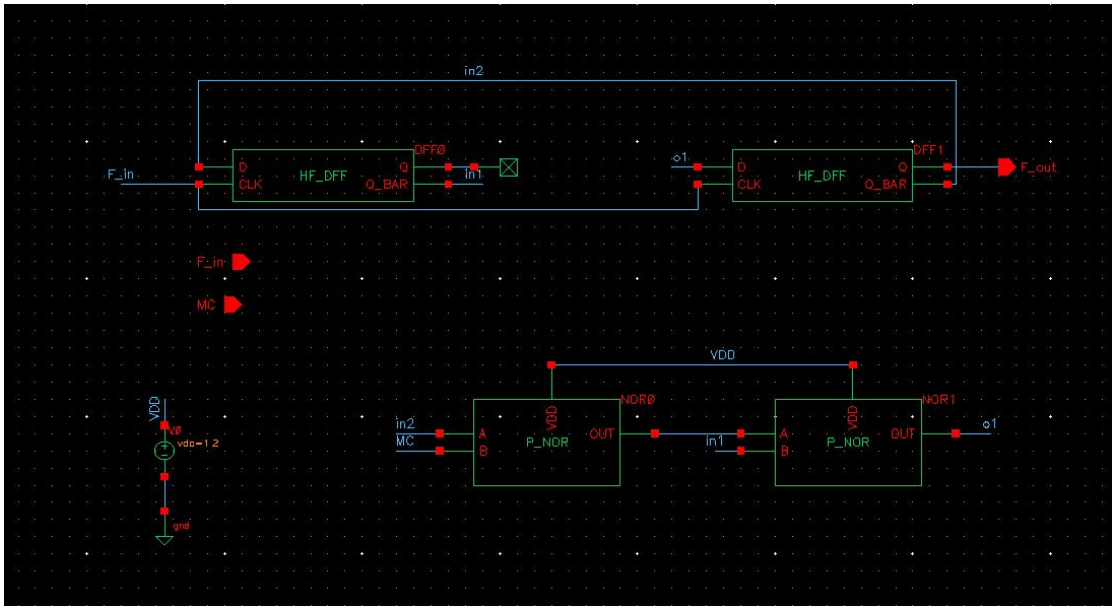
Voltage Controlled Oscillator



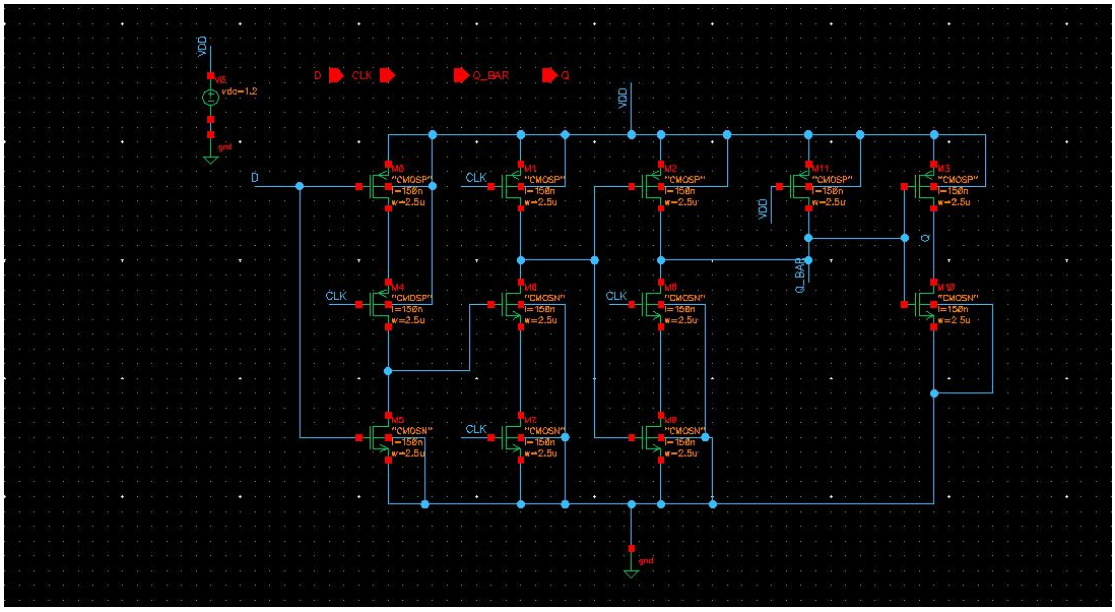
32/31 divider



Divide by 8 asynchronous block

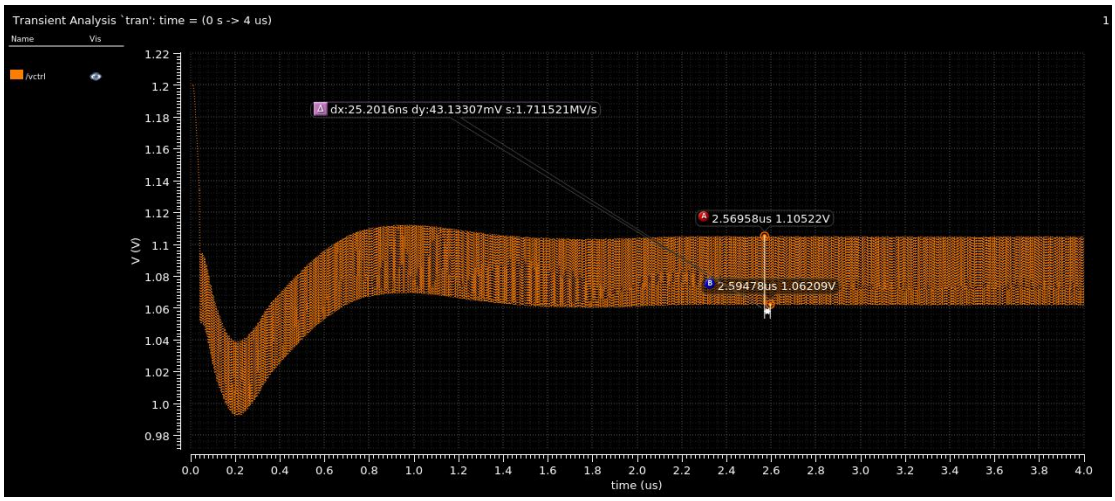


Divide by 3 or 4 synchronous block

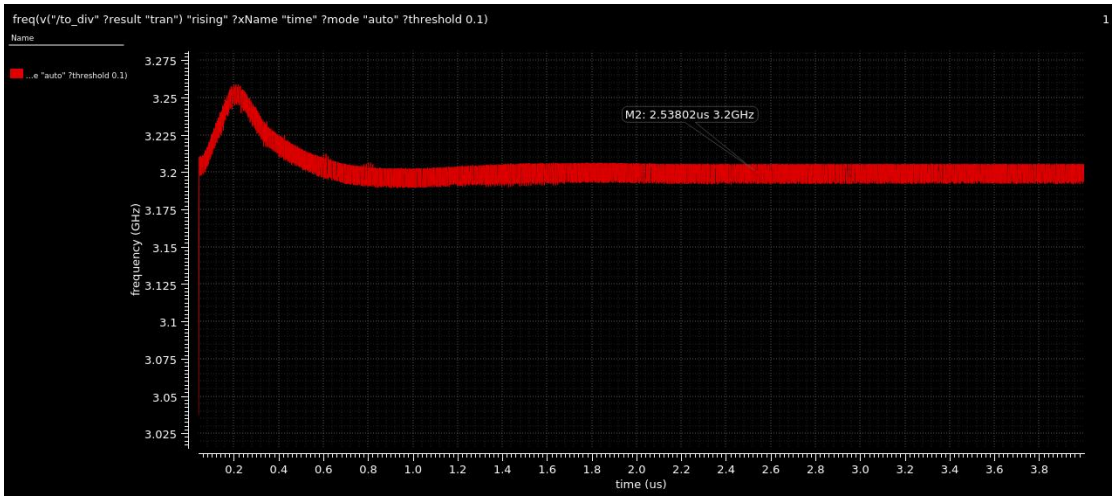


True Single-Phase Clock(TSPC) D Flip-Flop

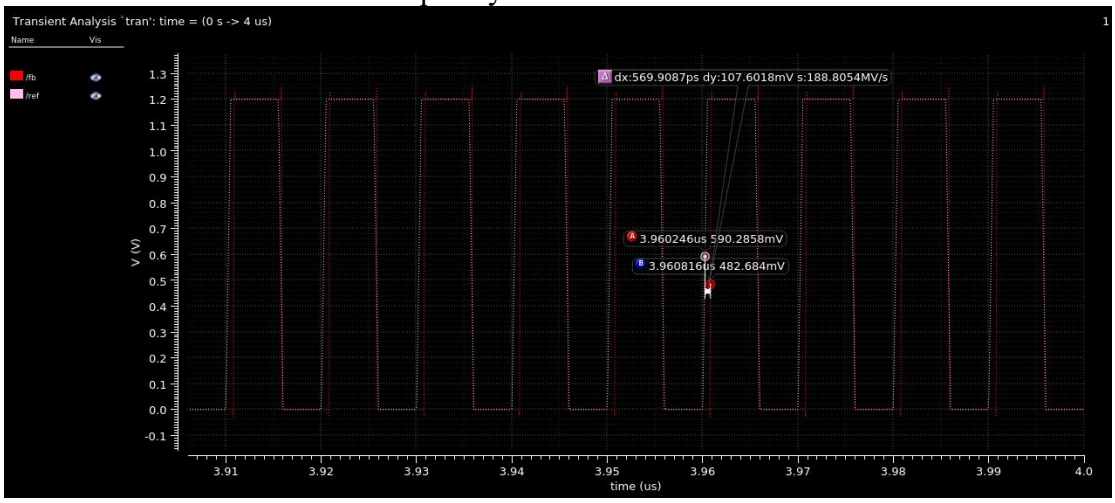
Performance:



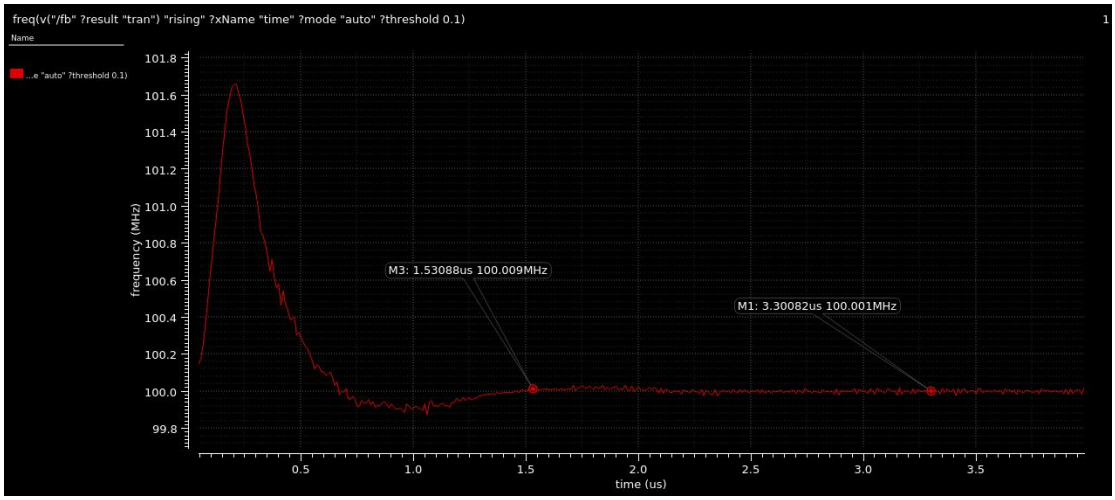
Control voltage in locked condition



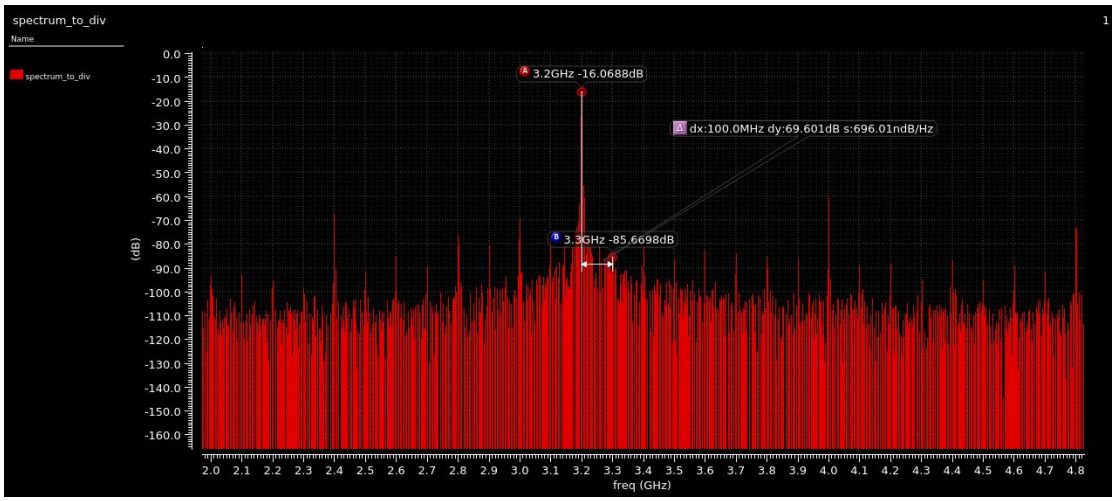
Frequency locked to 3.2 GHz



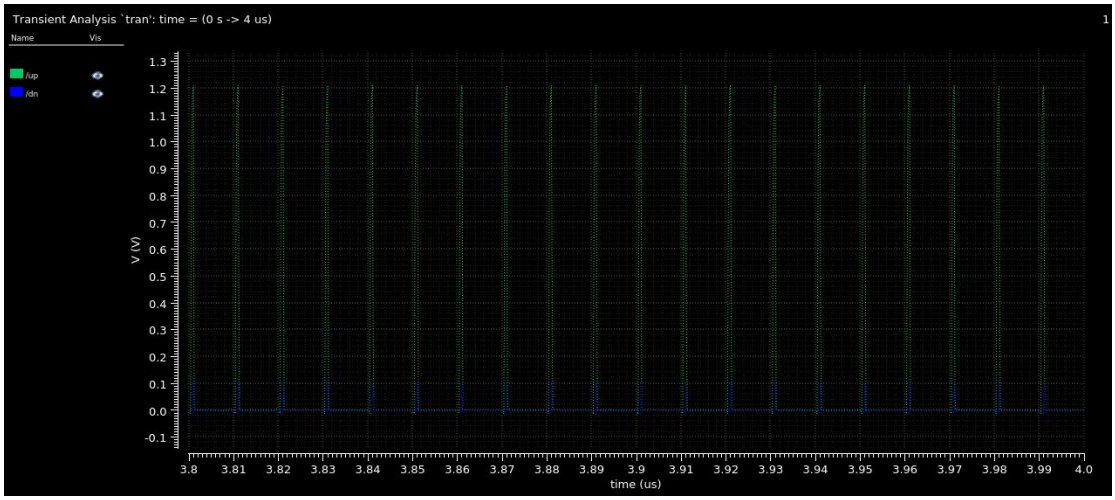
A phase offset of **0º** achieved at PLL lock point



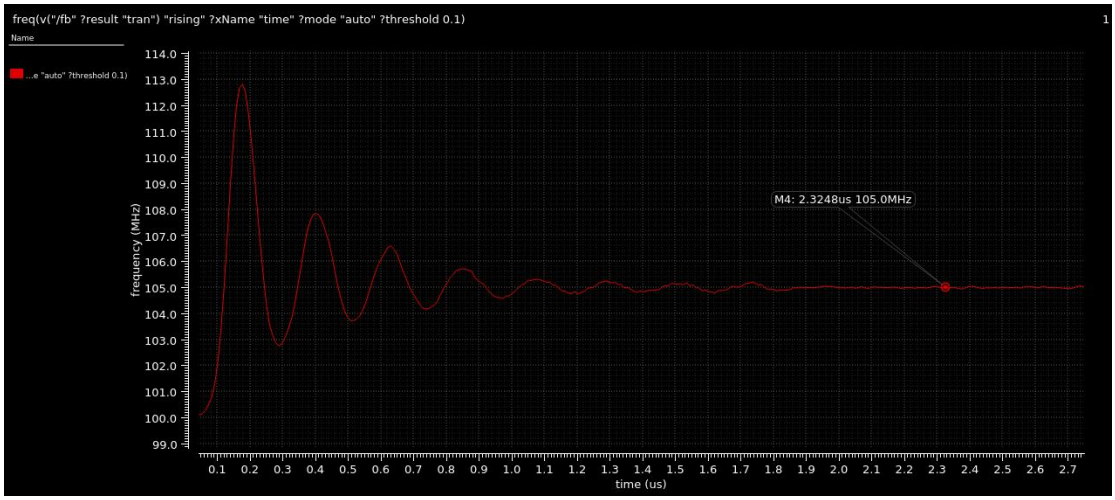
Feedback frequency settling to 100 MHz reference frequency during locked condition



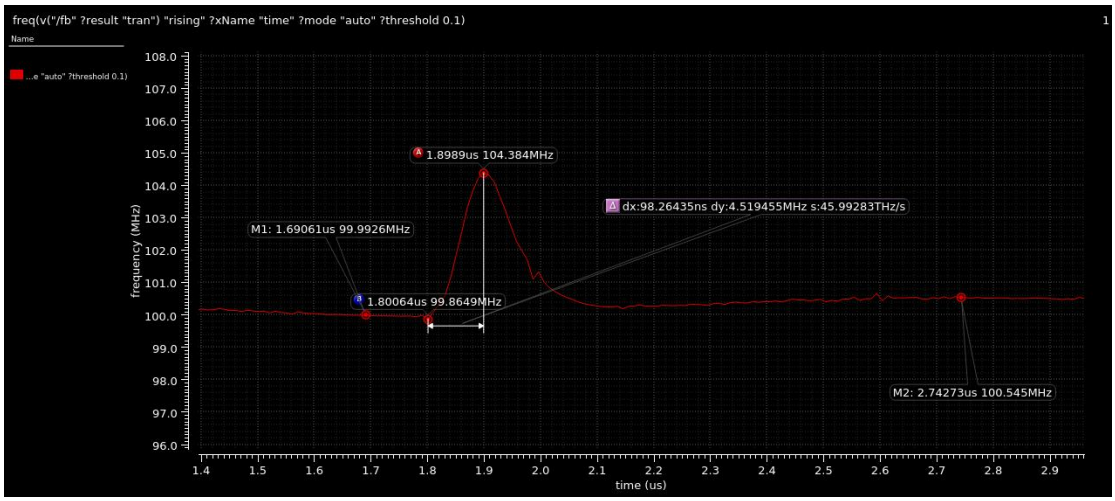
Reference spurs of **-69.6 dBc** achieved



UP and DOWN signal during locked condition

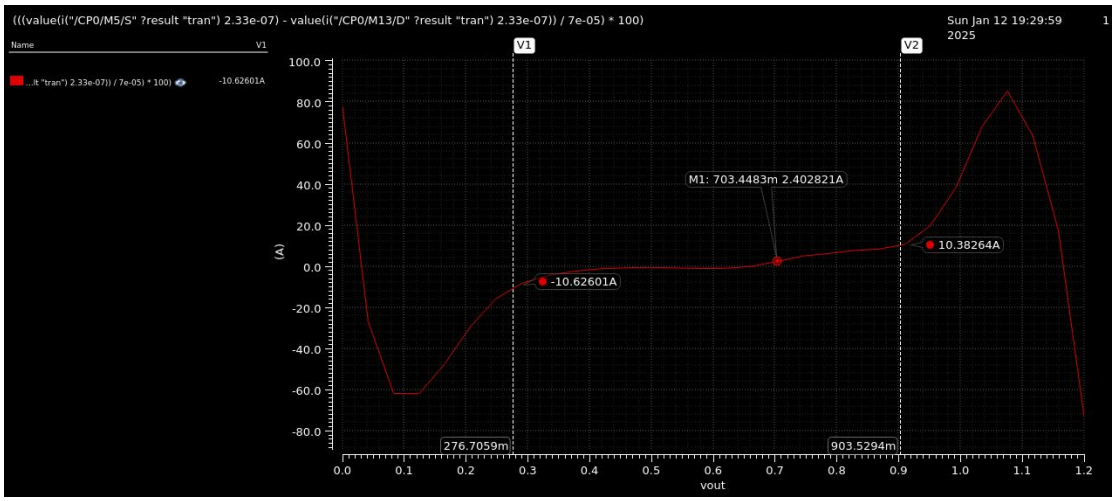


PLL locking to 105 MHz reference clock showing 5% tuning range

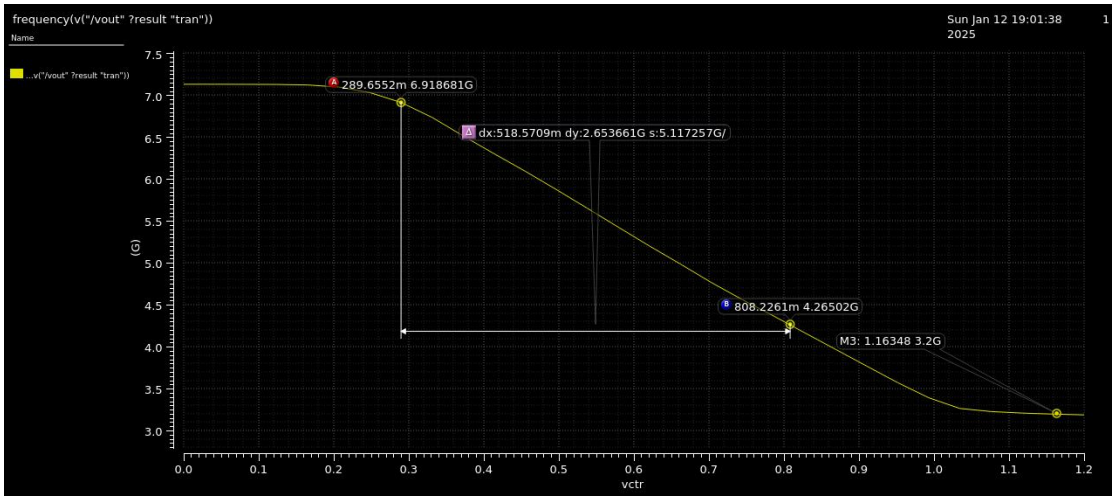


PLL's 0.5MHz step response; Phase margin=66.2º; Damping ratio=0.7206; Peak overshoot=3.82% ; Settling time=0.12us; Loop Bandwidth= 10.47 MHz

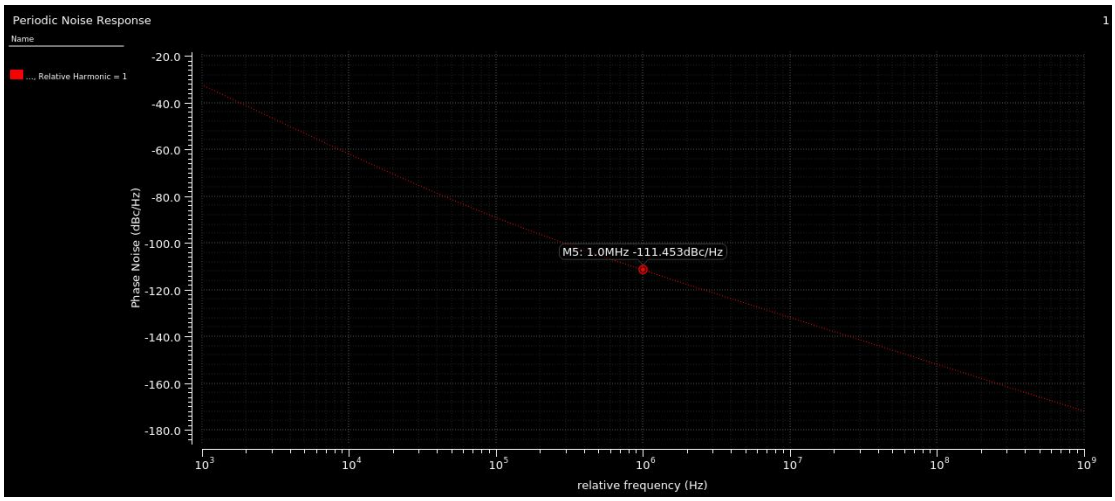
Performance of sub-blocks:



Charge pump achieving current mismatch of ~10% from 0.25 V to 0.9V



KVCO of 5 GHz/V



Phase noise of **-111.45 dBc/Hz** achieved at 1MHz offset