VISVESVARAYA TECHNOLOGICAL UNIVERSITY

Jnanasangama, Macche, Santibastwada Road
Belagavi-590018, Karnataka

A
UG PROJECT REPORT
on

Design of FinFET based Combinational and Sequential circuits.

Submitted in partial fulfillment of the requirement for the degree of

Bachelor of Engineering
in
Electronics & Communications Engineering - ECE
by

USN: 1DS19EC708	**Bhanu Prasad Nayak**
USN: 1DS19EC710	**Chinnappa Reddy Gari Indu**
USN: 1DS19EC742	**T Sai Gautham**
USN: 1DS20EC425	**Pavan M**

Under the guidance
of
Dr. Dinesha P
Professor, Dept. Of ECE
DSCE, Bengaluru-78

DAYANANDA SAGAR COLLEGE OF ENGINEERING
Department of Electronics & Communication Engineering
(An Autonomous College affiliated to VTU Belgaum, accredited by NBA & NAAC, Ranked by NIRF)
Shavige Malleshwara Hills, Kumaraswamy Layout,
Bengaluru-560078, Karnataka, India

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Certificate

Certified that the project work entitled, ***"Design of FinFET based Combinational and Sequential circuits"*** carried out by **Bhanu Prasad Nayak** (1DS19EC708), **Chinnappa Reddy Gari Indu** (1DS19EC710), **T Sai Gautham** (1DS19EC742), **Pavan M** (1DS20EC425) are bonafide students of the ECE Dept. of Dayananda Sagar College of Engineering, Bangalore, Karnataka, India in partial fulfillment for the award of Bachelor of Engineering in Electronics & Communication Engineering of the Visvesvaraya Technological University, Belagavi, Karnataka during the academic year 2022-23. It is certified that all corrections/suggestions indicated for project work have been incorporated in the report deposited to the ECE department, the college central library &to the university. This final year project report **(Course Code: 19EC8ICPR2)** Phase-II hasbeen approved as it satisfies the academic requirement in respect of project work prescribed for the said degree.

Dept. Project Coordinators (Section incharges)	Project Guide
Prof. Bindu H M	Dr. Dinesha P
Head of the Department	Dr. B.G. Prasad
Dr. T.C. Manjunath, Ph.D. (IIT Bombay)	Principal, DSCE

External Project Viva-Voce

Name of the project examiners (int & ext.) with date:

1: Signature: _____

2: Signature: _____

Declaration

Certified that the project work entitled, **"Design of FinFET Based Combinational and Sequential Circuits"** with the project work course code **19EC8ICPR2** is a bonafide work that was carried out by ourselves in partial fulfillment for the award of degree of Bachelor of Engineering in Electronics & Communication Engg. of the Visvesvaraya Technological University, Belagavi, Karnataka during the academic year 2022-23. We, the students of the project group/batch no. S-02 do hereby declare that the entire project work has been done on our own & we have not copied or duplicated any other's work or may bethe extension of the works done by the earlier students. The results embedded inthis UG project report has not been submitted elsewhere for the award of any type of undergraduate degree.

Mr. Bhanu Prasad Nayak
USN: 1DS19EC708

Sign: _____

Ms. Chinnappa Reddy Gari Indu
USN: 1DS19EC710

Sign: _____

Mr. T Sai Gautham
USN: 1DS19EC742

Sign: _____

Mr. Pavan M
USN: 1DS20EC425

Sign: _____

Date: / 06 /2023

Place: Bengaluru - 111

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Table of Contents

Title Sheet		i
Certificate		ii
Declaration		iii
Acknowledgement		iv
Table of Contents		v
List of Figures		vi
List of Tables		viii
Nomenclature and Acronyms		ix
Abstract		1
Chapter 1	Introduction	2
	1.1 Overview	3
	1.2 Motivation	4
	1.3 Problem statement	5
	1.4 Objectives	5
	1.5 Organization of the project report	5
Chapter 2	Literature Survey	7
Chapter 3	Circuit diagram and implementation	9
	3.1 Circuit Diagram	9
	3.2 Implementation	11
Chapter 4	Software Requirements	18
Chapter 5	Results and Discussion	20
Chapter 6	Applications, Advantages, Limitations	39
	6.1 Application	39
	6.2 Advantages	41
	6.3 Limitations	42
Chapter 7	Conclusion	44
References		45
Publication		
CO-PO Mapping Justification Sheets		46
Budget Estimation Sheet		49
Plagiarism report		

List of Figures

Fig. 3.1(a): Flash ADC Circuit Diagram 9

Fig. 3.1(b): Johnson Counter Circuit Diagram 10

Fig. 3.2(a): R2R Ladder Circuit Diagram 11

Fig. 3.2(b): Priority Encoder block Diagram 13

Fig. 3.2(c): CS Amplifier Circuit Diagram 14

Fig. 3.2(d): Differential amplifier Circuit Diagram 15

Fig. 3.2(e): Comparator using op-amp 16

Fig. 3.2(f): D Flip-Flop Circuit Diagram 17

Fig. 4.1(a) Cadence tool 18

Fig. 5.1.1(a): Schematic of Priority encoder (8:3) 20

Fig. 5.1.1(b): Simulation of priority encoder using CMOS 21

Fig. 5.1.1(c): Simulation of priority encoder using FinFET 21

Fig. 5.1.2(a): Schematic of common source 22

Fig. 5.1.2(b): Simulation of Common source using CMOS 23

Fig. 5.1.2(c): Simulation of Common source using FinFET 23

Fig. 5.1.3(a): Schematic of Differential amplifier 24

Fig. 5.1.3(b): Simulation of Differential amplifier using CMOS 24

Fig. 5.1.3(c): Simulation of Differential amplifier using FinFET 25

Fig. 5.1.4(a): Schematic of Comparator 26

Fig. 5.1.4(b): Simulation of Comparator using CMOS 26

Fig. 5.1.4(c): Simulation of Comparator using FinFET 27

Fig. 5.1.5(a): Schematic of 3-bit Flash ADC 28

Fig. 5.1.5(b): Simulation of 3-bit Flash ADC using CMOS 28

Fig. 5.1.5(c): Simulation of 3-bit Flash ADC using CMOS 29

Fig. 5.1.5(d): Simulation of 3-bit Flash ADC using FinFET 30

Fig. 5.1.5(e): Simulation of 3-bit Flash ADC using FinFET 31

Figure 5.1.5(f): Simulation of 3-bit Flash ADC using FinFET 32

Fig. 5.1.6(a): Schematic of D Flip-Flop 33

Fig. 5.1.6(b): Simulation of D Flip-Flop using CMOS 33

Fig. 5.1.6(c): Simulation of D Flip-Flop using FinFET 34

Fig. 5.1.7(a): Schematic of Johnson Counter 35

Fig. 5.1.7(b): Simulation of Johnson counter using CMOS 35

Fig. 5.1.7(c): Simulation of Johnson counter using FinFET 36

List of Tables

Table 1: Literature Survey 7

Table 2: Priority Encoder Truth Table 13

Table 3: Code transitions for Flash ADC 30

Table 4: Code transitions for Flash ADC 31

Table 5: Code transitions for Flash ADC 32

Table 6: Results of Johnson Counter 37

Table 7: Results of 3-bit Flash ADC 37

Nomenclature and Acronyms

Abbreviations (Alphabetical Order):

IEEE	Institute of Electrical & Electronics Engineers
DSCE	Dayananda Sagar College of Engineering
ECE	Electronics & Communication Engineering
ADC	Analog to Digital Converter
CMOS	Complementary metal oxide semiconductor
CS	Common Source Amplifier
DA	Differential Amplifier
FinFET	Fin-Shape Field Effect Transistors
ICs	Integrated Circuits
MOSFETs	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-Channel Metal Oxide Semiconductor
PMOS	P- Channel Metal Oxide Semiconductor
SCEs	Short Channel Effect

Symbols (Alphabetical Order):

f	Femto
j	Joule
n	Nanometer
s	Seconds
w	Watt
u	Micro

Abstract

The final year project focuses on designing a combinational circuit called Flash ADC and a sequential circuit known as Johnson Counter. These circuits are based on Fin-type field-effect transistors (FinFETs), which are specifically used to address the challenges associated with scaling transistors beyond the nanometer range.

Integrated circuits (ICs) are heavily influenced by power considerations. While scaling transistors reduces the size of ICs, it also introduces short channel effects when pushed beyond the nanometer scale. These effects lead to increased leakage power, which is undesirable. To mitigate these issues and achieve low power dissipation, FinFETs are utilized.

The objective of this project is to design and simulate both combinational and sequential logic circuits using both FinFETs and complementary metal-oxide-semiconductor (CMOS) technology. A comparison is made between these circuits in terms of power dissipation and delay, using CMOS with the same technology (22nm) employed for FinFETs.

By employing FinFETs, the project aims to explore their potential in reducing the short channel effects and achieving low power consumption compared to CMOS technology. Through the design and simulation of the Flash ADC and Johnson Counter circuits, the project will evaluate the performance and power characteristics of these circuits implemented with FinFETs and CMOS.

Keywords: *FinFET, CMOS, Combinational, Sequential Circuits, Flash ADC, Johnson Counter,Power delay, Area.*

Chapter-1

Introduction

In the present scenario, the issue of leakage power has become significant in various electronic devices such as microprocessors, microcontrollers, and DSPs. These devices require high performance and speed, which leads to the scaling down of transistor sizes to accommodate a larger number of transistors on a single chip. Scaling helps increase the packing density and demands low voltage supply and reduced threshold voltage for improved performance. However, scaling also results in increased leakage power during the standby mode of circuits, primarily due to the short channel effects observed when scaling CMOS technology into the nanometer regime.

To address these challenges and improve leakage power characteristics, several methodshave been proposed, including strained silicon, silicon-on-insulator, FinFET, and MEMS. Among these techniques, FinFET has emerged as an effective method. FinFET is a field effect transistor design where the channel is located above the substrate, and the gate wraps around the channel, providing better control over the carriers. It offers advantagessuch as reduced power consumption, immunity to short channel effects, smaller area requirements, and higher operational speed.

Analog to Digital Converters (ADCs) play a crucial role in converting analog signals into digital signals, facilitating efficient information extraction from real-world signals. Various ADC architectures exist, including pipeline ADC, SAR ADC, Sigma-delta ADC, and Flash ADC. The Flash ADC is particularly known for its high speed and low- resolution capability, making it suitable for high-speed, low-resolution applications. In this project, a 3-bit Flash ADC is utilized to perform the desired analog-to-digital conversion.

The Johnson Counter, also known as the Twisted Ring Counter, is a modified version of the Counter. It consists of a group of flip-flops, where the inverted output of the last flip-flop is fed back as input to the first flip-flop. The number of states in a Johnson Counter istwice the number of flip-flops used. This counter can be implemented using either D flip-flops or JK flip-flops. Johnson Counters are

commonly employed for storing, processing, or counting the number of events that. occur within a circuit.

This project aims to address the leakage power issue by utilizing FinFETs in the design and simulation of combinational and sequential logic circuits. The Flash ADC and JohnsonCounter are specifically chosen as circuit examples for comparison in terms of power dissipation and delay, highlighting the advantages of using FinFETs over CMOS technology.

1.1 Overview

FinFET is an advanced transistor design that offers significant advantages over traditional planar transistors. It is widely used in modern integrated circuits (ICs) for both combinational and sequential circuits. One of the key advantages of FinFET is its ability to vertically stack the transistors, which increases the gate density and packing density oflogic circuits. This enables the integration of more functionality within a given chip area.

Another important feature of FinFET is the ability to implement transistors with differentthreshold voltages. This flexibility allows designers to optimize power and performancebased on specific requirements. By tailoring the threshold voltages, FinFET circuits can be designed to operate at lower power supply voltages, resulting in reduced power consumption and improved energy efficiency.

Leakage power, which refers to the power consumed by a circuit even when it is in a standby or idle state, is a significant concern in IC design. FinFET technology provides enhanced control over leakage power compared to planar transistors. This means that FinFET circuits can achieve improved performance and reduced power consumption, both in combinational and sequential designs.

FinFET technology offers superior performance, increased gate density, and the ability tooptimize power and performance through threshold voltage adjustments. It enables the design of circuits that operate at lower power supply voltages, resulting in reduced powerconsumption and improved energy efficiency. Moreover, FinFET

technology effectively addresses the issue of leakage power, contributing to enhanced performance and reducedpower consumption in both combinational and sequential logic circuits.

1.2 Motivation

The Moore's Law, a fundamental principle in the semiconductor industry, describes the continuous scaling of feature sizes in metal-oxide-semiconductor field-effect transistors(MOSFETs). This scaling has been instrumental in driving advancements in electronic component technologies. However, as MOSFETs are further scaled down, they encounterchallenges related to device performance due to various short-channel effects (SCEs).

Short-channel effects refer to undesirable changes in the behavior of MOSFETs as their dimensions are reduced. These effects include an increase in tunneling current (leakage current), degradation of the subthreshold swing (the relationship between gate voltage and current in the off-state), and an increase in the off-state current. These issues pose significant obstacles to achieving optimal device performance at smaller scales.

To overcome these challenges, it has become crucial to identify suitable technologies forthe further scaling of MOS transistors. This need has led to the development of the FinFET technology. FinFETs address the short-channel effects by introducing a three-dimensional transistor structure. In a FinFET, the channel is raised above the substrate and is surrounded by a gate that wraps around it, resembling a fin-like structure. This design provides improved control over the flow of current, mitigating the issues associated withshort-channel effects.

The introduction of FinFETs as a replacement for traditional planar MOSFETs has proven to be an effective solution for achieving further scaling in semiconductor devices. By adopting the FinFET technology, device designers can continue to adhere to the principles of Moore's Law, enabling the development of increasingly sophisticated and powerful electronic components.

1.3 Problem statement

Scaling of transistors leads to reduction in size of IC (Integrated Circuit), also results in short channel effects if the scaling is done beyond nanometer.

Short channel effect occurs when channel length approx. equal to charge regions of source and drain. This causes rise in leakage current; threshold roll off (makes difficult for the transistors to turn on and off), mobility of carrier is reduced, velocity saturation (carrier drifting effected due to high electric field) etc.

1.4 Objectives

To design and performance evaluation of combinational logic circuit like 3bit Flash ADC and sequential logic circuit 4bit Johnson Counter on FinFET using 22nm technology.

To design basic circuits like comparator using op amp, and priority encoder (8:3) for Flash ADC and D-flipflop for Johnson Counter.

1.5 Organization of the project report

The project work undertaken by us is organized in the following sequence as follows.

Chapter 1: We briefly discussed CMOS and FinFETs then issues related to CMOS and how to overcome these issues by using FinFETs. We investigated our problem statement, objectives, and motivation involved in our project.

Chapter 2: we did some literature survey related to our project.

Chapter 3: We have designed combinational Circuits (3-bit flash ADC) and Sequential Circuits (Johnson counter). Implemented circuits required to design 3-bit flash ADC (R2Rladder, comparator, priority encoder) and for Johnson Counter (D- flipflop).

Chapter 4: To design circuits the software tool (Cadence) is required is discussed.

Chapter 5: We have discussed our simulated results of the circuits.

Chapter 6: We listed some advantages, applications, and limitations of the project.

Chapter 7: We head to the conclusion of our project.

Chapter 2

Literature Survey

The goal of the literature survey is to gain a comprehensive understanding of the currentstate of the circuit design and to identify potential solutions and approaches for the specific design problem.

Sl.no	Journal/Paper name	Year	Observation
1	Mr. Tilak Kumar L, Chandan A, Chethankumar K M, Dommeti Venkata Sai Krishna Vasanth, Hemant "Power Efficient 4 Bit Flash ADC Using Cadence Tool" International Research Journal of Engineering and Technology.[1]	2022	• Of all ADC types, flash or parallel converters operate at the fastest speed. • To boost performance while lowering power consumption, flash ADC design commonly plays a major part in other forms of ADCs
2	Vasudeva G, Shankar, Girish J R, "Design of High-Performance CMOSComparator using 90nm Technology''.[2]	2016	• Proposed a high-performance CMOS comparator with lowoffset voltage with high gain
3	M Reddi Sekhar, P Uma, D Venkataramana Pushpalatha D Viswanada reddy "an efficient priority encoder & decoder using 45nm finFET technology" JETIR March 2019.[3]	2019	• Reduction of power consumption &reduction of area are the most important issues in CMOS circuit design Analyzes and optimizes area, power and size of the encoder and decoder using 45nm technologies.

4	Vasudeva G, Uma B V 22nm FINFET Based High Gain Wide Band Differential Amplifier International Journal of Circuits, Systems and SignalProcessing.[4]	2021	• Differential Amplifier (DA) is a fundamental building block of complex analog circuits. • Power consumption of 58μWwas observed in their work on FINFET based DA at 1 V power supply
5	Shivali, Shobha Sharma, Amita Dev "Analysis of Various Master-Slave Configuration based D Flip-Flops" International Journal of Recent Technology and Engineering.[5]	2019	• Enumerates review on various earlier proposed master slave configuration-based D flip flop models.
6	S. Greeshma sai, N. Alivelu Manga, P. Chandra Sekhar "Design and Simulation of FinFET based digital circuits for low power applications".[6]	2020	• Johnson ring counter is designed and simulated in 45 nm CMOS and 22 nm FinFET technology. Powerdissipation is decreased in FinFET compared to CMOS
7	Rajuhajare, Dr.C. Lakshmi Narayana, Sunil.C, Sumanth, Anish.A. "Design and evaluation of FinFET based digitalcircuits for high-speed ICs".[7]	2020	• Simulation results for FinFET based digital application at 22nm and 14nm are studied here. The results obtained shows that the FinFETs application on the nanoscale devices has improved.

Chapter 3

Circuit Diagram and Implementation

3.1 Circuit Diagram

3.1.1 3-Bit Flash ADC

A Flash Analog-to-Digital Converter (ADC) typically consists of three main blocks: a Resistor ladder, a Comparator array, and a Priority encoder.

The Resistor ladder is responsible for generating a set of reference voltages. These reference voltages are usually evenly spaced and cover the desired range of the analog input signal. The purpose of the resistor ladder is to establish a voltage ladder that servesas a basis for comparison with the input signal.

The Comparator array compares the incoming analog signal with the reference voltagesgenerated by the resistor ladder. Each comparator in the array compares the input voltage with a specific reference voltage. The outputs of the comparators are in the form of a thermometer code. In a thermometer code, each comparator that detects the input voltage being greater than its corresponding reference voltage sets its output to a high logic level(1), while the other comparators remain at a low logic level (0).

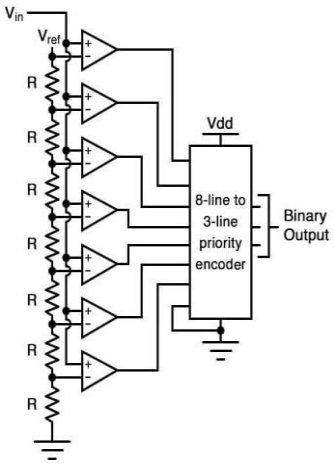

Fig.3.1(a): Flash ADC circuit Diagram

The Priority encoder receives the thermometer code from the comparator array and converts it into a binary code representation. The binary code represents the digital equivalent of the analog input signal. The encoder determines which bits in the binary code are set to logic high based on the thermometer code.

The Flash ADC works by comparing the input analog signal with a set of reference voltages, generating a thermometer code, and then converting it into a binary code. The binary code represents the digital representation of the analog signal and can be further processed or utilized by digital systems for various applications.

3.1.2 Johnson Counter

A Johnson Counter is a type of counter that consists of a cascaded arrangement of n flip-flops, where the inverted output of the last flip-flop is fed back as the input to the first flip-flop. In the case of a 4-bit Johnson counter, it is constructed using D flip-flops, and all the flip-flops share the same clock signal.

The operation of a Johnson Counter relies on the concept of shift registers. If a serial data signal is applied to the input of a serial-in to serial-out shift register, the same sequence of data will eventually exit from the last flip-flop in the register chain.

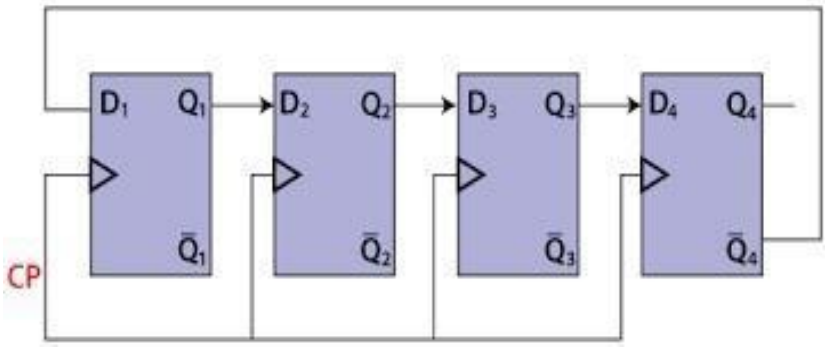

Fig.3.1(b): Johnson counter circuit diagram

The serial movement of data through the shift register occurs after a predetermined number of clock cycles, effectively creating a time delay circuit for the original input data signal. By connecting the output of the shift register back to its input, such that the output from the last flip-flop (Q4) becomes the input of the first flip-flop (Q1), a closed loop circuit is formed. This loop continuously "recirculates" the same bit of data around the circuit for each state of the sequence.

In simpler terms, a Johnson Counter is a counter that utilizes a feedback loop to create a continuous cycle of a specific bit sequence. The feedback allows the counter to create a repeating pattern of states. This type of counter can be implemented using shift registersand is commonly used in various applications, such as generating timing signals, decoding, and sequence detection.

3.2 Implementation

The Flash ADC is implemented by design the circuits like R2R ladder, Comparator i.e. Op-Amp (Common source Amplifier and Differential Amplifier) and Priority Encoder.Whereas the Johnson Ring counter is implemented by designing D-flipflop. These circuitsare simulated and implemented for 22 nm technology in cadence virtuoso, in transistorlevel using PMOS and NMOS for CMOS design and PFET and NFET for FinFET design.

3.2.1 R2R Ladder

A resistive voltage divider is a basic circuit configuration consisting of resistors connectedin series to scale down the voltage of an input signal. This voltage scaling is achieved through the distribution of the input voltage across the resistors in the circuit. The resistive voltage divider is commonly used to generate reference voltages or reduce the magnitudeof a high voltage to a desired level.

Figure 3.2(a): R2R Ladder Circuit Diagram

The voltage output (Vout) of a resistive voltage divider can be calculated using the formula derived from Kirchhoff's Laws. If two resistors, R1 and R2, are connected in series, the formula is as follows: Vout = R2 x Vin / (R1 + R2).

In this formula, Vin represents the input voltage that needs to be scaled down, R1 is the resistance value of the first resistor in the series, and R2 is the resistance value of the secondresistor. By adjusting the values of R1 and R2, the output voltage can be controlled relative to the input voltage.

The resistive voltage divider circuit is a straightforward and commonly used method forachieving voltage scaling. It is widely utilized in various applications, such as generatingreference voltages for analog circuits, biasing circuits, or attenuating high voltage signalsto levels suitable for specific components or systems.

3.2.2 Priority Encoder

An encoder is a digital circuit that takes a set of binary inputs and converts them into a unique binary code that represents the position or identity of the active input. It is commonly used in digital systems to convert parallel inputs into a serial code. The main purpose of an encoder is to assign a specific binary code to each possible input combination.

A priority encoder is a type of encoder that determines the highest priority input when multiple input lines are active simultaneously. It solves the issue of producing incorrect outputs when multiple input lines are highly active. The priority encoder gives priority tothe highest priority input, ignoring all other input lines, to generate the corresponding output.

In this project, an 8-bit priority encoder is used, which has 8 inputs and 3 outputs. The truth table provided describes the behavior of the 8-bit priority encoder, and the block diagram illustrates its structure. The output expressions for Q0, Q1, and Q2 are determined using a Karnaugh map (K-map) to simplify the logic.

For example, the output Q0 is determined by the logical OR operation of inputs D1, D3, D5, and D7. Similarly, Q1 is determined by the logical OR operation of inputs D2, D3, D6,and D7, and Q2 is determined by the logical OR operation of inputs D4, D5, D6, and D7.

In digital applications, priority encoders are commonly used to select and identify the highest priority input among a set of inputs. The output of the priority encoder indicates which input has the highest priority, providing valuable information for further processing or decision-making in digital systems.

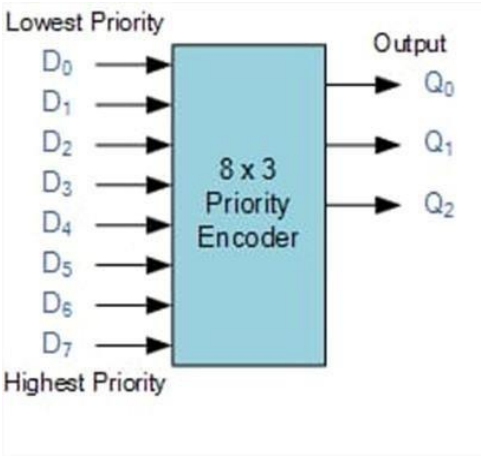

Figure 3.2(b): Priority Encoder Block Diagram

Table 2: Priority Encoder truth table

Inputs								Outputs		
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y_2	Y_1	Y_0
1	0	0	0	0	0	0	0	0	0	0
×	1	0	0	0	0	0	0	0	0	1
×	×	1	0	0	0	0	0	0	1	0
×	×	×	1	0	0	0	0	0	1	1
×	×	×	×	1	0	0	0	1	0	0
×	×	×	×	×	1	0	0	1	0	1
×	×	×	×	×	×	1	0	1	1	0
×	×	×	×	×	×	×	1	1	1	1

3.2.3 Common source amplifier

In a common source (CS) amplifier, an input signal is applied to the gate terminal of a field-effect transistor (FET), while the source terminal is connected to a reference voltage.The amplified output voltage is obtained across a resistor connected to the drain terminal,forming the load. The purpose of the CS amplifier is to amplify an analog signal and convert it into a voltage level that can be compared with a reference voltage.

To ensure stable operation and linear amplification, a biasing network is used to providea stable DC voltage to the gate terminal of the FET. This biasing voltage keeps

the amplifier in its linear amplification region, allowing for accurate amplification of the input signal. When an AC signal is applied to the amplifier, it modulates the current flowing through the FET channel, resulting in a voltage variation at the drain terminal. This voltage variation represents the amplified output signal of the CS amplifier.

The output of the CS amplifier is then connected to a comparator, which compares the voltage level with multiple reference voltages generated by a voltage divider network. The purpose of the comparator is to determine the relationship between the amplified signaland the reference voltages.

Based on the comparison results, the comparators produce a digital code that represents the input voltage level. This digital code is typically used for further processing, decision-making, or conversion of the analog signal into a digital format.

In summary, the CS amplifier amplifies an analog input signal and converts it into a voltage level that can be compared with reference voltages using a comparator. This process enables the determination of a digital code representing the input voltage level, allowing for further analysis and utilization of the signal.

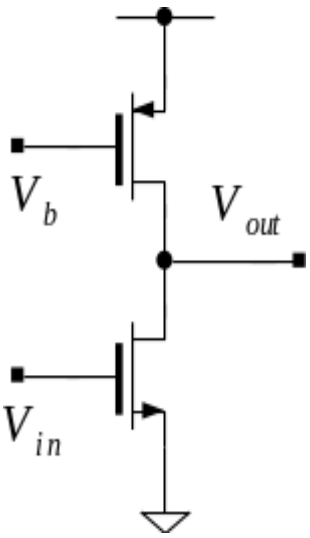

Figure 3.2(c): CS Amplifier Circuit Diagram

3.1.1 Differential amplifier

A differential amplifier is an electronic amplifier designed to amplify the voltage difference between two input signals while rejecting any common voltage that is presentin both inputs. In the context of a 3-bit flash ADC, the differential amplifier plays a crucial role in comparing the amplified input signal with the reference voltages.

The differential amplifier consists of two inputs, namely the non-inverting and invertinginputs. The amplified output signal from the common source (CS) amplifier is connectedto the non-inverting input of the differential amplifier. On the other hand, the reference voltages generated by the voltage divider network are connected to the inverting inputsof the differential amplifier.

The purpose of the differential amplifier is to amplify the voltage difference between thenon-inverting and inverting inputs and produce an output voltage that represents the result of the comparison. By amplifying the difference between the input signal and the reference voltages, the differential amplifier enables the identification of which referencevoltage closely matches the input signal.

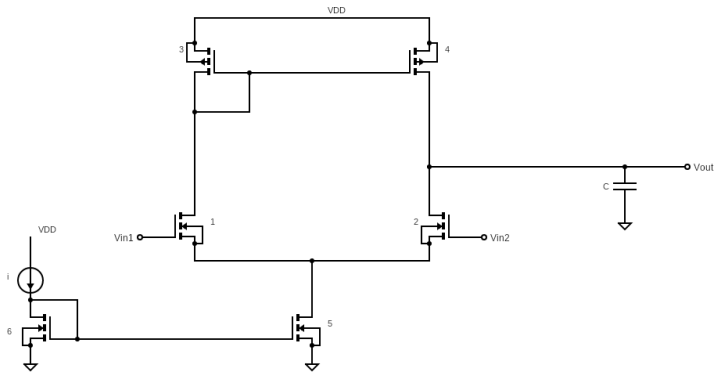

Figure 3.2(d): Differential Amplifier Circuit Diagram

The output of the differential amplifier is then typically fed into a logic circuit, such as a priority encoder, which converts the analog output into a digital code. The logic circuit takes the amplified voltage as input and generates a binary code that represents the corresponding reference voltage or input level.

3.1.2 Comparator

Comparators play a crucial role in the operation of analog-to-digital converters (ADCs). The choice of comparator type and architecture greatly impacts the performance of the overall ADC system. In the case of a Flash ADC, a common choice for the comparator is a differential comparator implemented using an operational amplifier (Op-Amp).

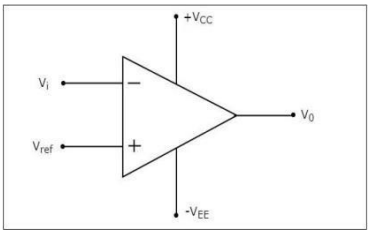

Figure 3.2(e): Comparator using op-amp

An operational amplifier, or Op-Amp for short, is a type of electronic amplifier that is DC-coupled and exhibits high gain. It is designed to amplify voltage signals and has a single-ended output waveform, meaning that the output is referenced to a single voltage level. However, the input to the Op-Amp is in the form of a differential signal, where two inputvoltages are compared.

The differential comparator based on an Op-Amp is well-suited for Flash ADCs because it allows for precise and accurate comparison of the amplified input signal with the reference voltages. The Op-Amp amplifies the voltage difference between the two input signals, which enhances the sensitivity and resolution of the comparator.

The high gain of the Op-Amp ensures that even small differences between the input voltages are amplified to a level that can be reliably detected and used for the ADC's decision-making process. This is crucial for achieving accurate digitization of the input signal.

3.2.6. D-flipflop

The Johnson Ring Counter, which is a cascaded arrangement of D-flipflops, is implemented using Master-Slave D-flipflops. In the design of the Master-Slave D-flipflop, an inverter cell is created with the same transistor specifications and is directly incorporated into the schematic. The purpose of the inverter cell is to invert the input signal and generate the complemented output.

To enable the reset operation in the Master-Slave D-flipflop, two additional NMOS transistors are included in the circuit. These transistors are responsible for resetting theflipflop to a specific state. The reset operation is important to initialize the counter and ensure a known starting point.

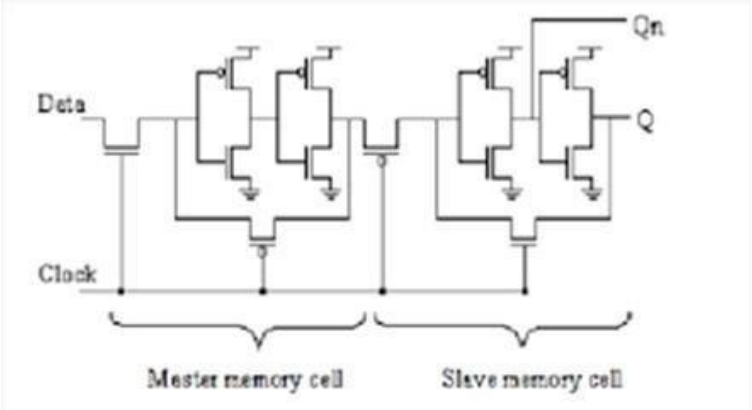

Figure 3.2(f): D-flipflop Circuit Diagram

To simplify the design and facilitate the implementation of the Johnson Ring Counter, a cell of the Master-Slave D-flipflop is created. This cell serves as a building block that can be replicated multiple times to create the complete Johnson counter. By reusing the designed flipflop cell as an instance, the circuit can be efficiently constructed, saving timeand effort.

The Master-Slave D-flipflop and the inverter cell are essential components in implementing the Johnson Ring Counter. They enable the sequential operation and the generation of the required states in the counter. By using these components and cascading them together, the Johnson Ring Counter can effectively store, process, or count the number of events occurring within the circuit.

Chapter 4

Software Requirements

Software tool is used to implement the circuit is cadence virtuoso of 22nm technology. Cadence Virtuoso is a software tool widely used in the field of integrated circuit (IC) design. Specifically, it is an analog design environment that provides designers with a range of capabilities to analyze, verify, and implement their circuit designs. Cadence Virtuoso is known for its robustness and versatility, making it a popular choice for designing complex digital, analog, and mixed-signal ICs.

The Cadence platform offers a comprehensive suite of tools that cover various stages of the design process. It includes features such as schematic capture, simulation, layout design, and physical verification. These tools enable designers to create and refine their circuit designs, perform accurate simulations to evaluate their performance, and ensurethat the designs meet the required specifications.

Fig 4.1(a): Cadence tool

One of the key advantages of using Cadence Virtuoso is its ability to handle advanced technologies, such as the 22nm technology mentioned. The tool provides support for designing circuits at the transistor level, allowing designers to work with intricate detailsand optimize their designs for the specific technology node. PTM files refer to Process Technology Model files. These files contain information about the characteristics and behavior of transistors and other components in a specific semiconductor process technology.

Process Technology Models, also known as SPICE models, are used in electronic design automation (EDA) tools to simulate and analyze the behavior of integrated circuits (ICs)at the transistor level. They provide information about how transistors and other components, such as resistors and capacitors, behave under different operating conditions.

PTM files typically include parameters such as threshold voltage, drain current, capacitances, resistances, and other electrical properties that define the behavior of the transistors. These models are crucial for performing accurate circuit simulations and optimizing the performance of VLSI designs.

SP files typically refer to SPICE (Simulation Program with Integrated Circuit Emphasis) netlist files. SPICE is a widely used circuit simulation program that allows designers to simulate the behavior of electronic circuits.

SPICE netlist files are text-based files that contain a description of the circuit componentsand their interconnections. They specify the circuit topology, component models, parameter values, and simulation settings. These files follow a specific syntax that is understood by SPICE simulators.

The. sp file extension is commonly used for netlist files in SPICE. The contents of a .sp file include statements that define circuit components such as resistors, capacitors, transistors, voltage sources, etc., along with their parameter values. The interconnections between components are defined using nodes or nets.

For FinFETs and CMOS 22nm we have used these files and obtained the transient response.

Chapter-5

Results and Discussions

5.1 Simulation Results

We have implemented basic combinational circuits required for 3-bit Flash ADC i.e., 8:3 Priority Encoder, Common Source Amplifier, Differential Amplifier and Comparator, andfor sequential circuit Johnson Counter and D-Flipflop.

5.1.1. Priority Encoder (8:3)

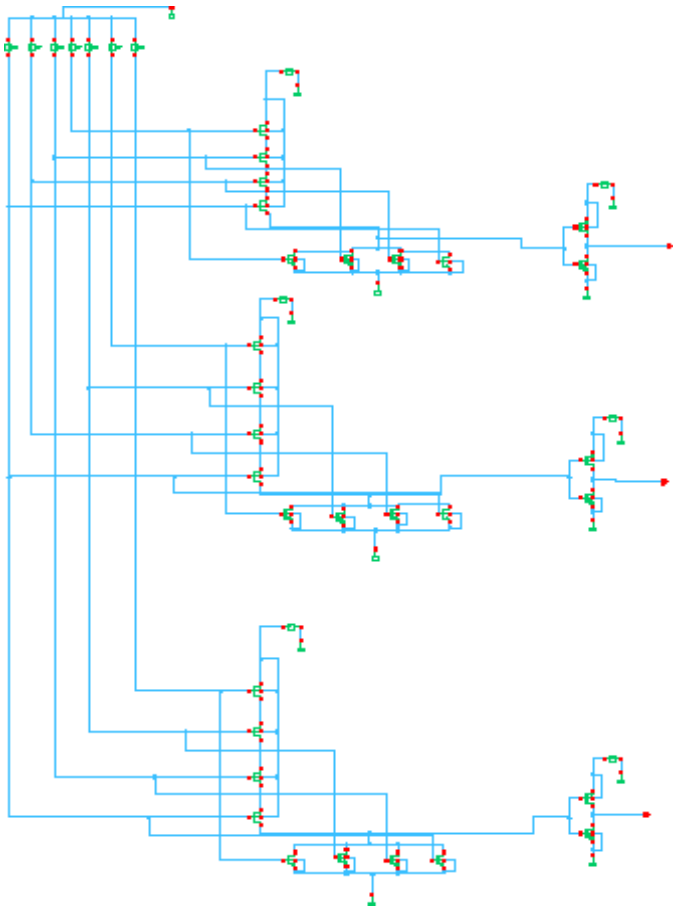

Figure 5.1.1(a): Schematic of Priority Encoder (8:3)

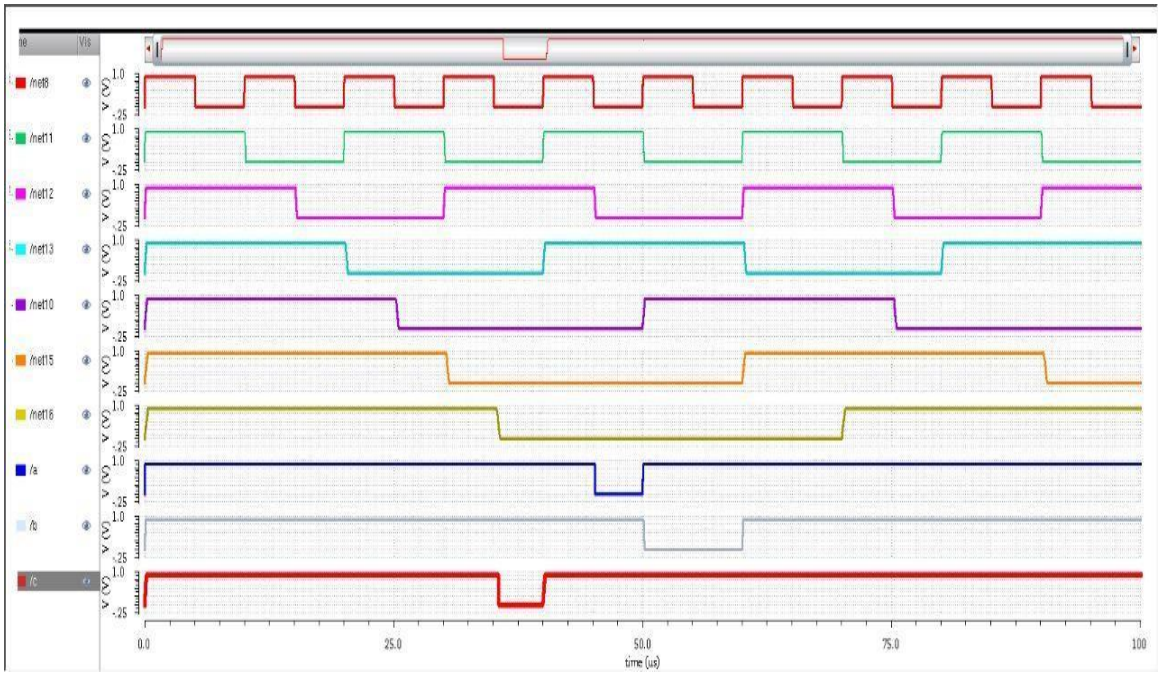

Figure 5.1.1(b): Priority Encoder Simulation using CMOS for 22nm technology.

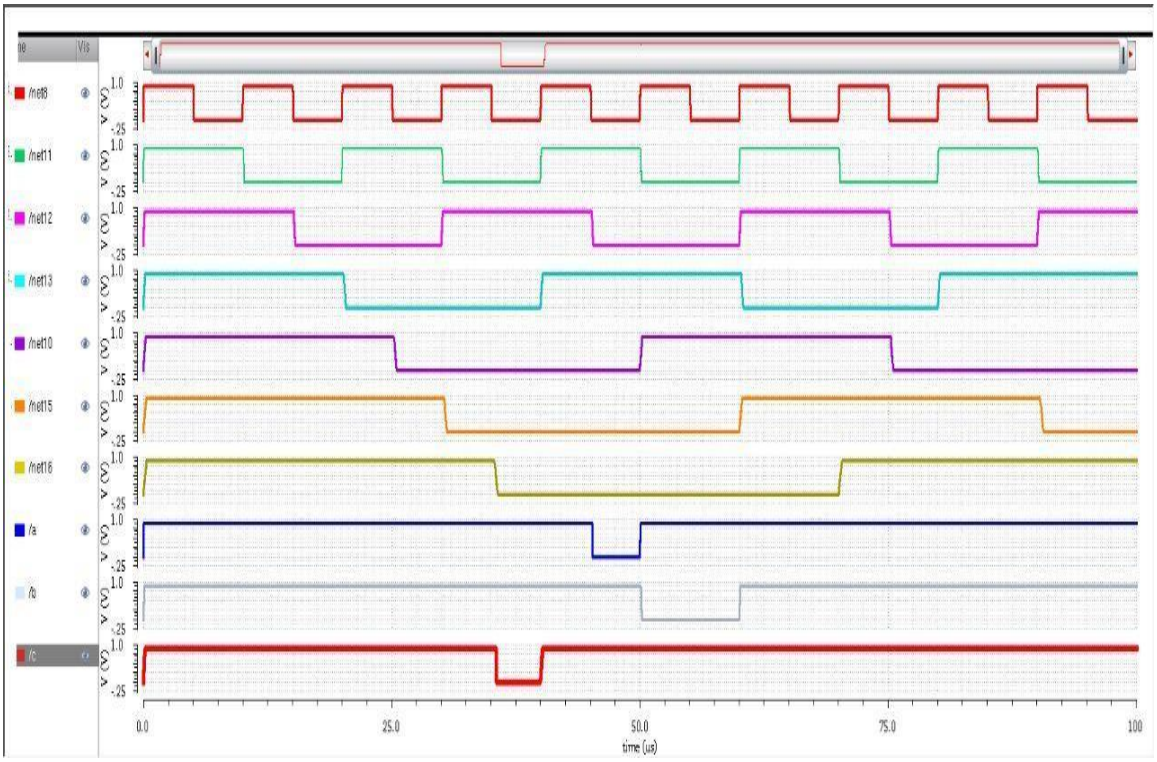

Figure 5.1.1(c): Priority Encoder simulation using FinFET for 22nm technology.

The above figures 5.1.1(a) illustrates the design of Encoder using cadence tool and 5.1.1(b) and 5.1.1(c) illustrates the simulated results Encoder using CMOS and FinFET for 22nm technology.From the figure 5.1.1(b) and (c) the seven inputs that are D1 which is net 8 with a time period of 20us and width of 10u, D2 which is net 11 with a time period of 30us and width15u, D3 which is net 12 with a time period of 40us and width of 20u, D4 which is net 13 with a time period of 15us and width 25u, D5 which is net 10 with a time period of 60usand width 30u, D6 which is net 15 with a time period of 70us and width 55u, D7 which isnet 16 with a time period of 80us and width 40u and D0 that can be grounded or kept VDD. a, b, and c are outputs, where a is LSB and C is MSB. When D7 is high the output is always seven that is 111, when D7 become low and D6, D5,D4, are low and D3 is high output is three which is 011. When D7, D6 are low it checks forD5, where D5 is high so will be getting output as five which is 101.

5.1.1. Common Source Amplifier

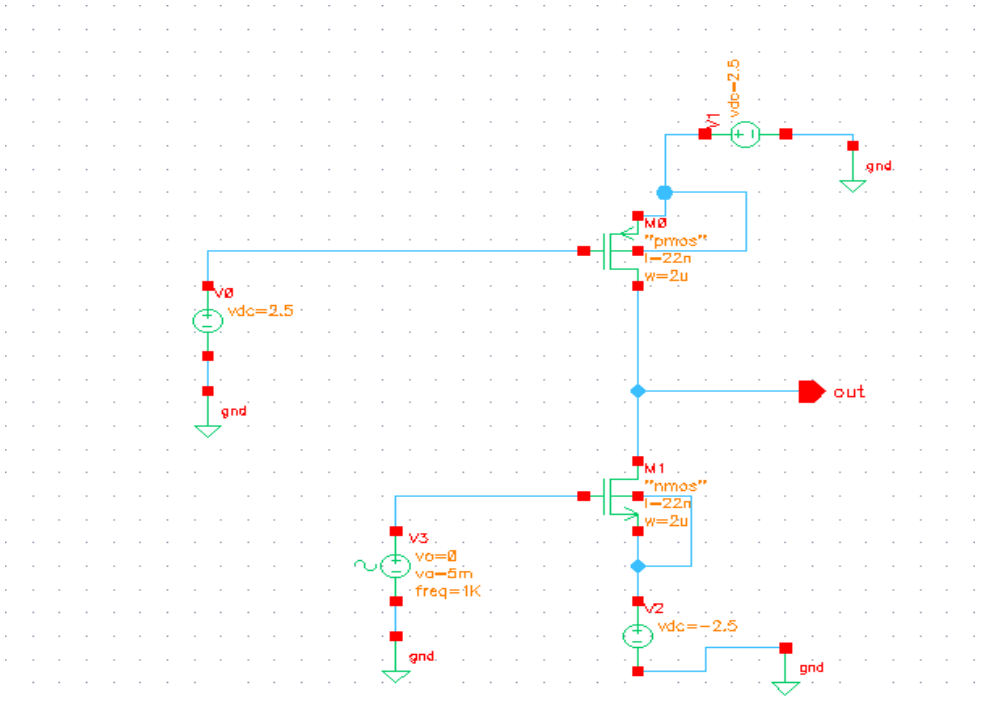

Figure 5.1.2(a): Common source amplifier schematic

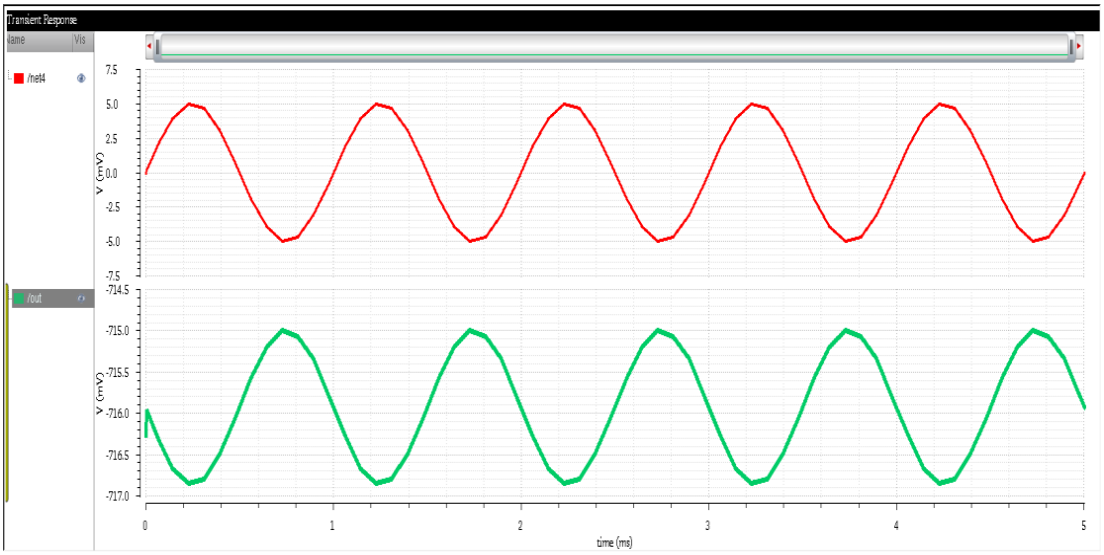

Figure 5.1.2(b): Common source amplifier simulation using CMOS for 22nm technology

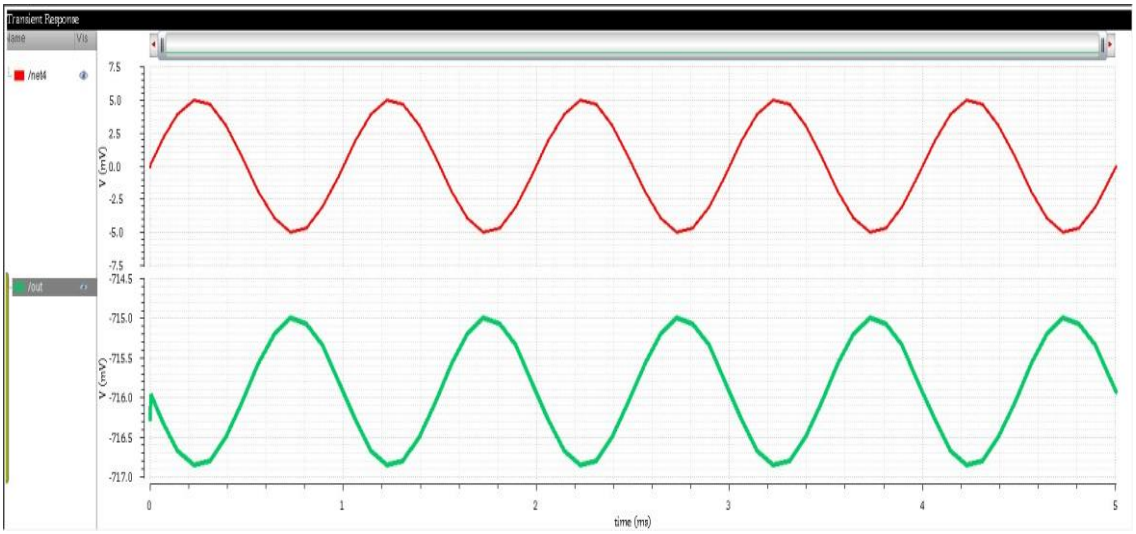

Figure 5.1.2(c): Common source amplifier simulation using FinFET for 22nm technology

The above figure 5.1.2(a) illustrates design of Common Source Amplifier and figures 5.1.2(b) and 5.1.2(c) illustrates the simulated results for CMOS and FinFET for 22nm technology.

The input is applied between the gate source terminal and output is taken at drain sourceterminal, Source is common for both input and output. In figure 5.1.2(b) and 5.1.2(c) the red color wave represents the input sine Wave with 5mv input, 1khz frequency and greencolor wave represents the output that is inverted amplified signal of input along with some noise.

5.1.1. Differential Amplifier

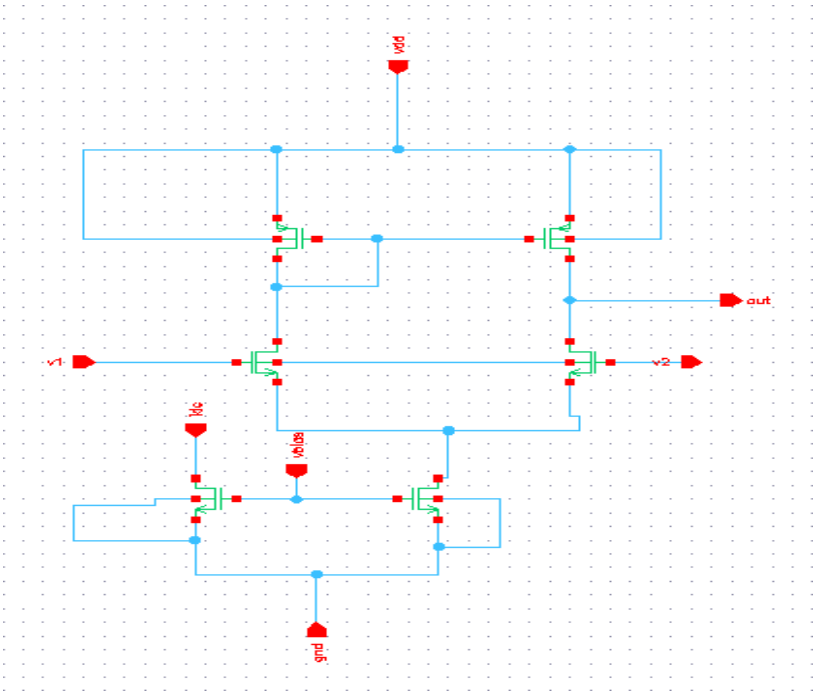

Figure 5.1.3(a): Differential Amplifier schematic

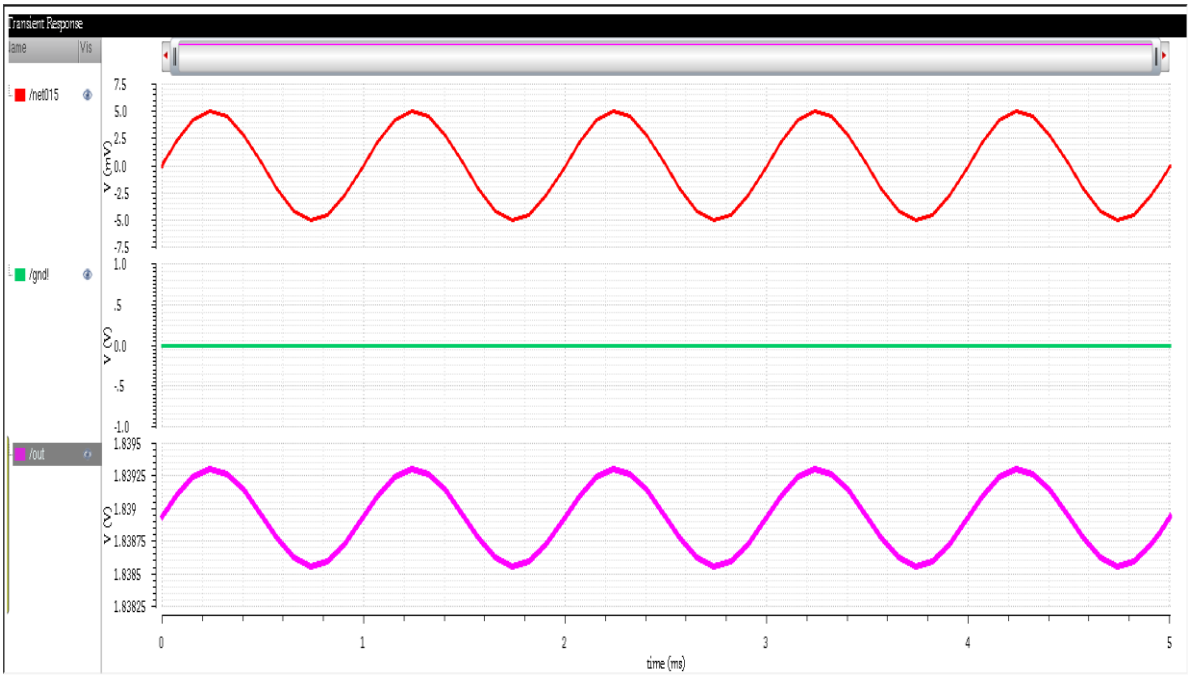

Figure 5.1.3(b): Differential amplifier simulation using CMOS for 22nm technology

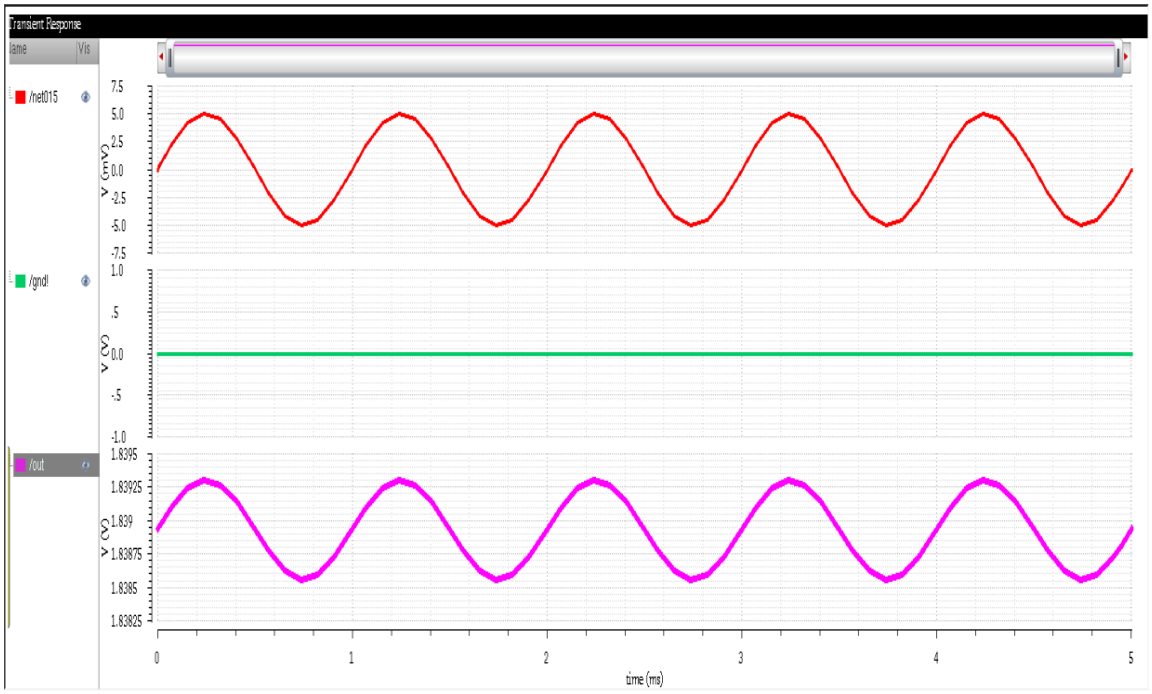

Figure 5.1.3(c): Differential amplifier simulation using FinFET for 22nm technology

The above figure 5.1.3(a) illustrates design of Differential Amplifier circuit and figures 5.1.3(b) and 5.1.3(c) illustrates the simulated results for CMOS and FinFET for 22nm technology. The differential amplifier consists of two inputs where one is applied to inverting terminal and another one to non-inverting terminal, the amplified output from CS amplifier is connected to non-inverting input and reference voltage to inverting inputs. In the figure 5.1.3(b) and 5.1.3(c), red color wave represents the input with 5v input voltage and green color wave is grounded, purple color wave represents the output amplified wave which is the difference of two input signals.

5.1.2. Comparator

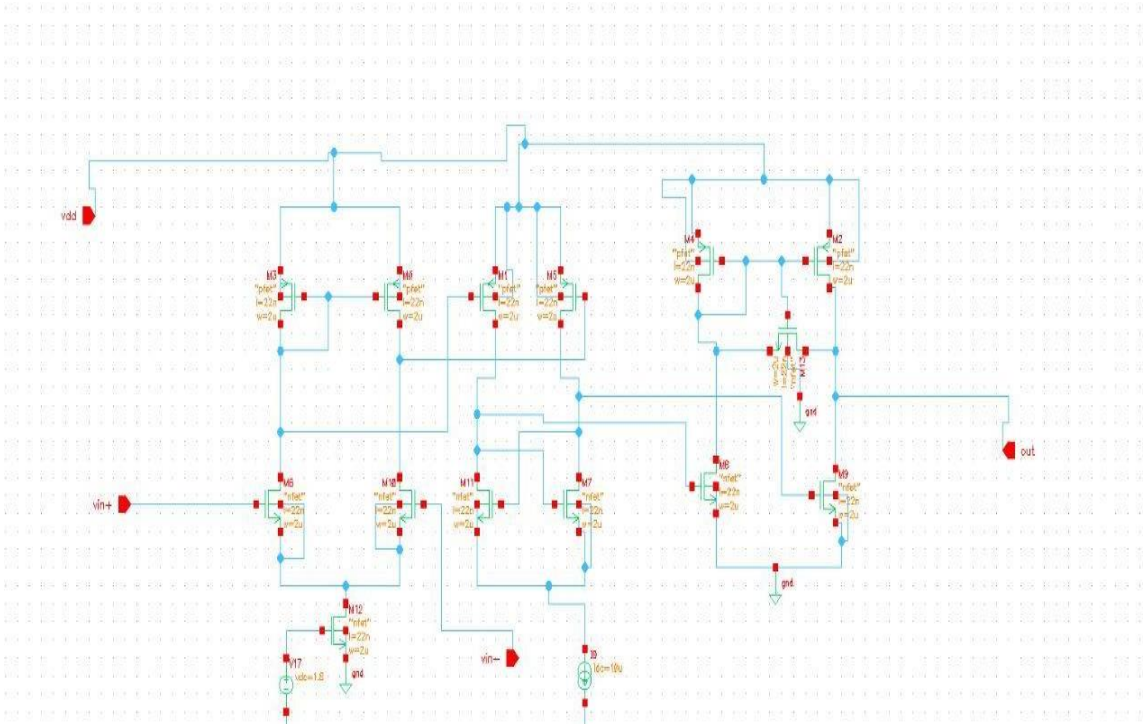

Figure 5.1.4(a): Comparator

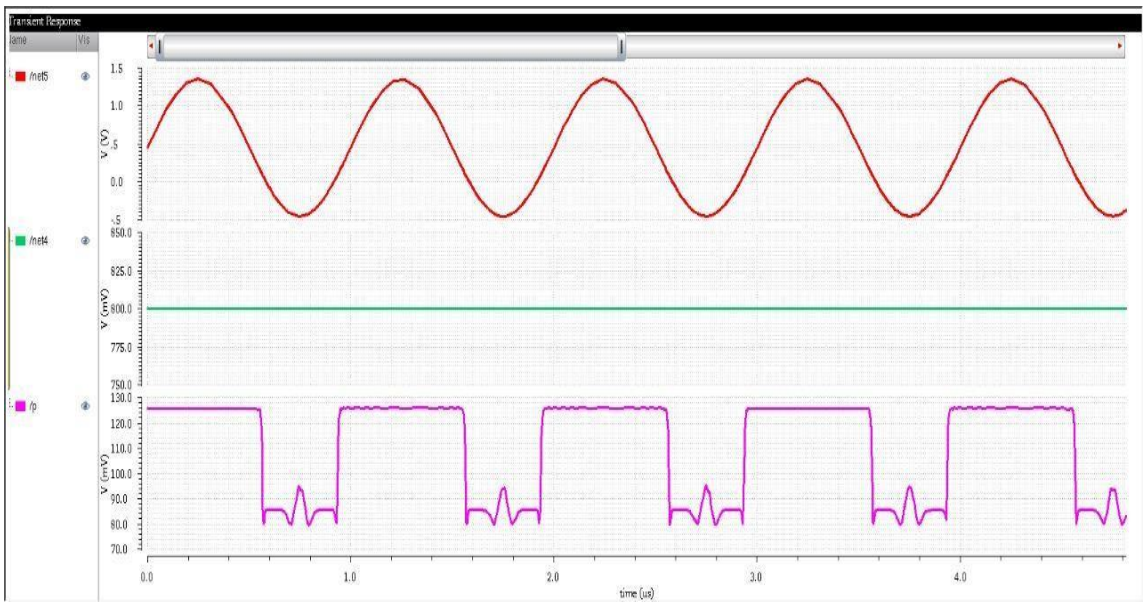

Figure 5.1.4(b): Comparator simulation using CMOS for 22nm technology

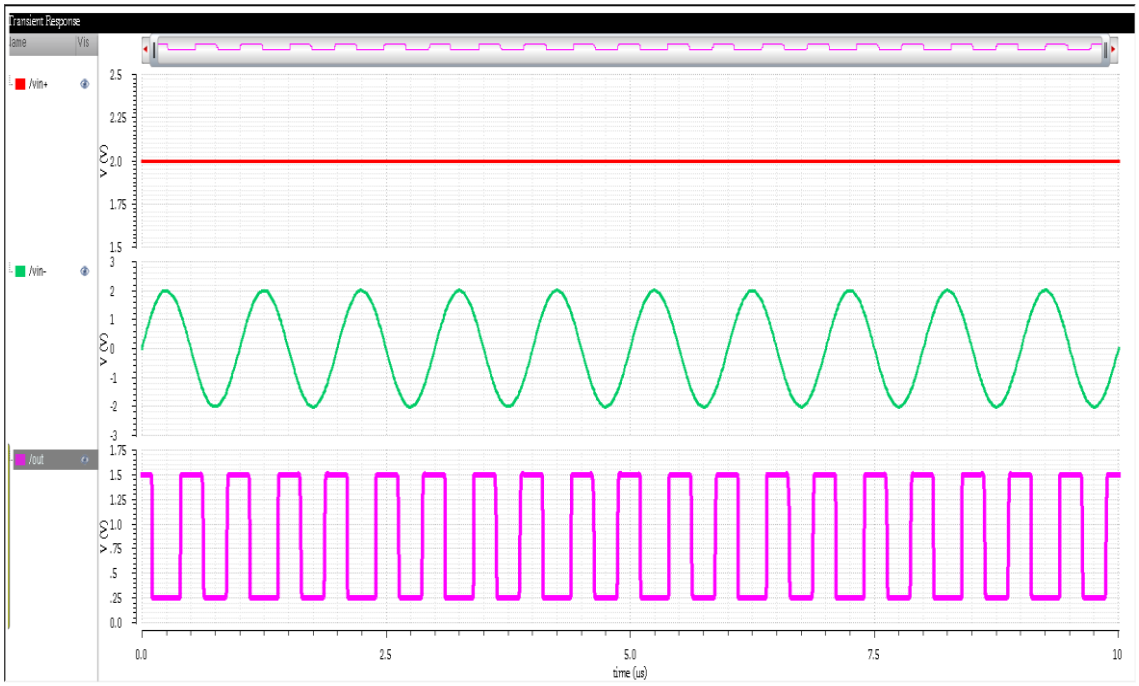

Figure 5.1.4(c): Comparator simulation using FinFET for 22nm technology

The above figure 5.1.4(a) illustrates design of Comparator circuit and figures 5.1.4(b) and 5.1.4(c) illustrates the simulated results for CMOS and FinFET for 22nm technology.

It is latched comparator, there are three parts: one is preamplifier which is differential amplifier two inputs, second, is decision circuit which selects +vsaturation or -vsaturationof the output and it is operated by the current mirror of preamplifier and third, is bufferis used to store and get output. It consists a one input as a positive sine wave of 1.5v, 1Mzfrequency and other input with negative vdc of 800mv input. In the figures 5.1.4(b), 5.1.4(c), the red color represents the input DC voltage with 2v, and green color sine waveinput with 2v. The purple color wave represents the compared output of the comparator.Here when the v ref voltage > v sin voltage then the output of the comparator will be low,else it is high.

5.1.3. 3-bit Flash ADC

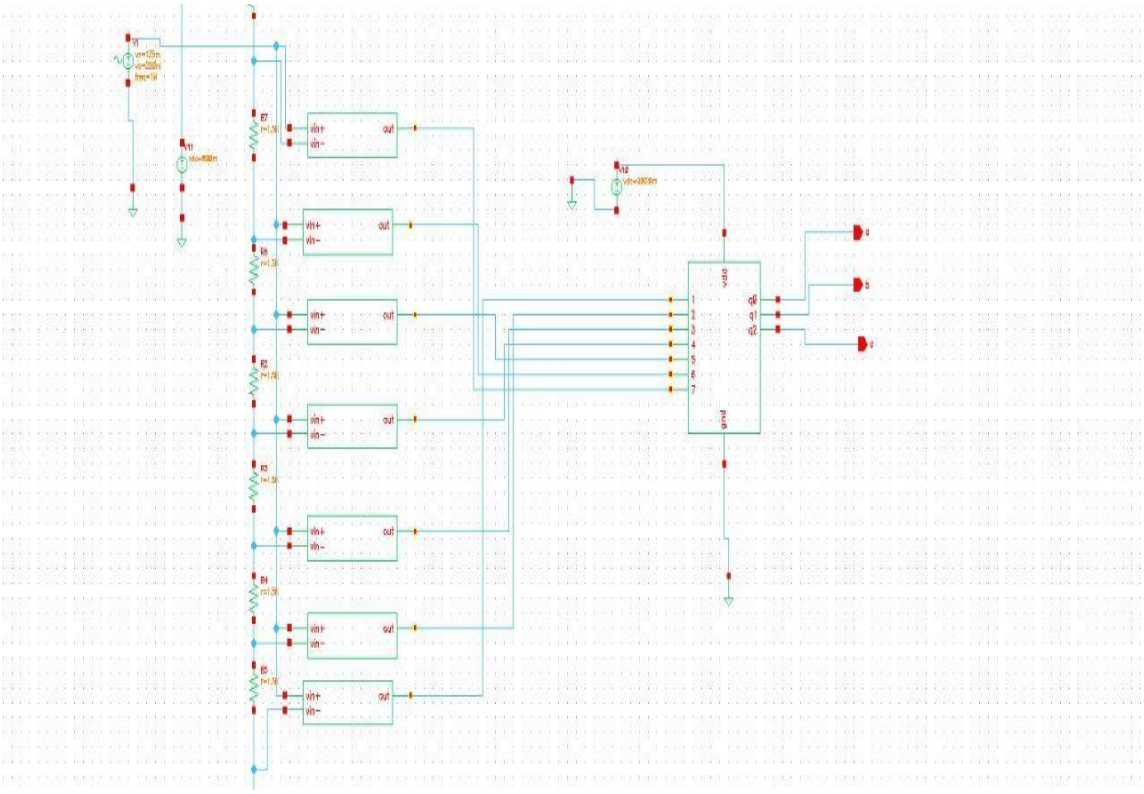

Figure 5.1.5(a): 3-bit Flash ADC

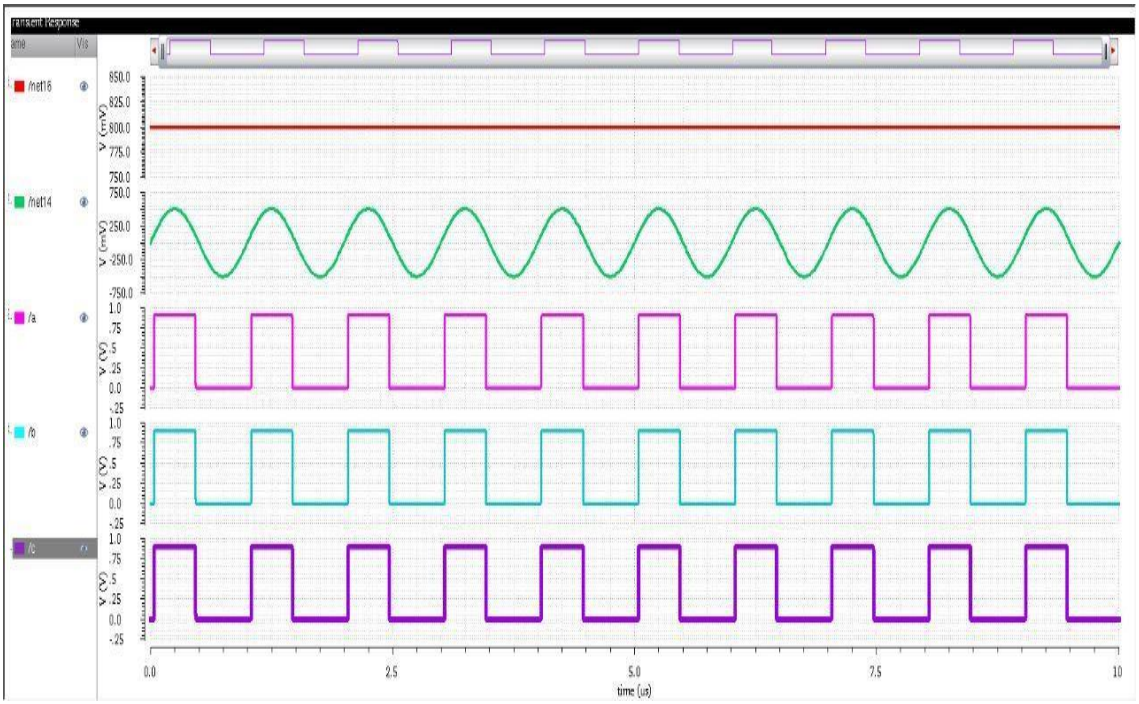

Figure 5.1.5(b): 3-bit flash ADC simulation using CMOS for 22nm technology

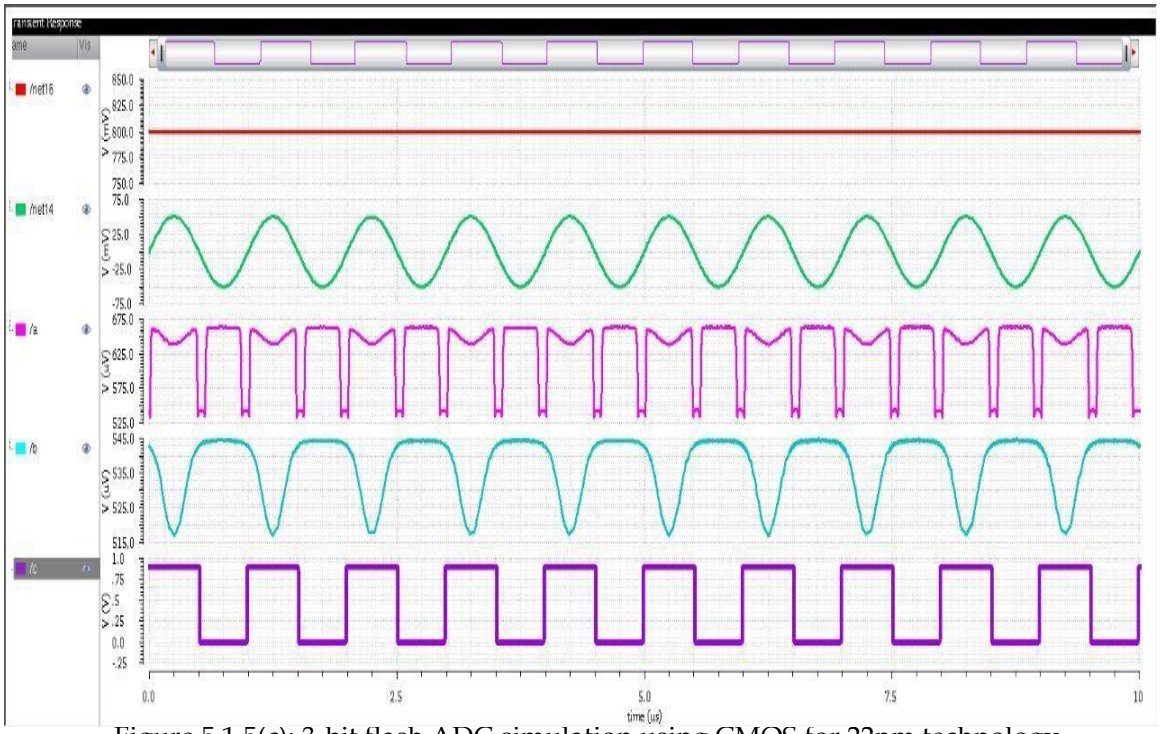

Figure 5.1.5(c): 3-bit flash ADC simulation using CMOS for 22nm technology

The above figure 5.1.5(a) illustrates design of 3-bit flash ADC circuit and figures 5.1.5(b)and 5.1.5(c) illustrates the simulated results for CMOS for 22nm technology. Individually we are getting all the components outputs correctly, but when we try to design 3-bit flash ADC by combing them in CMOS we are getting too any distortions and we are unable to figure out the output. Here net 16 is the reference voltage of 800m, net 14is a sine wave with 1MHz and 500m amplitude, we should be getting five (101) but herewe are unable to detect but if we check the voltage levels, we are be getting 101.Here a isthe MSB bit and c is the LSB bit.

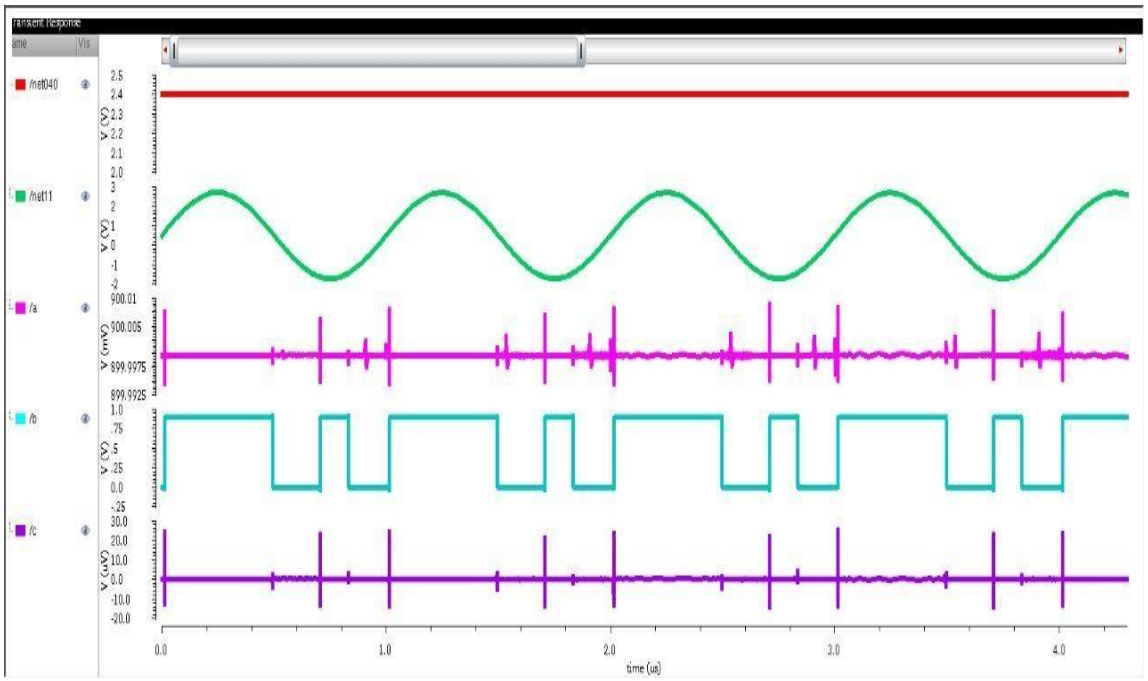

Figure 5.1.5(d): 3-bit flash ADC simulation using FinFET for 22nm technology

Table 3: Code transitions for Flash ADC

Vin	code	a b c
0<vin≤0.3	0000000	000
0.3<vin≤0.6	0000001	001
0.6<vin≤0.9	0000011	010
0.9<vin≤1.2	0000111	011
1.2<vin≤1.5	0001111	100
1.5<vin≤1.8	0011111	101
1.8<vin≤2.1	0111111	110
2.1<vin	1111111	111

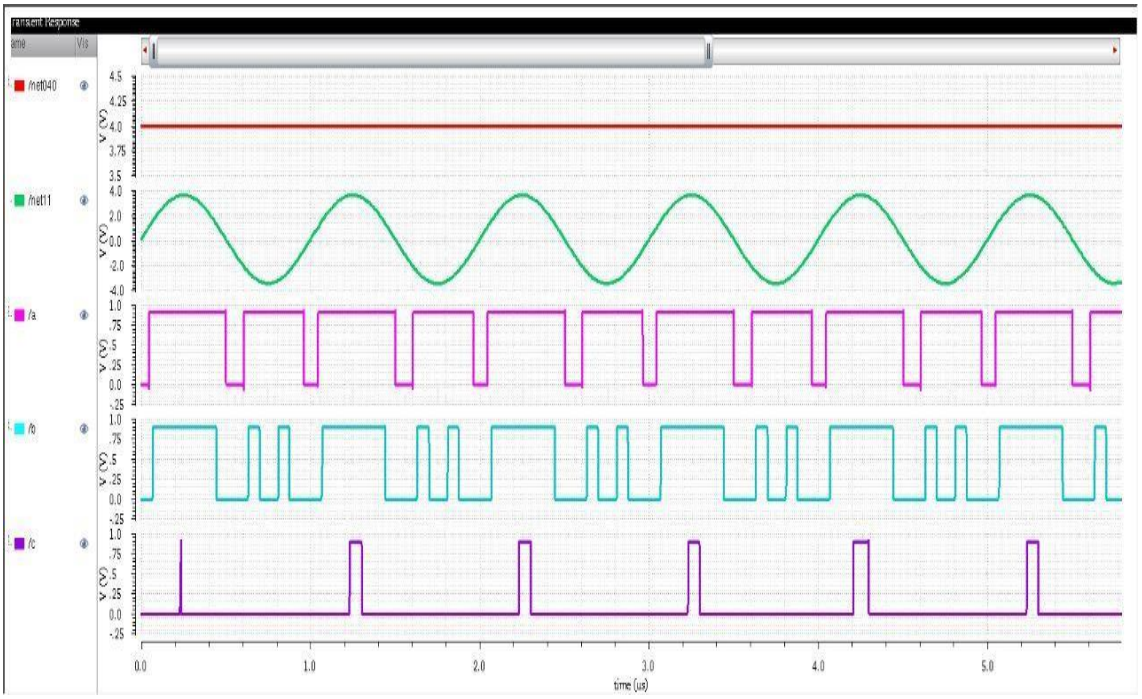

Figure 5.1.5(e): 3-bit flash ADC simulation using FinFET for 22nm technology

Table 4: Code transitions for Flash ADC

Vin	code	a b c
0<vin≤0.5	0000000	000
0.5<vin≤1	0000001	001
1<vin≤1.5	0000011	010
1.5<vin≤2	0000111	011
2<vin≤2.5	0001111	100
2.5<vin≤3	0011111	101
3<vin≤3.5	0111111	110
3.5<vin	1111111	111

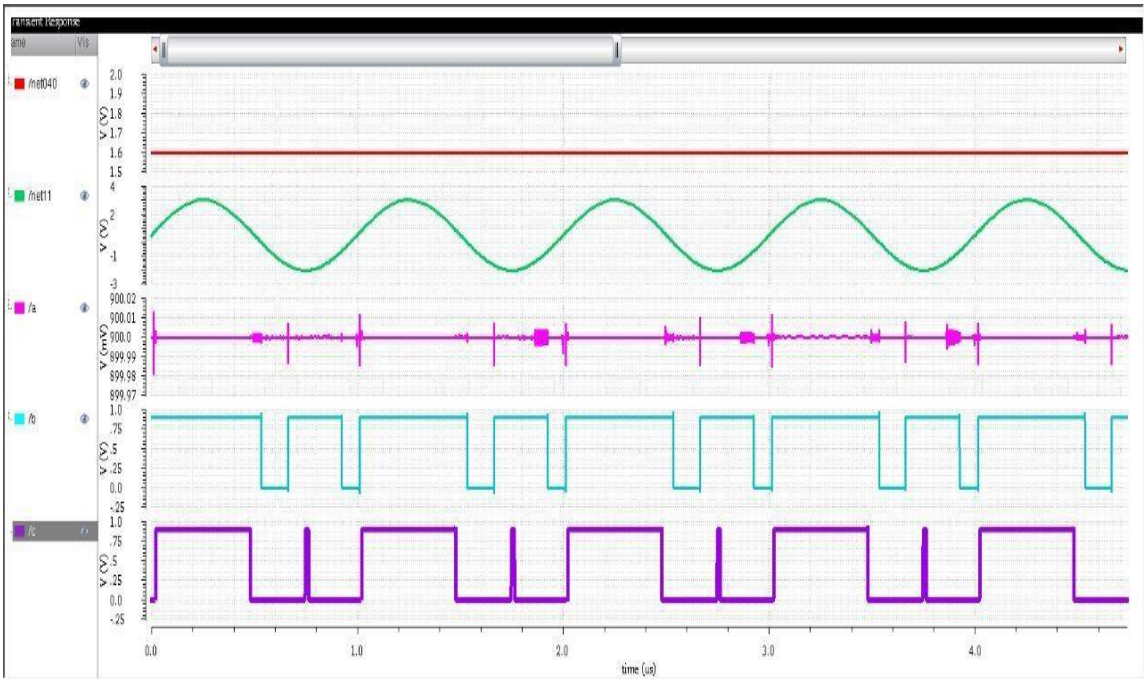

Figure 5.1.5(f): 3-bit flash ADC simulation using FinFET for 22nm technology

Table 5: Code transitions for Flash ADC

Vin	code	a b c
0<vin≤0.2	0000000	000
0.2<vin≤0.4	0000001	001
0.4<vin≤0.6	0000011	010
0.6<vin≤1.8	0000111	011
0.8<vin≤1	0001111	100
1.0<vin≤1.2	0011111	101
1.2<vin≤1.4	0111111	110
1.4<vin	1111111	111

The above figures 5.1.5(d), (e) and (f) illustrates the simulated results for FinFET for 22nm technology. The 3 graph represents the analog to digital conversion voltage graphs. Theortical and graphical values were verified. The theortical values have been tabulated,there are some distortions in the graphs, when the input voltage changes from positive tonegative cycles or vice versa. The three bit digital output is obtained where A is the MSBand C is the LSB.

5.1.1. D Flip-Flop

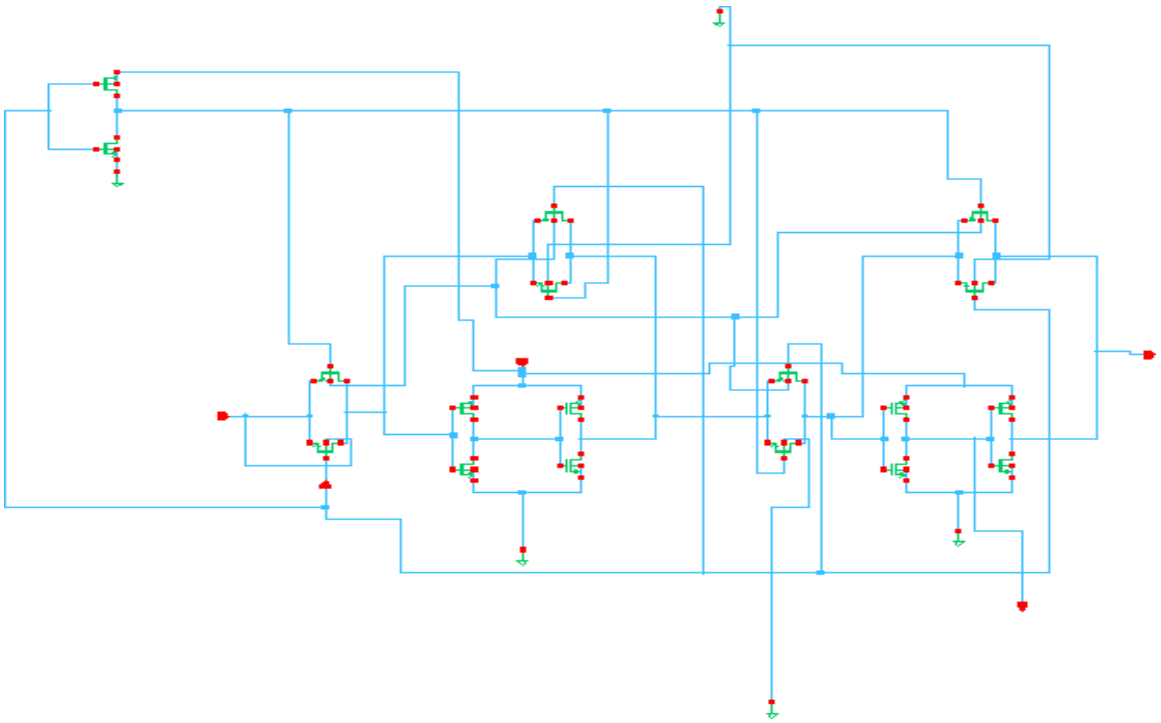

Figure 5.1.6(a): D Flip-Flop

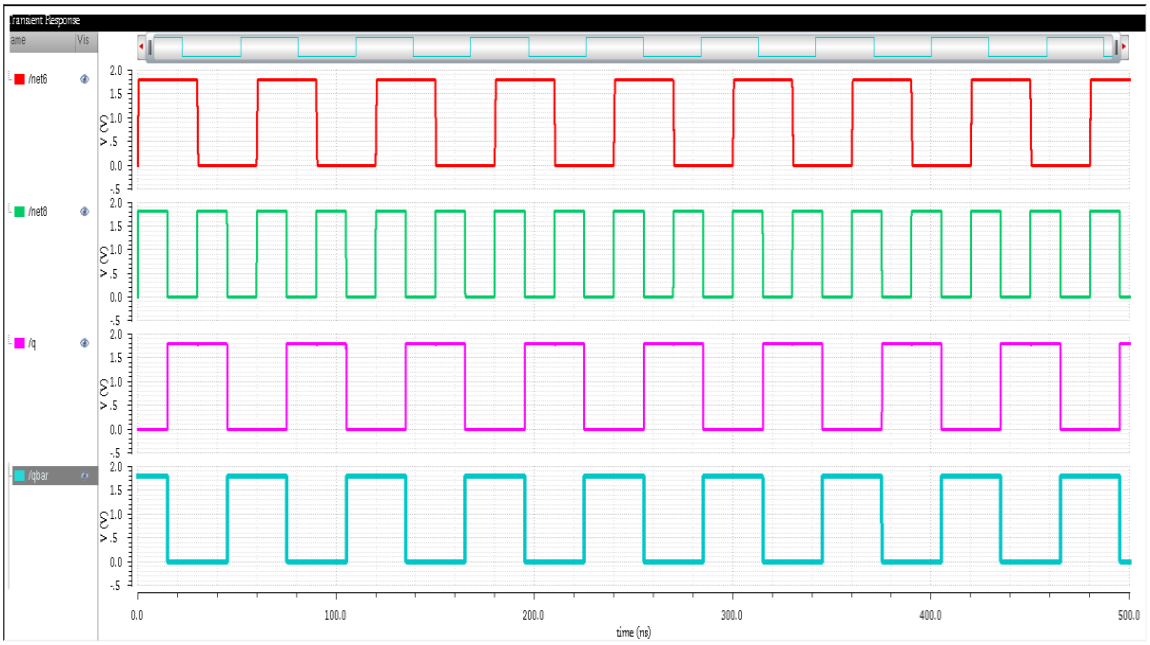

Figure 5.1.6(b): D Flip-Flop simulation using CMOS for 22nm technology

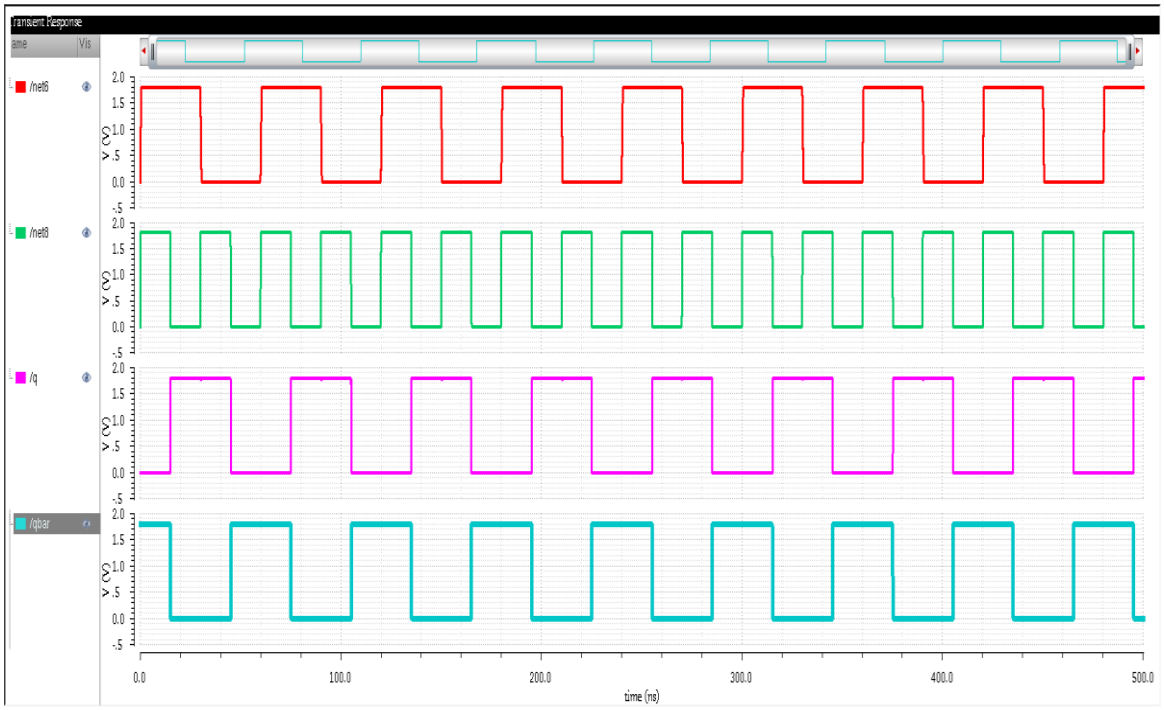

Figure 5.1.6(c): D Flip-Flop simulation using FinFET for 22nm technology

The above figure 5.1.6(a) illustrates design of D-flipflop circuit and figures 5.1.6(b) and 5.1.6(c) illustrates the simulated results for CMOS and FinFET for 22nm technology.

This is Master Slave D flop-flop with a transmission gate where clock and D are input, thisis a negative edge D flip-flop. Clock is sent to an inverter and clock-bar is taken from the inverter and fed to the transmission gate.

The Net 6 is in red color is input D with vpulse of 1.8v and time period of 60ns and pulsewidth of 30ns. The Net 8 is in green color is a clock with vpulse of 1.8v, time period 30ns, pulse width 15ns. Q and Qbar are the output of D flip-flop, at every negative edge of clock the output triggers as per the input. Q and Qbar are complementary to each other.

5.1.2. Johnson Counter

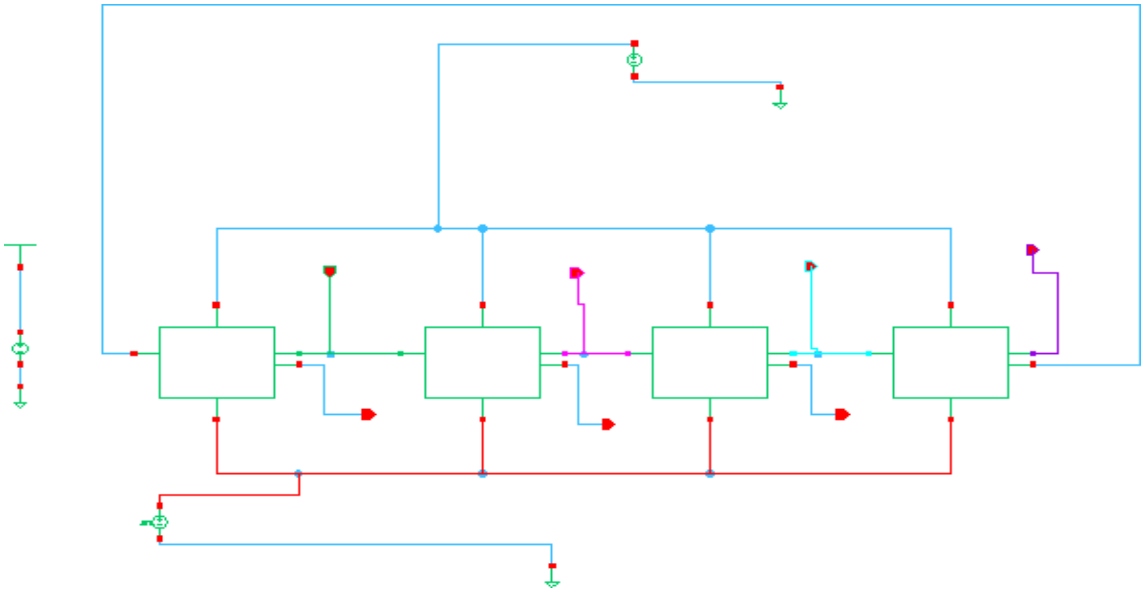

Figure 5.1.7(a): Johnson Counter

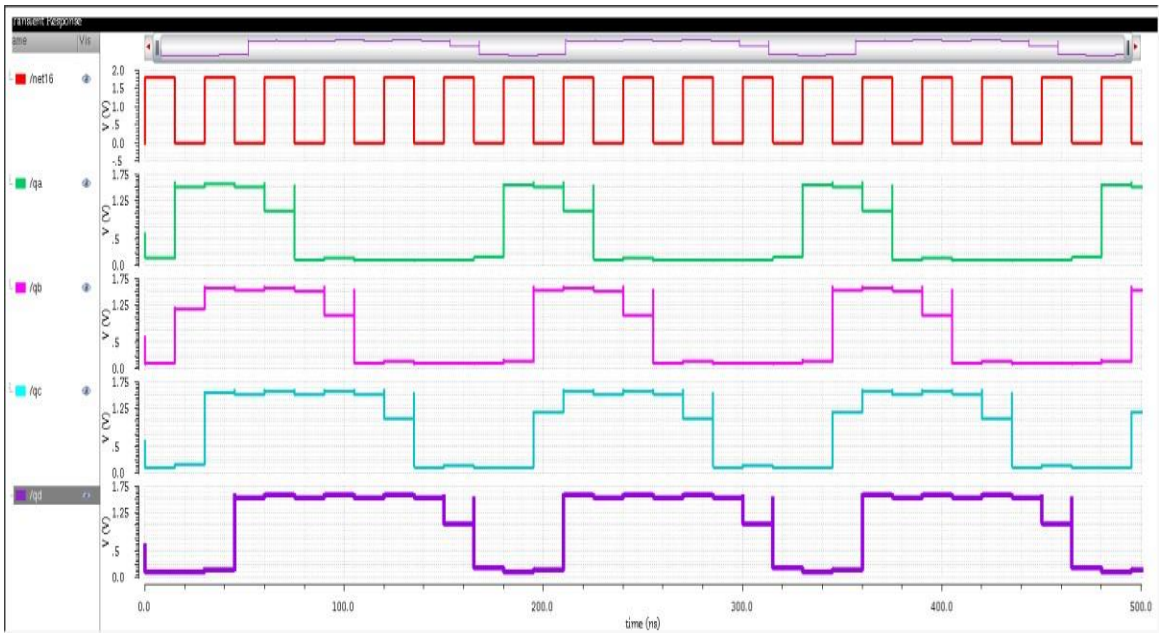

Figure 5.1.7(b): Johnson Counter simulation using CMOS for 22nm technology

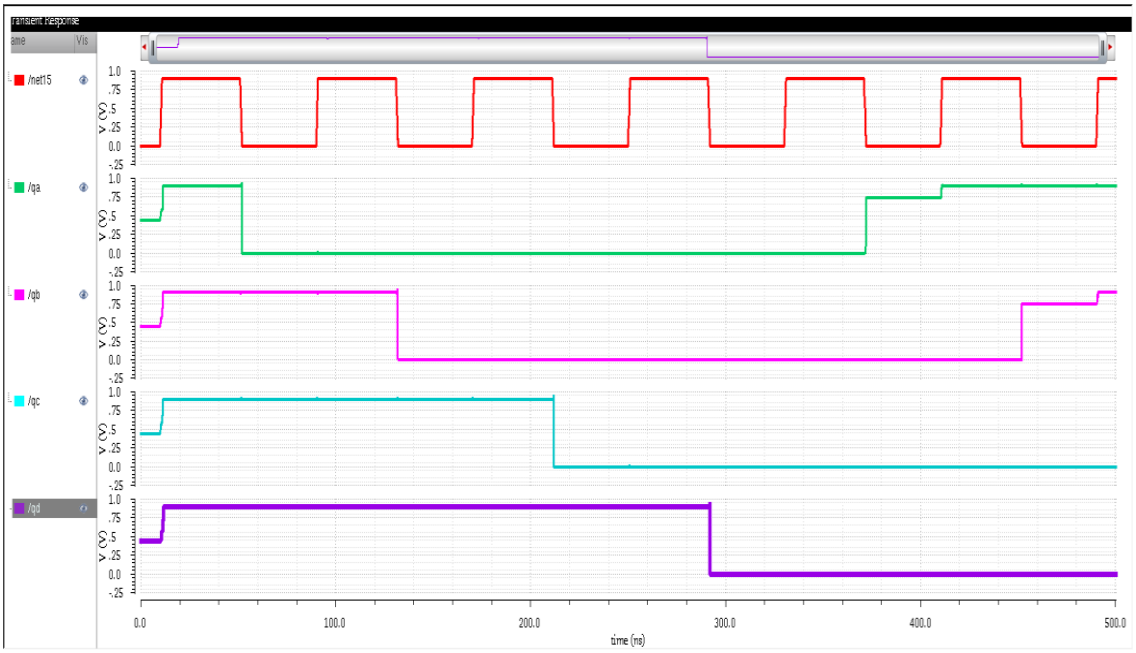

Figure 5.1.7(c): Johnson Counter simulation using FinFET for 22nm technology

The above figure 5.1.7(a) illustrates design of Johnson counter circuit and figures 5.1.7(b)and 5.1.7(c) illustrates the simulated results for CMOS and FinFET for 22nm technology.It is a cascade of four D flip-flops in series, the complementary output of forth flip-flop isfeedback to input of the first flip-flop. The output seen as a ring like structure. From thefigures 5.1.7(b) and (c) we can see that the CMOS has more distortions compare to FinFET.There are some glitches in output due to propagation delay, rise time and fall time etc. wetried to overcome using buffer but we did not see any changes in the glitches.

For performance evaluations of the CMOS and FinFET are evaluated by considering someparameters like delay, average power, area, leakage power, etc.

Figure of Merit: The figure of merit is the ratio of power and speed; Speed of the circuit is1/delay. So, figure of merit is power x speed consumed. Units is joule/ conversion rate. The lesser the figure of merit the greater is the performance.

Delay: This refers to the time it takes for a signal to travel from the input of a logic gate toits output.

Power: power refers to the power dissipated by a circuit even when it is not switching. Itis caused by the leakage currents that flow through the transistors, especially in the off state.

Area: calculations of area can be done by number of transistors used x length of transistor x width of transistor. But it is difficult to compare the area of both FinFET and CMOS. Because FinFET have more than one gate.

Table 6: Results of Johnson Counter

Parameter	**FinFET**	**CMOS**
Delay (S)	751.7 p	45.13 n
Power (avg)	38.90 uw	40.04 mw
Figure of merit	0.29 f J/conversion rate	1.8 f J/conversion rate

For the Johnson counter the delay is calculated between the clock and output of the fourthD flip-flop and we observed that for finFET delay is lesser than when compared to CMOSthat is 751.7 ps for FinFET and 45.13 ns for CMOS. Power consumption is also observed and we see that the FinFETs consumed less power compared to CMOS that is 38.90uw forfinFET and 40.04mw.

Table 7: Results of 3-Bit Flash ADC

Parameter	**FinFET**	**CMOS**
Delay (S)	17.21n	367.7 n
Power (avg)	5.569 mw	12.82 mw
Figure of merit	0.095 f J/conversion rate	4.7 f J/conversion rate

For the 3-Bit Flash ADC the delay is calculated between the vin and MSB of the output and we observed that for finFET delay is lesser than when compared to CMOS that is 17.21ns for FinFET and 376.7ns for CMOS. Power consumption is also observed and we see that the FinFETs consumed less power compared to CMOS that is 5.569mw for finFETand 12.82mw

Chapter 6

Applications, Advantages, And Limitations

6.1 Applications

A 3-bit flash ADC (Analog-to-Digital Converter) is a type of ADC that converts an analog input voltage into a digital representation using a resistor ladder network and a set of comparators. The output of the ADC is a 3-bit binary code that represents the input voltage within a specific range. Here are some common applications of 3-bit flash ADCs:

- Audio Processing: 3-bit flash ADCs can be used in audio applications where moderate resolution is sufficient, such as low-cost audio devices, voice recorders, or simple sound effect processors. The ADC can convert analog audio signals intodigital form for further processing or storage.
- Sensor Interfaces: Many sensors, such as temperature sensors, pressure sensors, or light sensors, provide analog output signals that need to be converted into a digital format for processing by a microcontroller or a digital system. A 3-bit flash ADC can be used to digitize the sensor outputs, providing a simple and cost-effective solution for basic sensing applications.
- Industrial Control Systems: In industrial control systems, analog signals from sensors or process variables often need to be converted into digital form for monitoring, control, and automation purposes. A 3-bit flash ADC can be employedto convert these analog signals into digital values, which can then be processed bya programmable logic controller (PLC) or a supervisory control and data acquisition (SCADA) system.
- Digital Communications: In certain digital communication systems, a 3-bit flash ADC can be used to sample analog signals and convert them into digital codes forfurther modulation or demodulation processes. For example, in some types of frequency-shift keying (FSK) or phase-shift keying (PSK) modulation schemes, a 3-bit ADC can be utilized to convert the analog signal into discrete digital symbols.

A Johnson counter, also known as a twisted ring counter, is a type of sequential circuit that has several applications in digital electronics. It is formed by connecting a ring of flip-flops in a particular feedback configuration. Here are some common applications of Johnson counters:

- Frequency Division: Johnson counters can be used as frequency dividers. By properly selecting the number of stages in the counter, you can divide the input clock frequency by 2^n, where n is the number of stages. This feature is useful inapplications where you need to generate lower-frequency clock signals for timingpurposes.
- Sequence Generation: Johnson counters can generate unique, non-repeating sequences of digital states. By observing the output of the counter, you can obtaina sequence of binary patterns that can be used in applications such as pattern recognition, code generation, or control signal generation.
- Time Multiplexing: Johnson counters can be used for time multiplexing, where a single resource is shared among multiple components or tasks. By using the outputs of the counter to enable or disable different components or tasks in a timed sequence, you can efficiently utilize a shared resource without conflicts.
- Error Detection: Johnson counters can be employed for error detection purposes.By comparing the output sequence of the counter with an expected pattern, you can identify errors or discrepancies in the system. This technique is used in errordetection codes, such as the Hamming code, for identifying and correcting errorsin data transmission or storage.
- Frequency Synthesis: Johnson counters can be part of frequency synthesis circuits. By using the counter outputs as inputs to a digital-to-analog converter (DAC) andfiltering the resulting waveform, you can generate analog signals with specific frequencies. This technique is used in applications such as frequency modulation(FM) synthesis in music synthesis systems.

- Random Number Generation: The unique sequence generated by a Johnson

counter can be used to generate pseudo-random numbers. By sampling the counter outputs at specific time intervals, you can obtain a sequence of binary digits that exhibit some statistical randomness. This technique finds applications in simulations, cryptography, and various randomization algorithms.

6.2 Advantages

FinFETs is a type of transistor design that offers several advantages over traditional planartransistor designs. Here are some of the key advantages of FinFETs technology.

- Improved Performance: FinFETs provides superior electrical performance compared to planar transistors. The three-dimensional fin structure allows for better control of the channel, resulting in improved on state current and leakage current. These leads to higher switching speeds and improved overall transistor performance.
- Low Power Consumption: FinFETs have an ability to operate at lower supply voltage without compromising performance. By reducing the voltage, the power consumption can be significantly reduced. This makes FinFETs more energyefficient, which is especially important in portable device which battery life is concern.
- Reduced Leakage Current: One of the major advantages of FinFET technology is its ability to efficiently control leakage current. Leakage current refers to the unwanted current that flows through a transistor when it is supposed to be turnedoff. FinFETs have a better ability to suppress leakage due to the multiple gate control provides by the fin structure, resulting in lower standby power consumption.
- Scalability: FinFETs offers better scalability compared to planar transistor. As transistor dimensions continue to shrink, planar transistor face challenges in maintaining control over the channel and leakage current. FinFETs, on the

other hand, have a more robust structure that allows for improved control a

transistorsizes decreases. This scalability enables the continued advancement semiconductor technology.

- Better Electrostatic control: The three-dimensional fin structure of FinFETs provides enhanced electrostatic control over the channel. This allows for better suppression for short channel effect, such as drain induced barrier lowering and subthreshold slope degradation, which can negatively impact the transistorsperformance.
- FinFET technology offers significant advantages in term of performance, leakagecontrol, scalability, and integration density. These benefits have made FinFETs a preferred choice for advanced semiconductor designs, enabling the developmentof more powerful and energy-efficient electronic devices.

6.3 Limitations

FinFET technology provides numerous advantages, it also has some limitations and challenges.

- Manufacturing Complexity: FinFETs have a more complex manufacturing process compared to planar transistor. The fabrication of the fin structure requires additional steps, such as fin patterning and etching, which adds complexity and cost to the manufacturing process.
- Increased Process Variability: FinFETs are more sensitive to process variations and parameters fluctuations compared to planar transistors. The complex manufacturing process of FinFETs can result in variations in devices dimensions,doping profiles, and electrical characteristics. This variation can impact circuit performances, power consumption.
- New Design Rules: FinFET technology introduces new design rules and guidelinesthat differs from those of planar transistors. These rules include specific constraints related to the fin structure, spacing, gate overlap, and proximity effects.

- Power Supply and Noise challenges: The reduced voltage scaling potential of

FinFETs can be present challenges in power supply voltages, which results in thenoise margins and increased vulnerability to power supply fluctuations.

- Limited Supply Voltage Scaling: While FinFETs offers improved performance andpower consumption at lower supply voltage, there is a practical limit to how muchthe supply voltage can be scaled. At extremely low voltages, FinFETs face challenges such as increased variability, reduced reliability, which can limit the achievable voltage scaling.

Chapter 7

Conclusion

We have undertaken the design, simulation, and analysis of the fundamental circuits needed for a 3-bit Flash ADC, including an 8:3 Priority Encoder, a Common Source Amplifier, and a Differential Amplifier. Our focus has been on implementing these circuitsusing FinFET technology with a 22nm process.

In the initial phase, we designed the 8:3 Priority Encoder, which is responsible for encoding the input analog voltage into a corresponding binary code. By utilizing FinFET technology, we were able to leverage its advantages, such as improved performance, reduced power consumption, and better scalability. The FinFET implementation of the Priority Encoder demonstrated enhanced efficiency and reliability compared to thetraditional CMOS implementation.

Next, we moved on to the design of the Common Source Amplifier, which is crucial for signal amplification and conditioning in the Flash ADC. By employing FinFET technology, we achieved improved linearity, lower leakage current, and higher gain compared to CMOS counterparts. The simulation results revealed superior performance characteristics, validating the effectiveness of FinFET technology in this circuit.

Similarly, we designed and simulated the Differential Amplifier, which is responsible forcomparing and amplifying the differential signals in the Flash ADC. With FinFET technology, we harnessed its superior properties, such as enhanced carrier mobility, reduced short-channel effects, and improved noise performance. The FinFET implementation outperformed the CMOS design in terms of linearity, noise immunity, and power efficiency.

Throughout the design and simulation process, we paid special attention to the 22nm FinFET technology node. This advanced technology offers significant advantages in terms of performance, power, and area, making it well-suited for high-density integrated circuits.

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Conference on Circuit, Power and Intelligent System, 2023 : Submission (242) has been edited.

1 message

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To: bhanuprasadnayak1012@gmail.com

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Track Name: CCPIS2023

Paper ID: 242

Paper Title: Design of FinFET based Digital Logic Circuits

Abstract:
This paper presents a detailed comparative analysis of FinFET and CMOS technologies for digital logic circuits, with a specific focus on a 4-bit Johnson counter. While the common source (CS) amplifier, differential amplifier, and D flip-flop (DFF) circuits are simulated using schematic-level designs, the Johnson counter undergoes comprehensive performance evaluation. The study investigates the impact of FinFET technology on the speed, power efficiency, and robustness of the Johnson counter, employing both FinFET and CMOS implementations in a 22nm process node. Through extensive simulations using Cadence tools, the results highlight the potential advantages of FinFET transistors in counter operations and provide valuable insights for future digital circuit designs.

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Authors:
- indureddy7755@gmail.com (Primary)
- bhanuprasadnayak1012@gmail.com
- Pavanmgowdam155@gmail.com
- saigautham1202@gmail.com

Primary Subject Area: Microelectronics Circuit & System design

Secondary Subject Areas: Not Entered
Submission Files: S02-IEEE_PAPER_FINAL.docx (293 Kb, Sat, 10 Jun 2023 15:26:36 GMT)

Submission Questions Response: Not Entered

Thanks,
CMT team.

Design of FinFET based Digital Logic Circuits

Dr. Dinesha P
Department of ECE,
Dayananda Sagar College of Engineering Bengaluru India

Bhanu Prasad Nayak
Department of ECE,
Dayananda Sagar College of Engineering Bengaluru India

Chinnappa Reddy gari Indu
Department of ECE,
Dayananda Sagar College of Engineering Bengaluru India

Pavan M
Department of ECE,
Dayananda Sagar College of Engineering Bengaluru India

Thota Sai Gautham
Department of ECE,
Dayananda Sagar College of Engineering Bengaluru India

***Abstract*— This paper presents a detailed comparative analysis of FinFET and CMOS technologies for digital logic circuits, with a specific focus on a 4-bit Johnson counter. While the common source (CS) amplifier, differential amplifier, and D flip-flop (DFF) circuits are simulated using schematic-level designs, the Johnson counter undergoes comprehensive performance evaluation. The study investigates the impact of FinFET technology on the speed, power efficiency, and robustness of the Johnson counter, employing both FinFET and CMOS implementations in a 22nm process node. Through extensive simulations using Cadence tools, the results highlight the potential advantages of FinFET transistors in counter operations and provide valuable insights for future digital circuit designs.**

Keywords— FinFET, 22nm technology, Common Source Amplifier, Differential Amplifier, Johnson-counter, power efficiency, performance evaluation

I. INTRODUCTION

As semiconductor technology continues to advance, the exploration of FinFET transistors has garnered significant interest due to their improved performance characteristics. This study focuses on the evaluation of FinFET technology specifically in the design of a 4-bit Johnson counter, while schematic-level simulations are employed for the common source (CS) amplifier, differential amplifier, and D flip-flop (DFF) circuits.

The primary objective of this research is to analyse and compare the performance of the Johnson counter implemented using FinFET and CMOS technologies in a 22nm process node. Key performance metrics, such as speed, power efficiency, and robustness, are assessed to investigate the potential benefits of utilizing FinFET transistors in counter operations.

Through comprehensive simulations using Cadence tools, the impact of FinFET technology on the speed of the Johnson counter is evaluated. Power efficiency measurements provide insights into the advantages offered by FinFET transistors in terms of reducing power consumption. Additionally, robustness analysis is performed to determine the capability of FinFET-based Johnson counters to withstand metastability and maintain reliable operation.

By focusing on the Johnson counter as a case study, this research provides a deeper understanding of the performance enhancements achievable through the adoption of FinFET technology. The findings contribute valuable insights into the selection and optimization of transistor technologies for future digital circuit designs, aiding in the development of efficient and robust digital systems.

Through extensive simulation and analysis using Cadence tools, we aim to provide valuable insights into the performance enhancements and design considerations specific to FinFET-based digital circuits at the 22nm technology node. The findings from this study can contribute to the advancement of integrated circuit design and further optimize the utilization of FinFET technology in digital systems.

II. RELATED WORK

1) Vasudeva, G., & Uma, B. V. (2021). "22nm FINFET Based High Gain Wide Band Differential Amplifier." International Journal of Circuits, Systems and Signal Processing. This reference study presents a comprehensive investigation into the design and evaluation of a high gain wide band differential amplifier using 22nm FinFET technology. The study explores the advantages of FinFET transistors in achieving high gain and wide bandwidth in differential amplifiers. The findings provide insights into the design considerations, circuit optimization techniques, and performance evaluation of the differential amplifier, which can serve as a valuable reference for your work.
2) Shivali, & Shobha Sharma, A., & Amita Dev. (2019). "Analysis of Various Master-Slave Configuration based D Flip-Flops." International Journal of Recent Technology and Engineering. This reference study provides an analysis of various master-slave configuration-based D flip-flop (DFF) models. It offers a comprehensive review of earlier proposed DFF designs based on the master-slave configuration. Although the focus is not specifically on FinFET technology, the study explores the design considerations and performance characteristics of

DFFs. The insights gained from this study can aid in adapting and optimizing DFF designs for FinFET-based implementation.

3) S. Greeshma sai, N., Alivelu Manga, N., & P. Chandra Sekhar. (2020). "Design and Simulation of FinFET based digital circuits for low power applications." This reference study focuses on the design and simulation of FinFET-based digital circuits for low power applications. It investigates the power dissipation characteristics of FinFET technology compared to CMOS in the design and simulation of a Johnson ring counter. The study demonstrates the advantages of FinFET transistors in reducing power consumption, which can be relevant to work as consider low power requirements.

4) Rajuhajare, Dr.C. Lakshmi Narayana, Sunil.C, Sumanth, Anish.A. (2020). "Design and evaluation of FinFET based digital circuits for high-speed ICs." This reference study delves into the design and evaluation of FinFET-based digital circuits for high-speed integrated circuits (ICs). It explores the considerations and techniques involved in leveraging FinFET technology to achieve high-speed performance in digital circuits. The study covers aspects such as circuit design, layout optimization, and performance evaluation, which can provide valuable insights for your work in designing high-speed digital circuits using FinFET technology.

III. Design and Simulation

common source amplifier Design

In a common source (CS) amplifier, an input signal is applied to the gate terminal of a field-effect transistor (FET), while the source terminal is connected to a reference voltage. The amplified output voltage is obtained across a resistor connected to the drain terminal, forming the load. The purpose of the CS amplifier is to amplify an analog signal. When an AC signal is applied to the amplifier, it modulates the current flowing through the FET channel, resulting in a voltage variation at the drain terminal. This voltage variation represents the amplified output signal of the CS amplifier.

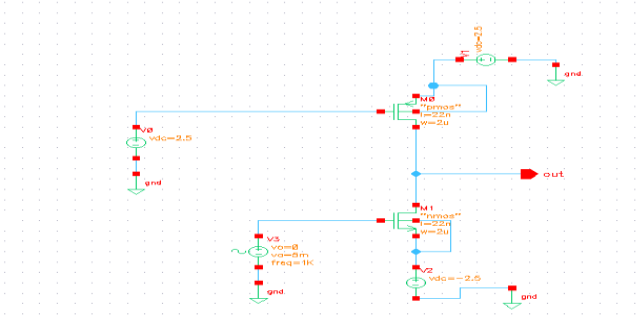


Figure 1 : Common source amplifier schematic

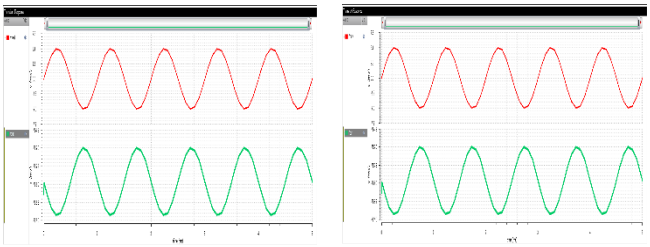


Figure 2: Common source amplifier simulation using
a) CMOS for 22nm b) FinFET for 22nm technology

A common-source amplifier is one of three basic single-stage field-effect transistor (FET) amplifier topologies, typically used as a voltage or transconductance amplifier. The easiest way to tell if a FET is common source, common drain, or common gate is to examine where the signal enters and leaves. When the input signal is applied at the gate terminal and source terminal, then the output voltage is amplified and obtained across the resistor at the load in the drain terminal. This is called a common source amplifier. Here source acts as a common terminal between the input and output. It is also known as a voltage amplifier or a transconductance amplifier. It produces current gain and voltage gain according to the input impedance and output impedance.

Differential amplifier Design

A differential amplifier is an electronic amplifier designed to amplify the voltage difference between two input signals while rejecting any common voltage that is present in both inputs. The output of the CMOS differential amplifier is taken from the differential output node, which provides a differential voltage output. The differential voltage amplification is achieved through the interaction between the input transistors and the biasing circuitry, which establishes the operating point and facilitates amplification of the input signal.

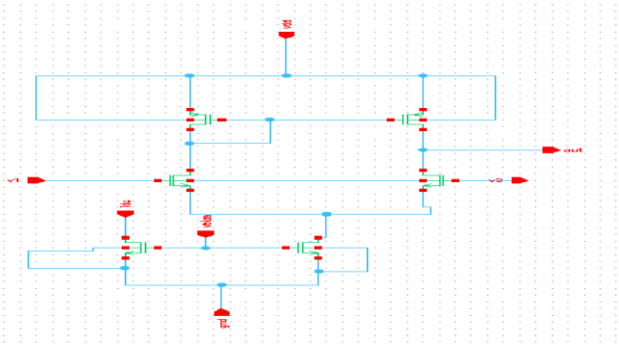
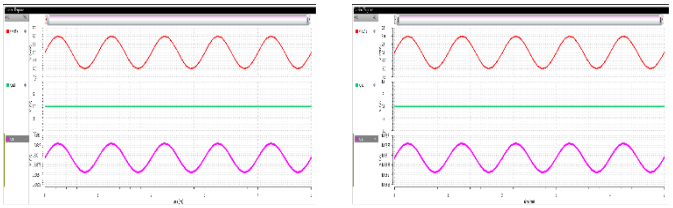


Figure 3: Differential Amplifier schematic



a) b)

Figure 4: Differential amplifier simulation using

a) CMOS for 22nm b) FinFET for 22nm technology

D Flip-Flop Design

A master-slave configuration-based D flip-flop (DFF) consists of two stages: the master stage and the slave stage. In the master stage, a latch circuit captures the input data on the rising edge of the clock signal. The slave stage, connected to the master stage, holds the captured data, and produces a stable output synchronized with the clock transitions. This configuration ensures proper data synchronization and stable output generation in the DFF.

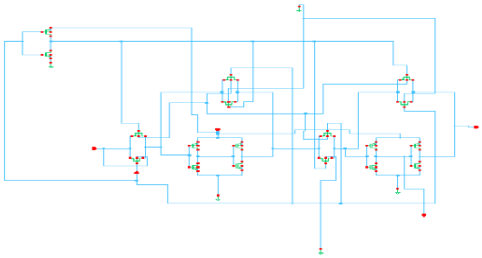
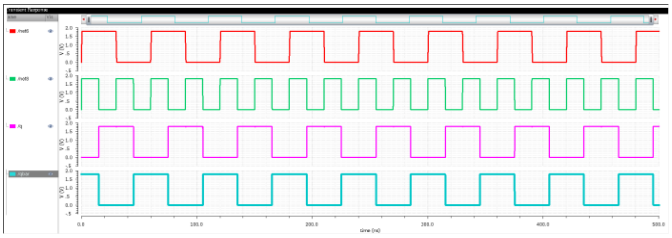


Figure 5: D Flip-Flop schematic



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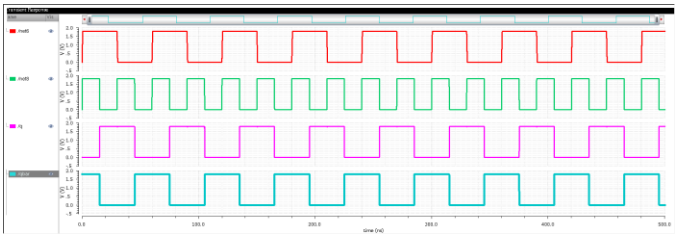


b)

Figure 6: D Flip-Flop simulation using

a) CMOS for 22nm b) FinFET for 22nm technology.

D Flip-Flop Design

In a 4-bit Johnson counter formed by cascading four D flip-flops (DFFs), the complemented output ($\bar{Q}$) of the last DFF is given feedback to the input of the first flip-flop. This connection completes the feedback loop and allows the counter to generate a cyclic sequence of unique binary states. The feedback from the complemented output helps in creating the desired cyclic pattern of the Johnson counter.

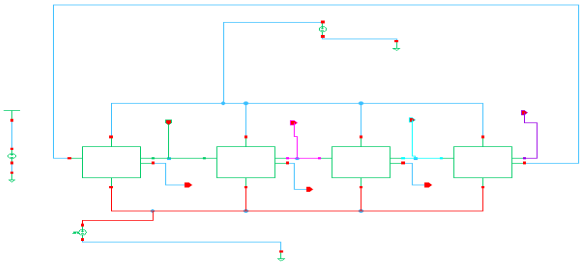
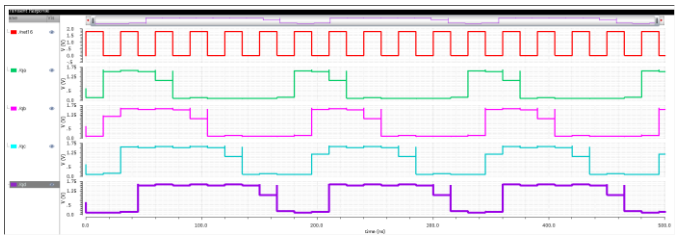


Figure 7: Johnson Counter schematic



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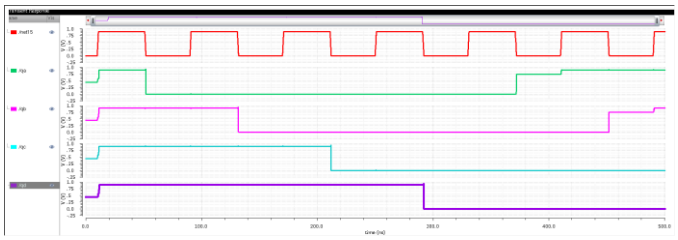

b)

Figure 8: Johnson Counter simulation using

a) CMOS for 22nm b) FinFET for 22nm technology.

Figure 1 : Block-diagram of the proposed methodology

When comparing a 4-bit Johnson counter implemented in CMOS and FinFET technology at the 22nm node, FinFET technology offers advantages in terms of delay, power consumption. FinFET transistors provide faster switching speeds, lower power consumption, and improved transistor density, resulting in reduced delay, lower power requirements.

4-bit Johnson Counter		
	finFET	**CMOS**
Delay(sec)	715 p	45.13 n
Power(avg)(w)	38.90 u	40.04 m
Figure Matrix	0.2f j/convert rate	1.8f j/convert rate

Table 1: Comparison of 4-bit Johnson Counter parameters in finFET and CMOS (22nm technology)

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[9] Rajuhajare, Dr.C. Lakshmi Narayana, Sunil.C, Sumanth, Anish.A. "Design and evaluation of Fin-FET based digital circuits for high-speed ICs."

CO-PO Mapping Justification Sheets

Project Title		Design of FinFET based Combinational and Sequential circuits
PO↓	Levels 3/2/1	Justification
PO1	3	Applied the knowledge of engineering fundamentals in determining the FinFET and CMOS technology and designing the FinFET and CMOS based combinationaland sequential circuits.
PO2	3	Analyzed and consolidated previous research on FinFET based circuits.
PO3	3	Designing the sequential and combinational circuits by using FinFET technology and compare it with the CMOS technology.
PO4	3	Comparison between CMOS and FinFET is done based on parameter like powerdissipation, area, delay and conclude FinFET is efficient than CMOS for nano-scaling IC's.
PO5	3	Cadence virtuoso software is used to design the schematic diagram of combinational and sequential circuits.
PO6	1	By designing schematic circuits based on FinFET technology the area used for Integrated Circuit is reduced.
PO7	2	FinFET based schematic circuits are developed to overcome parameters like power dissipation, delay, leakage current and area compared to CMOS.
PO8	3	All the software and libraries are open source and all the required information is cited thereby following the ethical principles
PO9	3	Functioned effectively as a team by sharing the work, ideas, and plan.
PO10	3	Held regular meetings to discuss our project, improved communication skills my making presentation and report periodically for each phase.
PO11	2	Our project is based on software so, did not invested large amount on our project.
PO12	2	The project is useful in understanding the concepts better for current learning.

PSO 1	2	Schematic Circuits are designed by using MOS transistor. The circuit is initially. designed by using FinFET and CMOS technology.
PSO 2	3	Applied knowledge of schematic design in terms of software and improved the knowledge of cadence virtuoso software and FinFET technology.

CO-PO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	POS1	POS2
CO1	3	2	2	2	2	1	1	2	1	1	1	3	2	3
CO2	2	3	2	2	1	1	1	3	-	1	1	3	1	2
CO3	2	2	3	2	2	1	2	3	-	1	1	3	2	2
CO4	2	2	2	1	3	1	1	2	1	1	-	2	3	2
CO5	2	2	2	2	1	3	2	3	2	1	-	3	1	1
CO6	1	1	1	1	1	1	1	3	1	-	-	-	-	-
CO AVG	2	2	2	1.6	1.6	1.3	1.3	2.6	0.8	0.8	0.5	2.3	1.3	1.5

Justification

CO1	We thoroughly understand the concepts related to our project like Flash ADC, Johnson Ring Counter.
CO2	We proposed to design circuits in FinFET to overcome Short Channel Effects in CMOS circuits.
CO3	Design and simulation of FinFET based circuits like Priority Encoder, Common Source Amplifier and Differential Amplifier for developing 3-bit Flash ADC circuit.
CO4	Design and simulation of FinFET based circuit like D Flip-Flop for developing Johnson Ring Counter circuit
CO5	We provided sustainable solutions considering societal needs by exhibiting individual and cooperating learning
CO6	We completed the stipulated work in the time span assigned to us.

Budget Estimation Sheets

Sl. No.	Particulars	Estimated Cost in Rs.
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2	Miscellaneous	1000

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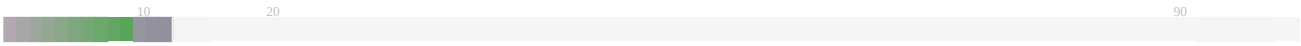

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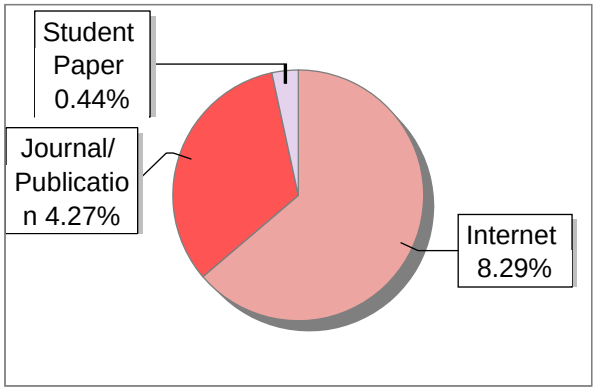

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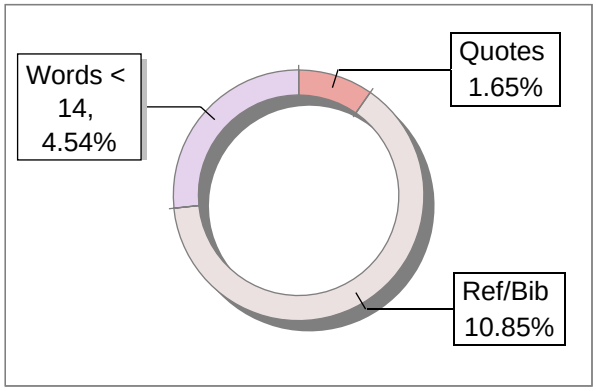

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