SSRG International Journal of VLSI & Signal Processing
ISSN: 2394-2584/ https://doi.org/10.14445/23942584/IJVSP-VXXXX
Volume X Issue X, 1-4, Month 2023

Review Article

Design of FinFET based Digital Logic Circuits

Bhanu Prasad Nayak[1], Chinnappa Reddy gari Indu[2], Thota Sai Gautham [3], Pavan M[4], Dinesha P[5]
[1,2,3,4,5] *Department of Electronics and Communication Engineering, Dayananda Sagar College of Engineering, Karnataka*

Received: Revised: Accepted: Published:

Abstract - *This paper presents a detailed comparative analysis of FinFET and CMOS technologies for digital logic circuits, with a specific focus on a 4-bit Johnson counter. While the common source (CS) amplifier, differential amplifier, and D flip-flop (DFF) circuits are simulated using schematic-level designs, the Johnson counter undergoes comprehensive performance evaluation. The study investigates the impact of FinFET technology on the speed, power efficiency, and robustness of the Johnson counter, employing both FinFET and CMOS implementations in a 22nm process node. Through extensive simulations using Cadence tools, the results highlight the potential advantages of FinFET transistors in counter operations and provide valuable insights for future digital circuit designs.*

Keywords - *FinFET, 22nm technology, Common Source Amplifier, Differential Amplifier, Johnson-counter, power efficiency, performance evaluation.*

1. Introduction

As semiconductor technology continues to advance, the exploration of FinFET transistors has garnered significant interest due to their improved performance characteristics. This study focuses on the evaluation of FinFET technology specifically in the design of a 4-bit Johnson counter, while schematic-level simulations are employed for the common source (CS) amplifier, differential amplifier, and D flip-flop (DFF) circuits.

The primary objective of this research is to analyse and compare the performance of the Johnson counter implemented using FinFET and CMOS technologies in a 22nm process node. Key performance metrics, such as speed, power efficiency, and robustness, are assessed to investigate the potential benefits of utilizing FinFET transistors in counter operations.

Through comprehensive simulations using Cadence tools, the impact of FinFET technology on the speed of the Johnson counter is evaluated. Power efficiency measurements provide insights into the advantages offered by FinFET transistors in terms of reducing power consumption. Additionally, robustness analysis is performed to determine the capability of FinFET-based Johnson counters to withstand metastability and maintain reliable operation.

By focusing on the Johnson counter as a case study, this research provides a deeper understanding of the performance enhancements achievable through the adoption of FinFET technology. The findings contribute valuable insights into the selection and optimization of transistor technologies for future digital circuit designs, aiding in the development of efficient and robust digital systems.

Through extensive simulation and analysis using Cadence tools, we aim to provide valuable insights into the performance enhancements and design considerations specific to FinFET-based digital circuits at the 22nm technology node. The findings from this study can contribute to the advancement of integrated circuit design and further optimize the utilization of FinFET technology in digital systems.

2. Reference Study

Vasudeva, G., & Uma, B. V. (2021). "22nm FINFET Based High Gain Wide Band Differential Amplifier." International Journal of Circuits, Systems and Signal Processing. This reference study presents a comprehensive investigation into the design and evaluation of a high gain wide band differential amplifier using 22nm FinFET technology. The study explores the advantages of FinFET transistors in achieving high gain and wide bandwidth in differential amplifiers. The findings provide insights into the design considerations, circuit optimization techniques, and performance evaluation of the differential amplifier, which can serve as a valuable reference for your work.

Shivali, & Shobha Sharma, A., & Amita Dev. (2019). "Analysis of Various Master-Slave Configuration based D Flip-Flops." International Journal of Recent Technology and Engineering. This reference study provides an analysis of various master-slave configuration-based D flip-flop (DFF) models. It offers a comprehensive review of earlier proposed DFF designs based on the master-slave configuration. Although the focus is not specifically on FinFET technology, the study explores the design considerations and performance characteristics of DFFs. The insights gained from this study can aid in adapting and optimizing DFF designs for FinFET-based implementation.

S. Greeshma sai, N., Alivelu Manga, N., & P. Chandra Sekhar. (2020). "Design and Simulation of FinFET based digital circuits for low power applications." This reference study focuses on the design and simulation of FinFET-based digital circuits for low power applications. It investigates the power dissipation characteristics of FinFET technology compared to CMOS in the design and simulation of a Johnson ring counter. The study demonstrates the advantages of FinFET transistors in reducing power consumption, which can be relevant to work as consider low power requirements.

Rajuhajare, Dr.C. Lakshmi Narayana, Sunil.C, Sumanth, Anish.A. (2020). "Design and evaluation of FinFET based digital circuits for high-speed ICs." This reference study delves into the design and evaluation of FinFET-based digital circuits for high-speed integrated circuits (ICs). It explores the considerations and techniques involved in leveraging FinFET technology to achieve high-speed performance in digital circuits. The study covers aspects such as circuit design, layout optimization, and performance evaluation, which can provide valuable insights for your work in designing high-speed digital circuits using FinFET technology.

*3.*Design and Simulation.

3.1 common source amplifier Design

In a common source (CS) amplifier, an input signal is applied to the gate terminal of a field-effect transistor (FET), while the source terminal is connected to a reference voltage. The amplified output voltage is obtained across a resistor connected to the drain terminal, forming the load. The purpose of the CS amplifier is to amplify an analog signal. When an AC signal is applied to the amplifier, it modulates the current flowing through the FET channel, resulting in a voltage variation at the drain terminal. This voltage variation represents the amplified output signal of the CS amplifier.

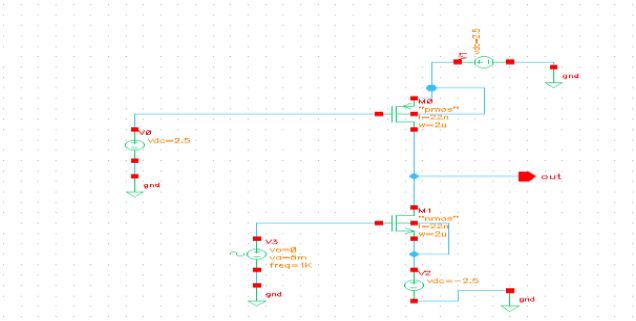
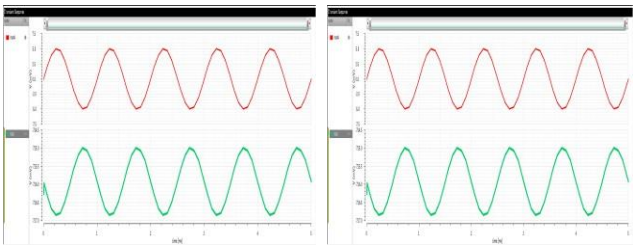


Figure 1 Common source amplifier schematic



a) **b)**

Figure 2 Common source amplifier simulation using a) CMOS for 22nm b) FinFET for 22nm technology.

A common-source amplifier is one of three basic single-stage field-effect transistor (FET) amplifier topologies, typically used as a voltage or transconductance amplifier. The easiest way to tell if a FET is common source, common drain, or common gate is to examine where the signal enters and leaves. When the input signal is applied at the gate terminal and source terminal, then the output voltage is amplified and obtained across the resistor at the load in the drain terminal. This is called a common source amplifier. Here source acts as a common terminal between the input and output. It is also known as a voltage amplifier or a transconductance amplifier. It produces current gain and voltage gain according to the input impedance and output impedance.

3.2 Differential amplifier Design

A differential amplifier is an electronic amplifier designed to amplify the voltage difference between two input signals while rejecting any common voltage that is present in both inputs. The output of the CMOS differential amplifier is taken from the differential output node, which provides a differential voltage output. The differential voltage amplification is achieved through the interaction between the input transistors and the biasing circuitry, which establishes the operating point and facilitates amplification of the input signal.

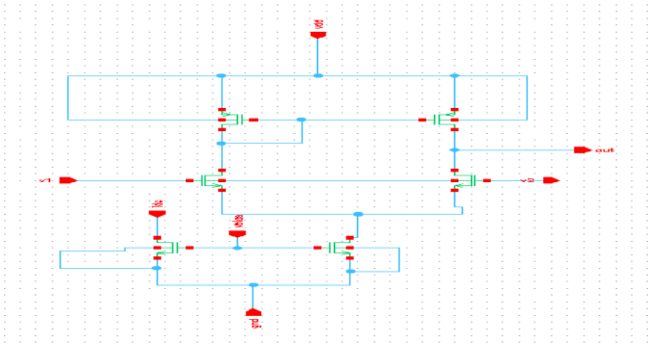
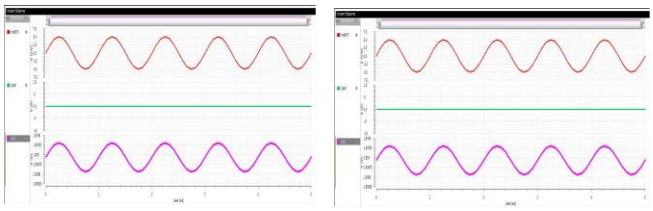


Figure 3 Differential Amplifier schematic



a) **b)**

Figure 4 Differential amplifier simulation using
a) CMOS for 22nm
b) FinFET for 22nm technology

3.3 D Flip-Flop Design

A master-slave configuration-based D flip-flop (DFF) consists of two stages: the master stage and the slave stage. In the master stage, a latch circuit captures the input data on the rising edge of the clock signal. The slave stage, connected to the master stage, holds the captured data, and produces a stable output synchronized with the clock transitions. This configuration ensures proper data synchronization and stable output generation in the DFF.

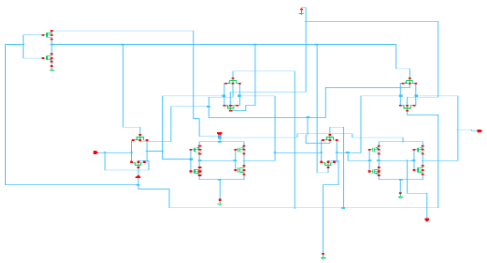
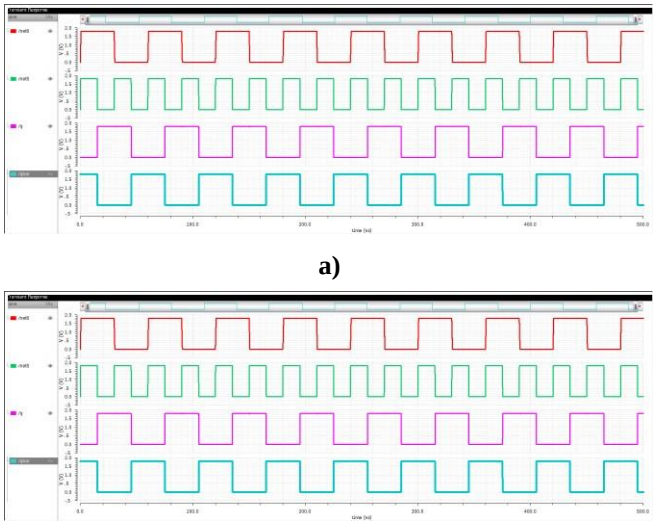


Figure 5 D Flip-Flop schematic



a)

b)

Figure 6 D Flip-Flop simulation using
a) CMOS for 22nm b) FinFET for 22nm technology.

3.4 4-bit Johnson Counter Design

In a 4-bit Johnson counter formed by cascading four D flip-flops (DFFs), the complemented output ($\overline{Q}$) of the last DFF is given feedback to the input of the first flip-flop. This connection completes the feedback loop and allows the counter to generate a cyclic sequence of unique binary states. The feedback from the complemented output helps in creating the desired cyclic pattern of the Johnson counter.

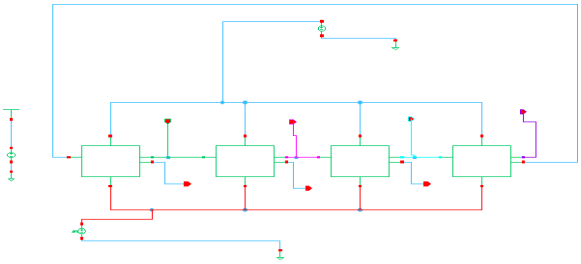
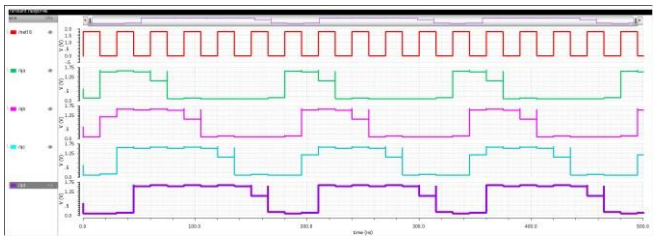
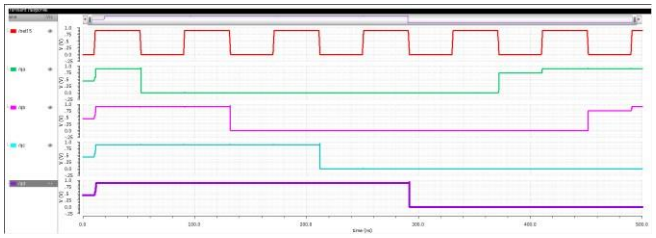


Figure 7 Johnson Counter schematic



a)



b)

Figure 8 Johnson Counter simulation using
a) CMOS for 22nm
b) FinFET for 22nm technology.

Table 1: Comparison of 4-bit Johnson Counter parameters in finFET and CMOS (22nm technology)

4-bit Johnson Counter		
	finFET	**CMOS**
Delay(sec)	715 p	45.13 n
Power(avg)(w)	38.90 u	40.04 m
Figure Matrix	0.2f j/convert rate	1.8f j/convert rate

When comparing a 4-bit Johnson counter implemented in CMOS and FinFET technology at the 22nm node, FinFET technology offers advantages in terms of delay, power consumption, and area. FinFET transistors provide faster switching speeds, lower power consumption, and improved transistor density, resulting in reduced delay, lower power requirements, and potentially smaller overall area for the Johnson counter.

References

[1] Mr. Tilak Kumar L, Chandan A, Chethankumar K M, Dommeti Venkata Sai Krishna Vasanth, Hemant, "Power Efficient 4 Bit Flash ADC Using Cadence Tool", International Research Journal of Engineering and Technology

[2] Nirali Hemant Patel "Power Efficient 4-bit Flash ADC using Cadence Virtuoso" International Journal of Engineering Research & Technology

[3] Vedura Appala Raju, B.V. R. Gowri "Johnson Counter Using Master Slave D Flip Flop" International Journal of Management, Technology and Engineering Volume 8,

[4] M Reddi Sekhar, P Uma, D Venkataramana, B. Pushpalatha D Viswanada reddy "An efficient priority encoder & decoder using 45nm FinFET technology" ,2019

[5] Vasudeva G, Uma B V 22nm FINFET Based High Gain Wide Band Differential Amplifier "International journal of circuits, systems and signal processing" DOI:

[6] Shivali, Shobha Sharma, Amita Dev "Analysis of Various Master-Slave Configuration based D Flip-Flops" International Journal of Recent Technology and Engineering.

[7] M Reddi Sekhar, P Uma, D Venkataramana, B Pushpalatha D Viswanada Reddy "An Efficient Priority Encoder& Decoder Using 45nm FinFET Technology".

[8] S. Greeshma sai, N. Alivelu Manga, P. Chandra Sekhar "Design and Simulation of FinFET based digital circuits for low power applications."

[9] Rajuhajare, Dr.C. Lakshmi Narayana, Sunil.C, Sumanth, Anish.A. "Design and evaluation of Fin-FET based digital circuits for high-speed ICs."