Computer Architechture Assignment

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1. Given, Leakage power = 0.07W

   Number of Accesses per second = $(5 * 10^7)$

   Dynamic energy = 0.8nJ/access

   Total leakage energy = (0.07W * 1sec) = 0.07J

   Total dynamic energy = $(0.8 * 10^{-9} * 5 * 10^7)J = 0.04$J

   Total cache energy = Total leakage energy + Total dynamic energy = 0.11J

   % of leakage energy from total cache energy = $\frac{Total\ leakage\ energy}{Total\ cache\ energy} * 100$

   = $\frac{0.07}{0.11} * 100 = 63.64\%$

2. The reach of the given DTLB = $\sum_{n=1}^{3}(PageSize_i * (number of entries)_i)$
   That is, let:
   a = 4KB * 64 = 256KB
   b = 2MB * 32 = 64MB
   c = 1GB * 8 = 8GB
   Reach = a + b + c = 256KB + 64MB + 8GB = 84,54,400KB

3. Address size = 8 bits
   Block size = 4 = 2^2, number of Offset bits = 2
   Number of sets = 8 = 2^3, number of SetIndex bits = 3
   Number of bits for tag = 3

   a) i) Sequence 1 : (Hit or Miss) Table for Cache 1

Sequence address	Address (8-bit)	Tag	Set-Index	Hit or Miss
0	00000000	000	000	Miss
63	00111111	001	111	Miss
1	00000001	000	000	Hit
62	00111110	001	111	Hit
2	00000010	000	000	Hit
61	00111101	001	111	Hit
3	00000011	000	000	Hit
60	00111100	001	111	Hit
4	00000100	000	001	Miss
59	00111011	001	110	Miss
5	00000101	000	001	Hit
58	00111010	001	110	Hit
6	00000110	000	001	Hit
57	00111001	001	110	Hit
7	00000111	000	001	Hit
56	00111000	001	110	Hit
8	00001000	000	010	Miss
55	00110111	001	101	Miss
9	00001001	000	010	Hit
54	00110110	001	101	Hit
10	00001010	000	010	Hit
53	00110101	001	101	Hit
11	00001011	000	010	Hit
52	00110100	001	101	Hit

Hit ratio = $\frac{Number\ of\ hits}{Number\ of\ accesses} = \frac{18}{24} = 0.75$

a) ii) Sequence 1 : (Hit or Miss) Table for Cache 2

Sequence address	Address (8-bit)	Tag	Set-Index	Hit or Miss
0	00000000	000	000	Miss
63	00111111	111	111	Miss
1	00000001	001	000	Miss
62	00111110	110	111	Miss
2	00000010	010	000	Miss
61	00111101	101	111	Miss
3	00000011	011	000	Miss
60	00111100	100	111	Miss
4	00000100	100	000	Miss
59	00111011	011	111	Miss
5	00000101	101	000	Miss
58	00111010	010	111	Miss
6	00000110	110	000	Miss
57	00111001	001	111	Miss
7	00000111	111	000	Miss
56	00111000	000	111	Miss
8	00001000	000	001	Miss
55	00110111	111	110	Miss
9	00001001	001	001	Miss
54	00110110	110	110	Miss
10	00001010	010	001	Miss
53	00110101	101	110	Miss
11	00001011	011	001	Miss
52	00110100	100	110	Miss

Hit ratio = $\frac{Number\ of\ hits}{Number\ of\ accesses} = \frac{0}{24} = 0$

b) i) Sequence 2 : (Hit or Miss) Table for Cache 1

Sequence address	Address (8-bit)	Tag	Set-Index	Hit or Miss
0	00000000	000	000	Miss
64	01000000	010	000	Miss
128	10000000	100	000	Miss
192	11000000	110	000	Miss
1	00000001	000	000	Miss
65	01000001	010	000	Miss
129	10000001	100	000	Miss
193	11000001	110	000	Miss
11	00001011	000	010	Miss
75	01001011	010	010	Miss
139	10001011	100	010	Miss
203	11001011	110	010	Miss
9	00001001	000	010	Miss
137	10001001	100	010	Miss
201	11001001	110	010	Miss
73	01001001	010	010	Miss

Hit ratio = $\frac{Number\ of\ hits}{Number\ of\ accesses} = \frac{0}{16} = 0$

b) ii) Sequence 2 : (Hit or Miss) Table for Cache 2

Sequence address	Address (8-bit)	Tag	Set-Index	Hit or Miss
0	00000000	000	000	Miss
64	01000000	000	000	Hit
128	10000000	000	000	Hit
192	11000000	000	000	Hit
1	00000001	001	000	Miss
65	01000001	001	000	Hit
129	10000001	001	000	Hit
193	11000001	001	000	Hit
11	00001011	011	001	Miss
75	01001011	011	001	Hit
139	10001011	011	001	Hit
203	11001011	011	001	Hit
9	00001001	001	001	Miss
137	10001001	001	001	Hit
201	11001001	001	001	Hit
73	01001001	001	001	Hit

Hit ratio = $\frac{Number\ of\ hits}{Number\ of\ accesses} = \frac{12}{16} = 0.75$

4. Processor speed of P1 = 2.2 GHz
Processor speed of P2 = 1.6 GHz
Here, Total number of clock cycles = $\sum_{class=A}^{D}(CPI_{class} * (Instructioncount)_{class})$
According to given conditions,
For P1: Total number of clock cycles = ((1 * $\frac{20}{100} * 10^6$) +
(2 * $\frac{25}{100} * 10^6$) + (3 * $\frac{45}{100} * 10^6$) + (4 * $\frac{10}{100} * 10^6$)) = 2.45 * 10^6
$Time_{P1} = \frac{Cycles_{P1}}{Frequency_{P1}} = \frac{2.45*10^6}{2.2*10^9}$ = 1.114 * $10^{-3} sec$

For P2: Total number of clock cycles = ((2 * $\frac{20}{100} * 10^6$) +
(2 * $\frac{25}{100} * 10^6$) + (2 * $\frac{45}{100} * 10^6$) + (2 * $\frac{10}{100} * 10^6$)) = 2 * 10^6
$Time_{P2} = \frac{Cycles_{P2}}{Frequency_{P2}} = \frac{2*10^6}{1.6*10^9}$ = 1.25 * $10^{-3} sec$
Since, Time taken by P1 is less than that of P2, we conclude that ,
P1 is faster than P2 for the given program.

5.

Operation	P1	P2	P3	P4	Exclusive Bit
i.	1	0	0	0	0
ii.	0	1	0	0	1
iii.	0	0	0	1	1
iv.	0	0	1	1	0
v.	0	0	1	0	1
vi.	1	0	1	0	0

6. Given, number of misses scale linearly.
Let M be function of number of misses.
For $application_1$, slope = $\frac{miss_2 - miss_1}{number\ of\ ways_2 - number\ of\ ways_1}$ =
$\frac{400-1000}{6-2}$ = -150
If x is number of ways, M_1(x) = -150x + 1300

For $application_2$, slope = $\frac{miss_2 - miss_1}{number\ of\ ways_2 - number\ of\ ways_1}$ =
$\frac{1800-2000}{6-2}$ = -50
If x is number of ways, M_2(x) = -50x + 2100

Since, cache has 8 ways, let $application_1$ have y ways and $application_2$ have 8-y ways, so that the total number of misses attains minimum value.

That is : $M_1(y) + M_2(8-y)$ attains minimum value.
But, $M_1(y) + M_2(8-y)$ = -150y + 1300 - (50 * (8-y)) + 2100
= -100y + 3000

Since, total number of misses is proportional to -y.
Total number of misses is minimum when x attains maximum that si when y = 6.
Therefore, 6 ways for $application_1$ and 2 ways for $application_2$

7. Transaction rate of P = 34 per minute.
Transaction rate of Q = 58 per minute.
Transaction rate of R = 81 per minute.
Number of transactions for each application = 500.
Time taken by $application_x$ to complete y transactions = $\frac{y}{(transation\ rate)_x}$

Average number of Transactions per minute = $\frac{Total\ number\ of\ transactions}{Total\ time\ taken}$
= $\frac{3*500}{\frac{500}{34}+\frac{500}{58}+\frac{500}{81}}$ = 50.848 transactions per minute.

8. Let T_0 be total time by $system_0$.
For $system_0$:
time taken by initialization = $\frac{25}{100} * T_1 = t_1$
time taken by vision processing = $\frac{37}{100} * T_1 = t_2$
time taken by signal processing = $\frac{38}{100} * T_1 = t_3$

Given, speedup of vision processing for $system_1$ = 6 times
speedup of signal processing for $system_1$ = 10 times
Therefore, for $system_1$:
time taken by initialization = t_1
time taken by vision processing $\frac{t_2}{6}$
time taken by signal processing = $\frac{t_3}{10}$
Total time (T_1) = $t_1 + \frac{t_2}{6} + \frac{t_3}{10}$
= $0.35T_0$

Hence, speedup of $system_1$ over $system_0$ = $\frac{T_0}{T_1}$ = 2.857

9. Since, Voltage and frequency follow a linear relationship,
V α f

i. For getting minimum time, frequency has to be maximum.
Initially, Voltage is 1V and frequency is 3 GHz.
If multiplied by 1.2 factor,
Voltage is 1.2V which is safe and is the maximum it can attain
Since, time taken is inversely proportional to frequency
time taken reduces by a factor of 1.2
that is : minimum time = $\frac{30}{1.2} sec$ = 25sec

ii. Let voltage be V.
$Power_{leakage}$ = 30W
$Power_{dynamic}$ = (110-30)W = 80W
Also, $Power_{leakage} \alpha$ V and $Power_{dynamic} \alpha V^3$
Since, $Power_{dynamic} \alpha V^2 * f$ and $f \alpha V$

Total power = (30V + 80V^3)W.
Clearly, for minimum power , V should be minimum.
The lowest Voltage for which processes safely works = 0.8 V
If Voltage is multiplied by a factor of 0.8 (initial voltage is 1V).
We have, Total Power = (30 * (1*0.8)) + (80 * (1 * 0.8)^3)W
= 64.96W

iii. Let voltage be V.
similar to calculations of (i), new time = $\frac{30}{V}$
Since energy = Power * time
Total energy = ((30V + 80V^3) * $\frac{30}{V}$)J = ((30 + 80V^2) * 30)J
Clearly, For minimum energy , V should attain minimum.
The lowest Voltage for which processes safely works = 0.8 V
If Voltage is multiplied by a factor of 0.8 (initial voltage is 1V).
We have, minimum energy = ((30 + 80(1*0.8)^2) * 30)J = 2436 J

10. Given, memory addresses are defined at the level of each byte.
Page size = 2KB.
Therefore, there are 2^{11} Memory addresses
number of page offset bits = 11.
number of page number bits = 48 - 11 = 37
number of frames in physical memory = $\frac{2GB}{2KB} = \frac{2^{31}}{2^{11}} = 2^{20}$ frames
Since, we need 20 bits for frame number.
We have, size of one entry = 37 + 20 = 57 bits
Size of TLB = (number of entries * size of one entry)
Size of TLB = 57 * 32 = 1824 bits.

11. Frame size = 2^{10} bytes (Given, 1KB)
0x4795BA21 = 0000 0000 0100 0111 1001 0101 1011 1010 0010 0001
0x4795BB21 = 0000 0000 0100 0111 1001 0101 1011 1011 0010 0001
0x5795BA21 = 0000 0000 0101 0111 1001 0101 1011 1010 0010 0001
0x4785BA21 = 0000 0000 0100 0111 1000 0101 1011 1010 0010 0001

Since, all memory address have 10 offset bits and virtual address have 32 bits.

The first 22 bits are stored in the page table.
that is : 0x4795B, 0x4795B, 0x5795B and 0x4785B are stored in the page table.

Here, the virtual addresses of first and second are same, so, we need only one access.
Therfore, we need three unique accesses.

12. a. Using LRU policy,

Address	Hit or Miss
A	Miss
B	Miss
C	Miss
D	Miss
A	Miss
B	Miss
C	Miss
D	Miss
A	Miss
B	Miss
C	Miss
D	Miss

b. Using MRU policy,

Address	Hit or Miss
A	Miss
B	Miss
C	Miss
D	Miss
A	Hit
B	Miss
C	Miss
D	Hit
A	Miss
B	Miss
C	Hit
D	Miss