CS2323 Computer Architecture 2018

Homework 2

Important: Your submission should be named as RollNumber_CA_HW2.pdf. For example, if your roll number is cs16mtech11075, then your submission should be cs16mtech11075_CA_HW2.pdf. Except pdf, no other format is acceptable. **10 marks will be deducted for not following these instructions or if you submit a zipped file.**

To reduce TA efforts, please answer the questions in the order in which they are given.

1. (2 mark) Consider a single-precision floating point number: 00111110101010101010101010101010. Find out its equivalent decimal number.

2. (3 marks) Represent 5.6677 in single-precision and double-precision floating point notation (you may use online tool for this). Also, find the difference between the number (i.e., 5.6677) and what is stored for both single and double precision-numbers.

3. (4 marks) Consider the values stored in a 4 contiguous memory locations.

Address Value

0x1000 0x4795BA21

0x1004 0x4795BB21

0x1008 0x5795BA22

0x100C 0x4785BA21

We have a 128bit vector register vr1, into which we want to load the above mentioned values. Write the code to do that. Use of vector instructions is mandatory.

4. (3 marks) Assume following accesses to a DRAM bank. Find number of row-buffer misses with (a) open-row and (b) close-row policy (here, the row is always closed without seeing the requests which are queued). Here (p,q) means column p, row q. Assume FCFS policy.

(4,15) (4,6), (6,150), (7,150), (3,9), (4,9), (4,12), (4,150), (5,10), (6,10), (11,10)

5. (1 mark) In the question above, can a reordering of accesses improve row-buffer hit rate for open-row policy? If so, show that reordering.

6. (1 mark) For an application with high spatial locality, should the size of row-buffer (i.e., the size of each DRAM row) be high or low. (Max 2 sentence answer)

7. (1 mark) Does branch-prediction reduce or increase energy consumption. If the answer is not always a yes/no, write the conditions under which a particular answer is applicable. (Max 2 sentence answer)

8. (4 mark) Assume a neural predictor entry has the weight vector as [10, -4, 19, -2, 2] (bias weight is the last one) and branch history register as [1, -1, 1, 1]. Find its prediction. Assume that the outcome is taken, show updated weights and second prediction.

9. (1 mark) What is the impact of using voltage-scaling technique on soft-error vulnerability. That means, will this technique increase the soft-error rate or reduce it? (Max 2 sentence answer).

10. (1 mark) Write a minimum working example of a code where RW → MA forwarding is useful

11. (1 mark) Write a minimal sequence of instructions which shows WAR hazard.

12. (1 mark) Write a minimal sequence of instructions which shows control hazard.

13. (2 mark) Is there a forwarding path which can remove the pipeline bubble completely in this sequence of instructions. If so, write it.

ld r1,4[r2]

add r2,r1,r4

sw r1,10[r3]

14. (4 mark) Show pipeline diagram for the following instructions assuming interlocking technique is used.

add r1, r2, r3

mul r7, r9, r10

sub r4, r1, r5

15. (6 mark) Consider a DRAM, where row-buffer hit, row-buffer miss and row-buffer conflict take 20ns, 40ns and 60ns, respectively.

The DRAM has only one bank. Assume addresses X0, X1, X2, X3 are in same row, whereas Y0 is in a different row. Initially, the row-buffer is closed.

Find out the completion time for following sequence of accesses for open-row and closed-row policy.

Request	Time of Arrival (ns)	Open-row policy	Closed-row policy
X0	0		
Y0	10		
X1	100		
X2	200		
Y0	250		
X3	300		

16. (2 mark) Differentiate between strongly coupled, and loosely coupled multiprocessors. (write maximum of 2 sentences for each of the two, clearly showing the difference.)

17. (3 mark) A main memory unit with a capacity of 4 megabytes is built using 1Mb DRAM chips. Each DRAM chip has 1K rows of cells with 1K cells in each row. The time taken for a single refresh operation (i.e., refreshing a single cell) is 100 nanoseconds. It is given that inside a chip, refresh operations of different cells happen in serial. Also, at a time, four chips can be refreshed in parallel.

Find out the time required to perform one refresh operation on the entire memory.

18. (5 mark) Consider the following instructions:

```
add    r10,r10, 5
mul  r2, r10, 90
add    r8,     r8,     r2
sub    r7,     r7,     5
ld       r0, 55(r7)
```

Assume the pipeline has only 3 stages: fetch, decode and execute (as assumed in L13). Show the pipeline diagram assuming (1) simple pipelining (2) superscalar execution and (3) out-of-order execution.

19. (1 mark) An application sees frequent last-level cache misses which lead to a stall. The caches are small so these misses cannot be hidden. Which of the three multithreading strategies should it use? (no need to write the reasoning).

20. (2 mark) Write the assembly code corresponding to the following commands using predicated instruction on a vector processor.

if (x > 50) x = x * 50

21. (3 mark) A DRAM main memory system has one 64-bit wide channel. The channel can have up to 4 DRAM ranks. All the 4 ranks are filled with 16Gbit DRAM chips. Each DRAM chip provides 8 bit wide data. Find out how many chips are required for filling all DRAM ranks and what is the total capacity of DRAM?

22. (1 mark) For the following access sequence A C Z V K L Z V C H R B A K, what is the reuse distance of C? (no need to write the reasoning).

23. (2 mark) The following is the code used for convolution. Rewrite the following code after tiling the first loop below.

```
for ( row=0; row<R; row++)
 for ( col =0; col<C; col++)
  for ( to=0; to<M; to++)
   for ( ti =0; ti <N; ti++)
 for ( i =0; i<K; i++)
  for ( j =0; j<K; j++)
    Output_fmaps [to] [row] [col]
+= Weights [to] [ti] [i] [j] *
Input_fmaps[ti] [S*row+i] [S*col+j]
```

24. (4mark) Consider the code below and answer the following two questions:

```
for ( int i=0; i<N; i++) { /* B1 */
val = array [ i ] ;
if ( val % 20 == 0) { /* B2 */
sum += val ;} }
```

For branch B1 to be a biased branch, what should be the condition on the value of N and what should be the condition on values of array[]. If no condition is required, just say so.

For branch B2 to be an un-biased branch, what should be a condition on the value of N and and what should be the condition on values of array[]. If no condition is required, just say so.

25. (2 mark) Name and describe the strategies to address temporal and spatial multi-bit errors. (maximum 2 sentences each along with the condition for effectiveness of those techniques, if any. Drawing a figure is not required).