NC State University

Department of Electrical and Computer Engineering

ECE 463/521: Spring 2012 (Rotenberg)

Project #1: Cache Design, Memory Hierarchy Design

by

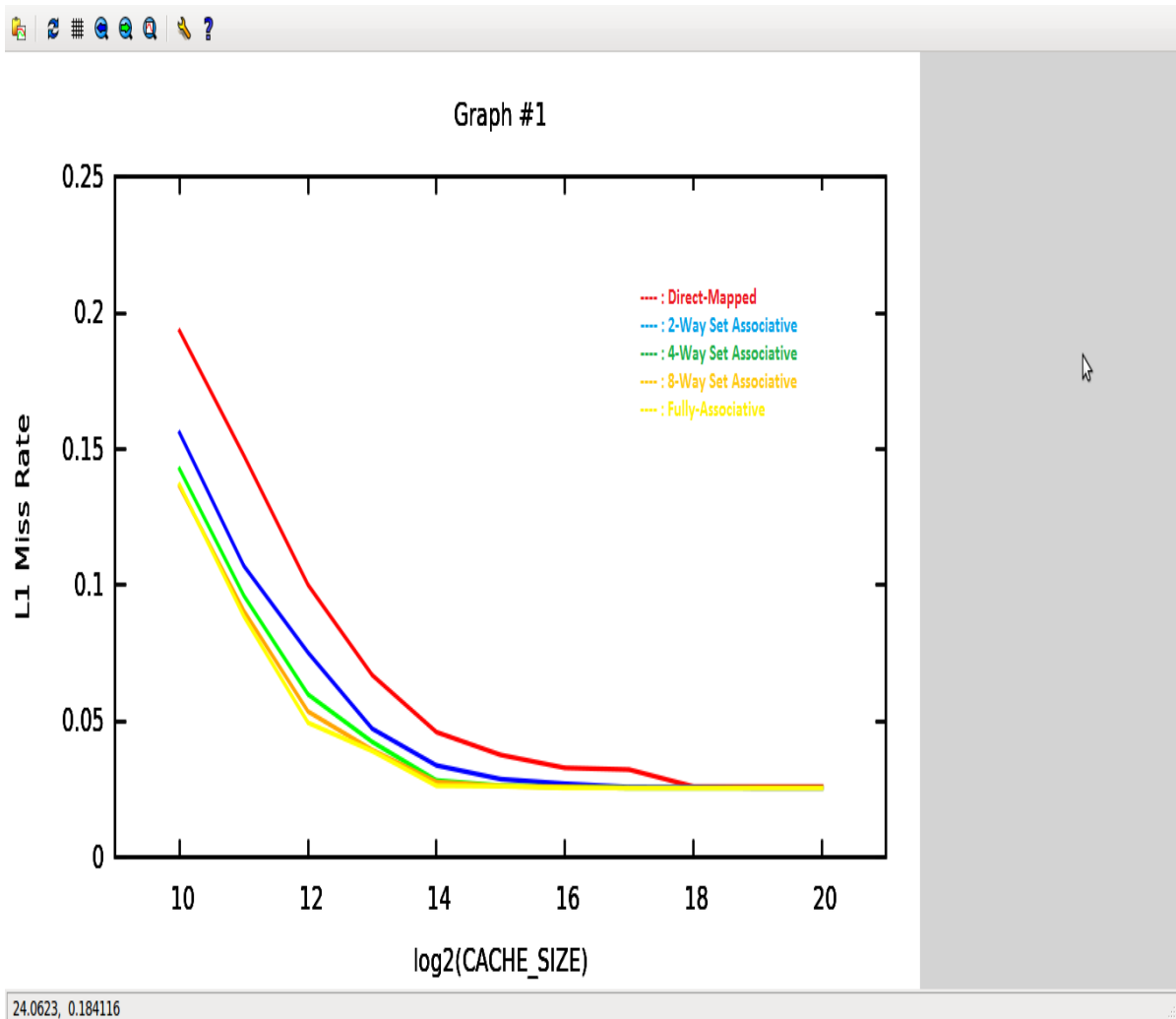**<< Salil Kanitkar >>**

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Student's electronic signature: Salil Kanitkar
                                  (sign by typing your name)

Course number: _____521_____
                   (463 or 521 ?)

Graph #1

Graph #1

0.25

0.2

0.15

L1 Miss Rate

0.1

0.05

0

---- : Direct-Mapped
---- : 2-Way Set Associative
---- : 4-Way Set Associative
---- : 8-Way Set Associative
---- : Fully-Associative

10   12   14   16   18   20

log2(CACHE_SIZE)

24.0623, 0.184116

1. Trends in the Graph -->
(1) For a given Associativity, increasing cache size reduces the miss rate. It can be seen from that graph that Miss rate goes on reducing to its minimum value, which in turn is dependent on the number of Compulsory Misses.
(2) For a given cache size, **as the associativity increases, the Miss Rate reduces.** This can be seen from the graph.

2. Compulsory Miss Rate = 0.025820

3. Conflict Miss Rate = Miss rate – Compulsory Miss rate
(1) Direct Mapped, Conflict Miss rate = 0.193460 – 0.025820 = **0.16764**
(2) 2-Way Set Associative, Conflict Miss rate = 0.156030 – 0.025820 = **0.13021**

(3) 4-Way Set Associative, Conflict Miss rate = 0.142700 – 0.025820 = **0.11688**
(4) 8-Way Set Associative, Conflict Miss rate = 0.136270 – 0.025820 = **0.11045**
(5) Fully-Associative, Conflict Miss rate = 0.136960 – 0.025820 = **0.11114**
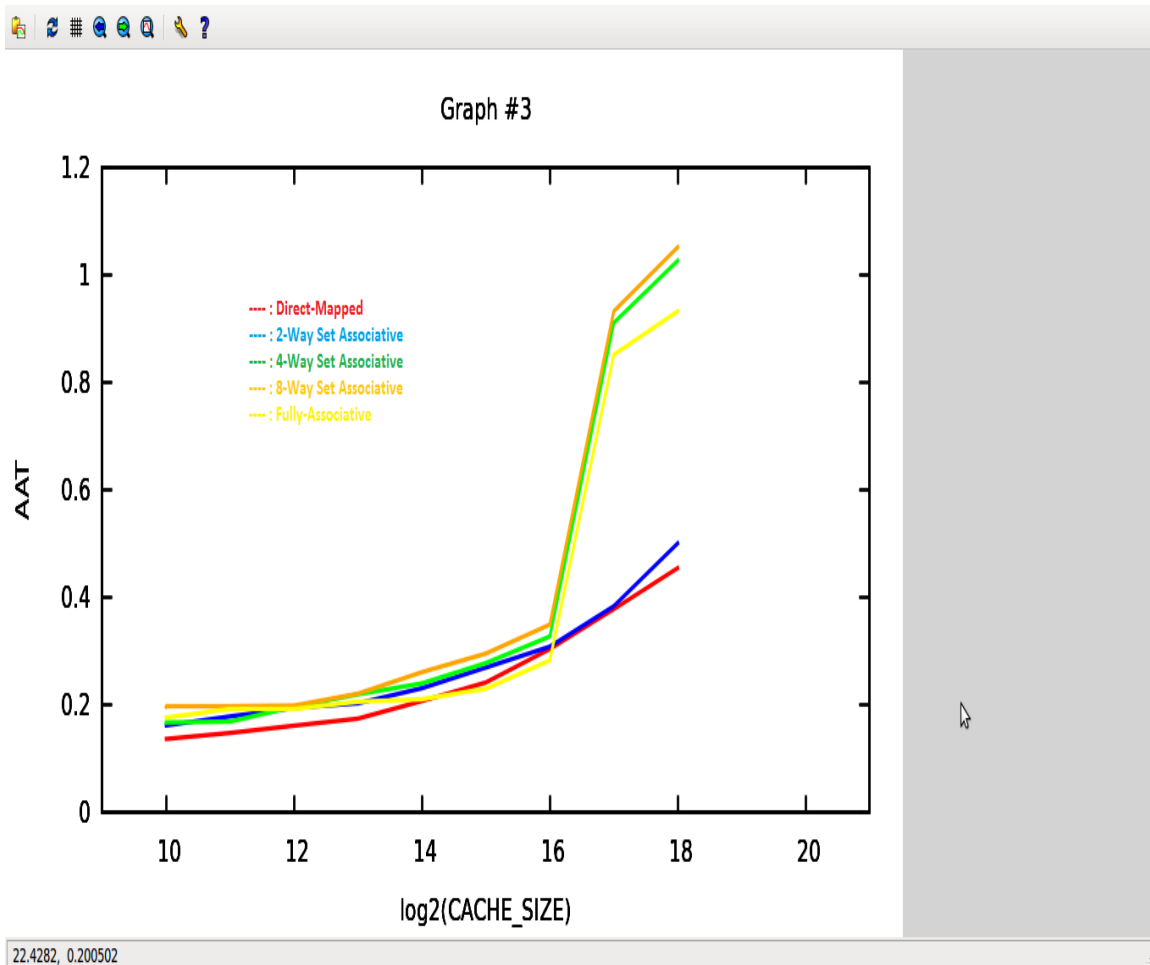
<u>Graph #2</u>
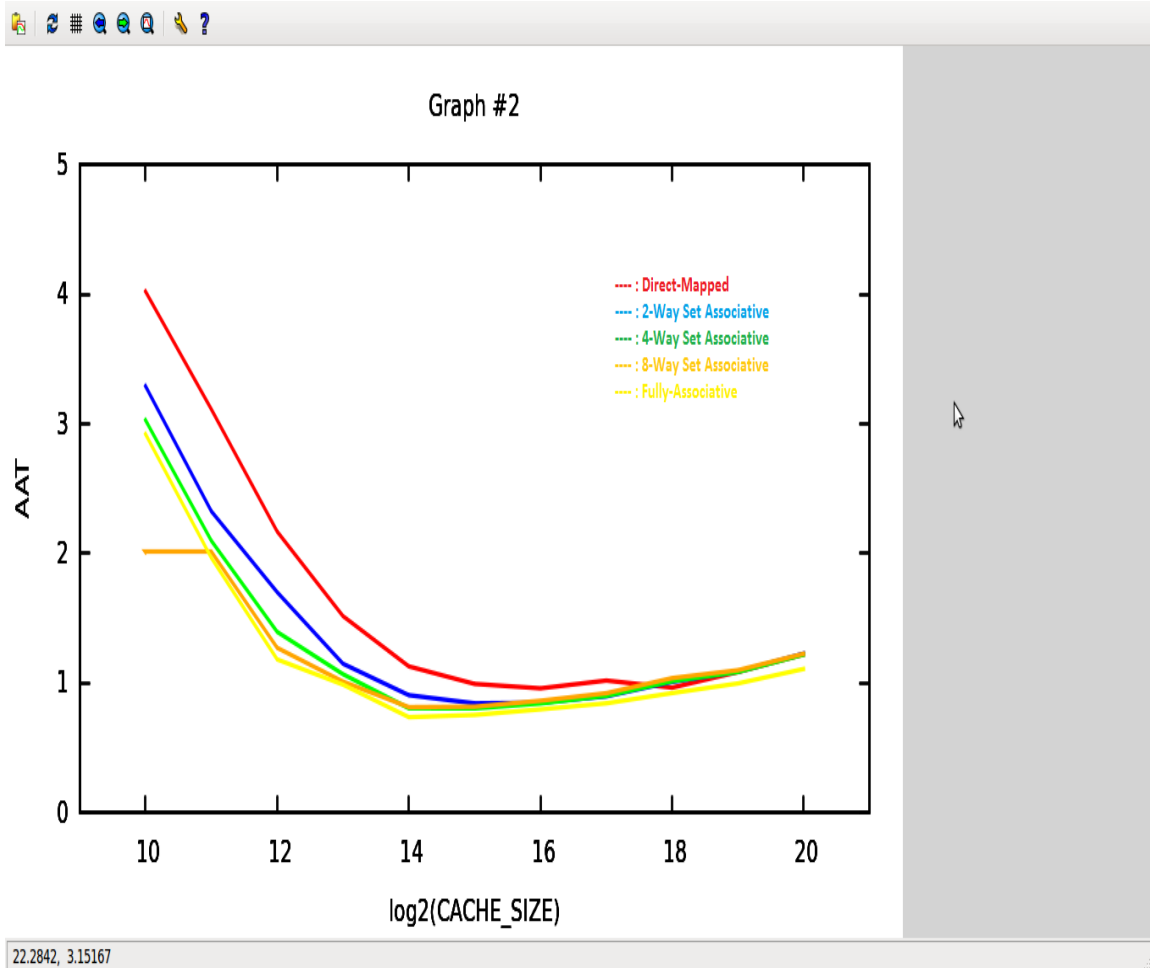
1. The configuration for which lowest AAT is seen –

L1 Cache Size = 16k (log(CacheSize)=14)
Fully-Associative Cache
Area of the above configuration = 0.063446019

Graph #3

1. The best AAT observed in Graph2 was for 16k Size and Fully-Associative L1 Cache and the value was "**0.737676**"
From the graph, following configurations are closer to graph2 values –
   1) 128k L1 Cache, 4-Way Set Associative
   2) 128k L1 Cache, 8-Way Set Associative
   3) 128k L1 Cache, Fully-Associative.
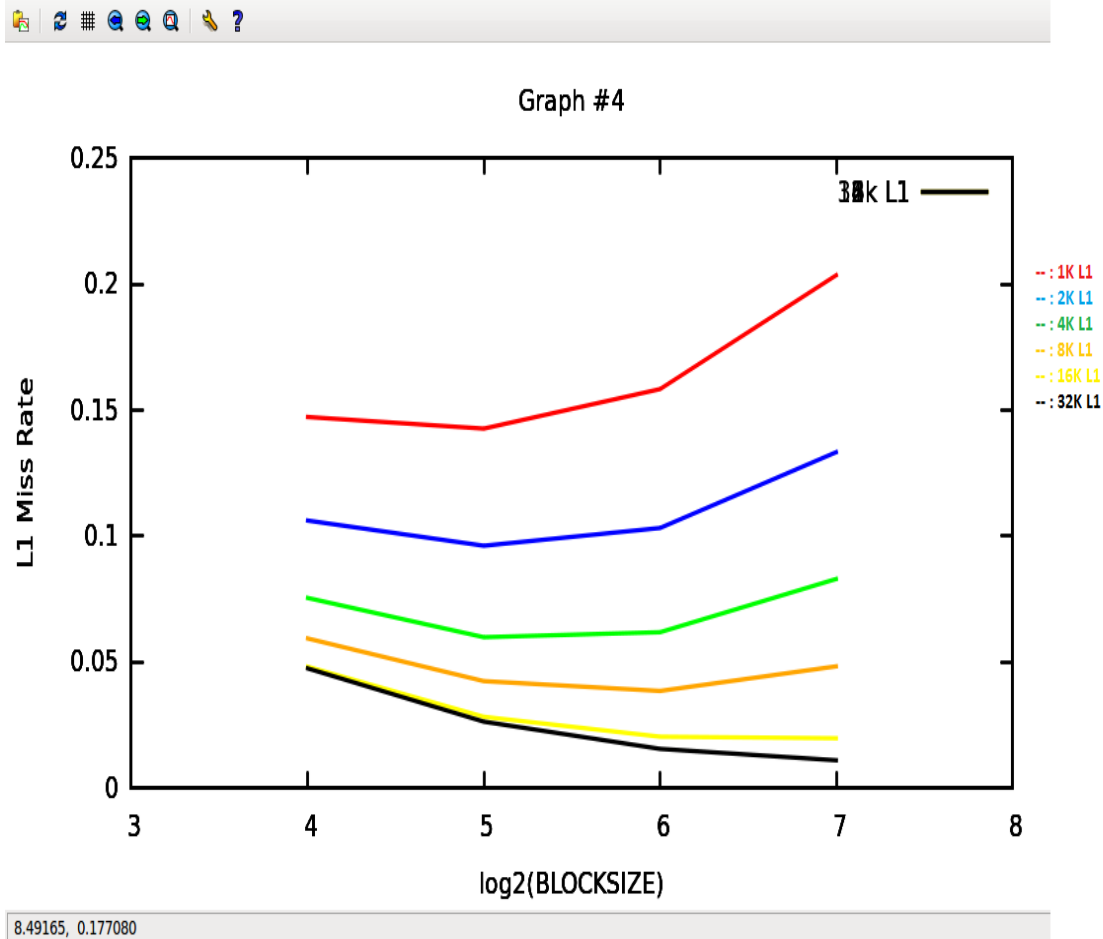
2. Following Configuration shows the lowest AAT –
   1K L1 Cache, Direct-Mapped. the value is "**0.137005**"
   It is almost 5 times lower than least of graph2. (0.737676 – 0.137005 = **0.600671**)

3. **Area of the above configuration = 0.010298466**
   Difference in Area wrt to graph2 = 0.063446019 - 0.010298466
   **= 0.053147553**

Graph #4

Graph #4

1. Trends in the Graph –
(1) Smaller Caches prefer Smaller Block Sizes. As can be seen from the graph, for 1K L1 (red line), the Miss rate increases as the BlockSize is increased.
(2) Larger Caches prefer Larger Block Sizes. As can be seen from the graph, for 32K L1 (black line), as the block size increases, the miss rate reduces.
(3) For small cache size, as the block size increases, Cache Pollution comes into picture. More useless data is brought in with the intent of exploiting Spatial Locality, but resulting in higher miss rate.
(4) This tradeoff is also evident from the graph. Initially, as the block size increases, the miss rate drops. This is region where increasing block size is exploiting spatial locality more effectively without causing cache pollution. But then, if the block size is further increased, the Miss rate drops, showing that Cache Pollution is taking place.
(5) However, the point at which this balance is seen (Point (5, 0.15) on the Graph for 1K L1), changes as the Cache Size increases. The balance point shifts more to the right i.e. with Larger sized caches, larger blocksizes can be effectively used without Cache Pollution coming into picture.

Graph #5
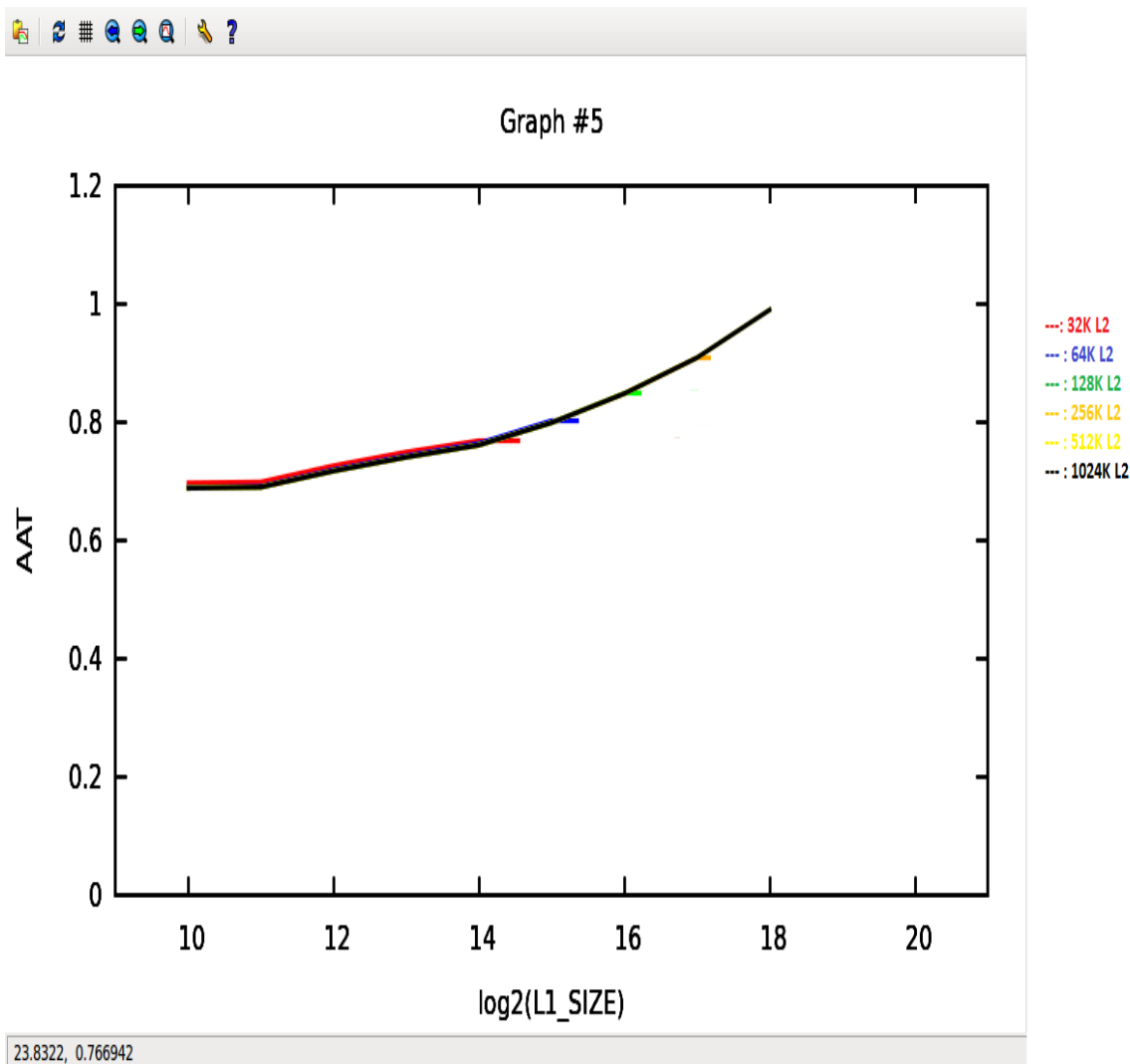
1. Following Configurations yield the lowest AAT – (BlockSize is 32 and ASSOC is 4)
(1) 1K L1 Cache, 128K L2 Cache – AAT Value = 0.689335214
(2) 1K L1 Cache, 256K L2 Cache – AAT Value = 0.689335214
(3) 1K L1 Cache, 512K L2 Cache – AAT Value = 0.689335214
(4) 1K L1 Cache, 1024K L2 Cache – AAT Value = 0.689335214

2. Areas of above 4 configurations are as follows –
(1) 0.015114948 + 0.667017966 = 0.682132914
(2) 0.015114948 + 1.141294802 = 1.15640975
(3) 0.015114948 + 2.177361671 = 2.192476619
(4) 0.015114948 + 4.673162925 = 4.688277873
Smallest Area Config – 1K L1 Cache, 128K L2 Cache

Graph #6

I have created an Excel Sheet which computes and shows 240 AAT values for following changing configurations –
BlockSize varies as 16, 32, 64.
L1_SIZE varies from 1K to 16K
L1_PREF_N varies from 1 to 4 and so does L1_PREF_M
Therefore, 4*4*3*5 = 240 simulations.

The Submitted Excel sheet Graph6 contains these simulation results and calculated AAT values.

1. The Best AAT value out of all these 240 simulations is: **0.053652 ns**
Following two configurations have that value – (L2 Size, ASSOC is fixed)
    (1) BlockSize=64, 1K L1, L1_PREF_N=3, L1_PREF_M=4.
    (2) BlockSize=64, 1K L1, L1_PREF_N=4, L1_PREF_M=4.