Energy Efficient 1-Bit Approximate Adders Using CNTFET

PROJECT REPORT

Submitted

In the partial fulfilment of the requirements for
the award of the degree of

Bachelor of Technology

in

Electronics and Communication Engineering

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VIGNAN'S FOUNDATION FOR SCIENCE, TECHNOLOGY AND RESEARCH

(Deemed to be University)

VADLAMUDI, GUNTUR – 522 213, INDIA

June-2022

CERTIFICATE

This is to certify that the project report entitled **ENERGY EFFICIENT 1-BIT APPROXIMATE ADDERS USING CNTFET** that is being submitted by **G. APURUPA (181FA05089), P. SAI KRISHNA REDDY (181FA05114)** in partial fulfilment for the award of IV year II semester B.Tech degree in Electronics and Communication Engineering to Vignan's Foundation for Science Technology and Research University, is a record of bonafide work carried out by them under the guidance of Dr. M. SARADA, Professor of ECE Department.

Signature of the faculty guide	Signature of Head of the Department
Dr. M. Sarada, M.Tech, Ph.D, MIEEE	Dr. T. Pitchaiah, M.E, Ph.D, MIEEE
Professor	HOD&Professor

DECLARATION

We hereby declare that the project work entitled ENERGY EFFICIENT 1-BIT APPROXIMATE ADDERS USING CNTFET is being submitted to Vignan's Foundation for Science, Technology andResearch (Deemed to be University) in partial fulfilment for the award of B. Tech degree in Electronics and Communication Engineering**.** The work was originally designed and executed by usunder the guidance of Dr. M. Sarada, Professor at Department of Electronics and Communication Engineering, Vignan's Foundation for Science Technology and Research (Deemed to be University) and was not aduplication of work done by someone else. We hold the responsibility of the originality of the workincorporated into this thesis.

Signature of the candidate

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ACKNOWLEDGEMENT

The satisfaction that accompanies the successful completion of any task would be incomplete without the mention of people who made it possible and whose constant guidance and encouragement crownall the effort with success.

We are greatly indebted to Dr. M. Sarada, my revered guide and Professor in the Departmentof Electronics and Communication Engineering, VFSTR (Deemed to be university), Vadlamudi, Guntur, for her valuable guidance in the preparation of this dissertation. She has been a source of great inspiration and encouragement to us. She has been kind enough to devote considerable amount of her valuable time in guiding us at every stage. This is our debut, but we are sure that we are able to do many more such studies, purely become of the lasting inspiration and guidance given by respectable guide.

We would like to specially thank **Dr. T. Pitchaiah**, Head of the Department, ECE **Dr. SK. Jakeer Hussain**, Deputy Head of the Department, ECE **Dr. G.N.V.R. Vikram, Dr. Satyajeet Sahoo** Project Coordinators, Department of ECE, VFSTR (Deemed to be University) for their help and support during the program.

We wish to express our gratitude to **Prof. P. Nagabhushan** Vice-Chancellor, VFSTR (Deemed to be University) for providing us the greatest opportunity to have a great exposure and to carry out the Project.

We would like to thank **Susmitha**, Lab Technician of VLSI for her help and support during till the end of the project.

We would like to dedicate this book to our parents

Name of the Student

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Abstract

Approximate computing is to design a circuit with good accuracy by exchanging the circuit performance.The purpose is to reduce the circuit area, delay, and power. In this project, various authors proposed various approximate adders by reducing the number of transistors. Due to a decrease in transistor numberthe circuit area and delay decreases compared to the exact adder. In this project, all the adders were designed using Carbon Nano-Tube Field Effect Transistor (CNTFET) technology. All the circuits are simulated using the Cadence Virtuoso tool with 32nm CNFET technology. The supply voltage Vdd provided for these circuits is 0.9v. Here this project, Delay, Power, and PDP of the approximate adder circuits are discussed. All the Approximate Circuits are implemented in 4-bit RCA and 2*4 Multiplier.

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CHAPTER 1

INTRODUCTION

1.1Motivation

Regarding advances in science and technology, the human need for information, processing speed, and storage has increased considerably over time. The fabrication of compact integrated circuits hasreduced energy consumption and increased system speeds. With the advent of complementary metal- oxide-semiconductor (CMOS) technology, CMOS transistors encountered challenges such as short channel effects, leakage currents, increased power consumption, and high sensitivity to orbitalparameters that encouraged scientists to take advantage of new technologies at the nanoscale. The similarities between Carbon NanoTube Field-Effect Transistors (CNTFETs) and metal-oxide-semiconductor field-effect transistors have been studied by researchers. CNTFETs have a high carrier mobility, low power consumption, lower latency, and small intrinsic capacitors that result in high- performance speeds. Due to the similar electron and hole mobilities, the P- and N-types of these transistors have similar channel lengths. One unique feature of CNTFETs is the variation in the threshold voltage by hanging the channel length. Using these transistors and multi-value logic (MVL) greatly reduces the integrated circuit volume. MVL circuits do not exhibit common problems of binary circuits including a high number of connections and power consumption, which reduces the circuit complexity and chip surface. This allows rational and mathematical functions to be implemented at a faster rate and the number of computations. The multi-valued logic is divided into ternary, quaternary, and pentanary groups. Most of this research is performed in the ternary field. Thequaternary logic between the highest and the lowest levels in the MVL circuits can be considered a suitable option when designing microprocessors. Different circuits have been designed using CNTFETs and MVL logic.

1.2 Approximate Computing

Nowadays, the demand for appropriate and moveable applications like mobiles, Pcs, chargers, etc. is high. Because power consumption became a crucial factor. An increase in circuit area causes the decrease in battery life of moveable applications like mobiles, PCs, chargers, etc., Due to this powerconsumption of the devices also increased. To boost the portable device's energy effectiveness, various approaches such as nanotechnologies and approximate computation have been implanted crucial elements such as adders, subtractors, multipliers, Approximate adders, and ripple carry adders are designed using the Carbon Nanotube Field Effect Transistors (CNTFET) technology to minimizethe transistor count, energy usage, and circuit size. The energy efficiency of the circuit is accomplished under various factors like supply voltage, average power, delay, and power-delay product (PDP).

The arithmetic logic circuit is a dominant part of Very Large Scale Integrated (VLSI) and has a crucialimpact on the overall performance of VLSI. Adder is the fundamental unit of VLSI. Hence,approximate adder design draws the researcher's interest widely. The method used to minimize the circuit area, delay, and power dissipation is the use of an approximate adder. The inexact full adder is used to perform the LSBs of an approximate adder, and MSBs are performed by an exact full adderwhich can optimize the error at LSB and makes the approximate adder more "accurate". The arithmetic circuits mean which bought improvements like energy, the performance of a circuit, and the area of the circuit in the error tolerance applications. Error tolerance applications like video and image processing applications where the exactness is not much important.

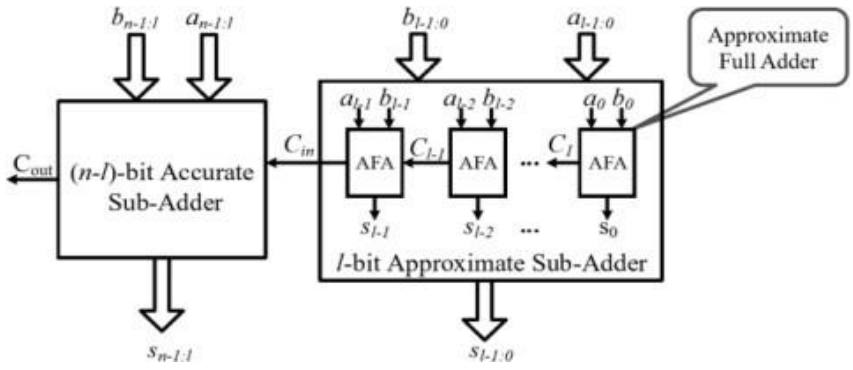


Fig 1.1. Block diagram of n-bit approximate adder

The approximate computation systems have played a vital role at all levels, such as computer and data servers, ensuring the ability to reach substantial enhancements typically through continuously reducing the complementary metal oxide semiconductor (CMOS) feature size that has increased the number of transistors used on a chip gradually in each generation of technology. With the increasingtechnological development in integrated circuits, enhancement in efficiency has become a renewed challenge among digital circuits and has also become an important barrier across all the circuit platforms. To contain error-tolerant applications, high computer flexibility is afforded in multi-media,machine learning, neural networks, pattern recognition, and data mining, which are imprecision tolerant. In this case, the outcome is not necessarily required. It is thus ensured that the function of logic circuits, to an acceptable level of accuracy under reduced delay and power consumption, remain in the trade. According to one study, error tolerant applications, such as neural networks, recognition, and mining, are devoid of exactness in order to create meaningful results which are sufficient enough to generate human perception and capability. The arithmetic circuits are the means by which the improvements are brought about in conditions such as energy, performance, and area in the corresponding applications as they utilize inherent error tolerance. Approximation on computation as such is often used to design energy efficient circuits.

1.3 Carbon Nano Tube Field Effect Transistor Technology (CNTFET)

Carbon Nanotubes (CNTs) came into existence in 1991 and the credit for its discovery was given toa Japanese physicist, S. lijima. CNTs are one-atom-thick grapheme tubes that have been transformed into pipes. CNTFET has garnered increased interest among new nanotechnology devices because toits unique characteristics, which include high electric conductivity, high thermal conductivity,mechanical strength, thermal resistivity/ stability, low voltage actuation qualities, and field emission.

The CNTs employ two types, as follows: single walled carbon nanotube (SWCNT) and multi walledcarbon nanotube (MWCNT). The SWCNT consists of a sheet of single cylinder of 1–2 nm and MWCNT consists of more single cylinder with 10 nm as illustrated in Figure 1. A SWCNT operatesas semiconductor or a conductor which depends on the arrangement of atoms along the CNTs. Thereare three types of SWCNT models, as follows: zigzag, armchair, and chiral CNTs. The three types ofCNTs are shown in Figure 2. The n1 and n2 are the co-

effificients that signify the positive integers and features the chirality of the CNTs. If n1 and n2 are equal to zero, it is zigzag, and if n1not equalto n2 or n1or n2 not equal to 0, it is chiral CNT. Furthermore, the armchair is described as n1 and n2equal to n.

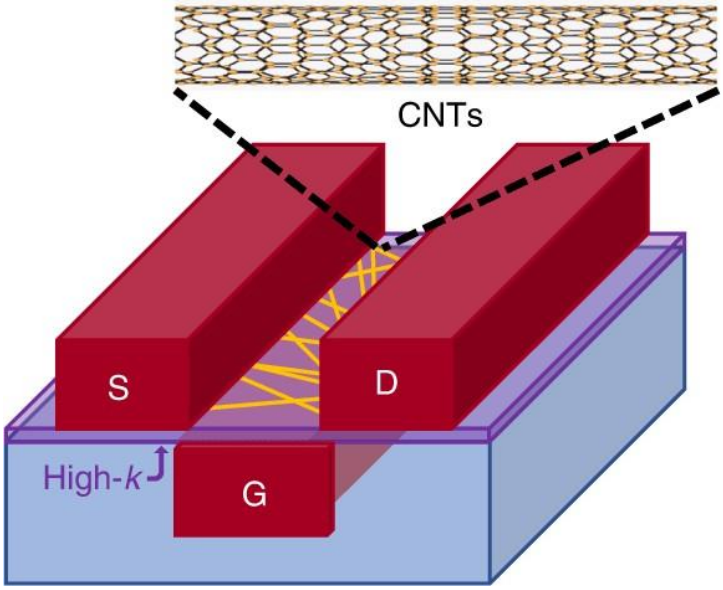


Fig 1.2. Structure of CNTFET

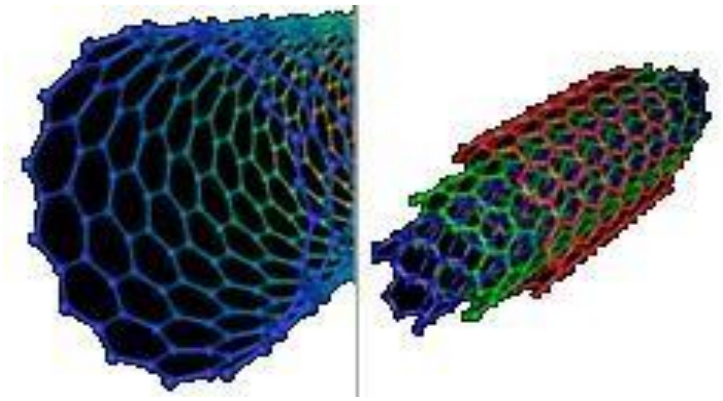


Fig 1.3. SWCNT and MWCNTs.

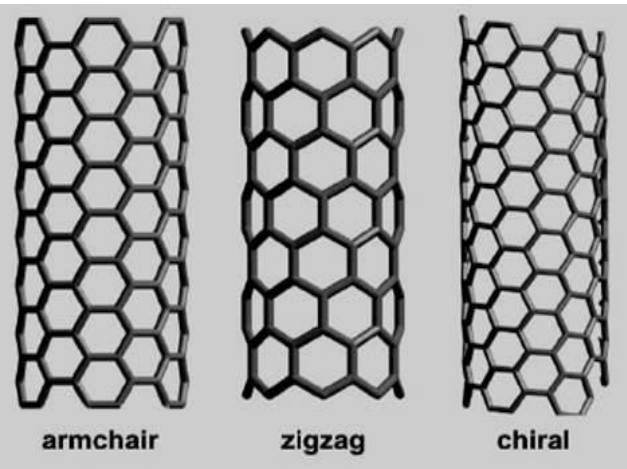


Fig 1.4. CNFET Models

The semiconductor industry confronts several obstacles as the scale of semiconductor components and integrated circuits shrinks to nano scale range. Short-channel effects, decreased gate controllability, greater leakage currents, and huge parameter changes result from reducing the size.

The decline in CMOS technology has been fast over the previous three decades due to increased short-channel effects and power dissipation restrictions, although it may be nearing completion. As a result, alternative silicon transistor technologies are being investigated. Using a carbon nano tube field effect transistor to solve numerous CMOS difficulties is an alternative (CNTFET).

In order to calculate the diameter of the CNT.

$$D_{CNT} = \frac{\sqrt{3}a0}{\pi}\sqrt{n^2 + m^2 + \text{ nm}}$$

where a0 = 0.142 nm is the distance between the neighbouring carbon atoms and n, m are the chirality vectors that specify the orientation of CNT.

Therefore, Equation for DCNT in nanometers can berewritten as

$$D_{CNT}= 0.0783\sqrt{n^2 + m^2 +} \text{ nm}$$

CNFETs have the unique property of being able to change their threshold voltage simply by altering the diameter of the nano tubes under the gate. This distinguishes them as ideal candidates for logicalcircuit design. The diameter of the CNT is computed using the equation below:

$$Vth \cong \frac{Ebg}{2e} = \frac{\sqrt{3}aV\pi}{3eDCNT} \cong \frac{0.436}{DCNT(nm)}$$

Where $a = 2.49$ Å is the carbon-to-carbon atom distance, $V\pi = 3.033\ eV$ is the carbon π–πbond energy in the tight bonding model, e is the unit electron charge, and DCNT is the CNT diameter.

There are benefits and cons to the technology:

- The threshold voltages of CNTFETs may be adjusted. This is a huge advantage over CMOStechnology, which requires multiple masks to achieve varied threshold voltages.
- High electron mobility, high current density, and high trans conductance are just a few of theadvantages that may be mentioned.
- Longevity concerns, dependability challenges, mass manufacturing difficulties, and productionexpenses are all mentioned as drawbacks.

The CNTFET technology is still in its infancy. A 16-bit RISC CPU with 14,000 CNFET transistors was constructed in 2019. [9]. While this is a big step forward for CNTFET technology, it's worth remembering that the Intel 8086 CPU, a 16-bit microprocessor, was debuted in 1978 with 29,000 transistors, more than 40 years ago! CNTFETs, on the other hand, may be used to propose a new quaternary operator implementation and compare it to previously published recommendations because CMOS and CNTFET circuits have comparable circuit architectures.

1.4 Objectives of the Work

The broad objective of the project is to propose a new 1-bit approximate adders. The specific objectives of the project are:

- To design the approximate full adder
- To reduce the number of transistors
- To reduce the power consumption and delay
- To implement 4-Bit RCA and 2*4 multiplier using the proposed approximate adder

1.5 Overview of the project

To design the new 1-Bit approximate adder with less number of transistors so that the adder circuit consumes less power and less delay. The errors count also reduces with less number of transistors. Then after the proposed circuits are implemented in Ripple carry adders and Multiplier applications for checking the overall performance of the proposed 1-Bit approximate adder circuits.

1.6 Contribution of the Thesis

In this project, the existing circuits are simulated in CNTFET 32 nm technology and 5 new 1-bit approximate adder circuits are proposed (AA11-AA15). The proposed 1-bit approximate adders require less transistors with less number of errors and low PDP. The quantitate results of all the approximate adders are shown in Table 2. All the 1-bit approximate adders (AA1-AA15) are implemented with 4-bit approximate Ripple Carry Adder and approximate 2*4 multiplier. The propagation delay, Power dissipation and PDP comparison of RCA and 2*4 multiplier are shown in Table 3 and 4 respectively.

1.7 Organizations of the Thesis

This project report has been divided into four different sections. The first section focuses on the literature required to get basic knowledge about previous approximate adders that are already existingand their working. The second section is about the Proposed adders and its simulation results. In the third section, For Approximate computing Ripple Carry Adder is proposed for the application as wellas in fourth section Approximate multiplier also proposed.

CHAPTER 2

EXISTING 1-BIT APPROXIMATE ADDERS

Here in this chapter total of 10 various 1-Bit approximate adders are discussed by different authors. All the 10 adders are discussed with the help of circuit diagrams as well as Sum and Carry equations. Here the transistor count and number of errors in the adders are going to observe.

2.1 Existing Approximate Adder 1

The Authors M. Ramaswamy, G. Narmadha, and S. Deviasigamani proposed new approximate Adderwith less number of transistors, by removing the transistors from the exact adder. In doing so, they ensure the combinations of A, B, and Cin doesn't result in open circuits or short-circuited. Here in Fig 2.1, the adder has a total 14 transistors as compared to the exact adder it having 10 less numberof transistors. This adder contains total four errors whereas, sum having three errors and carry contains one error. The sum and carry expression of the approximate adder is shown in equation 1 and 2. The authors proposed the circuit using gpdk 180nm technology. The circuit uses the Static logic for implementation of the circuit. The Sum is inverter of Carry circuit.

$$Sum = \sim Carry \qquad (1)$$

$$Carry = (A \,.\, B) + C \qquad (2)$$

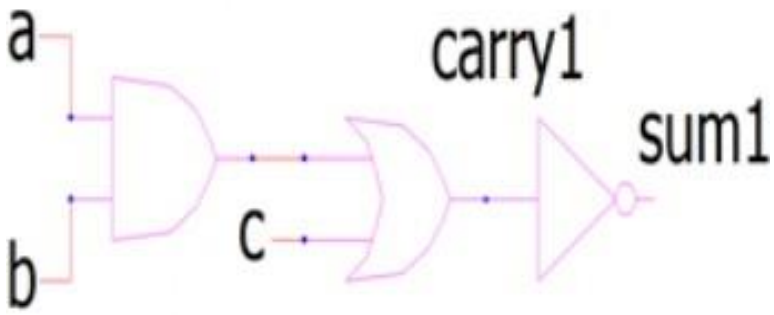


Fig 2.1. Existing Approximate Adder 1 circuit (AA1)

2.2 Existing Approximate Adder 2

The Authors M. Ramaswamy, G. Narmadha, and S. Deviasigamani proposed another new approximate adder as shown in Fig 2.2, with 14 number of transistors. The proposed approximate adder having three errors in sum and no error in carry. As compared to the exact adder the proposedadder has10 less number of transistors. This adder results the three errors in sum and one error in carry. The sum and carry expression of the approximate adder is shown in equation 3 and 4. The authors proposed the circuit using gpdk 180nm technology. The circuit uses the Static logic for implementation of the circuit. The Sum is inverter of Carry circuit.

$$Sum = \sim Carry \qquad (3)$$

$$Carry = (B.\ C) + A \qquad (4)$$

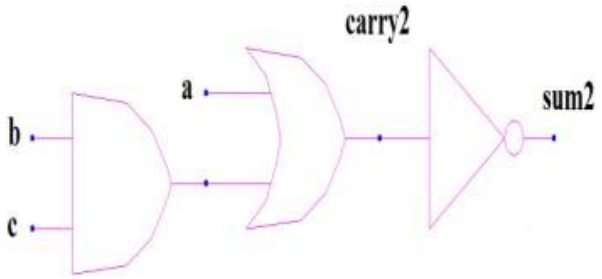


Fig 2.2. Existing Approximate Adder 2 circuit (AA2)

2.3 Existing Approximate Adder 3

The Authors M. Ramaswamy, G. Narmadha, S. Deviasigamani proposed another new approximate adder as shown in Fig 2.3, with 18 number of transistors. The proposed approximate adder consistsof sum have two errors whereas carry contains two errors. As compared to the exact adder the proposed adder has 6 less number of transistors. This adder has circuit area when compared to previous adders. The sum and carry expression of the approximate adder is shown in Equations 5 and 6. The authors proposed the circuit using gpdk 180nm technology. The circuit uses the Static logicfor implementation of the circuit. The Sum

is inverter of Carry circuit.

$$Sum = \sim Carry \quad (5)$$

$$Carry = (A \,.\, B) \wedge C \quad (6)$$

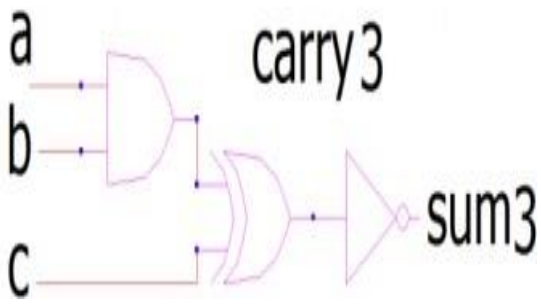


Fig 2.3. Existing Approximate Adder 3 circuit AA3)

2.4 Existing Approximate Adder 4

The Authors M. Ramaswamy, G. Narmadha, S. Deviasigamani proposed another new approximate adder as shown in Fig 2.4, with 14 transistors. The proposed approximate adder having two errorsin sum and no errors in carry. As compared to the exact adder the proposed adder has 10 less numberof transistors. The sum and carry expression of the approximate adder is shown in equation 7 and 8.The authors proposed the circuit using gpdk 180nm technology. The circuit uses the Static logic for implementation of the circuit. The Sum is inverter of Carry circuit.

$$Sum = \sim Carry \quad (7)$$

$$Carry = AB + BC + CA \quad (8)$$

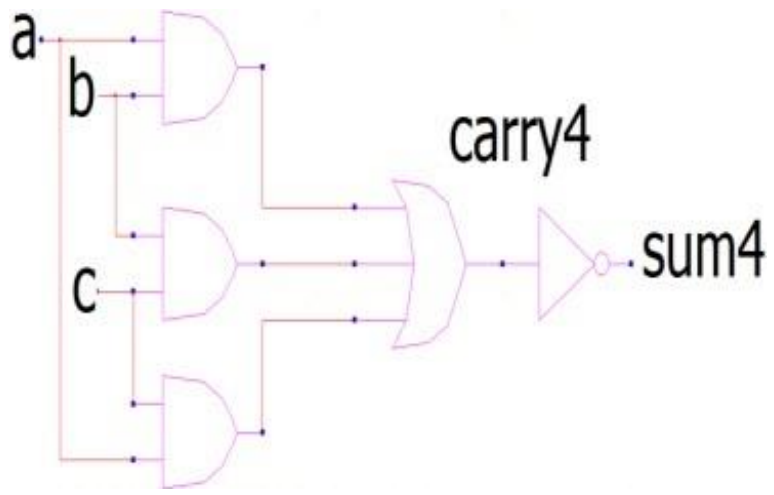


Fig 2.4. Existing Approximate Adder 4 circuit(AA4)

2.5 Existing Approximate Adder 5

The Authors V. Gupta, D. Mohapatra, A.Raghu Nathan Proposed a new approximate adder as shownin Fig 2.5, with 16 number of transistors. The proposed approximate adder results outputs sum having two errors and carry doesn't contain any error. This adder having more number of transistorsand less number of errors. As compared to the exact adder the proposed adder has 8 less number of transistors. The sum and carry expression of the approximate adder is shown in equation 9 and 10. The authors proposed the circuit using gpdk 180nm technology. The circuit uses the Static logic for implementation of the circuit. The Sum is inverter of Carry circuit.

$$Sum' = ABC + \bar{A}BC \qquad (9)$$

$$Carry' = ABC + AB\bar{C} + \bar{A}B\bar{C} + A\bar{B}C + \bar{A}\,B\bar{C} \qquad (10)$$

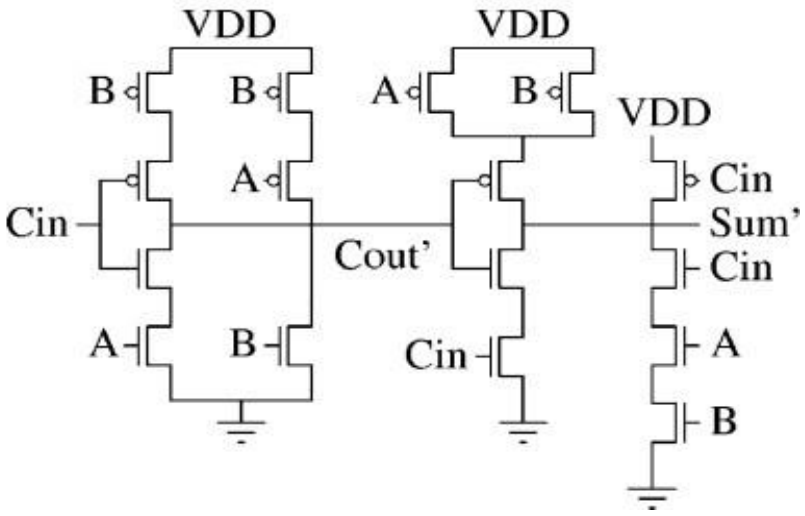


Fig 2.5. Existing Approximate Adder 5 circuit (AA5)

2.6 Existing Approximate Adder 6

The Authors V. Gupta, D. Mohapatra, A. Raghu Nathan Proposed another new approximate adder asshown in Fig 2.6, with 16 number of transistors. The proposed approximate adder sum results twoerrors where carry have zero errors. This adder comprises 8 less transistors when compared with exact adder. The sum and carry expression of the approximate adder is shown in equation 11 and 12.The authors proposed the circuit using gpdk 180nm technology. The circuit uses the Static logic forimplementation of the circuit. The Sum is inverter of Carry circuit.

$$Sum=\overline{Carry'} \qquad (11)$$

$$Carry' = AB+\bar{A}BC+A\bar{B}C \qquad (12)$$

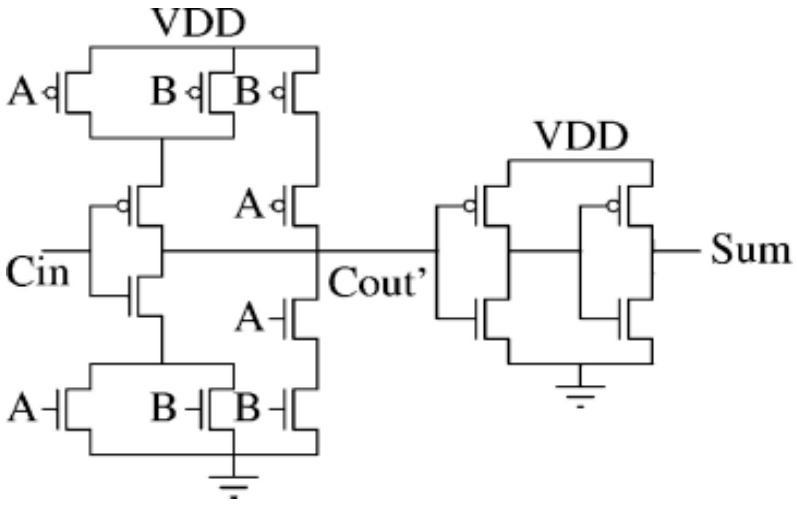


Fig 2.6. Existing Approximate Adder 6 circuit(AA6)

2.7 Existing Approximate Adder 7

The Authors V. Gupta, D. Mohapatra, A. Raghu Nathan Proposed another new approximate adder asshown in Fig 2.7, with 13 number of transistors. The proposed approximate adder containing threeerrors in sum and one error in carry. This adder comprises 11 less transistors when compared with exact adder. Even-though it having less number of transistors but it having the more number of errors,Which causes the adder inefficient. The sum and carry expression of the approximate adder is shownin equation 13 and 14. The authors proposed the circuit using gpdk 180nm technology. The circuit uses the Static logic for implementation of the circuit. The Sum is inverter of Carry circuit.

$$Sum = \sim carry' \tag{13}$$

$$Carry' = ABC + AB\bar{C} + \bar{A}BC + A\bar{B}C + \bar{A}B\bar{C} \tag{14}$$

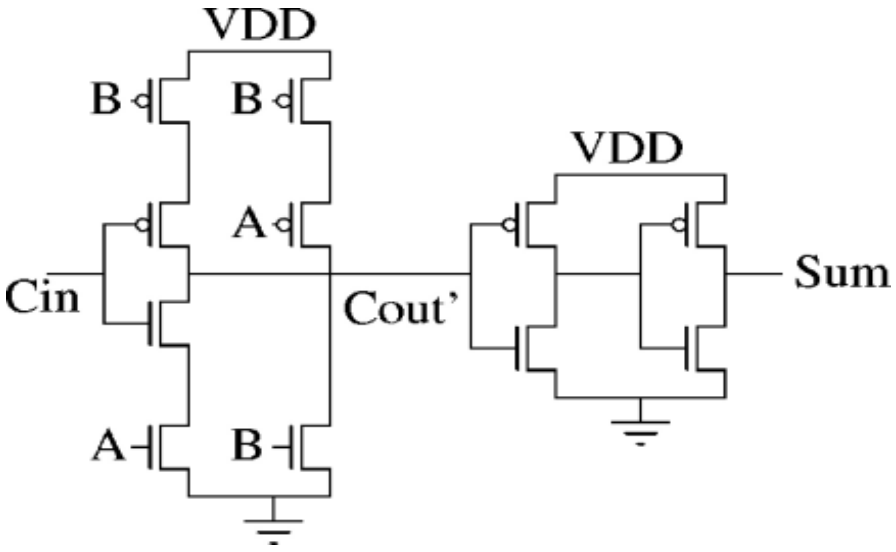


Fig 2.7. Existing Approximate Adder 7 circuit (AA7)

2.8 Existing Approximate Adder 8

The Authors V. Gupta, D. Mohapatra, A. Raghu Nathan Proposed another new approximate adder asshown in Fig 2.8, with 11 number of transistors. The proposed approximate adder contains three errors in sum and carry contains two errors a total of five errors which leads to adder inefficient. Thisadder comprises 13 less transistors when compared with exact adder. The sum and carry expressionof the approximate adder is shown in equation 15 and 16. The authors proposed the circuit using gpdk180nm technology. The circuit uses the Static logic for implementation of the circuit. The Sum is inverter of Carry circuit.

$$Sum' = \bar{A}BC + A\bar{B}C + ABC \quad (15)$$

$$Carry' = A \quad (16)$$

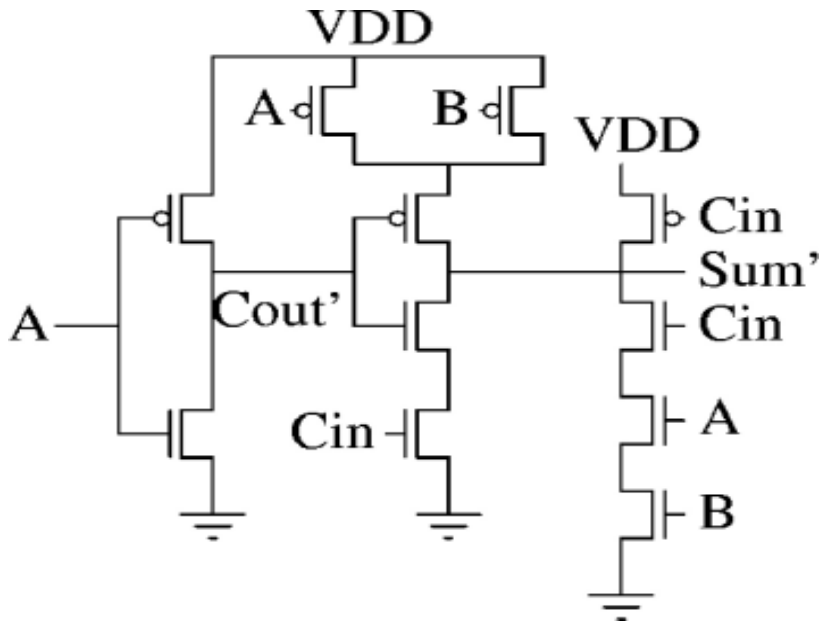


Fig 2.8. Existing Approximate Adder 8 circuit (AA8)

2.9 Existing Approximate Adder 9

The Authors Bhargav A, Huynh p proposed a new approximate adder as shown in Fig 2.9, with 13number of transistors. The proposed approximate adder has two errors in sum and no errors in carry.They proposed the adder using CNFET 32nm technology. This adder comprises 11 less transistors when compared with exact adder. The sum and carry expression of the approximate adder is shown in equation 17 and 18. The circuit uses the Static logic for implementation of the circuit. The Sum is inverter of Carry circuit.

$$Sum=\overline{(A+BC)+\bar{A}BC} \qquad (17)$$

$$Carry=(A+BC)+\bar{A}BC \qquad (18)$$

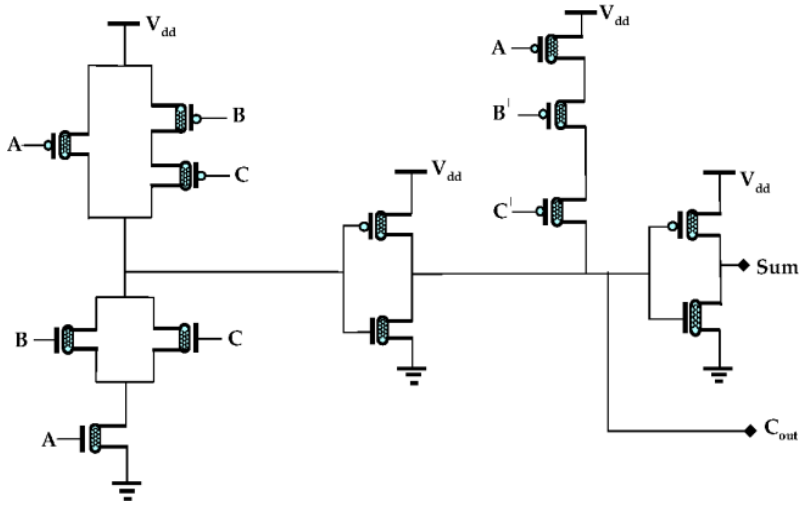


Fig 2.9 Existing Approximate Adder 9 circuit (AA9)

2.10 Existing Approximate Adder 10

The Authors Bhargav A, Huynh p proposed a new approximate adder as shown in Fig 2.10, with 10 number of transistors. The proposed approximate adder has two errors in sum and no errors in carry. They proposed the adder using CNFET 32nm technology. Due to less number of transistors this adder occupies the less circuit area. This adder comprises 14 less transistors when compared withexact adder. The sum and carry expression of the approximate adder is shown in equation 19 and 20.The circuit uses the Static logic for implementation of the circuit. The Sum is inverter of Carry circuit.

$$\text{Sum}=\overline{(A+BC)}+A\overline{BC} \qquad (19)$$

$$\text{Carry}=\overline{(\overline{A+BC})+A\overline{BC}} \qquad (20)$$

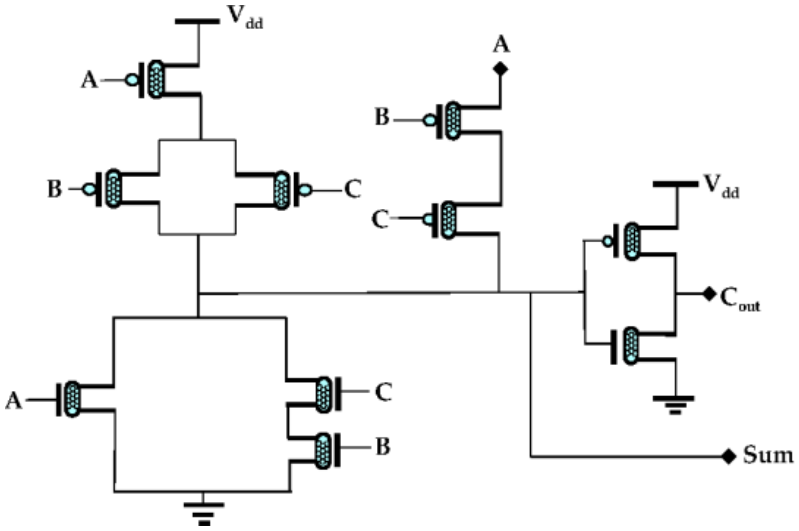


Fig 2.10. Existing Approximate Adder 10 circuit (AA10)

Summary:

In this chapter, all the 10 existing adders are discussed. In those 10 existing approximate adders, AA3(Fig 2.3) has more number of transistors i.e., 18. The approximate adder AA10(Fig 2.10) has less number of transistors i.e.,10. In those 10 1-Bit approximate adders AA8(Fig 2.8) has more number of errors i.e.,5 errors. For AA8, Sum has 3 errors and Carry has 2 errors. The 1-bit approximate adders AA4(Fig 2.4), AA9(Fig 2.9), AA10(Fig 2.10) has the less number of errors i.e., 2 errors. For AA4, AA9, AA10 those 2 errors are present in Sum.All the 10 adders are designed in different technologies.

CHAPTER 3

PROPOSED 1-BIT APPROXIMATE ADDERS

In this chapter all the 10 Existing adders are simulated with the help of CNFET 32nm technology for low power consumption and five new approximate adder circuits are proposed. With the help of existing adders 5 different 1-bit approximate adders are proposed using CNTFET 32nm technology. Here we can observe the power, delay and PDP of all the 15 approximate adders.

3.1 Proposed Approximate Adders

3.1.1 Proposed Approximate Adder1

The Proposed adder was designed using equations (1) and (2) with CNTFET transistors, which is designed using Fig 3.1. It consists of 14 transistors. Table 1(a) shows the errors in sum and carry for the Fig 3.1. It having 3 errors in Sum and 1 error in Carry respectively. It uses Static logic for Implementation. This proposed adder has seven P- CNFET transistors and seven N-CNFET transistors. It uses 32nm CNFET Technology forthe simulation of the results. Here, Sum is inverter of the carry output.

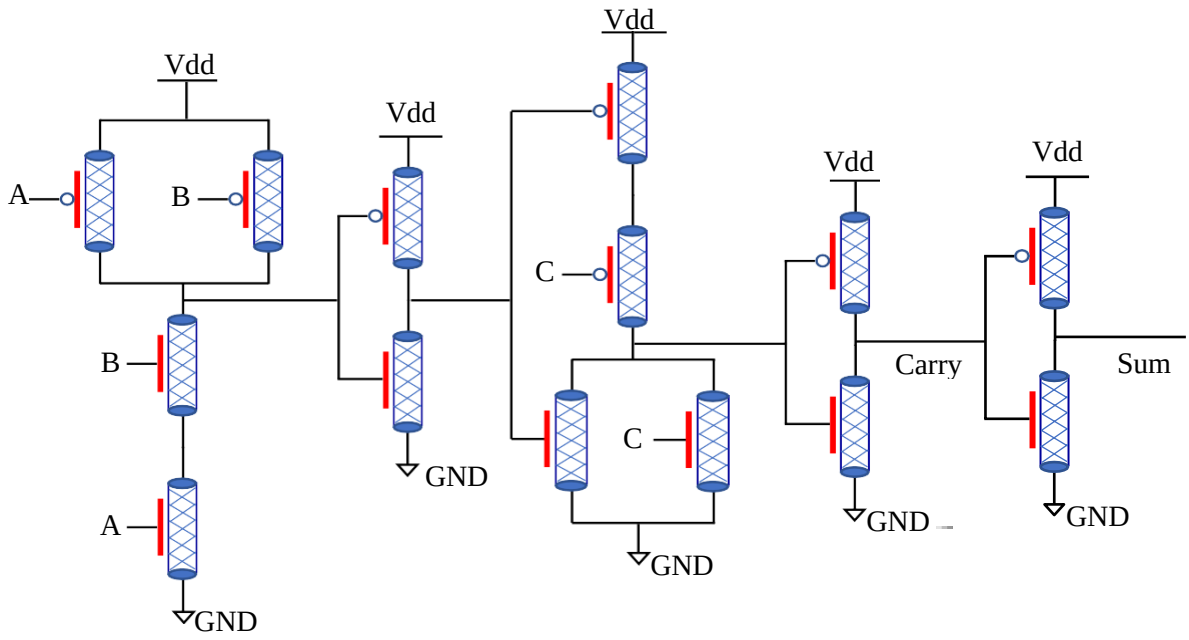


Fig 3.1. Proposed Approximate Adder 1 circuit (AA1)

3.1.2 Proposed Approximate Adder 2

The proposed adder was designed using equation (3) and (4) with CNTFET transistors, which is designed using Fig 3.2. It consists of 14 transistors. Table 1(a) shows the errors in Sum and Carry for the Fig 3.2. It having three errors in Sum and zero errors in Carry respectively. It uses Static logic for Implementation. It has 14 less number of transistors than the conventional adder. Due to this it comprises of less power and delay compared to conventional full adder. This proposed adder has seven P- CNFET transistors and seven N- CNFET transistors. It uses 32nm CNFET Technologyfor the simulation of the results. Here, Sum is inverter of the Carry output.

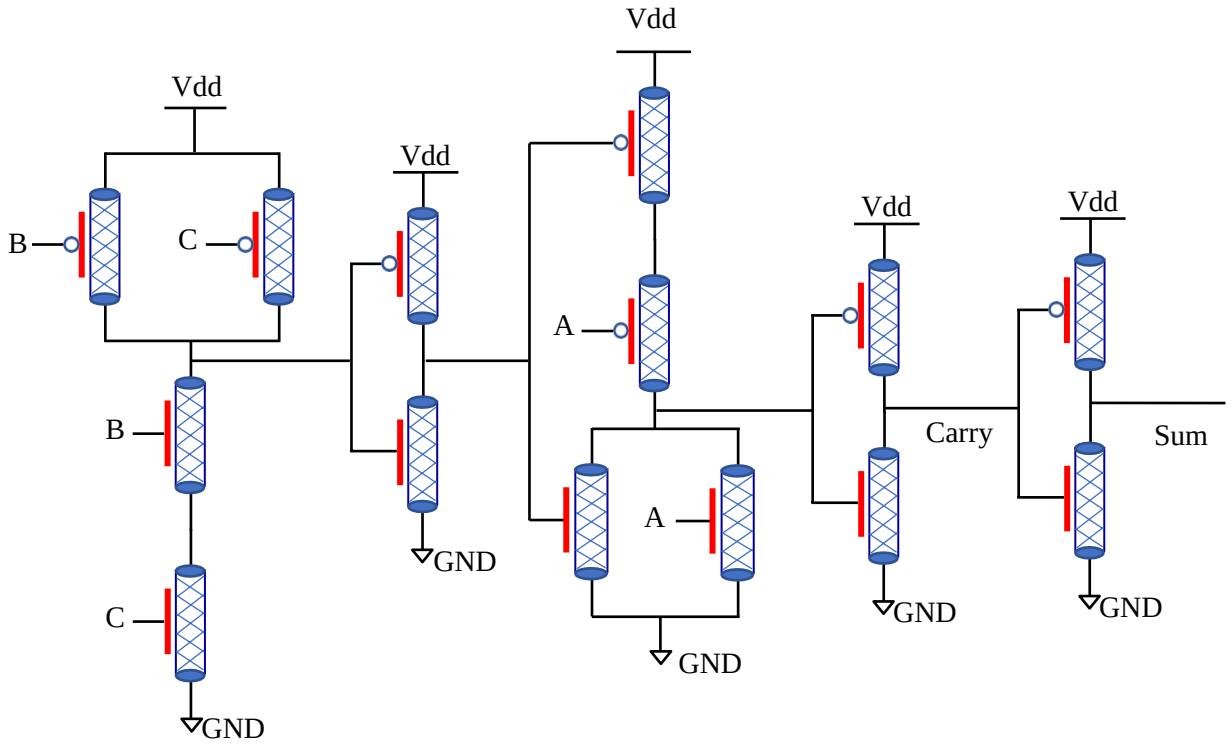


Fig 3.2. Proposed Approximate Adder 2 circuit (AA2)

3.1.3 Proposed Approximate Adder 3

The proposed adder was designed using equation (5) and (6) with CNTFET transistors, which is designed using Fig 3.3. It consists of 18 transistors. Table 1(a) shows the errors in Sum and Carry for the Fig 3.3. It having two errors in Sum and two errors in Carry respectively. It uses Static logicfor Implementation. It has 10 less number of transistors than the conventional adder. Due to this it comprises of less power and delay compared to conventional full adder. This proposed adder has nineP- CNFET transistors and nine N- CNFET transistors. It uses 32nm CNFET Technology for the simulation of the results. Here, Sum is inverter of the Carry output.

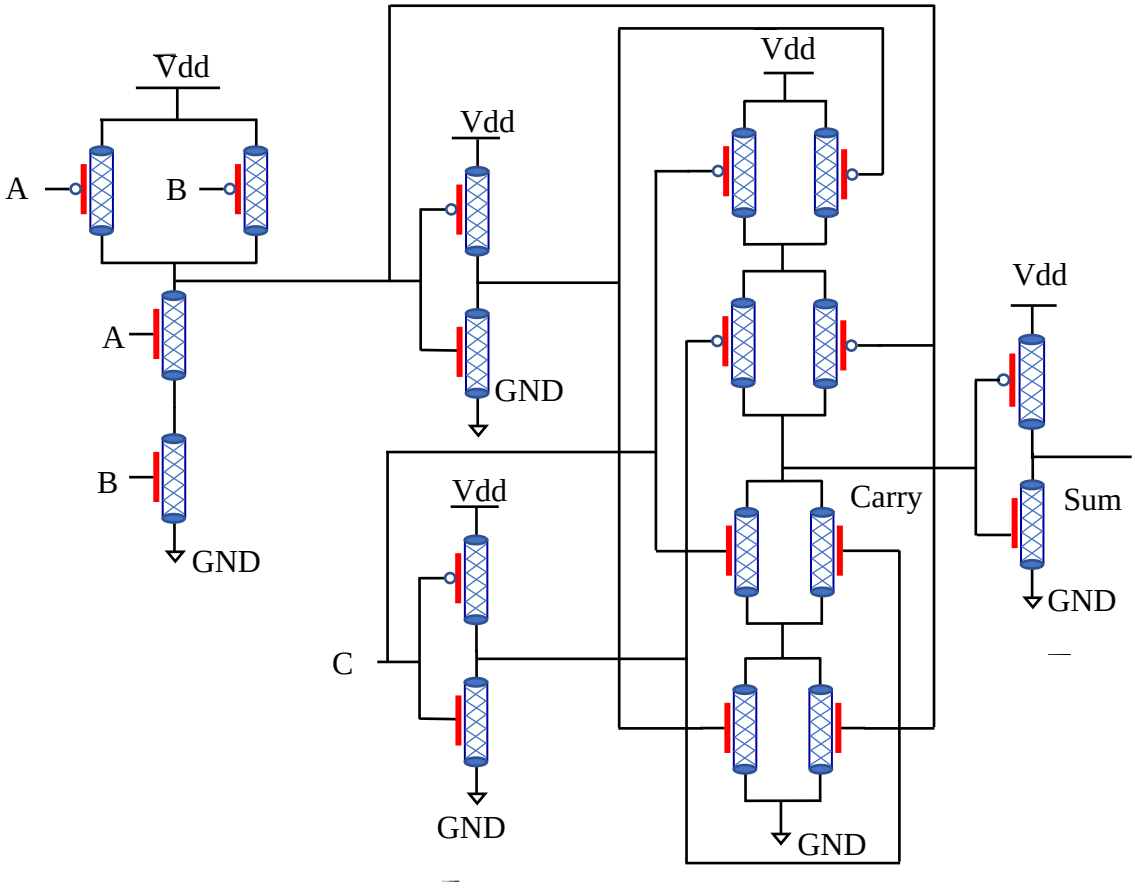


Fig 3.3. Proposed Approximate Adder3 circuit (AA3)

3.1.4 Proposed Approximate Adder 4

The proposed adder was designed using equation (7) and (8), with CNTFET transistors, which is designed using Fig 3.4. It consists of 14 transistors. Table 1(a) shows the errors in sum and carry for the Fig 3.4. It having two errors in Sum and zero errors in Carry respectively. It uses Static logicfor Implementation. It has 14 less number of transistors than the conventional adder. Due to this it comprises of less power and delay compared to conventional full adder. This proposed adder has seven P- CNFET transistors and seven N- CNFET transistors. It uses 32nm CNFET Technology forthe simulation of the results. Here, Sum is inverter of the carry output.

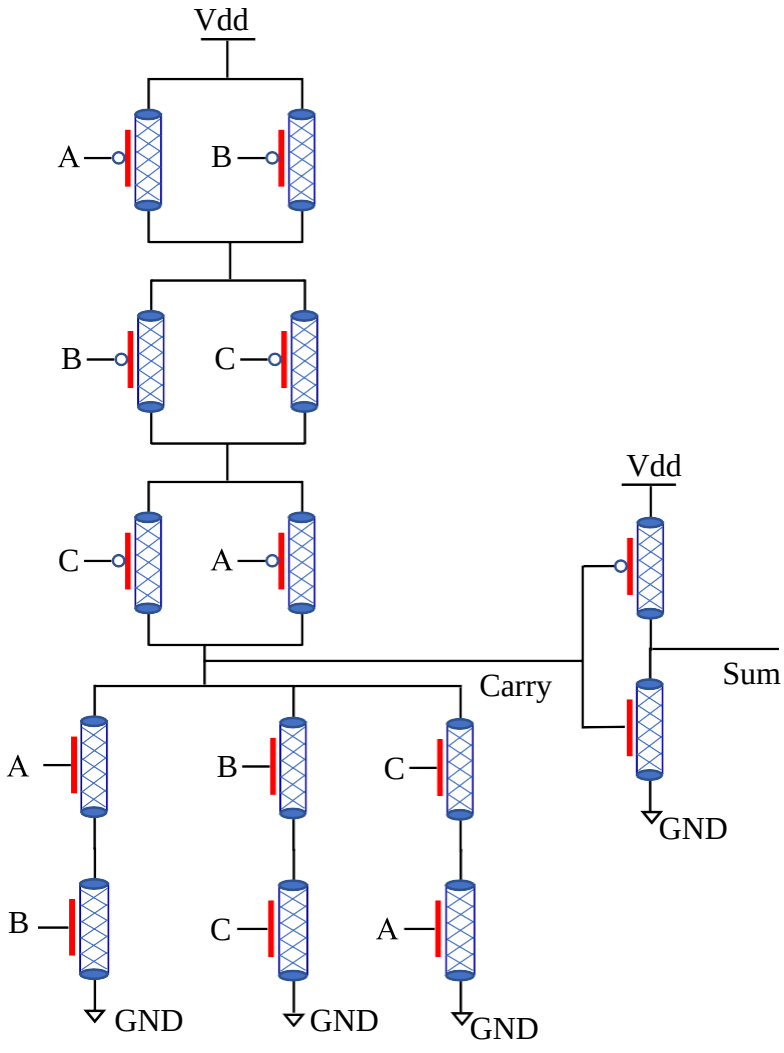


Fig 3.4. Proposed Approximate Adder 4 circuit (AA4)

3.1.5 Proposed Approximate Adder 5

The proposed adder was designed using equation (9) and (10) with CNTFET transistors, which is designed using Fig 3.5. It consists of 16 transistors. Table 1(a) shows the errors in Sum and Carry for the Fig 3.5. It having two errors in Sum and zero errors in Carry respectively. It uses Static logicfor Implementation. It has 12 less number of transistors than the conventional adder. Due to this it comprises of less power and delay compared to conventional full adder. This proposed adder has eight P- CNFET transistors and eight N- CNFET transistors. It uses 32nm CNFET Technology for the simulation of the results.

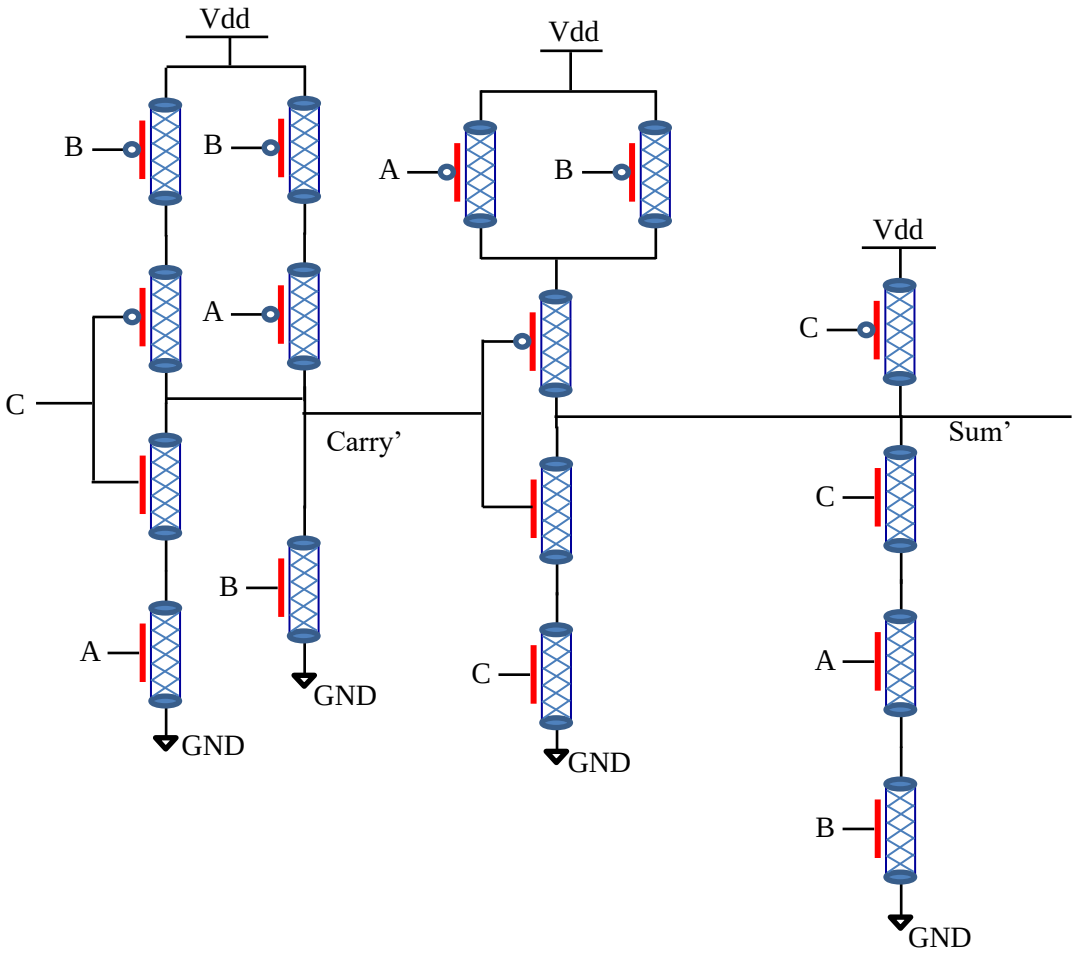


Fig 3.5. Proposed Approximate Adder 5 circuit (AA5)

3.1.6 Proposed Approximate Adder 6

The proposed adder was designed using equation (11) and (12) with CNTFET transistors, which is designed using Fig 3.6. It consists of 14 transistors. Table 1(b) shows the errors in Sum and Carryfor the Fig 3.6. It having two errors in Sum and zero errors in Carry respectively. It uses Static logicfor Implementation. It has 14 less number of transistors than the conventional adder. Due to this it comprises of less power and delay compared to conventional full adder. This proposed adder has seven P- CNFET transistors and seven N- CNFET transistors. It uses 32nm CNFET Technology forthe simulation of the results. Here, Sum is inverter of the Carry output.

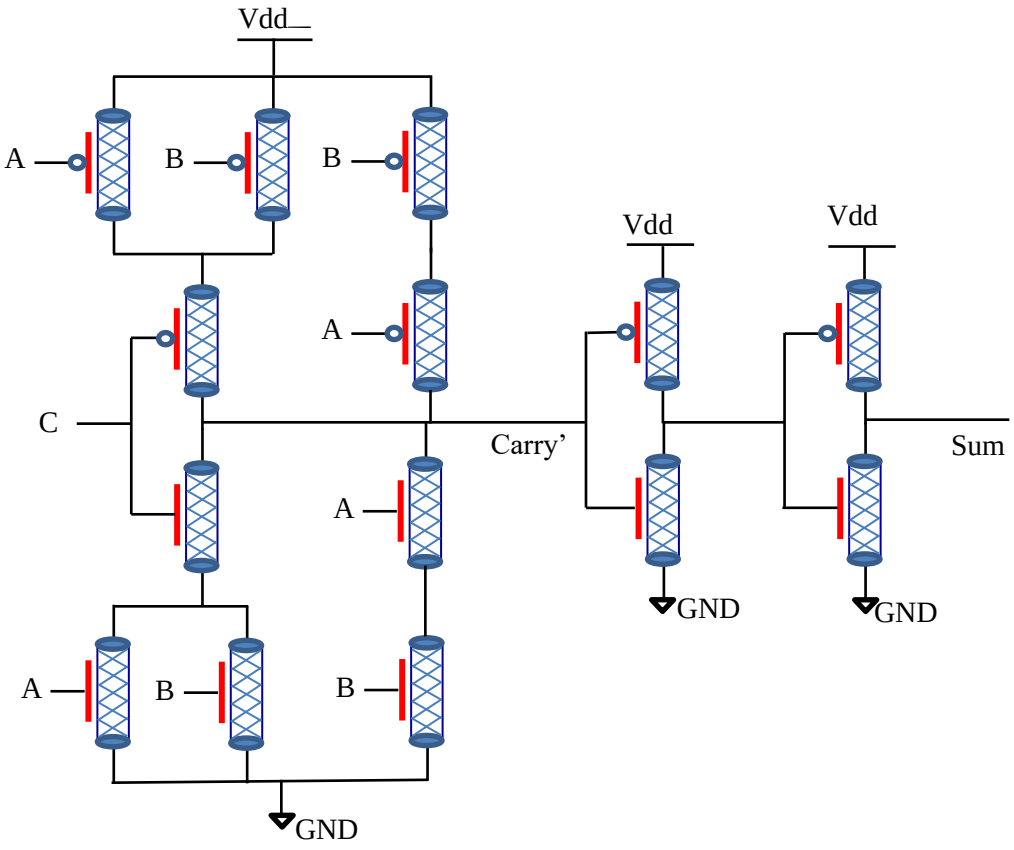


Fig 3.6. Proposed Approximate Adder 6 circuit (AA6)

3.1.7 Proposed Approximate Adder 7

The proposed adder was designed using equation (13) and (14) with CNTFET transistors, which is designed using Fig 3.7. It consists of 13 transistors. Table 1(b) shows the errors in Sum and Carryfor the Fig 3.7. It having three errors in Sum and one error in Carry respectively. It uses Static logicfor Implementation. It has 15 less number of transistors than the conventional adder. Due to this it comprises of less power and delay compared to conventional full adder. This proposed adder has seven P- CNFET transistors and six N- CNFET transistors. It uses 32nm CNFET Technology for thesimulation of the results. Here, Sum is inverter of the Carry output.

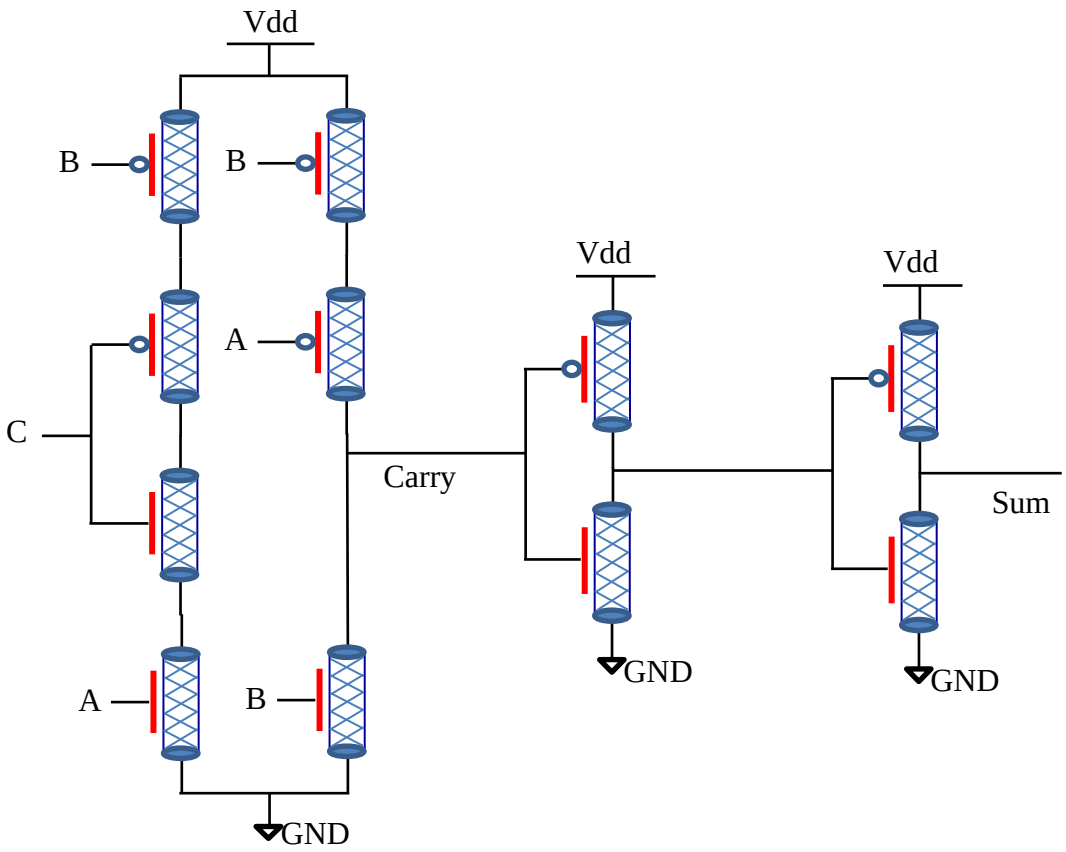


Fig 3.7. Proposed Approximate Adder 7 circuit (AA7).

3.1.8 Proposed Approximate Adder 8

The proposed adder was designed using equation (15) and (16) with CNTFET transistors, which is designed using Fig 3.8. It consists of 11 transistors. Table 1(b) shows the errors in Sum and Carry for the Fig 3.8. It having three errors in Sum and two errors in Carry respectively. It uses Static logic for Implementation. It has 17 less number of transistors than the conventional adder. Due to this it comprises of less power and delay compared to conventional full adder. This proposed adder has five P- CNFET transistors and six N- CNFET transistors. It uses 32nm CNFET Technology for the simulation of the results. Here, Sum is inverter of the carry output.

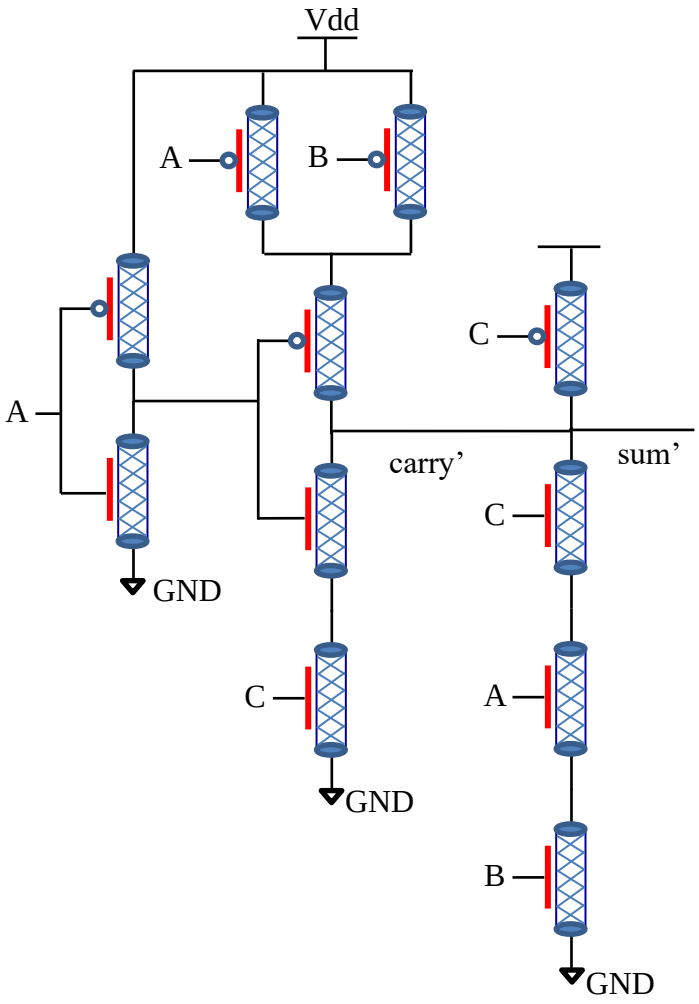


Fig 3.8. Proposed Approximate Adder 8 circuit (AA8)

3.1.9 Proposed Approximate Adder 9

The proposed adder was designed using equation (17) and (18) with CNTFET transistors, which is designed using Fig 3.9. It consists of 13 transistors. Table 1(b) shows the errors in Sum and Carryfor the Fig 3.9. It having two errors in Sum and zero error in Carry respectively. It uses Static logicfor Implementation. It has 15 less number of transistors than the conventional adder. Due to this it comprises of less power and delay compared to conventional full adder. This proposed adder has eight P- CNFET transistors and five N- CNFET transistors. It uses 32nm CNFET Technology for thesimulation of the results. Here, Sum is inverter of the carry output.

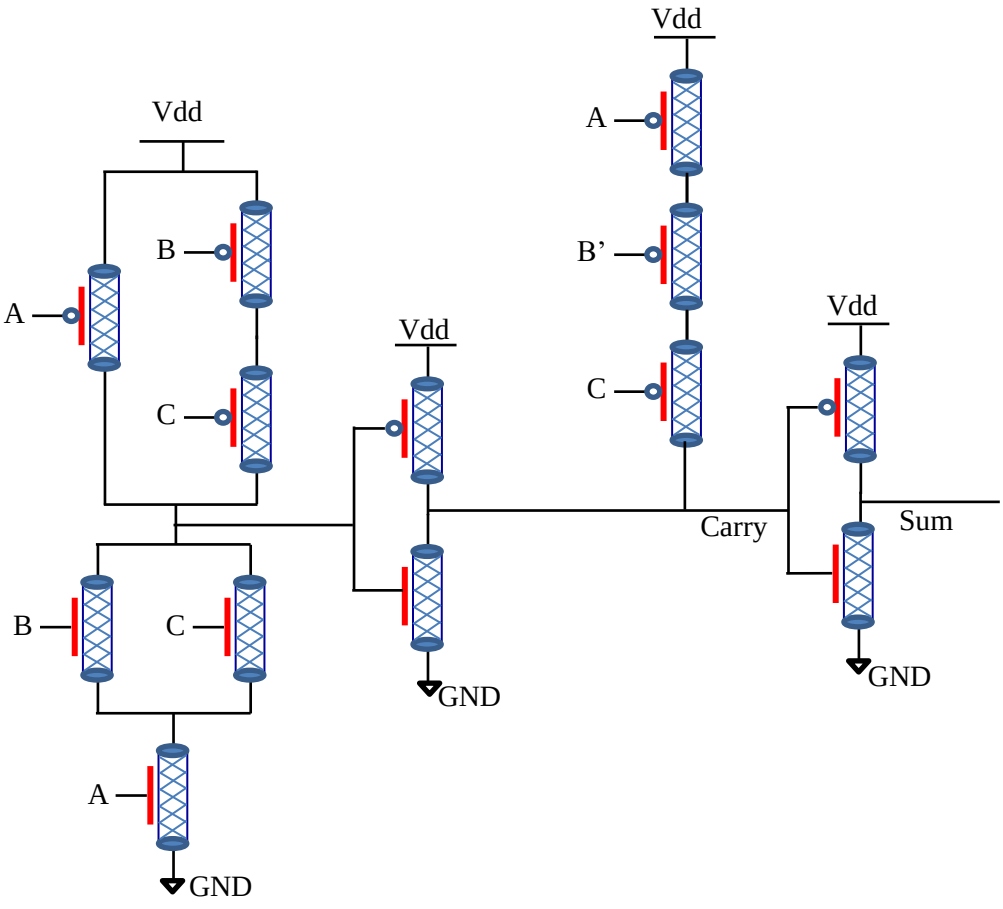


Fig 3.9. Proposed Approximate Adder 9 circuit (AA9)

3.1.10 Proposed Approximate Adder 10

The proposed adder was designed using equation (19) and (20) with CNTFET transistors, which is designed using Fig 3.10. It consists of 10 transistors. Table 1(b) shows the errors in Sum and Carryfor the Fig 3.10. It having two errors in Sum and zero error in Carry respectively. It uses Static logic for Implementation. It has 18 less number of transistors than the conventional adder. Due to this it comprises of less power and delay compared to conventional full adder. This proposed adder has six P- CNFET transistors and four N- CNFET transistors. It uses 32nm CNFET Technology forthe simulation of the results. Here, Carry is inverter of the Sum output.

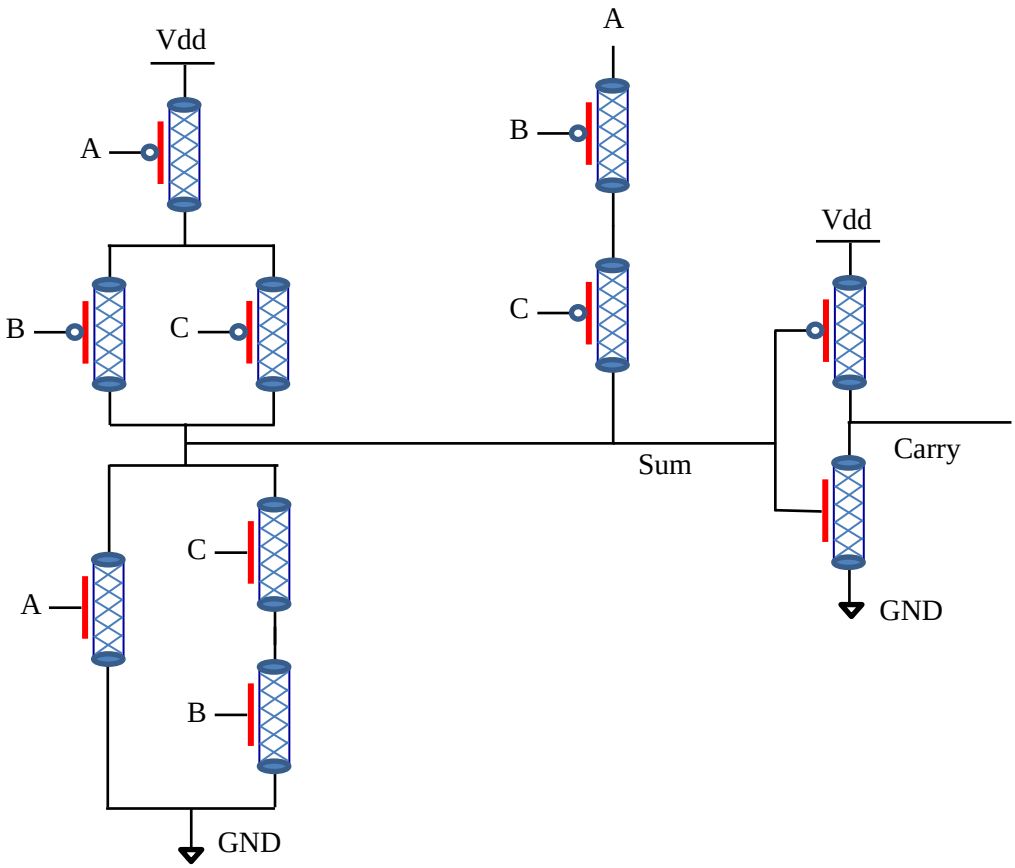


Fig 3.10. Proposed Approximate Adder 10 circuit (AA10)

3.1.11 Proposed Approximate Adder 11

The proposed adder was designed using equations (21) and (22) with CNTFET transistors, which is designed using Fig 3.11. It consists of 10 transistors. Table 1(c) shows the errors in Sum and Carry forFig 3.11. It has one error in Sum and three errors in Carry respectively. It uses Pass Transistor Logic (PTL) for Implementation. It has 18 less number of transistors than the conventional adder. Due to this it comprises of less power and delay compared to conventional full adder. This proposed adder has fiveP- CNFET transistors and five N- CNFET transistors. It uses 32nm CNFET Technology for the simulation of the results. Here, Carry is inverter of the Sum output.

$$\text{Sum= A } (\overline{B \wedge C}) + \bar{A}(\text{B}\wedge\text{C}) \qquad (21)$$

$$\text{Carry = A(B}\wedge\text{C) + } \bar{A}\ (\overline{B \wedge C}) \qquad (22)$$

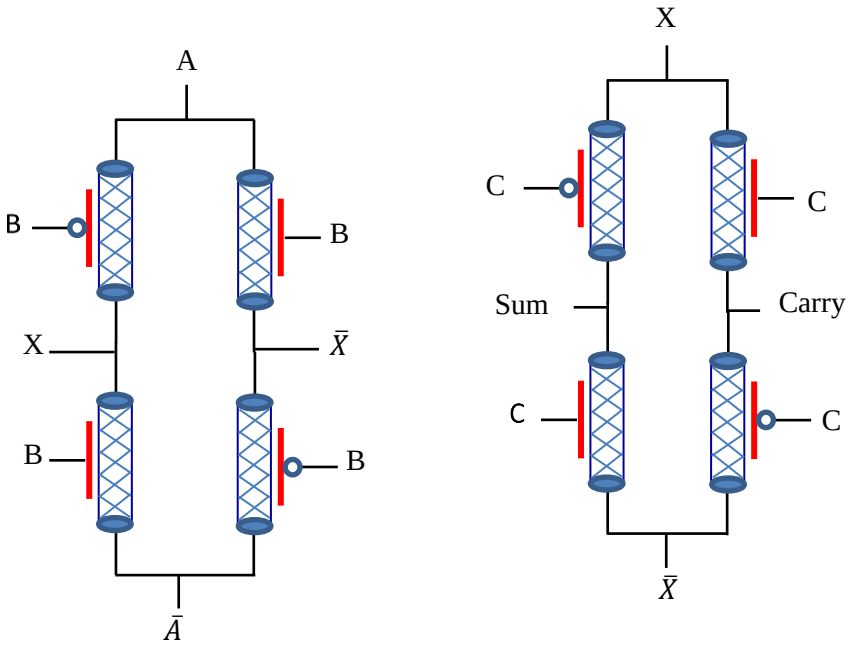


Fig 3.11. Proposed Approximate Adder 11 circuit (AA11)

3.1.12 Proposed Approximate Adder 12

The proposed adder was designed using equations (23) and (24) with CNTFET transistors, which is designed using Fig 3.12. It consists of 10 transistors. The omissions in Sum and in Carry for Fig 3.12are shown in Table 1(c). Sum and Carry has one error each. It uses Pass Transistor Logic (PTL) for Implementation. It has 18 less number of transistors than the conventional adder. Due to this it comprisesof less power and delay compared to conventional full adder. This proposed adder has six P- CNFET transistors and four N- CNFET transistors. It uses 32nm CNFET Technology for the simulation of the results. Here, Sum is inverter of the Carry output.

$$\text{Sum}= \bar{A}(B\hat{}C)+A\bar{B}\bar{C} \qquad (23)$$

$$\text{Carry}=AB+ \bar{A}\bar{B}\bar{C} +C(A+B) \qquad (24)$$

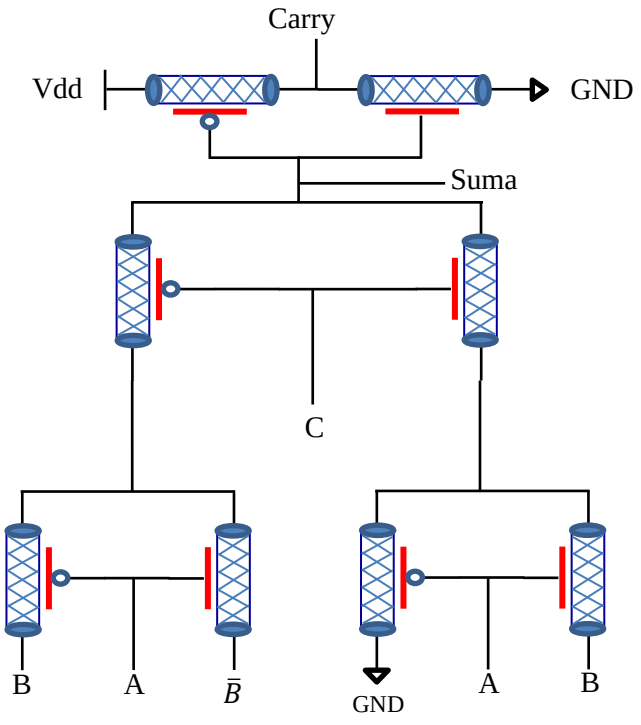


Fig 3.12. Proposed Approximate Adder 12 circuit (AA12)

3.1.13 Proposed Approximate Adder 13

The proposed adder was designed using equation (25) and (26) with CNTFET transistors, which is designed using Fig 3.13. It consists of 10 transistors. Table 1(c) shows the errors in Sum and Carryfor the Fig 3.13. It having zero errors in Sum and two errors in Carry respectively. It uses Pass Transistor logic (PTL) for Implementation. It has 18 less number of transistors than the conventionaladder. Due to this it comprises of less power and delay compared to conventional full adder. This proposed adder has five P- CNFET transistors and five N- CNFET transistors. It uses 32nm CNFET Technology for the simulation of the results. Here, Carry is inverter of the Sum output.

$$\text{Sum} = \bar{A}(B \hat{} C) + ABC \qquad (25)$$

$$\text{Carry} = \bar{A}BC + A(\bar{B} + \bar{C}) + \bar{B}\bar{C} \qquad (26)$$

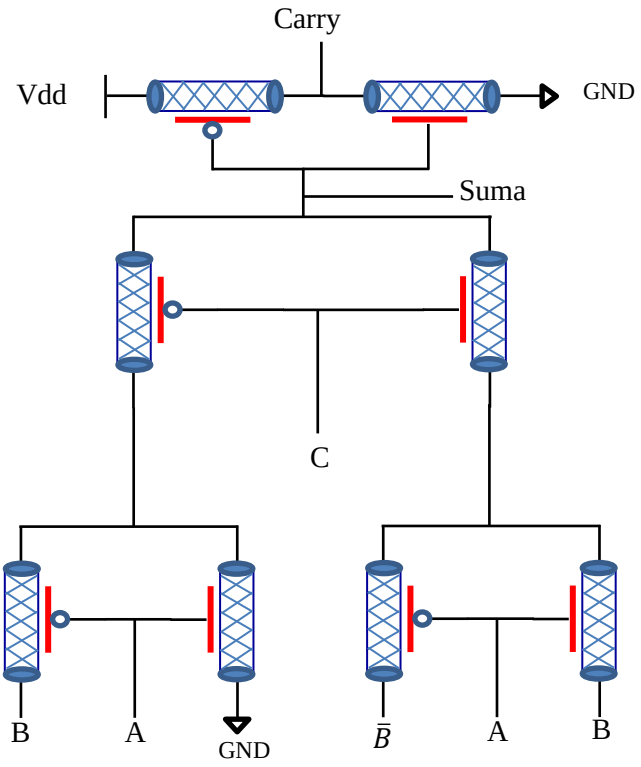


Fig 3.13. Proposed Approximate Adder 13 circuit (AA13)

3.1.14 Proposed Approximate Adder 14

The proposed adder was designed using equation (27) and (28) with CNTFET transistors, which is designed using Fig 3.14. It consists of 8 transistors. Table 1(c) shows the errors in Sum and Carry for the Fig 3.14. It having two errors in Sum and zero errors in Carry respectively. It uses Pass Transistorlogic (PTL) for Implementation. It has 20 less number of transistors than the conventional adder. Due to this it comprises of less power and delay compared to conventional full adder. This proposed adder has four P- CNFET transistors and four N- CNFET transistors. It uses 32nm CNFET Technology for the simulation of the results. Here, Carry is inverter of the Sum output.

$$Sum = \bar{B}(\bar{A} + \bar{C}) + \bar{A}B\bar{C} \qquad (27)$$

$$Carry = AB + BC + CA \qquad (28)$$

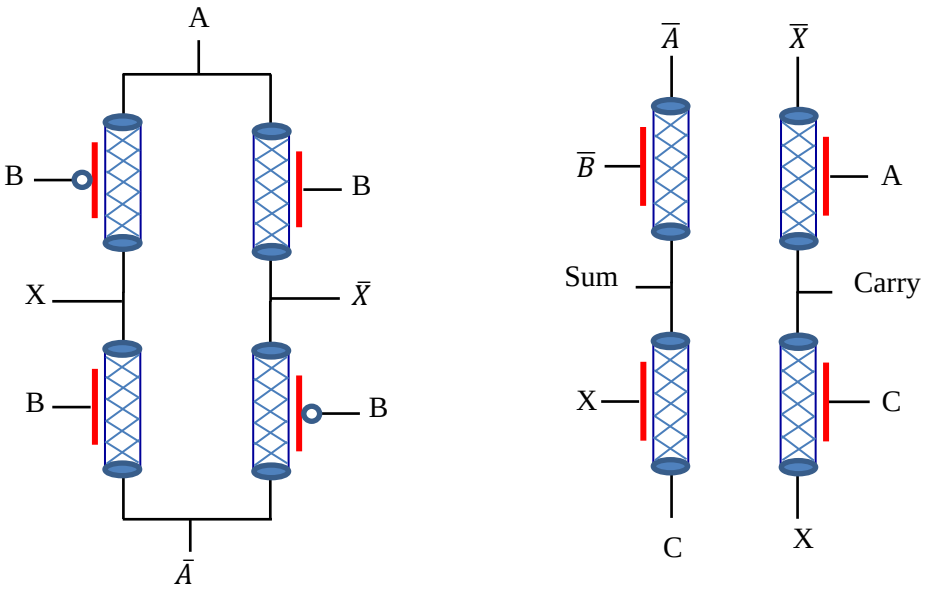


Fig 3.14. Proposed Approximate Adder 14 circuit (AA14)

3.1.15 Proposed Approximate Adder 15

The proposed adder was designed using equation (29) and (30) with CNTFET transistors, which is designed using Fig 3.15. It consists of 8 transistors. Table 1(c) shows the errors in Sum and Carry for the Fig 3.15. It having two errors in Sum and zero errors in Carry respectively. It uses Pass Transistorlogic (PTL) for Implementation. It has 22 less number of transistors than the conventional adder. Due to this it comprises of less power and delay compared to conventional full adder. This proposed adder has three P- CNFET transistors and three N- CNFET transistors. It uses 32nm CNFET Technology for the simulation of the results. Here, Sum is inverter of the Carry output.

$$Sum = \bar{B}(\bar{A} + \bar{C}) + \bar{A}B\bar{C} \qquad (27)$$

$$Carry = AB + BC + CA \qquad (28)$$

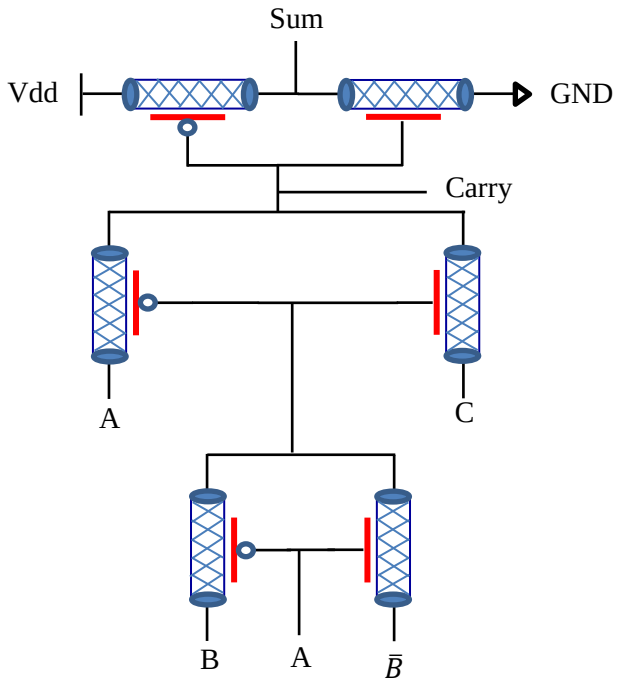


Fig 3.15. Proposed Approximate Adder 15 circuit (AA15)

Table 1(a). Truth table for Approximate Adder 1-5

Inputs			Exact Adder		AA1		AA2		AA3		AA4		AA5	
A	B	C	Sum	Carry	Sum	Carry	Sum	Carry	Sum	Carry	Sum	Carry	Sum	Carry
0	0	0	0	0	1	0	1	0	1	0	1	0	0	0
0	0	1	1	0	0	1	1	0	0	1	1	0	1	0
0	1	0	1	0	1	0	1	0	1	0	1	0	0	1
0	1	1	0	1	0	1	0	1	0	1	0	1	0	1
1	0	0	1	0	1	0	0	0	1	0	1	0	0	0
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
1	1	0	0	1	0	1	0	1	0	1	0	1	0	1
1	1	1	1	1	0	1	0	1	1	0	1	1	1	1

Table 1(b). Truth table for Approximate Adder 6-10

Inputs			Exact Adder		AA6		AA7		AA8		AA9		AA10	
A	B	C	Sum	Carry	Sum	Carry	Sum	Carry	Sum	Carry	Sum	Carry	Sum	Carry
0	0	0	0	0	1	0	1	0	0	0	1	0	1	0
0	0	1	1	0	1	0	1	0	1	0	1	0	1	0
0	1	0	1	0	1	0	0	1	0	0	1	0	1	0
0	1	1	0	1	0	1	0	1	1	0	0	1	0	1
1	0	0	1	0	1	0	1	0	0	1	1	0	1	0
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
1	1	0	0	1	0	1	0	1	0	1	0	1	0	1
1	1	1	1	1	0	1	1	1	1	1	0	1	0	1

Table 1(c). Truth table for Approximate Adder 11-15

Inputs			Exact Adder		AA11		AA12		AA13		AA14		AA15	
A	B	C	Sum	Carry	Sum	Carry	Sum	Carry	Sum	Carry	Sum	Carry	Sum	Carry
0	0	0	0	0	0	1	0	1	0	0	1	0	1	0
0	0	1	1	0	1	0	1	0	1	0	1	0	1	0
0	1	0	1	0	0	0	0	0	0	0	1	0	1	0
0	1	1	0	1	1	0	0	1	1	0	0	1	0	1
1	0	0	1	0	0	1	0	0	0	1	1	0	1	0
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
1	1	0	0	1	0	1	0	1	0	1	0	1	0	1
1	1	1	1	1	1	0	0	1	1	1	0	1	0	1

Summary:

Finally, all the 15 1-bit approximate adders are simulated using CNTFET 32nm technology and Power, Delay, and PDP of all the adders are verified in those AA1-AA10 are existing adders simulated in CNTFET 32nm technology and remaining AA1-AA15 are newly proposed adders. From all the 15 adders AA15 has less number of transistors i.e.,6 and AA3 has more number of transistors i.e., 18. From those 15 adders AA8 has more number of errors i.e., 5 errors and AA4, AA9, AA10, AA12, AA13, AA14, AA15 has less number of errors i.e., 2 errors.

3.2 Transient Responses of 1-Bit Approximate Adders

3.2.1 Approximate Adder 1 Output Waveform

Fig 3.16 shows the transient response of Approximate adder1 as shown in Fig 3.1. Here a, b, c are the inputs of the adder and sum, carry are the outputs. The below figure represents all the combinations of the Proposed approximate adder1. In those at 000, 001, 111 cases having the error bits. The Adder has the supply voltage of +0.9v.

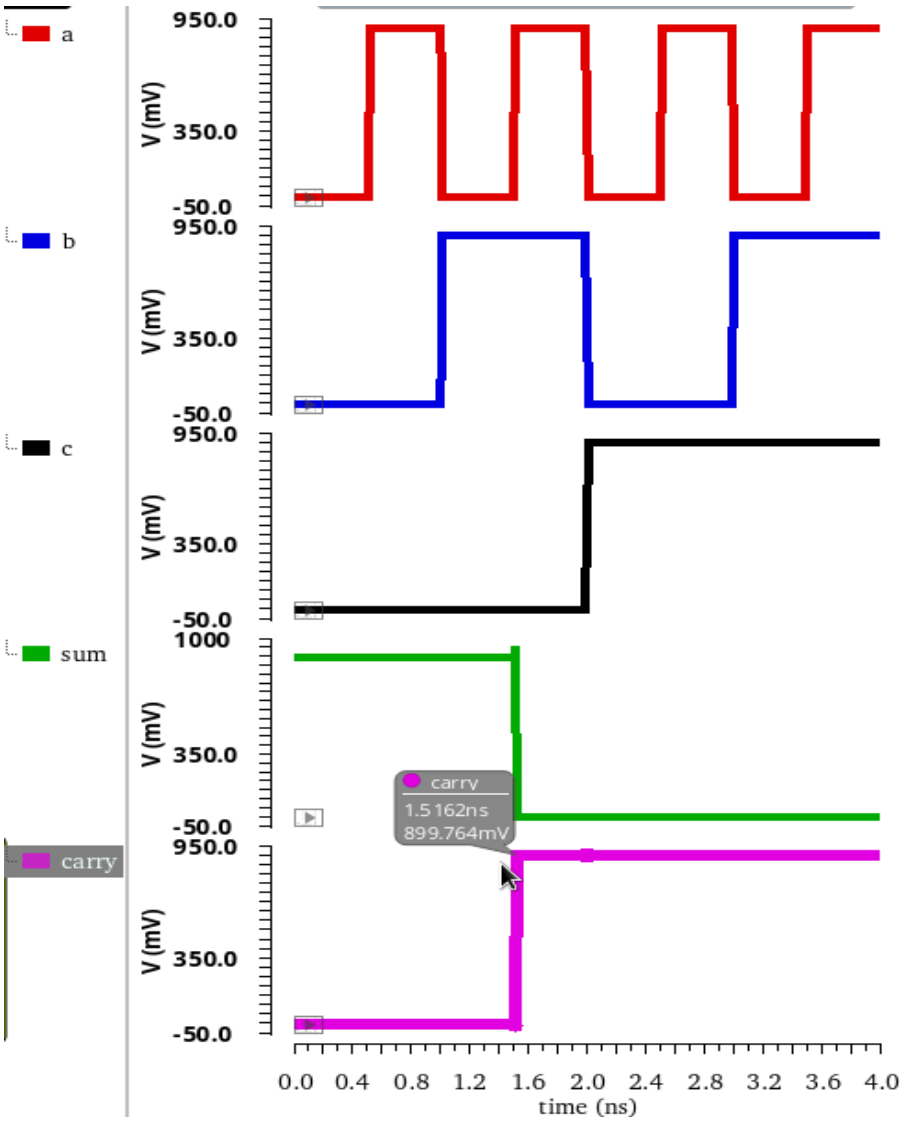


Fig 3.16 Output waveform of AA1 (Fig 3.1)

3.2.2 Approximate Adder 2 Output Waveform

Fig 3.17 shows the transient response of Approximate adder2 as shown in Fig 3.2. Here a, b, c are the inputs of the adder and sum, carry are the outputs. The below figure represents all the combinations of the Proposed approximate adder2. In those at 000, 100, 111 cases having the error bits. The Adder has the supply voltage of +0.9v.

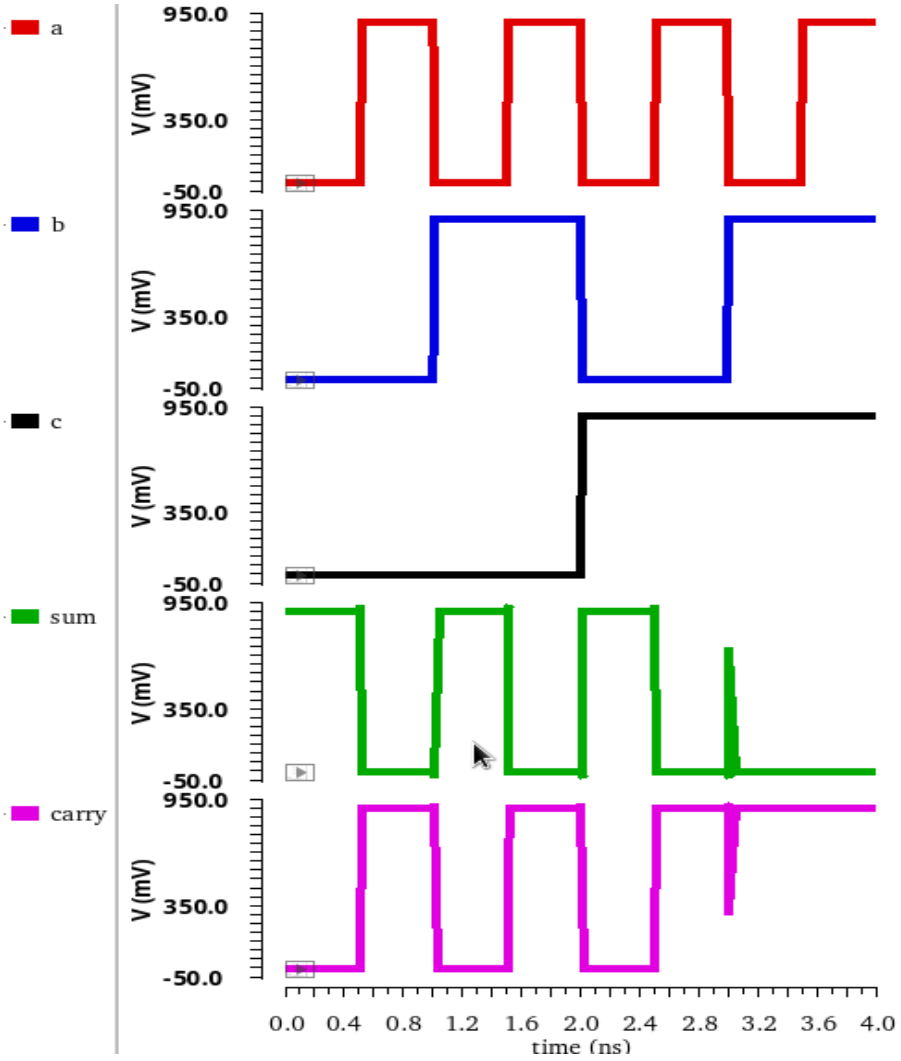


Fig 3.17 Output waveform of AA2 (Fig 3.2)

3.2.3 Approximate Adder 3 Output Waveform

Fig 3.18 shows the transient response of Approximate adder3 as shown in Fig 3.3. Here a, b, c are the inputs of the adder and sum, carry are the outputs. The below figure represents all the combinations of the Proposed approximate adder3. In those at 000, 001, 111 cases having the error bits. The Adder has the supply voltage of +0.9v.

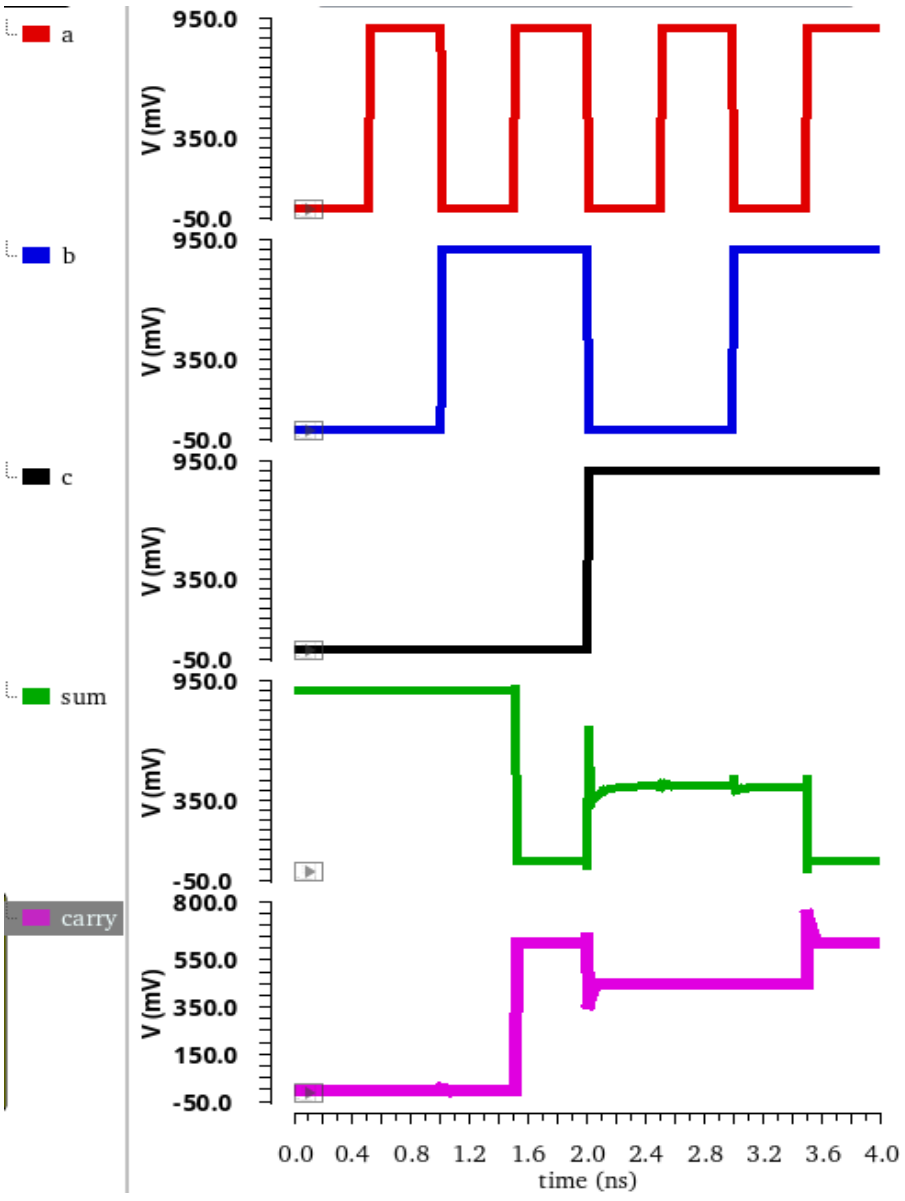


Fig 3.18. Output waveform of AA3 (Fig 3.3)

3.2.4 Approximate Adder 4 Output Waveform

Fig 3.19 shows the transient response of Approximate adder4 as shown in Fig 3.4. Here a, b, c are the inputs of the adder and sum, carry are the outputs. The below figure represents all the combinations of the Proposed approximate adder4. In those at 000, 111 cases having the error bits. The Adder has the supply voltage of +0.9v.

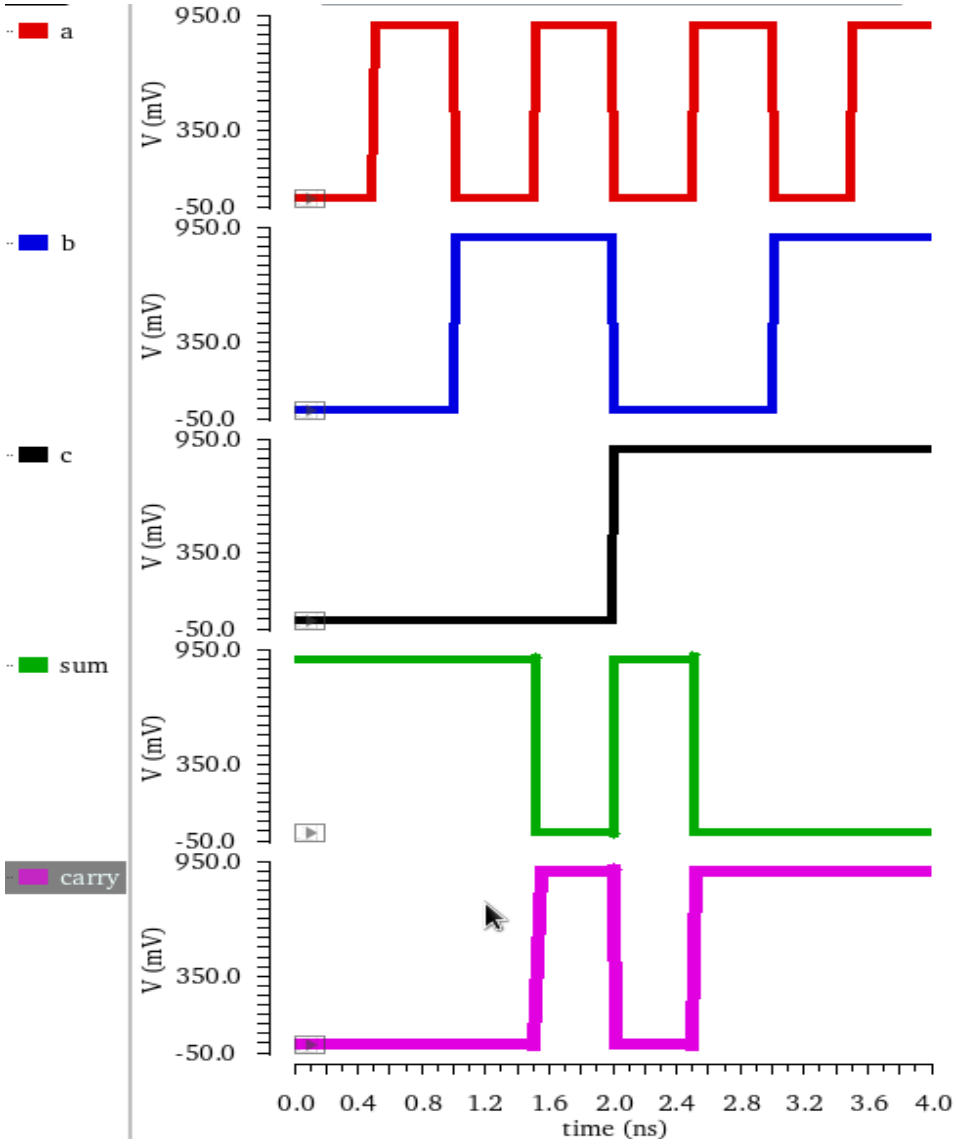


Fig 3.19. Output waveform of AA4 (Fig 3.4)

3.2.5 Approximate Adder 5 Output Waveform

Fig 3.20 shows the transient response of Approximate adder5 as shown in Fig 3.5. Here a, b, c are the inputs of the adder and sum, carry are the outputs. The below figure represents all the combinations of the Proposed approximate adder5. In those at 010, 100 cases having the error bits. The Adder has the supply voltage of +0.9v.

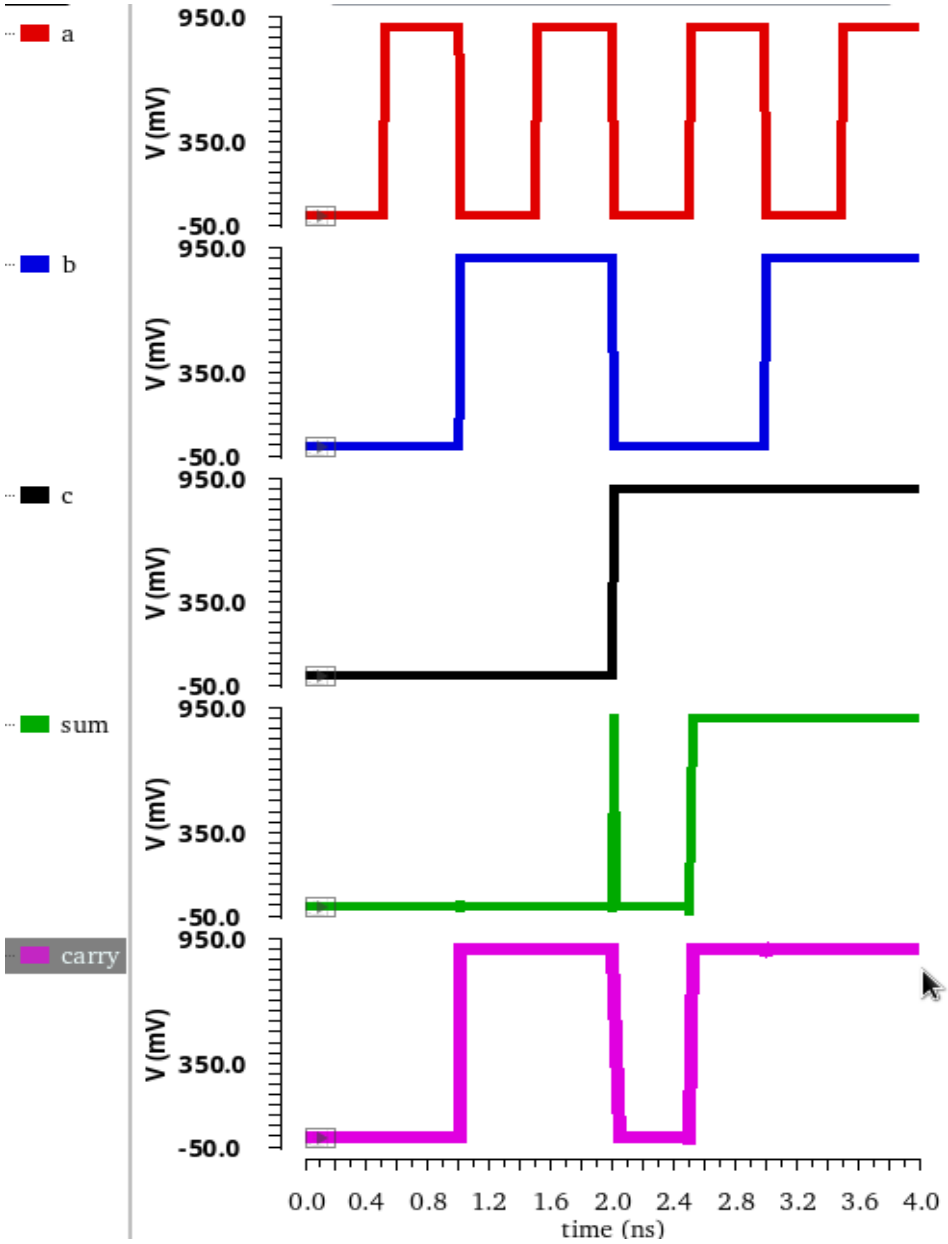


Fig 3.20. Output waveform of AA5 (Fig 3.5)

3.2.6 Approximate Adder 6 Output Waveform

Fig 3.21 shows the transient response of Approximate adder 6 as shown in Fig 3.6. Here a, b, c are the inputs of the adder and sum, carry are the outputs. The below figure represents all the combinations of the Proposed approximate adder 6. In those at 000, 111 cases having the error bits. The Adder has the supply voltage of +0.9v.

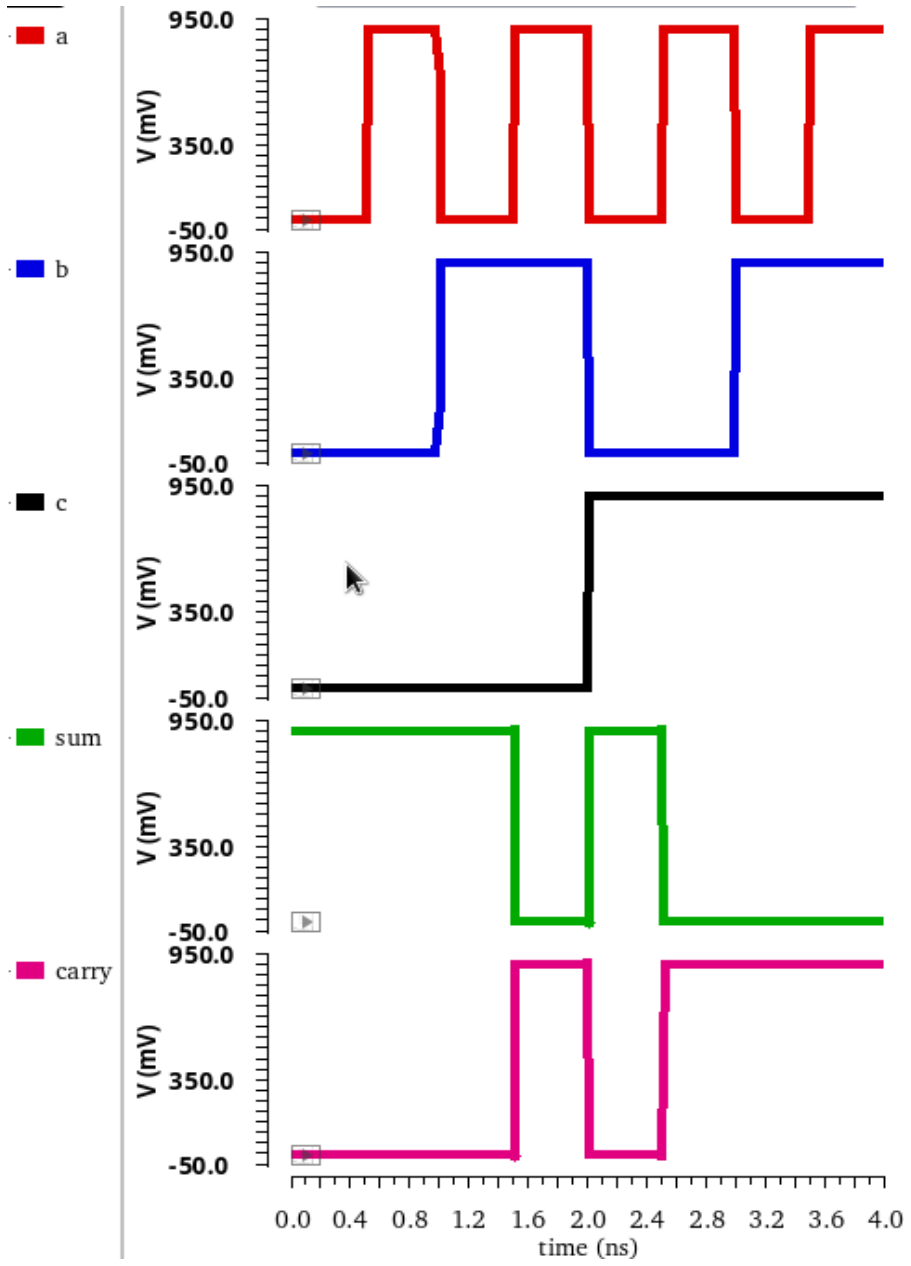


Fig 3.21. Output waveform of AA6 (Fig 3.6)

3.2.7 Approximate Adder 7 Output Waveform

Fig 3.22 shows the transient response of Approximate adder 7 as shown in Fig 3.7. Here a, b, c are the inputs of the adder and sum, carry are the outputs. The below figure represents all the combinations of the Proposed approximate adder 7. In those at 000, 010, 111 cases having the error bits. The Adder has the supply voltage of +0.9v.

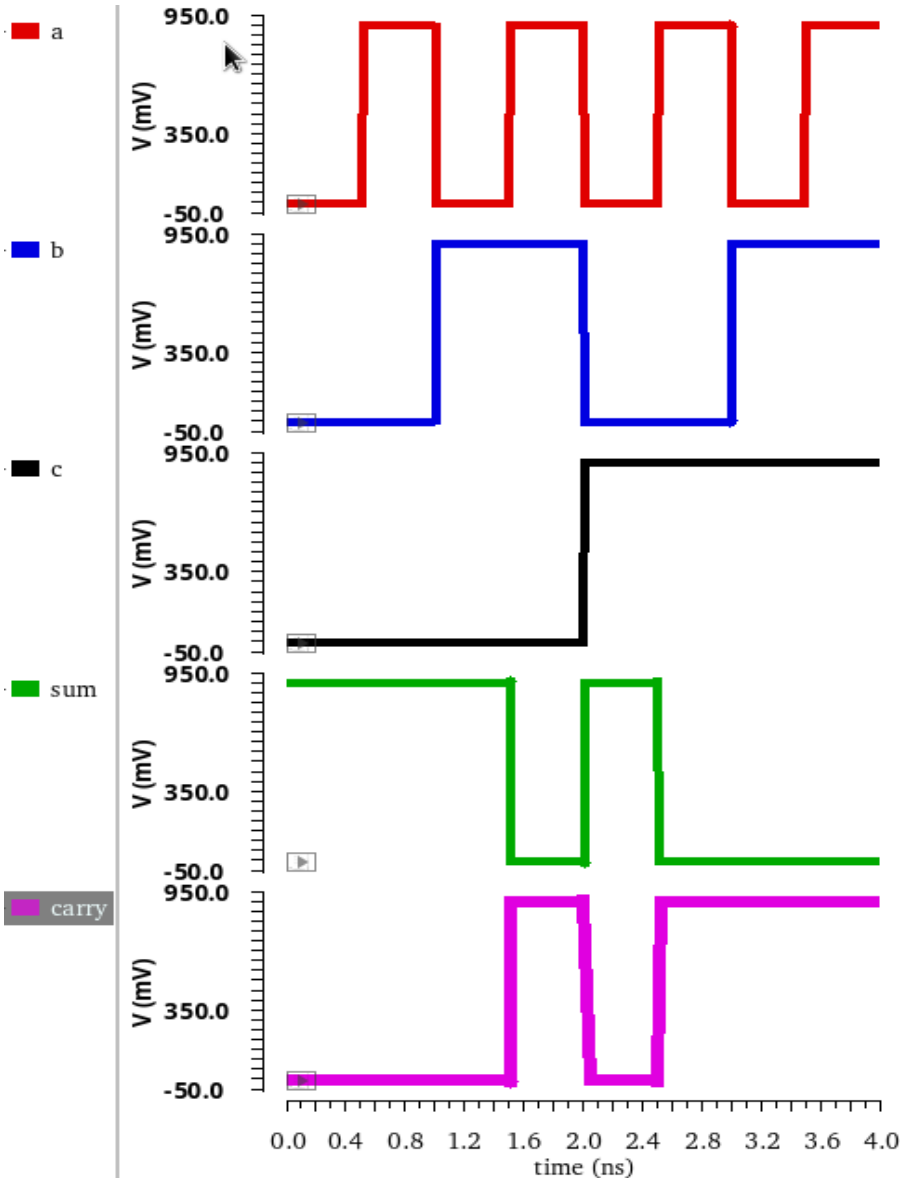


Fig 3.22. Output waveform of AA7 (Fig 3.7)

3.2.8 Approximate Adder 8 Output Waveform

Fig 3.23 shows the transient response of Approximate adder 8 as shown in Fig 3.8. Here a, b, c are the inputs of the adder and sum, carry are the outputs. The below figure represents all the combinations of the Proposed approximate adder 8. In those at 010, 011, 100 cases having the error bits. The Adder has the supply voltage of +0.9v.

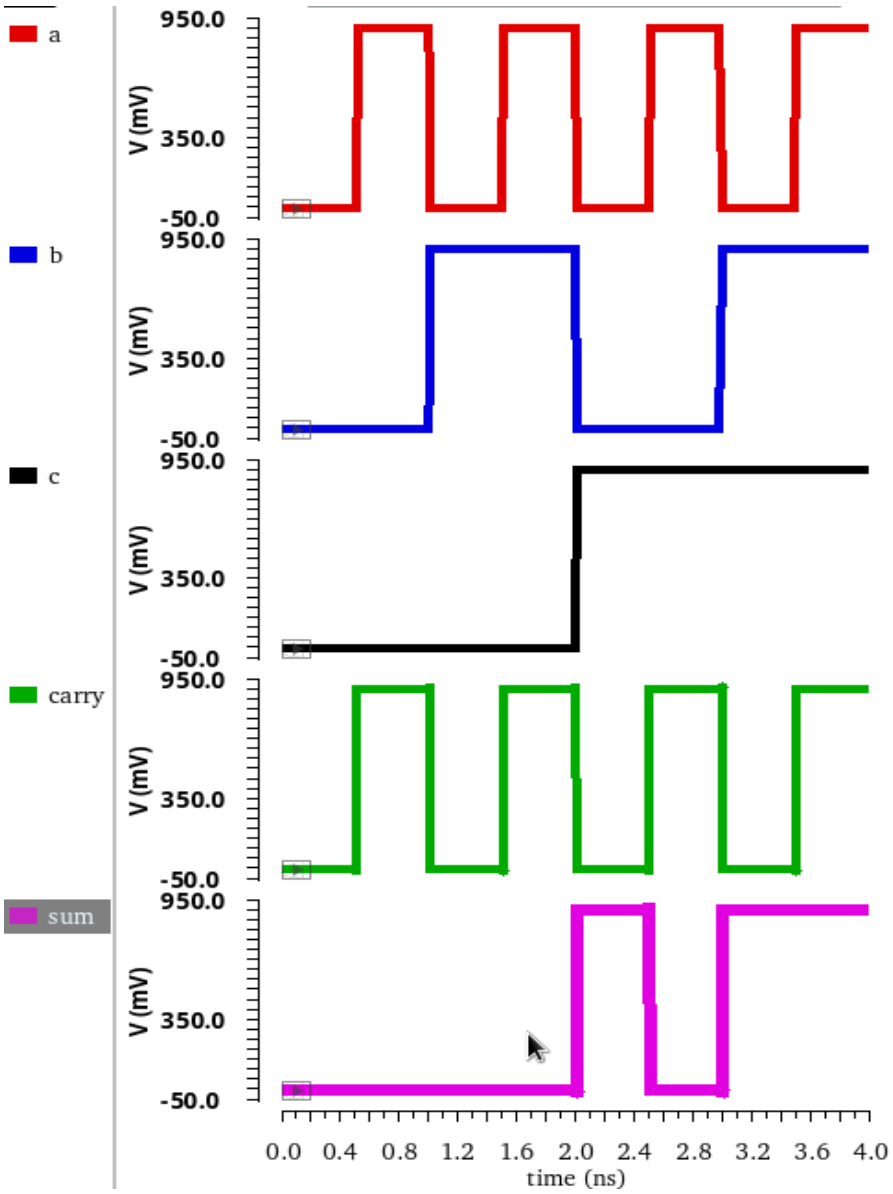


Fig 3.23. Output waveform of AA8 (Fig 3.8)

3.2.9 Approximate Adder 8 Output Waveform

Fig 3.24 shows the transient response of Approximate adder 9 as shown in Fig 3.9. Here a, b, c are the inputs of the adder and sum, carry are the outputs. The below figure represents all the combinations of the Proposed approximate adder 9. In those at 000, 111 cases having the error bits. The Adder has the supply voltage of +0.9v.

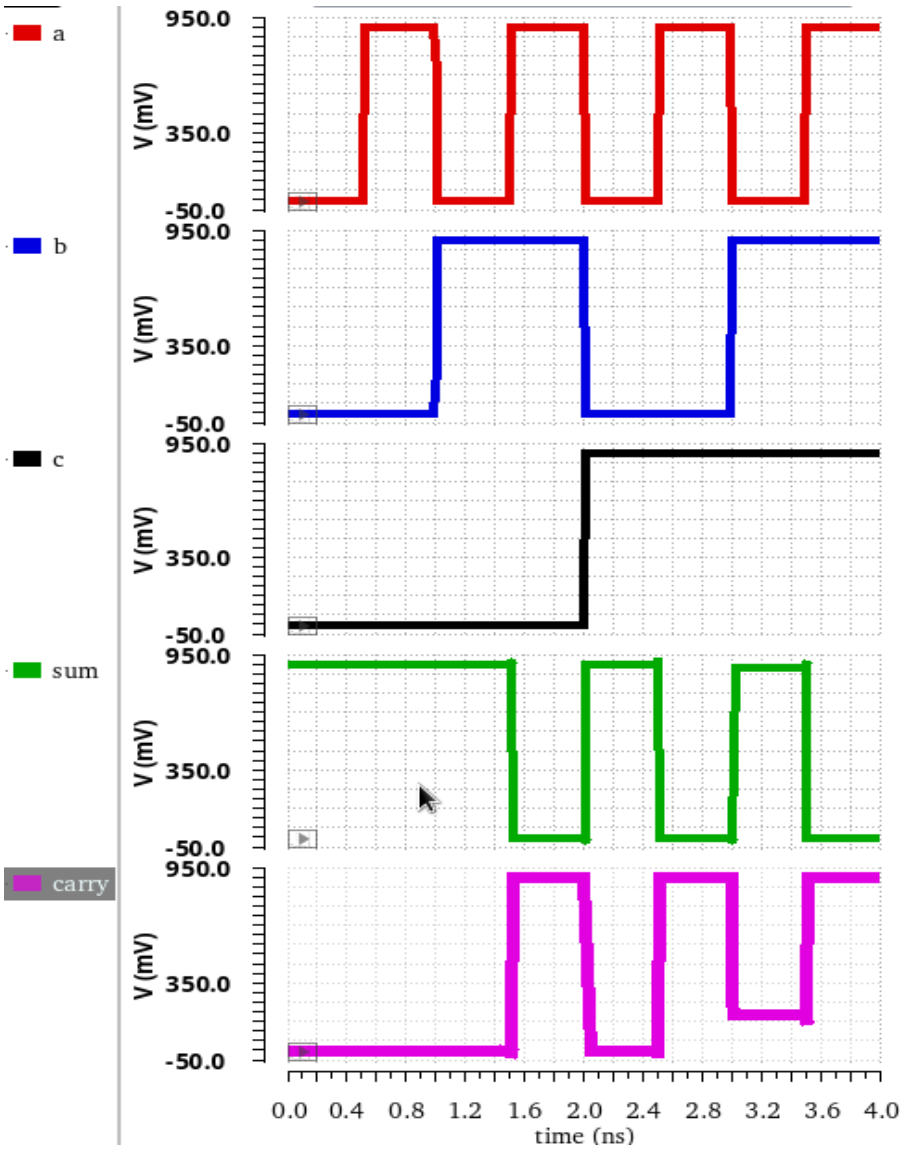


Fig 3.24. Output waveform of AA9 (Fig 3.9)

3.2.10 Approximate Adder 10 Output Waveform

Fig 3.25 shows the transient response of Approximate adder 10 as shown in Fig 3.10. Here a, b, c are the inputs of the adder and sum, carry are the outputs. The below figure represents all the combinations of the Proposed approximate adder 10. In those at 000, 111 cases having the error bits. The Adder has the supply voltage of +0.9v.

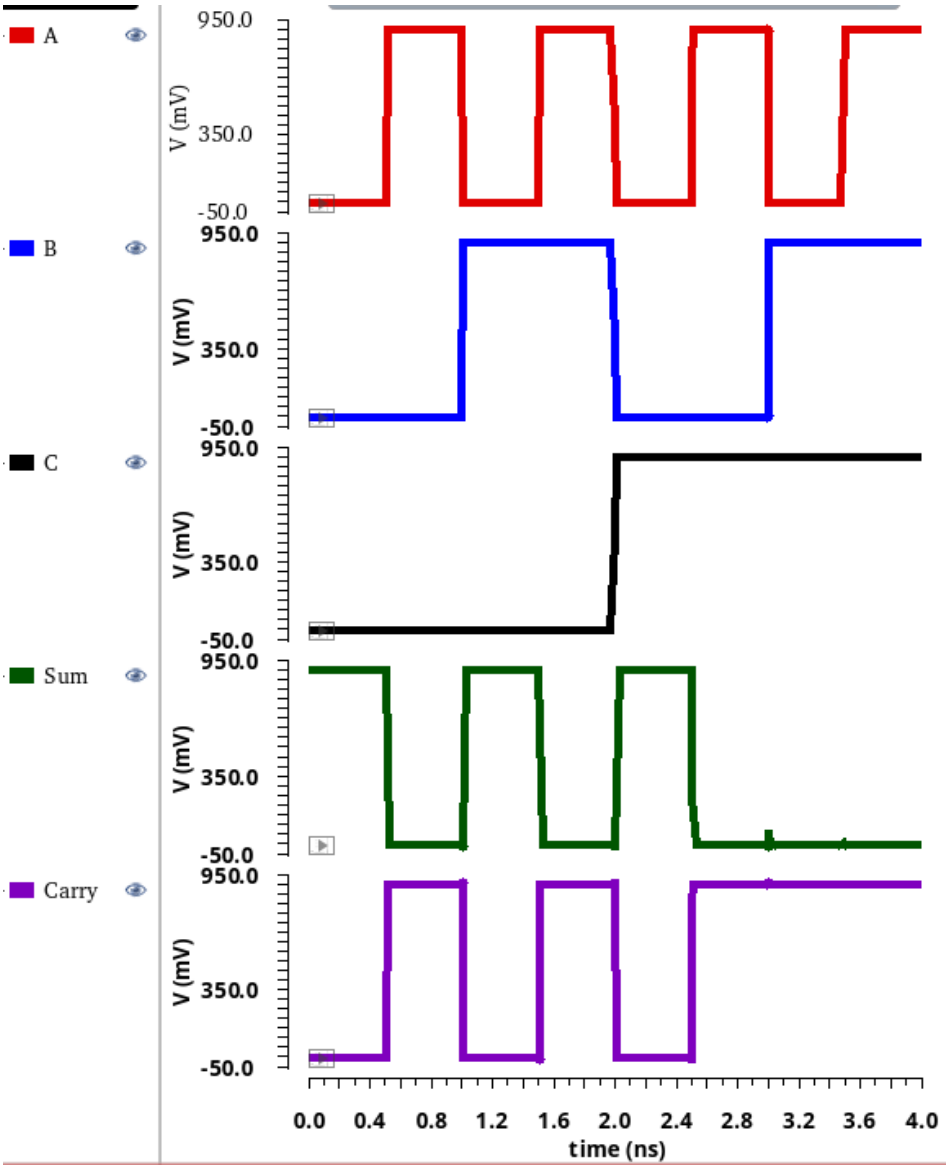


Fig 3.25. Output waveform of AA10 (Fig 3.10)

3.2.11 Approximate Adder 11 Output Waveform

Fig 3.26 shows the transient response of Approximate adder 11 as shown in Fig 3.11. Here a, b, c are the inputs of the adder and sum, carry are the outputs. The below figure represents all the combinations of the Proposed approximate adder 11. In those at 000, 111 cases having the error bits. The Adder has the supply voltage of +0.9v.

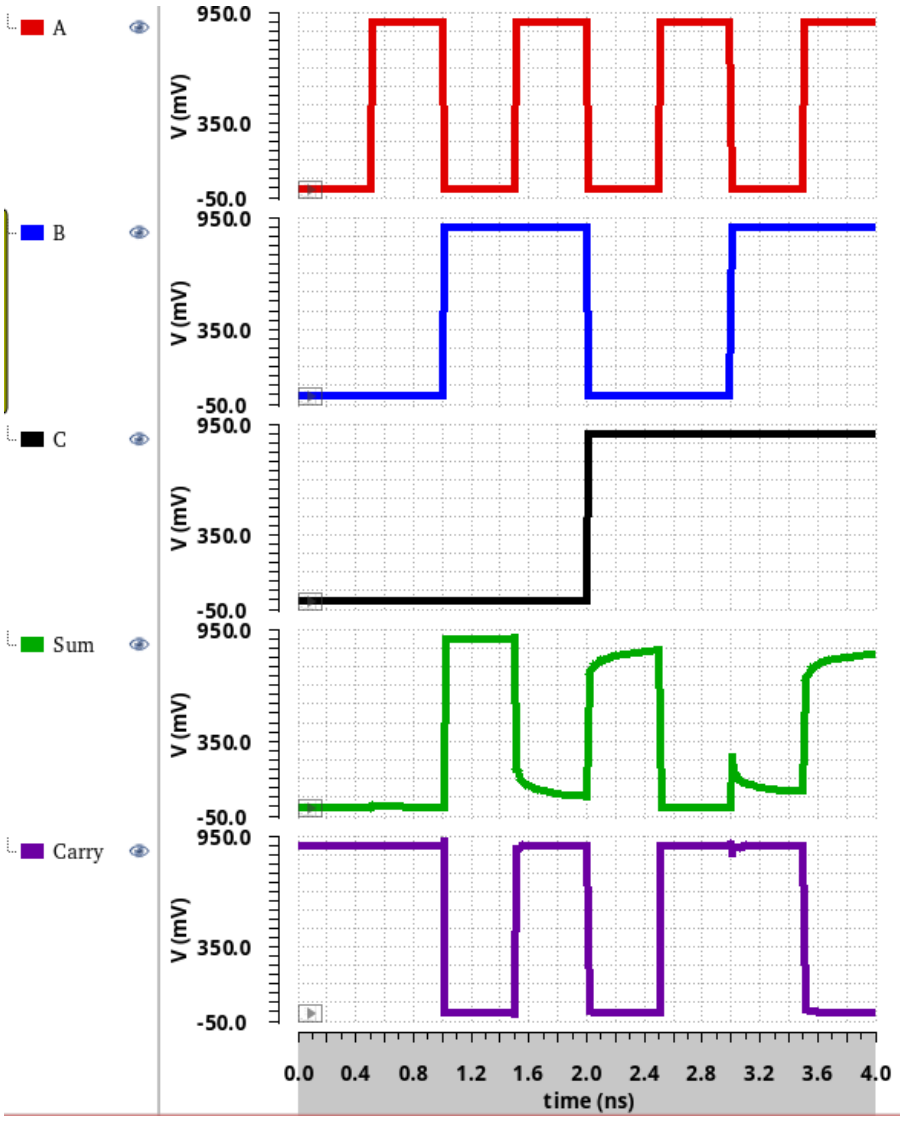


Fig 3.26. Output waveform of AA11 (Fig 3.11)

3.2.12 Approximate Adder 12 Output Waveform

Fig 3.27 shows the transient response of Approximate adder 12 as shown in Fig 3.12. Here a, b, c are the inputs of the adder and sum, carry are the outputs. The below figure represents all the combinations of the Proposed approximate adder 12. In those at 000, 111 cases having the error bits. The Adder has the supply voltage of +0.9v.

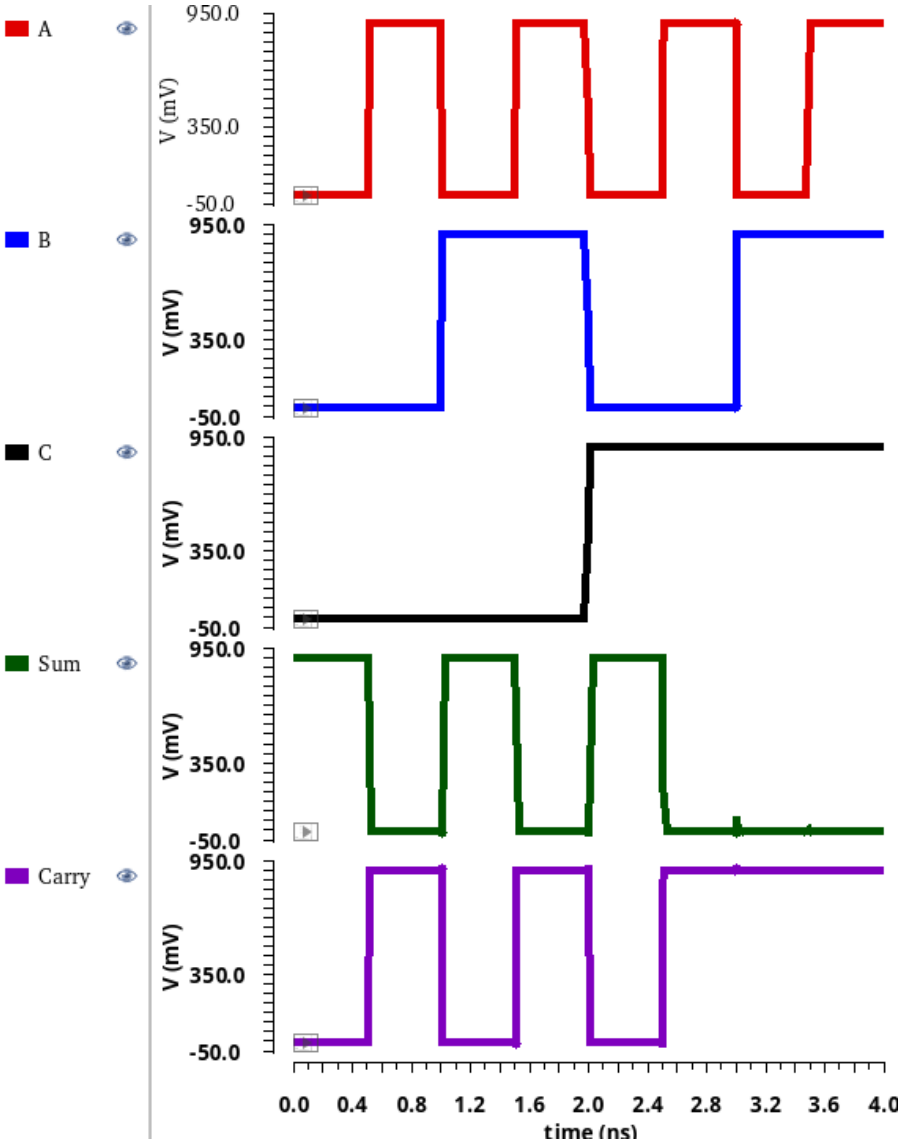


Fig 3.27. Output waveform of AA12 (Fig 3.12)

3.2.13 Approximate Adder 13 Output Waveform

Fig 3.28 shows the transient response of Approximate adder 13 as shown in Fig 3.13. Here a, b, c are the inputs of the adder and sum, carry are the outputs. The below figure represents all the combinations of the Proposed approximate adder 13. In those at 000, 111 cases having the error bits. The Adder has the supply voltage of +0.9v.

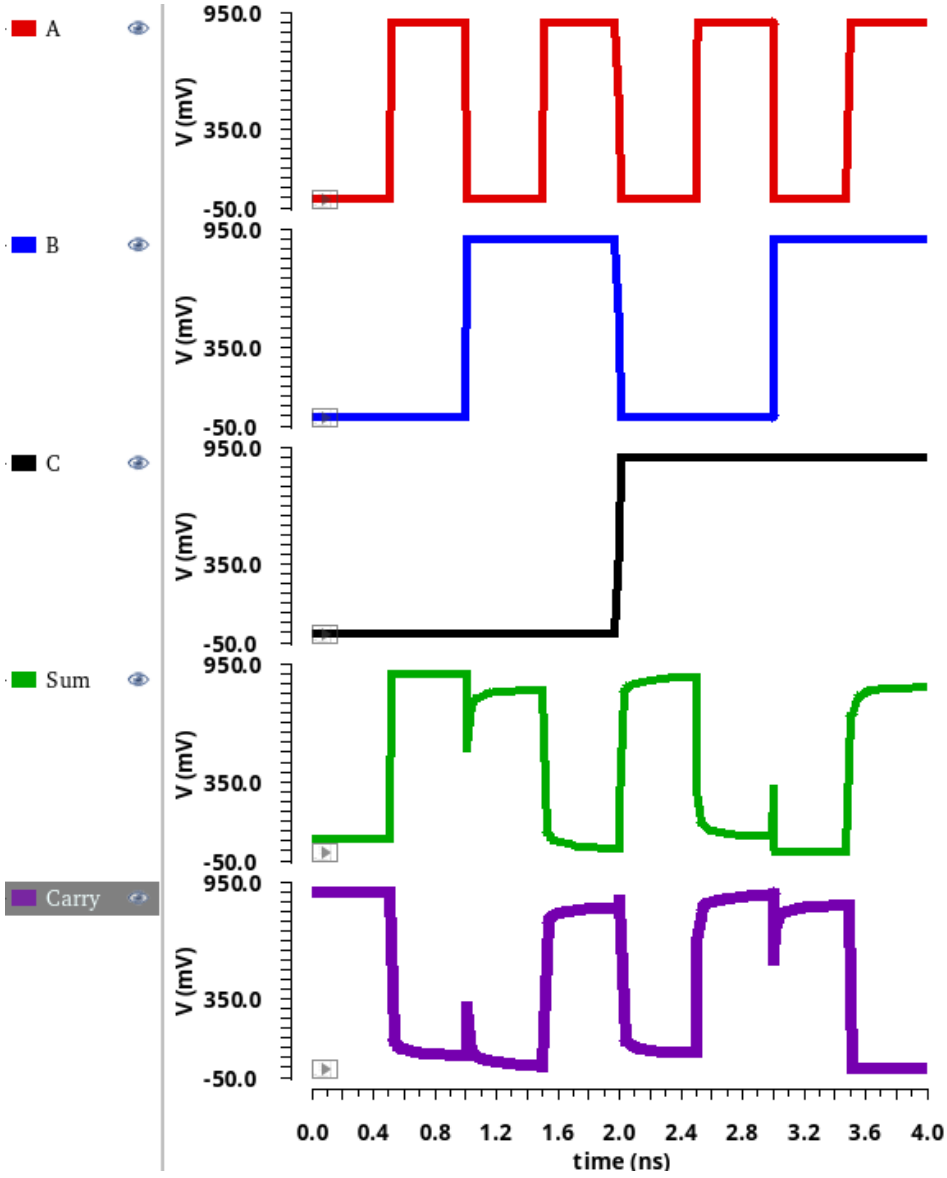


Fig 3.28. Output waveform of AA13 (Fig 3.13)

3.2.14 Approximate Adder 14 Output Waveform

Fig 3.29 shows the transient response of Approximate adder 14 as shown in Fig 3.14. Here a, b, c are the inputs of the adder and sum, carry are the outputs. The below figure represents all the combinations of the Proposed approximate adder 14. In those at 000, 111 cases having the error bits. The Adder has the supply voltage of +0.9v.

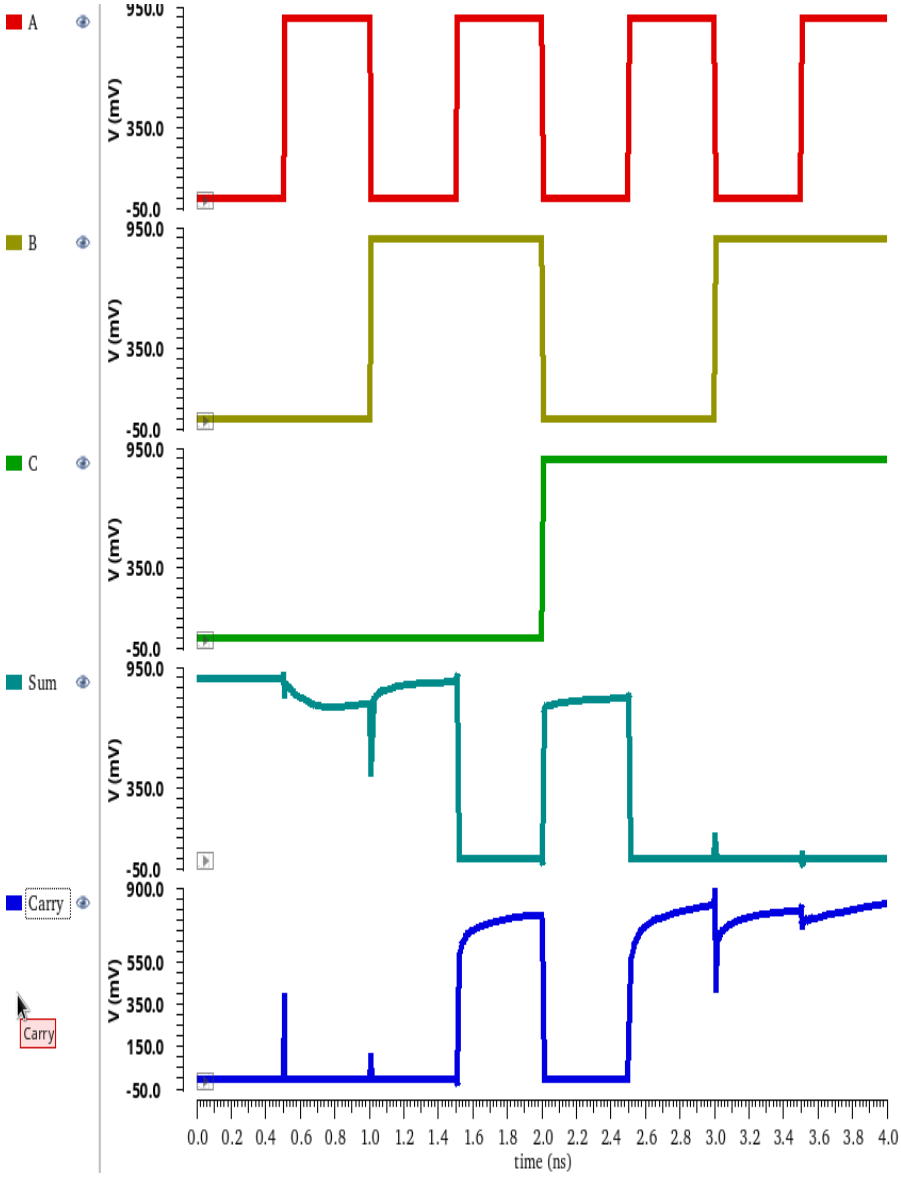


Fig 3.29. Output waveform of AA14 (Fig 3.14)

3.2.15 Approximate Adder 15 Output Waveform

Fig 3.30 shows the transient response of Approximate adder 15 as shown in Fig 3.15. Here a, b, c are the inputs of the adder and sum, carry are the outputs. The below figure represents all the combinations of the Proposed approximate adder 15. In those at 000, 111 cases having the error bits. The Adder has the supply voltage of +0.9v.

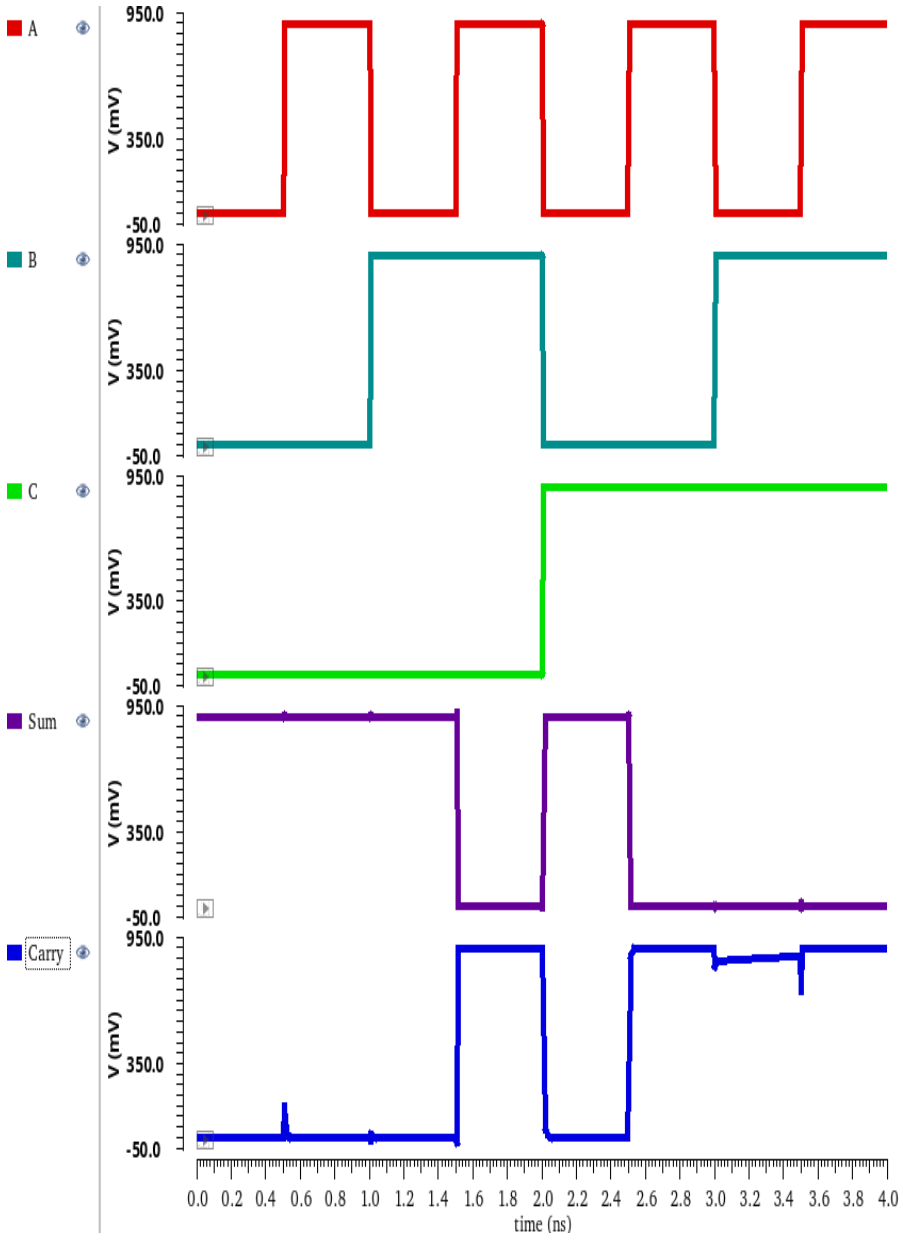


Fig 3.30. Output waveform of AA15 (Fig 3.15)

3.3 Quantitative Results of Delay, Power and PDP of Approximate Adders

In this project, CNFET 32nm technology is used to simulate 15 proposed approximate adders. Table2 summarizes the simulation results for all of the adders. All 15 proposed approximate adders having less Propagation Delay, Power Consumption and Power Delay Product compares to the existing work. From those adders AA7 & AA11 have less delay, AA15 has less power, and AA15has less PDP value. Finally, AA15 is suitable for approximate computing because of less PDP, less delay and less circuit area.

Table.2 Transient response of all approximate adders.

S. No	Adders	No. of Errors		No. of Transistors	Delay(ns)	Power(µw)	PDP(fJ)
		Sum	Carry				
1	AA1	3	1	14	1.005	0.5602	0.5630
2	AA2	3	0	14	1.498	0.5607	0.8382
3	AA3	2	2	18	1.006	0.5078	0.5742
4	AA4	2	0	14	1.005	0.4518	0.4540
5	AA5	2	1	16	1.002	0.5609	0.5620
6	AA6	2	0	16	1.006	0.4521	0.4548
7	AA7	3	1	13	0.996	0.5609	0.5586
8	AA8	3	2	11	1.504	0.4484	0.6743
9	AA9	2	0	13	1.004	0.5632	0.5654
10	AA10	2	0	10	1.497	0.5608	0.7890
11	AA11	1	3	8	0.996	0.1339	0.1336
12	AA12	0	2	8	1.495	0.1239	0.1852
13	AA13	1	1	8	1.499	0.0648	0.0971
14	AA14	2	0	8	1.007	0.1267	0.1268
15	AA15	2	0	6	1.004	0.0624	0.0062

CHAPTER 4

APPROXIMATE 4-BIT RIPPLE CARRY ADDER

In this chapter 4-bit RCA is implemented with the help of all the 15 1-bit approximate adders. To verify the overall performance of the all the adders those approximate adders are placed in LSB position and exact adder is placed in MSB position and Power, Delay and PDP of all the Approximate RCAs are going to verified. The 4-bit RCA is used for the Addition of 4 bits. The simulation results are also shown in below chapter.

4.1 RIPPLE CARRY ADDER

Multiple full adder circuits can be cascaded in parallel to add an N-bit number. For an N-bit parallel adder, there must be N number of full adder circuits. A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs. Propagation delays inside the logic circuitry is the reason behind this. Propagation delay is time elapsed between the application of an input and occurrence of the corresponding output. Consider a NOT gate, When the input is “0” the output will be “1” and vice versa. The time taken for the NOT gate’s output to become “0” after the application of logic “1” to the NOT gate’s input is the propagation delay here. Similarly the carry propagation delay is the time elapsed between the application of the carry in signal and the occurance of the carry out (Cout) signal.

Ripple Carry Adder is a combinational logic circuit. It is used for the purpose of adding two n-bit binary numbers. It requires n full adders in its circuit for adding two n-bit binary numbers. It is also known as n-bit parallel adder. structure of multiple full adders is cascaded in a manner to gives the results of the addition of an n bit binary sequence. This adder includes cascaded full adders in its structure so, the carry will be generated at every full adder stage in a ripple-carry adder circuit. Thesecarry output at each full adder stage is forwarded to its next full adder and there applied as a carry input to it. This process continues up to its last full adder stage. So, each carry output bit is rippled tothe next stage of a full adder. By this reason, it is named as “RIPPLE CARRY ADDER”.

The most important feature of it is to add the input bit sequences whether the sequence is 4 bit or 5 bit or any. One of the most important point to be considered in this carry adder is the final output is known only after the carry outputs are generated by each full adder stage and forwarded to its next stage. So there will be a delay to get the result with using of this carry adder.

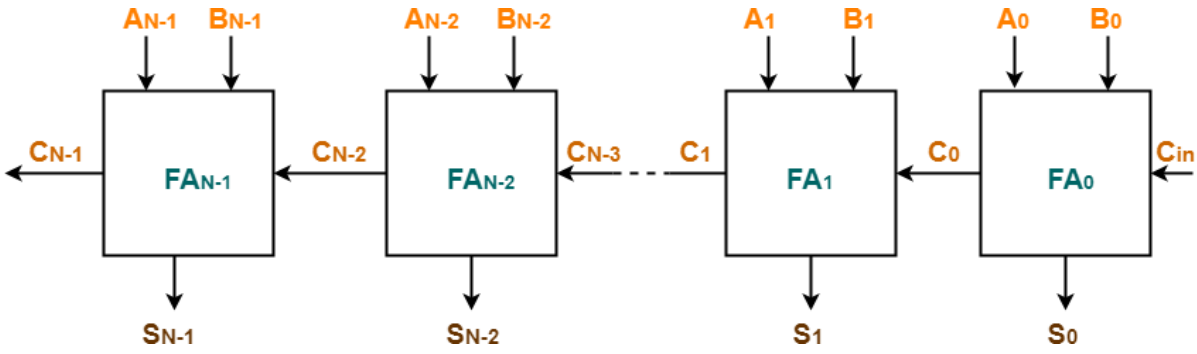


Fig 4.1. Block diagram of n-bit Ripple Carry Adder

4 Bit RCA

The below diagram represents the 4-bit ripple-carry adder. In this adder, four full adders are connected in cascade. Co is the carry input bit and it is zero always. When this input carry 'Cin' is applied to the two input sequences A0, A1, A2, A3 and B0, B1, B2, B3 then sum output represented with S0, S1, S2 and S3 and output carry is C3.

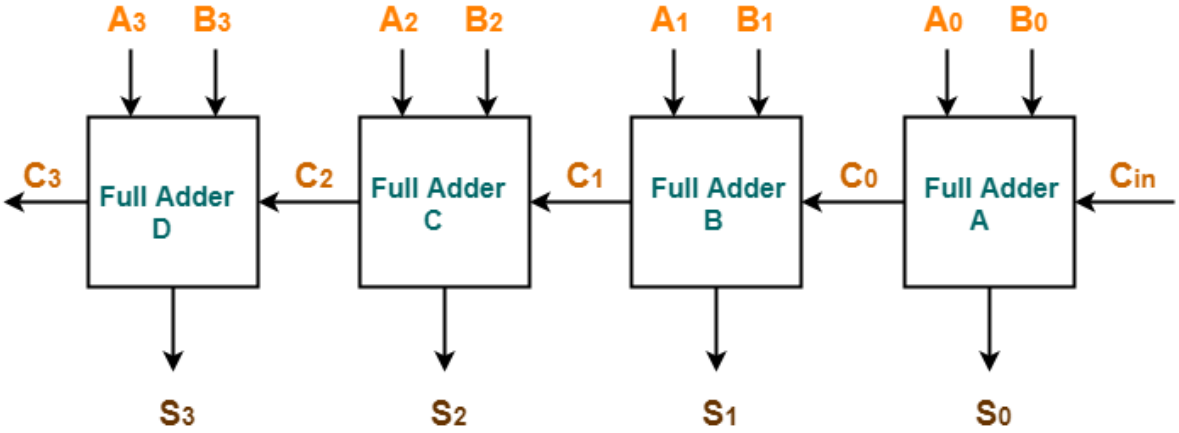


Fig 4.2. Block Diagram of 4- Bit RCA

4.2 Proposed Ripple Carry Adder

4.2.1 Proposed Ripple Carry Adder 11

Figure 4.3 illustrates the block diagram of a 4-Bit Ripple Carry Adder 11. It consists of A, B, and C inputs where the Proposed adder (AA11) is placed in Least Significant Bit (LSB) Side and the Accurate Full Adder is placed in MSB Side. Here the Carry acts like full adder input, it propagates from one adder to another adder. It requires two four-bit inputs running from A0-A3 and B0-B3 respectively. Figure 4.8 depicts the simulation results for the 4-Bit RCA.

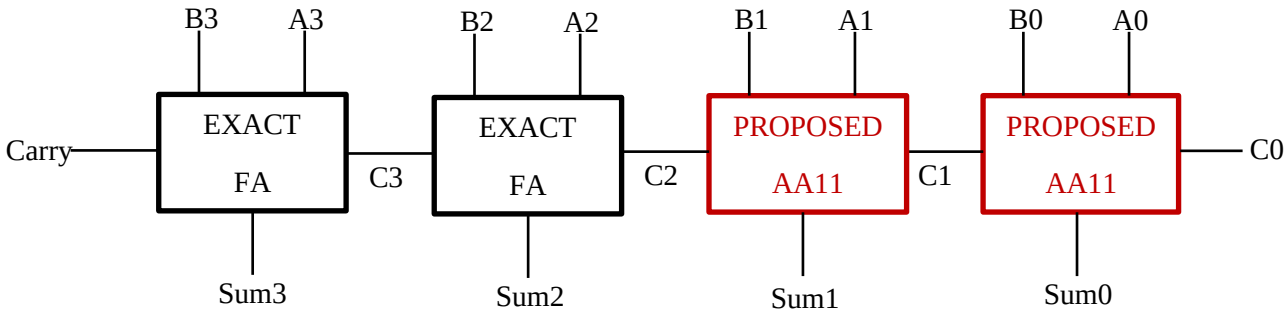


Fig 4.3. Block diagram of Proposed 4-bit Ripple Carry Adder 11

4.2.2 Proposed Ripple Carry Adder 12

Figure 4.4 illustrates the block diagram of a 4-Bit Ripple Carry Adder 12. It consists of A, B, and C inputs where the Proposed adder (AA12) is placed in Least Significant Bit (LSB) Side and the Accurate Full Adder is placed in MSB Side. Here the Carry acts like full adder input, it propagates from one adder to another adder. It requires two four-bit inputs running from A0-A3 and B0-B3 respectively. Figure 4.9 depicts the simulation results for the 4-Bit RCA.

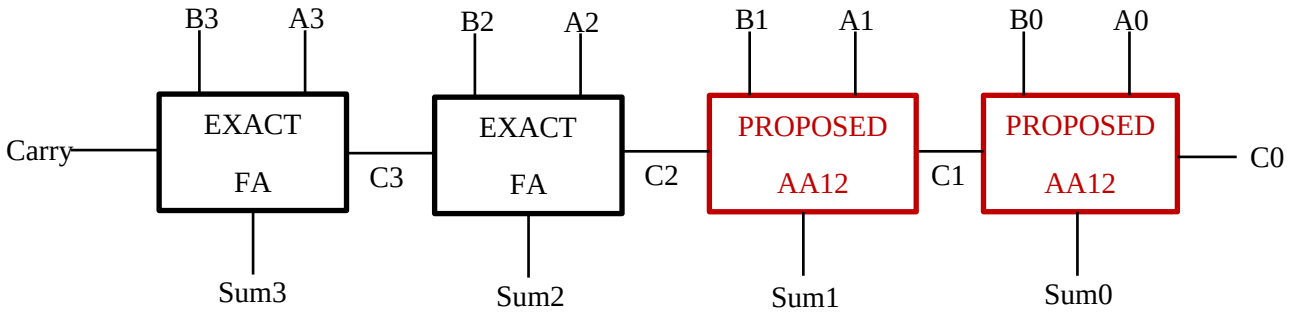


Fig 4.4. Block diagram of Proposed 4-bit Ripple Carry Adder

4.2.3 Proposed Ripple Carry Adder 13

Figure 4.5 illustrates the block diagram of a 4-Bit Ripple Carry Adder 13. It consists of A, B, and C inputs where the Proposed adder (AA13) is placed in Least Significant Bit (LSB) Side and the Accurate Full Adder is placed in MSB Side. Here the Carry acts like full adder input, it propagates from one adder to another adder. It requires two four-bit inputs running from A0-A3 and B0-B3 respectively. Figure 4.10 depicts the simulation results for the 4-Bit RCA.

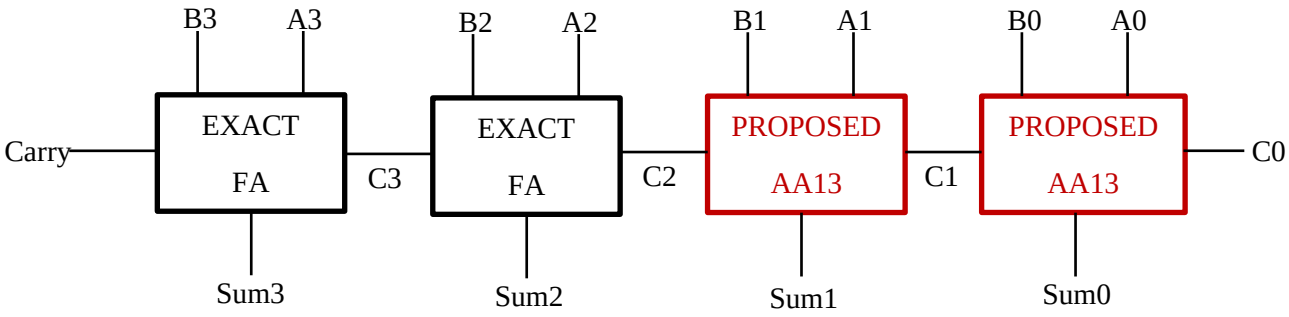


Fig 4.5. Block diagram of Proposed 4-bit Ripple Carry Adder 13

4.2.4 Proposed Ripple Carry Adder 14

Figure 4.6 illustrates the block diagram of a 4-Bit Ripple Carry Adder 14. It consists of A, B, and C inputs where the Proposed adder (AA14) is placed in Least Significant Bit (LSB) Side and the Accurate Full Adder is placed in MSB Side. Here the Carry acts like full adder input, it propagates from one adder to another adder. It requires two four-bit inputs running from A0-A3 and B0-B3 respectively. Figure 4.11 depicts the simulation results for the 4-Bit RCA.

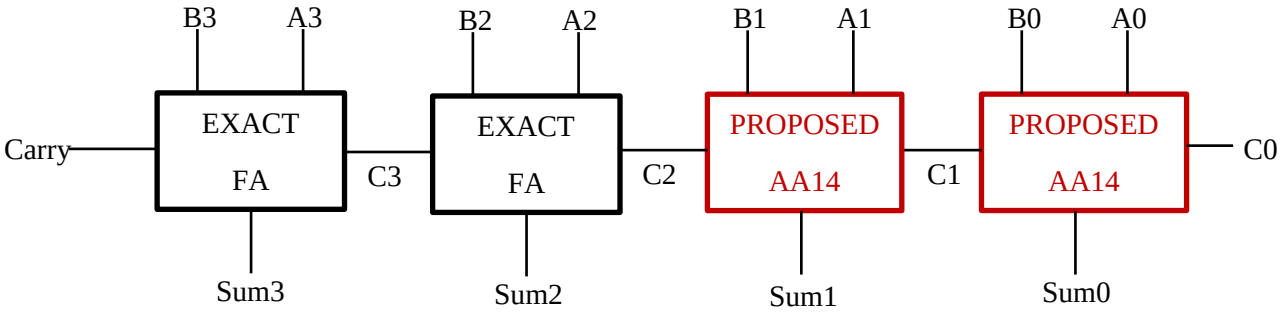


Fig 4.6. Block diagram of Proposed 4-bit Ripple Carry Adder 14

4.2.5 Proposed Ripple Carry Adder 15

Figure 4.7 illustrates the block diagram of a 4-Bit Ripple Carry Adder 15. It consists of A, B, and C inputs where the Proposed adder (AA15) is placed in Least Significant Bit (LSB) Side and the Accurate Full Adder is placed in MSB Side. Here the Carry acts like full adder input, it propagates from one adder to another adder. It requires two four-bit inputs running from A0-A3 and B0-B3 respectively. Figure 4.12 depicts the simulation results for the 4-Bit RCA.

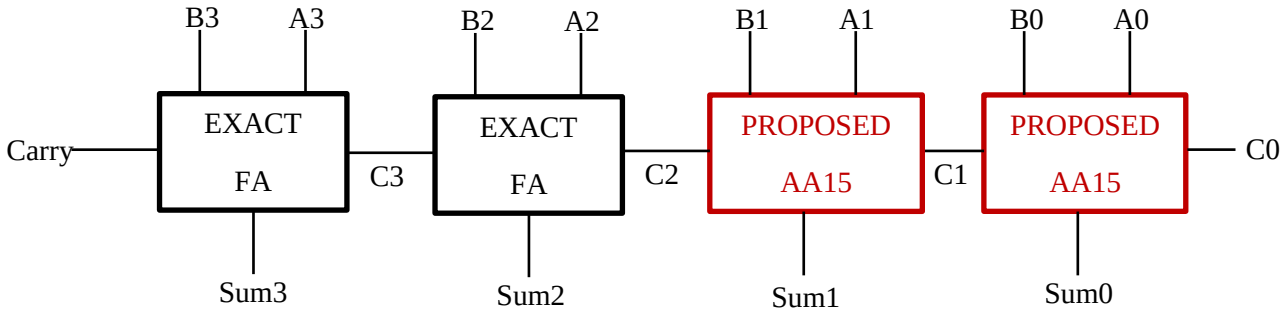


Fig 4.7. Block diagram of Proposed 4-bit Ripple Carry Adder 15

Summary

Finally in this chapter total all 15 1-bit approximate adders are verified with the help of proposed 4-Bit RCA which was shown in Fig 4.6. In those LSBs are replaced by Approximate Adders and MSBs are replaced by exact adders. The Carry is propagated from one block to another block. The final carry is the output of the RCA. The simulation results of the proposed 4-Bit RCAs are shown in below graphs and power, delay, PDP of the Approximate multipliers are shown in table.

4.3 Transient Responses of 4-Bit Approximate Ripple Carry Adders

4.3.1 Approximate 4-Bit RCA 11 Output Waveform

In the Fig 4.8 shows the simulation results of the Approximate 4-Bit RCA11 in which A0, A1, A2, A3, B0, B1, B2, B3, C0 are the input bits Sum0, Sum1, Sum2, Sum3 and Carry are the output bits. In which S0,S1 are the output bits of Approximate adder11 and S2, S3 are the output bits of Exact adder. Here Carry is propagated from one block to another block.

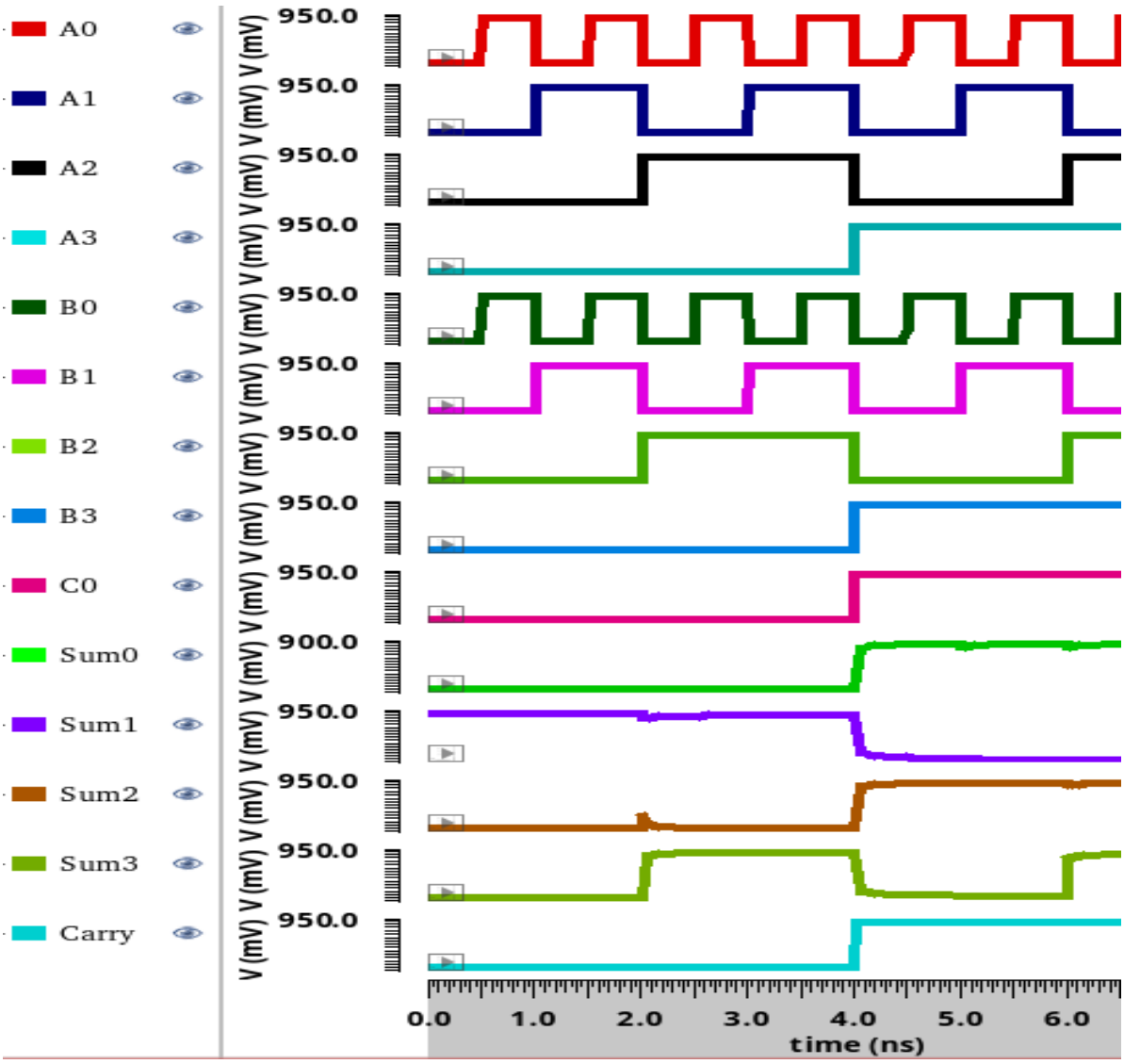


Fig 4.8. Output Waveform of RCA11

4.3.2 Approximate 4-Bit RCA 12 Output Waveform

In the Fig 4.9 shows the simulation results of the Approximate 4-Bit RCA12 in which A0, A1, A2, A3, B0, B1, B2, B3, C0 are the input bits Sum0, Sum1, Sum2, Sum3 and Carry are the output bits. In which S0,S1 are the output bits of Approximate adder12 and S2, S3 are the output bits of Exact adder. Here Carry is propagated from one block to another block.

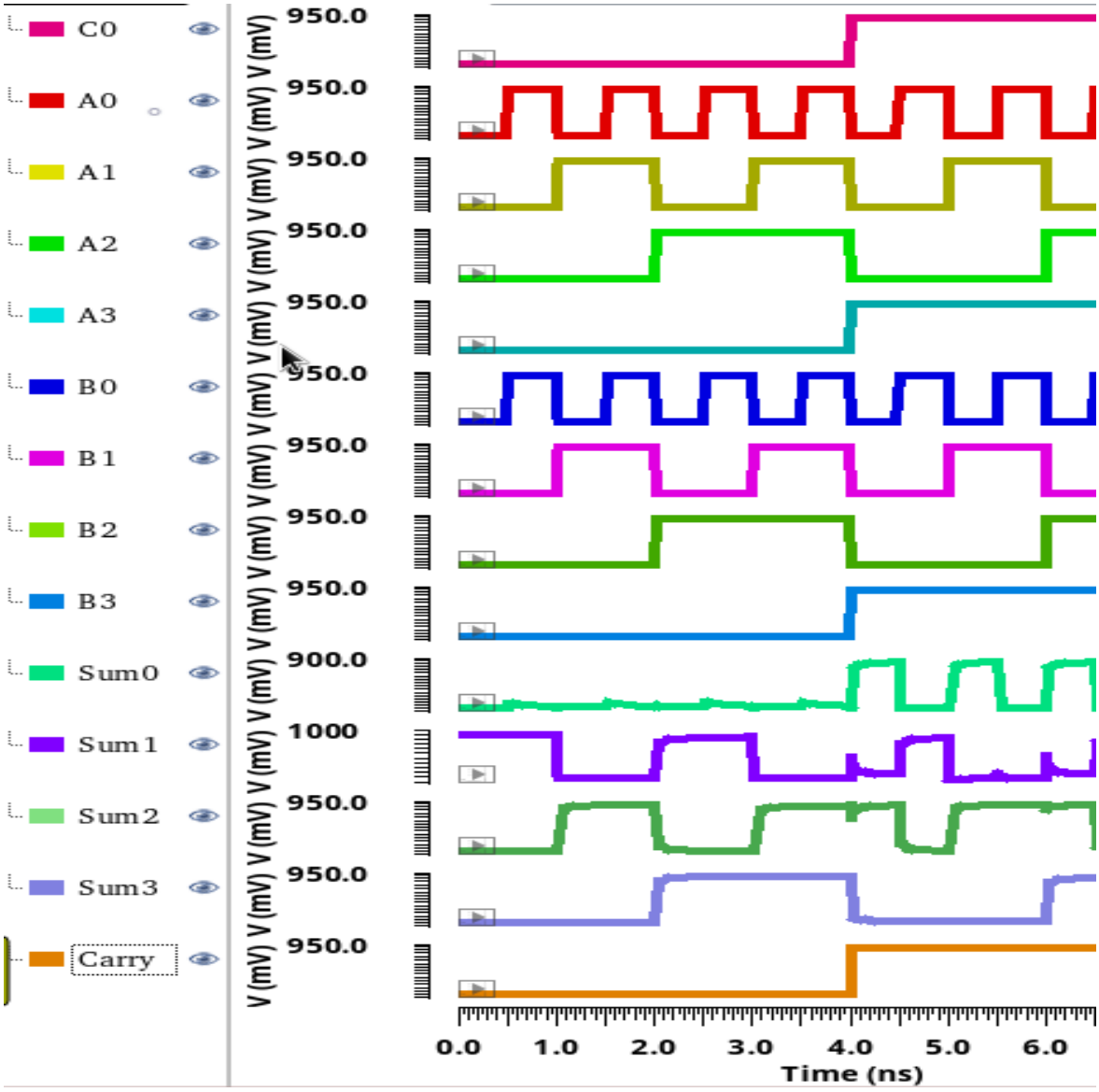


Fig 4.9. Output Waveform of RCA12

4.3.3 Approximate 4-Bit RCA 13 Output Waveform

In the Fig 4.10 shows the simulation results of the Approximate 4-Bit RCA13 in which A0, A1, A2, A3, B0, B1, B2, B3, C0 are the input bits Sum0, Sum1, Sum2, Sum3 and Carry are the output bits. In which S0,S1 are the output bits of Approximate adder13 and S2, S3 are the output bits of Exact adder. Here Carry is propagated from one block to another block.

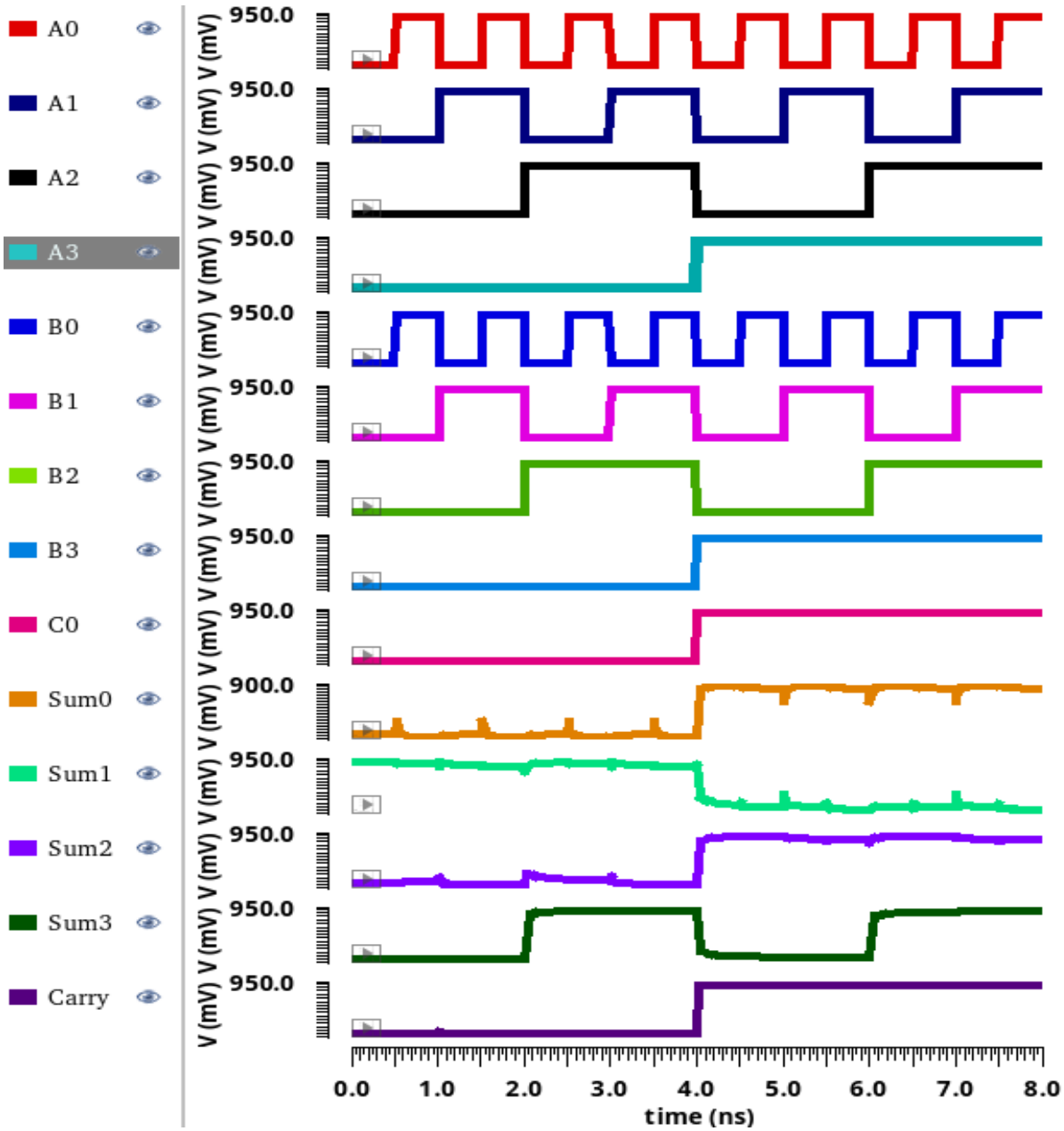


Fig 4.10. Output Waveform of RCA13

4.3.4 Approximate 4-Bit RCA 14 Output Waveform

In the Fig 4.11 shows the simulation results of the Approximate 4-Bit RCA12 in which A0, A1, A2, A3, B0, B1, B2, B3, C0 are the input bits Sum0, Sum1, Sum2, Sum3 and Carry are the output bits. In which S0,S1 are the output bits of Approximate adder14 and S2, S3 are the output bits of Exact adder. Here Carry is propagated from one block to another block.

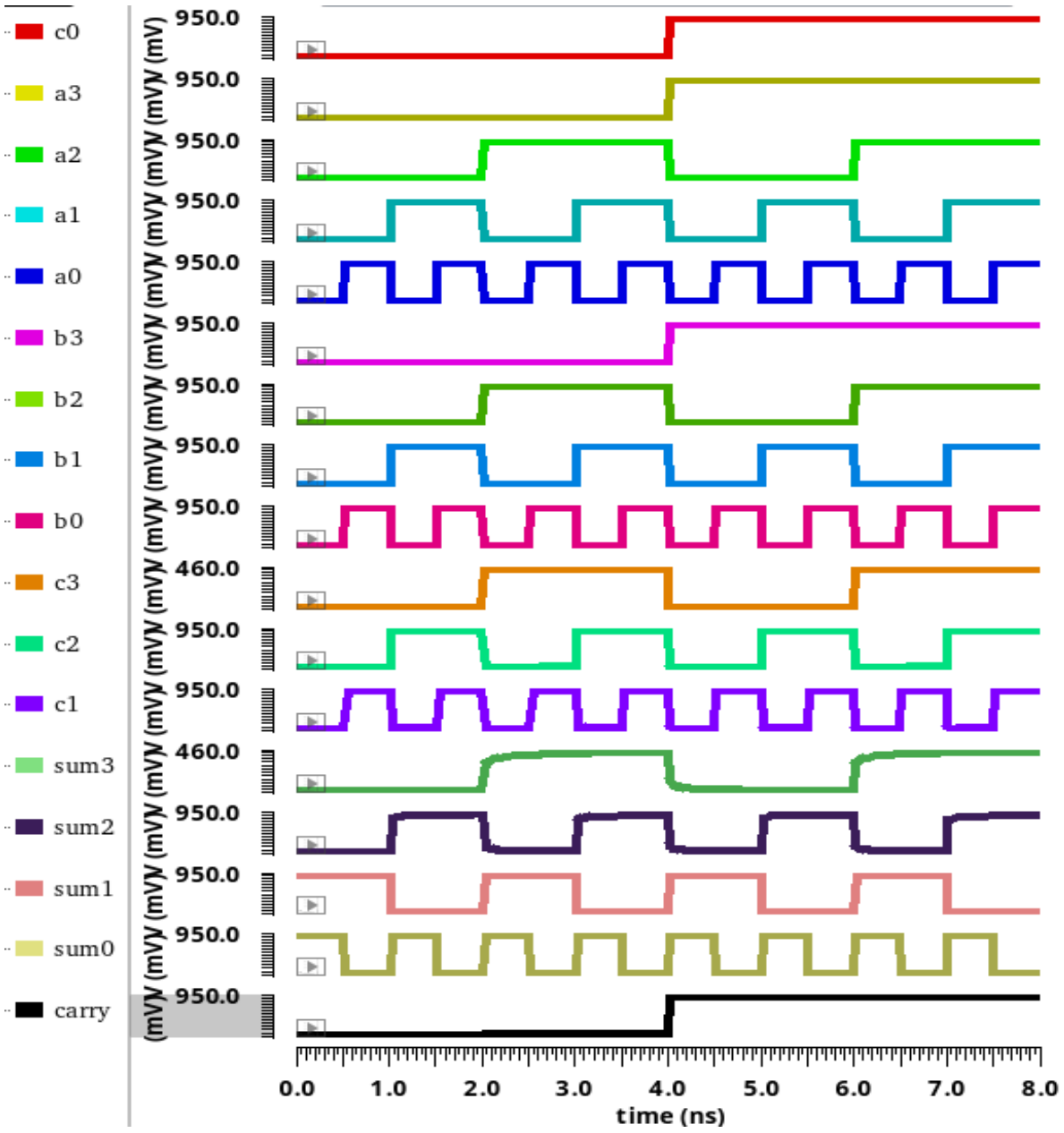


Fig 4.11. Output Waveform of RCA14

4.3.5 Approximate 4-Bit RCA 15 Output Waveform

In the Fig 4.9 shows the simulation results of the Approximate 4-Bit RCA15 in which A0, A1, A2, A3, B0, B1, B2, B3, C0 are the input bits Sum0, Sum1, Sum2, Sum3 and Carry are the output bits. In which S0,S1 are the output bits of Approximate adder15 and S2, S3 are the output bits of Exact adder. Here Carry is propagated from one block to another block.

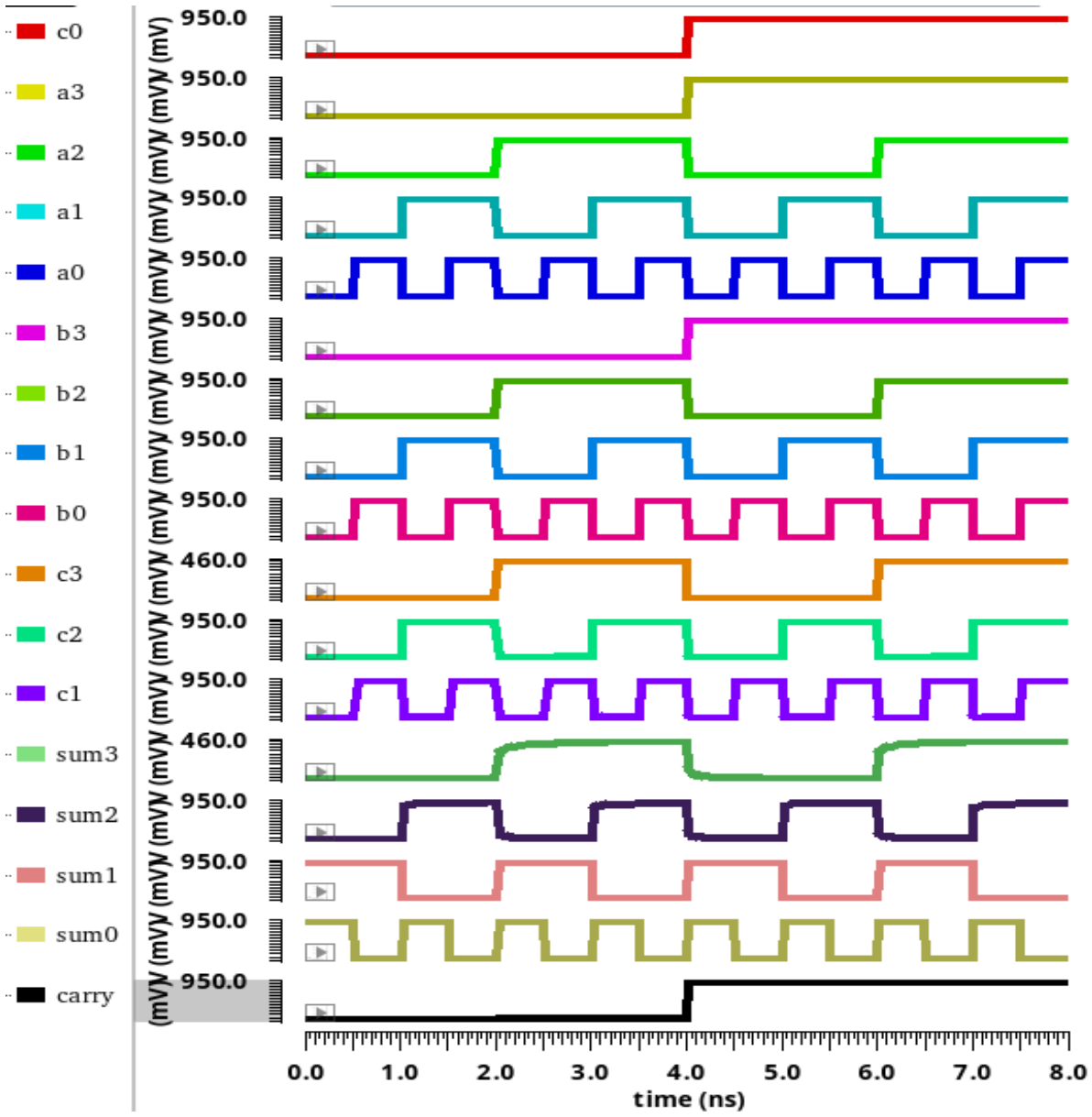


Fig 4.12. Output Waveform of RCA15

4.4 Quantitative Results of Power, Delay, PDP of 4-Bit RCA

Here all the 15 Approximate 4-Bit RCAs are simulated and shown in below table 3. In thoseRCA15 has less number of transistors also all the RCAs has same Delay. RCA15 has the less Power, RCA3 has more power and RCA15 has the less PDP from all the 15 Approximate 4-Bit RCAs.

Table 3. Simulation results of RCA 1-15

S. No	Name	Adders	No. of Transistors	Delay(ns)	Power(nw)	PDP(fJ)
1	RCA1	AA1	48	4.005	364.0	1.457881
2	RCA2	AA2	48	4.005	452.6	1.812739
3	RCA3	AA3	56	4.005	16630	66.60597
4	RCA4	AA4	48	4.005	2308	9.243932
5	RCA5	AA5	52	4.005	445.2	1.783101
6	RCA6	AA6	52	4.005	377.8	1.513153
7	RCA7	AA7	46	4.005	295.2	1.18227
8	RCA8	AA8	42	4.005	415.4	1.663747
9	RCA9	AA9	46	4.005	483.8	1.937701
10	RCA10	AA10	40	4.005	232.7	0.932000
11	RCA11(Fig 4.3)	AA11	36	4.00517	211.4	0.84669
12	RCA12(Fig 4.4)	AA12	36	4.00517	318.0	1.27364
13	RCA13(Fig 4.5)	AA13	36	4.00517	231.5	0.92715
14	RCA14(Fig 4.6)	AA14	36	4.005	265.7	1.06412
15	RCA15(Fig 4.7)	AA15	32	4.005	204.3	0.81822

CHAPTER 5

APPROXIMATE MULTIPLIER

Here in this chapter 2*4 Approximate Multiplier is implemented with the help of all the 15 1-bit approximate adders. To verify the overall performance of the all the adders those approximate adders are placed in Full Adder blocks of the Proposed Multiplier and Power, Delay and PDP of all the Approximate Multipliers are going to verified. This Multiplier is used for the Multiplication of 2* 4 bits. The simulation results are also shown in below chapter.

5.1 Multiplier

The multiplier operator is one of the most important and commonly used operators in the arithmeticlogic unit. An array multiplier is a digital combinational circuit used for multiplying two binary numbers by employing an array of full adders and half adders. This array is used for the nearly simultaneous addition of the various product terms involved. To form the various product terms, an array of AND gates is used before the Adder array.

Checking the bits of the multiplier one at a time and forming partial products is a sequential operationthat requires a sequence of add and shift micro-operations. The multiplication of two binary numberscan be done with one micro-operation by means of a combinational circuit that forms the product bitsall at once. This is a fast way of multiplying two numbers since all it takes is the time for the signalsto propagate through the gates that form the multiplication array. However, an array multiplier requires a large number of gates, and for this reason it was not economical until the development of integrated circuits.

Multiplier can be classified into two categories namely, serial and parallel multipliers. In a serial multiplier, each bit of multiplier is used for evaluating the partial product whereas in parallel multiplier, partial products from each bit of multiplier are computed in parallel. The main parameterthat determines the performance of the parallel multiplier is the number of partial products, that is tobe added. In a parallel multiplier, the speed is compromised to achieve better performance in terms of area and consumption.

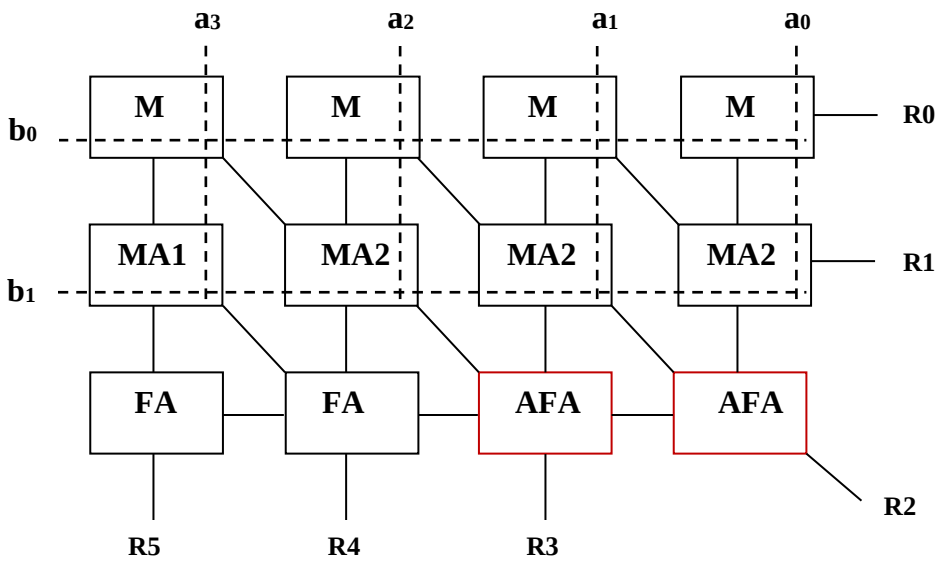
Depending upon the type of application, the parallel or the serial multiplier can be used. Some of theknown parallel multipliers are array multiplier, Wallace tree multiplier, Booth multiplier andmodified Booth multiplier. These multipliers are discussed in following text keeping focus on Boothmultipliers.

5.2 Approximate Multiplier

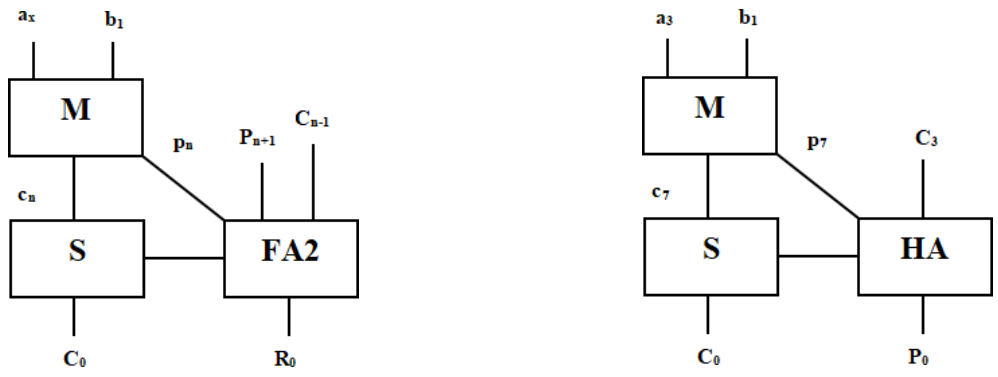
Approximate multipliers are widely being advocated for energy-efficient computing in applications that exhibit an inherent tolerance to inaccuracy. However, the inclusion of accuracy as a key design parameter, besides the performance, area and power, makes the identification of the most suitable approximate multiplier quite challenging.

5.3 Proposed Approximate Multiplier

The Multiplier shown in Fig. 5.12 was proposed based on the Wallace and array multiplier. In Fig.19M block denotes multiplier units, MA2 block contains one approximate full adder, one multiplier andone sum unit. The MA1 Block contains full adders, multiplier and sum unit. The MA1& MA2 blocksare shown in Fig 5.1(b) and Fig 5.1(c). The multiplier used for this circuit is as shown in Fig. 5.2 and approximate adder shown in Fig. 3.1.13. So with the help this proposed multiplier the approximate multiplication becomes easy and also computation speed is faster. As, Multiplication is important in arithmetic andlogic unit.



(A)



(B) **(C)**

Fig 5.1. (A) Structure of 2x4 multiplier, (B) Structure of MA1 Block, (C) Structure of MA2 Block

Summary

Finally in this chapter total all 15 1-bit approximate adders are verified with the help of proposed 2*4 multiplier which was shown in Fig 5.1.In those it having MA1 and MA2 block which consists of Full adder, Sum block and Multiplexer block. In the sum block the proposed Approximate 1-bit adders are replaced and simulated. The simulation results of the proposed multipliers are shown in below graphs and power, delay, PDP of the Approximate multipliers are shown in table 4.

5.4 Transient Responses of 2*4 Approximate Multiplier

5.4.1 2*4 Approximate Multiplier 11 Output Waveform

In the Fig 5.2 shows the simulation results of the 2*4 Approximate Multiplier 11 in which A0, A1, A2, A3, B0, B1,are the input bits and R0, R1, R2, R3, R4, R5 are the Product bits. In which 0110 is mulplied with 11 and produces the product as 000010. The simulation results has both exact and approximate outputs are shown.

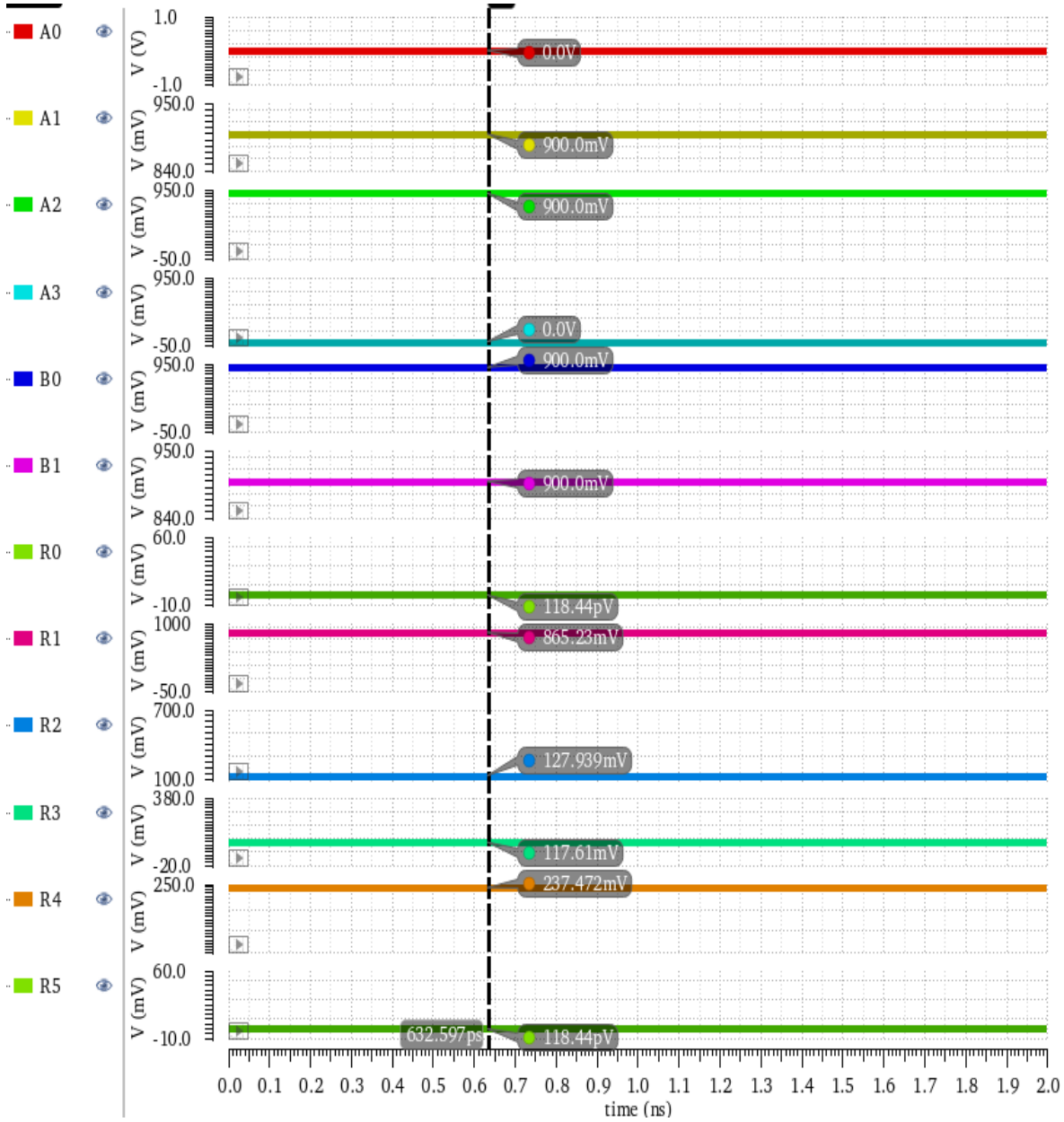


Fig 5.2. Output Waveform of AM11

5.4.2 2*4 Approximate Multiplier 12 Output Waveform

In the Fig 5.3 shows the simulation results of the 2*4 Approximate Multiplier 12 in which A0, A1, A2, A3, B0, B1,are the input bits and R0, R1, R2, R3, R4, R5 are the Product bits. In which 0110 is mulplied with 11 and produces the product as 011100. The simulation results has both exact and approximate outputs are shown.

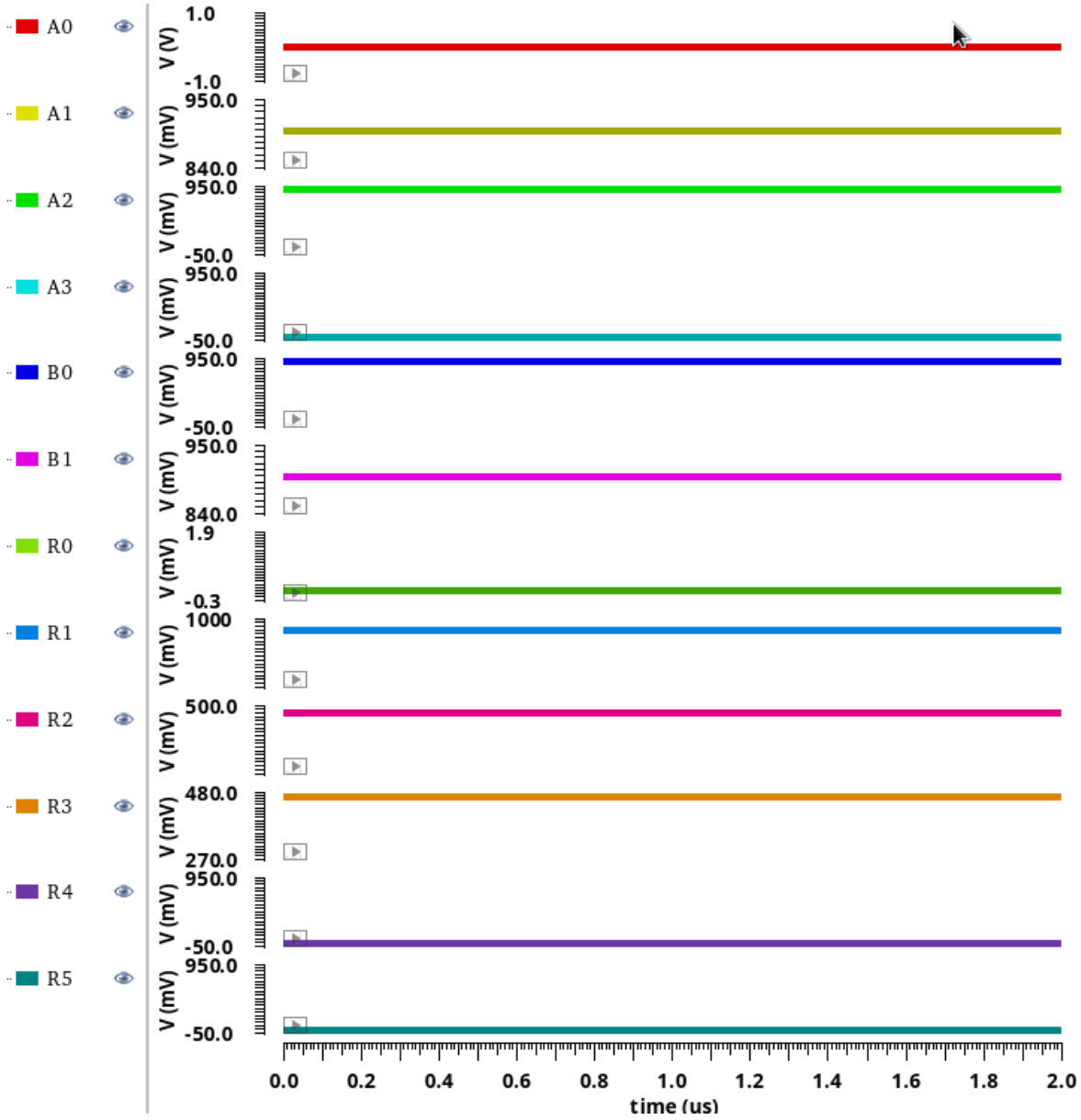


Fig 5.3. Output Waveform of AM12

5.4.3 2*4 Approximate Multiplier 13 Output Waveform

In the Fig 5.4 shows the simulation results of the 2*4 Approximate Multiplier 13 in which A0, A1, A2, A3, B0, B1,are the input bits and R0, R1, R2, R3, R4, R5 are the Product bits. In which 0110 is mulplied with 11 and produces the product as 011100. The simulation results has both exact and approximate outputs are shown.

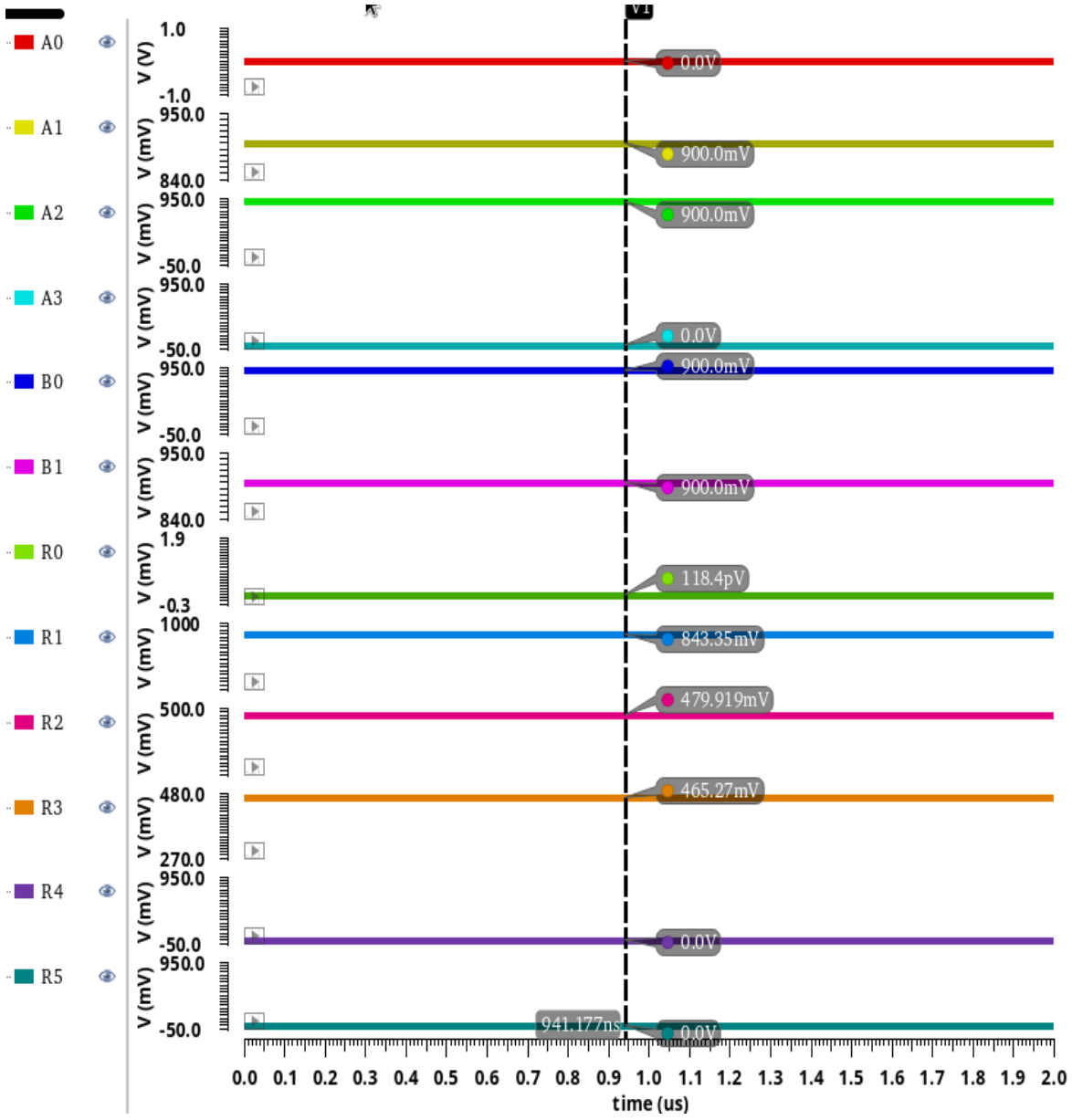


Fig 5.4. Output Waveform of AM13

5.4.4 2*4 Approximate Multiplier 14 Output Waveform

In the Fig 5.5 shows the simulation results of the 2*4 Approximate Multiplier 14 in which A0, A1, A2, A3, B0, B1,are the input bits and R0, R1, R2, R3, R4, R5 are the Product bits. In which 0110 is mulplied with 11 and produces the product as 010100. The simulation results has both exact and approximate outputs are shown.

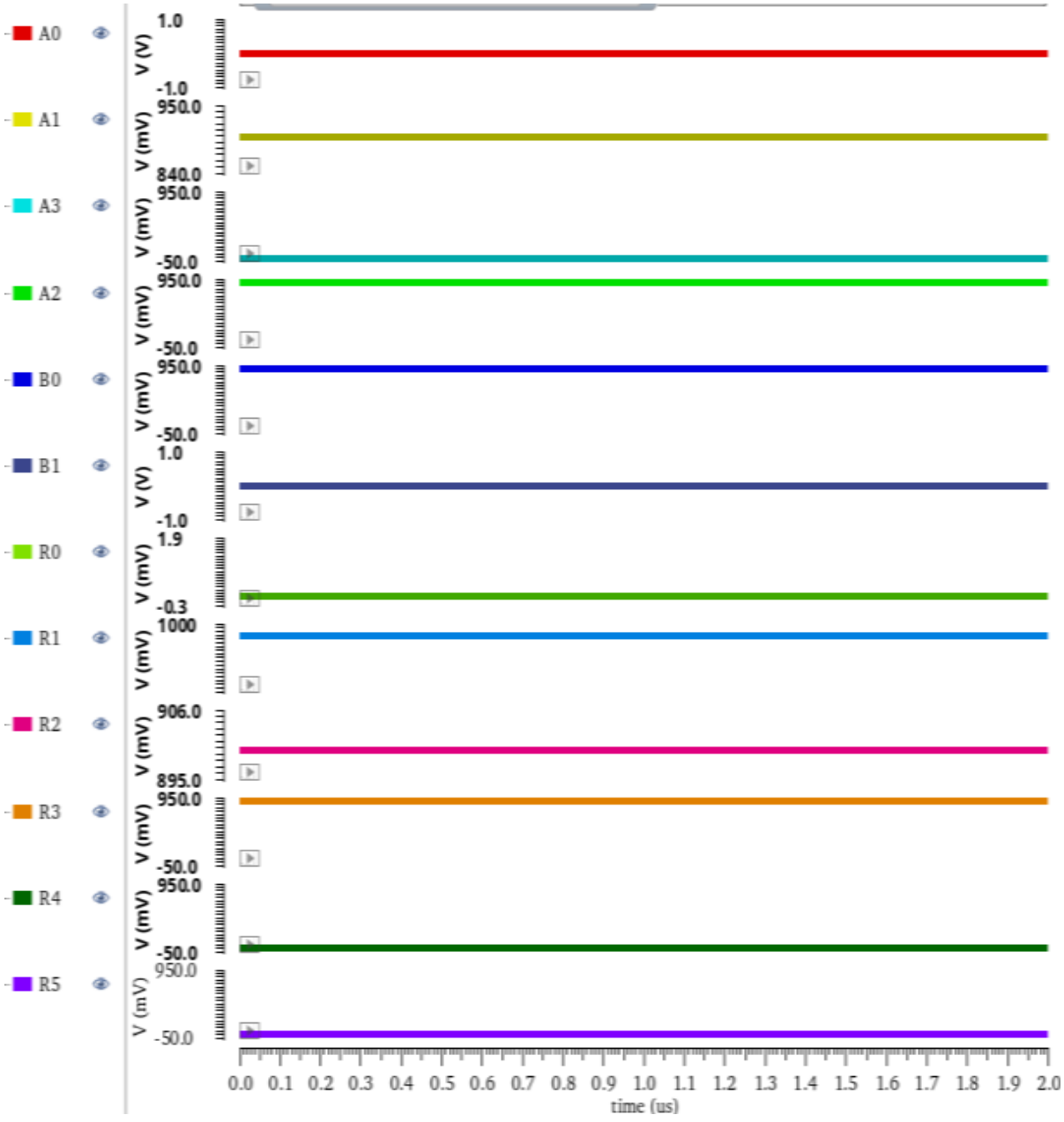


Fig 5.5. Output Waveform of AM14

5.4.5 2*4 Approximate Multiplier 15 Output Waveform

In the Fig 5.6 shows the simulation results of the 2*4 Approximate Multiplier 14 in which A0, A1, A2, A3, B0, B1,are the input bits and R0, R1, R2, R3, R4, R5 are the Product bits. In which 0110 is mulplied with 11 and produces the product as 010100. The simulation results has both exact and approximate outputs are shown.

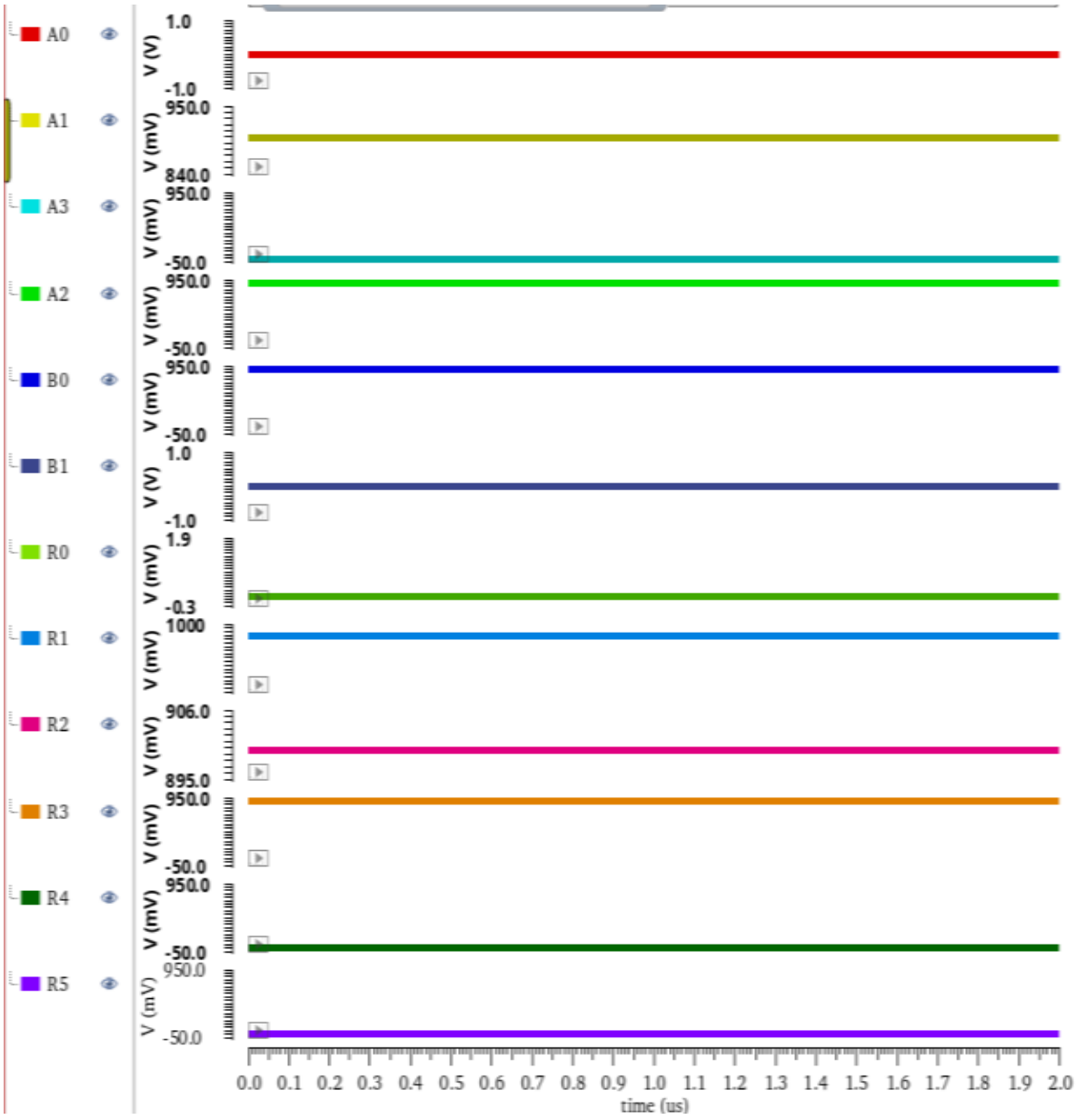


Fig 6.6. Output Waveform of AM15

5.5 Quantitative Results of Power, Delay, PDP of Approximate 2*4 Multiplier

Here all the 15 Approximate multipliers are simulated and shown in below table 4. In those AM10, AM11, AM 13 has the less Delay. AM15 has the less Power, AM2 has more power and AM15 has the less PDP from all the 15 Approximate Multipliers.

Table 4. Simulation results of approximate 2*4 multiplier

S. No	Name	Adders	Delay(μs)	Power(μw)	PDP(nJ)
1	AM1	AA1	2.006	128.1	0.257032
2	AM2	AA2	2.003	140.3	0.281098
3	AM3	AA3	2.006	128.6	0.258075
4	AM4	AA4	2.006	131.7	0.264275
5	AM5	AA5	2.006	134.7	0.270299
6	AM6	AA6	2.006	138.4	0.277650
7	AM7	AA7	2.006	134.8	0.270503
8	AM8	AA8	2.006	128.8	0.258450
9	AM9	AA9	2.006	129.6	0.260084
10	AM10	AA10	2.003	121.9	0.244165
11	AM11	AA11	2.052	135.4	0.277908
12	AM12	AA12	2.003	135.7	0.271883
13	AM13	AA13	2.003	130	0.260461
14	AM14	AA14	2.006	128.1	0.257083
15	AM15	AA15	2.006	119	0.23877

CHAPTER 6

Conclusion

In this project, the design of various approximate adders are simulated using the 32nm Carbon Nano-Tube Field Effect Transistor (CNTFET) technology with supply voltage of +0.9v. The Approximate adders simulations are done through Cadence tool. There are 10 existing 1-bit approximate adders proposed by different authors which are implemented using the gpdk 180nm technology. The existing 1-bit approximate adders are simulated with Cadence tool using CNTFET 32nm technology along with them 5 new 1-bit approximate adders are proposed naming AA11- AA15. The new proposed 1-bit approximate adders are simulated with Cadence tool using CNTFET 32nm technology. From all the 15 adders, AA15 has less number of transistors i.e.,6 and AA3 has more number of transistors i.e., 18. From those 15 adders AA8 has more number of errors i.e., 5 errors and AA4, AA9, AA10, AA12, AA13, AA14, AA15 has less number of errors i.e., 2 errors. The above 15 different approximate adders AA7 & AA11 having the less delay compared to all the proposed approximate adders. The approximate full adder AA15 has less power dissipation and less Power Delay Product (PDP). Finally, from all the above approximate adders AA15 is used for the Approximate computing technique. With the help of all the 15 approximate adder Ripple Carry Adder and Multiplier Applications are implemented.

In chapter 5, total all 15 1-bit approximate adders are implemented with the help of proposed 4-Bit RCA which was shown in Fig 4.6. In those LSBs are replaced by Approximate Adders and MSBs are replaced by exact adders. The power dissipation, delay propagation and PDP of the proposed 4-Bit RCAs are shown in table 3. The delay for all the approximate ripple carry adders are almost same. The approximate RCA15 which is implemented using AA15 has less power dissipation and less PDP compared to all the approximate ripple carry adders.

In chapter 6, total all 15 1-bit approximate adders are implemented with using proposed 2*4 multiplier which was shown in Fig 5.1. The power, delay, PDP of the Approximate multipliers are shown in table 4. The approximate multipliers AM2, AM10, AM12 and AM13 has less propagation delay and AM15 is dissipates low power compared to all the approximate multipliers. The approximate multiplier AM15 has less PDP.

From All the quantitate results which are shown in Table 2,3 and 4, we conclude that proposed approximate adder 15(AA15) is energy efficient circuit. when the approximate adder AA15 is implemented in approximate 4-bit RCA and approximate 2*4 multiplier has the less PDP compared to all the proposed adder circuits.

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