Analog PID Controller Design with Op-Amps

From control intuition to circuit blocks

Zhicheng Sun

Analog Circuits Course Project

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Motivation (Why analog PID?)

- I usually implement PID in software; this project tries to **build it in analog circuitry**.
- Goal: a simple structure that is **fast, low-cost, and requires no programming**.
- Most importantly, it helps me understand what **integrators and differentiators** mean in real circuits.

PID in one equation

Error definition

$$e(t) = r(t) - y(t)$$

Control law

$$u(t) = K_p e(t) + K_i \int_0^t e(\tau)\, d\tau + K_d \frac{de(t)}{dt}$$

Intuition: do not only look at the current error; combine **present**, **accumulated**, and **trend** information.

What P / I / D actually do

- **P (Proportional):** stronger error $\Rightarrow$ stronger correction.
  - Too small: slow response and noticeable steady-state error.
  - Too large: overshoot or even oscillation.
- **I (Integral):** accumulates error to remove steady-state error.
  - Risk: integral windup when the actuator saturates.
- **D (Derivative):** uses the error trend to reduce overshoot.
  - Risk: sensitive to high-frequency noise $\Rightarrow$ use band-limited differentiation.

Analog implementation: block view

1. **Error detector:** a differential amplifier computes $e(t) = r(t) - y(t)$.
2. **Three parallel paths:**
   - P path: inverting amplifier (gain set by resistor ratio)
   - I path: op-amp integrator (RC time constant)
   - D path: band-limited differentiator (practical noise control)
3. **Summing & shaping:** inverting summer + output limiting to reduce windup.

Mapping parameters to components

Proportional path

$$G_P(s) = -\frac{R_f}{R_{in}} \quad \Rightarrow \quad K_p \approx \frac{R_f}{R_{in}}$$

Integral path

$$G_I(s) = -\frac{1}{RCs} \quad \Rightarrow \quad K_i \approx \frac{1}{RC}$$

Practical notes

- Add a large resistor in parallel with the integrator capacitor to reduce DC drift.
- Add limit/clamp at the output to mitigate integral windup.
- Use a band-limited differentiator to avoid noise amplification.

Simulation plan & conclusion

What to check in simulation

- Step response: overshoot, settling time, and steady-state error.
- Internal signals: outputs of P / I / D branches and the summed output.
- Saturation behavior: does integral windup appear and how do clamps help?

Takeaway

Analog PID is feasible and intuitive: gains map directly to resistor ratios and RC time constants. The key engineering issues are **noise** (especially D) and **saturation** (especially I).