SPI -Final Report

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Abstract:

This lab explores the functionality of an SPI (Serial Peripheral Interface) Master Core integrated with sub-blocks including a Wishbone Master, SPI Clock Generation, and SPI Shift Register. We aim to understand how the SPI Master Core communicates with SPI Slaves, handles clock generation and data serialization, and observe its interaction with external devices.

Introduction:

The SPI (Serial Peripheral Interface) protocol is widely used for communication between microcontrollers and peripheral devices. In this experiment, we investigate the operation of an SPI Master Core, which plays a vital role in orchestrating communication with multiple SPI Slave devices. The SPI Master Core comprises three primary sub-blocks: a Wishbone Master for control, SPI Clock Generation for generating clock signals, and SPI Shift Register for data serialization.

Project Blocks:

- Wishbone Master Block
- SPI Master core
- SPI Clock Generation (Sub-Block)
- SPI Shift Register (Sub-Block):
- SPI Shift Register Block

SERIAL PERIPHERAL INTERFACE:

- **SPI Overview**: SPI is a full-duplex, high-speed communication protocol that allows data exchange between a master and one or more slave devices. It is commonly used in embedded systems and microcontroller applications.

- **Data Shifting**: SPI relies on shifting data in a shift register in both the master and slave devices. This shifting allows data to be transmitted and received simultaneously.
- **Synchronous Clock Signal**: The transmission in SPI is synchronized to a clock signal generated by the master device. This clock signal controls the timing of data exchange.
- **Two-Way Communication**: SPI is a bidirectional communication protocol where the master sends data to the slave, and the slave keeps the received data in its shift register. This allows for full duplex communication.
- **Minimal Signal Lines**: SPI uses only four signal lines for communication between the master and the slave, making it efficient in terms of pin usage. These four signals are:

1. Serial Clock (SCLK): Generated by both master and slave.
2. Slave Select (SS or SS_bar): Output from the master to select a specific slave for communication.
3. Master Out Slave In (MOSI): Data output from the master.
4. Master In Slave Out (MISO): Data output from the slave.

- **Single Master, Multiple Slaves**: SPI can operate with a single master device and multiple slave devices. The master can select which slave to communicate with by activating the corresponding Slave Select line.
- **SPI Modes**: SPI operates in four different modes, which are often defined by the data transmission and reception edges concerning the clock signal. These modes are used to specify the clock polarity and phase and are important for ensuring proper data synchronization.

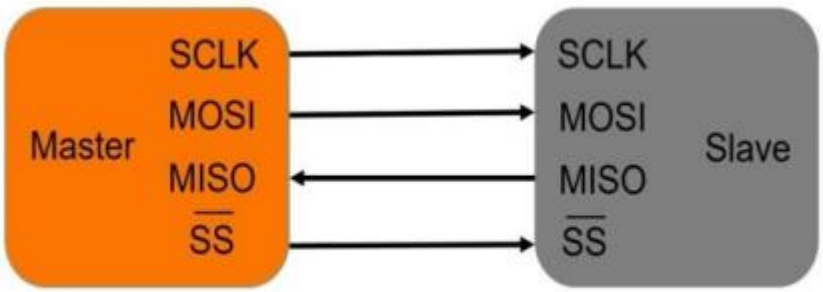
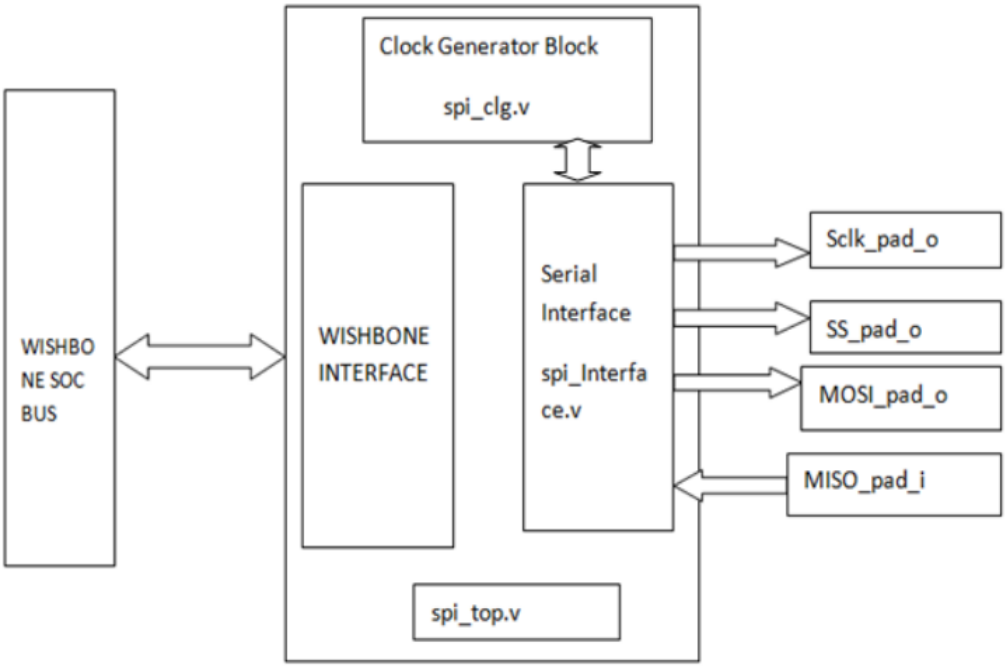
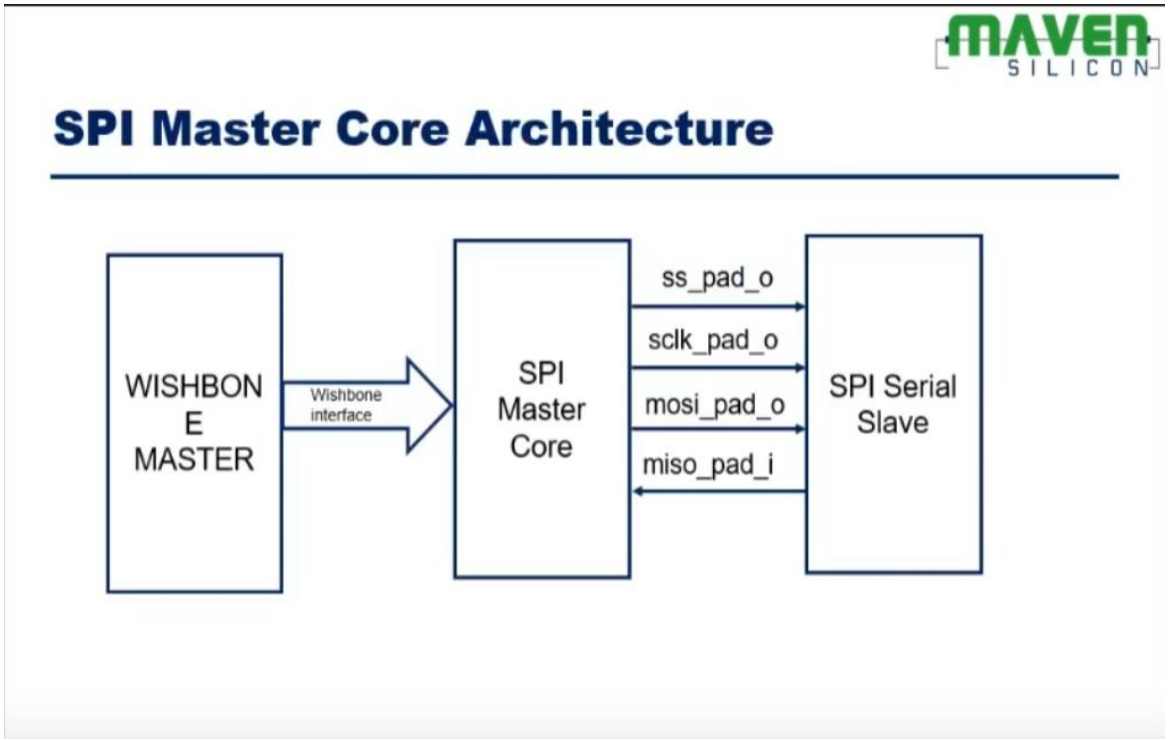


Figure 1: Serial Peripheral Interface

Top module block diagram:

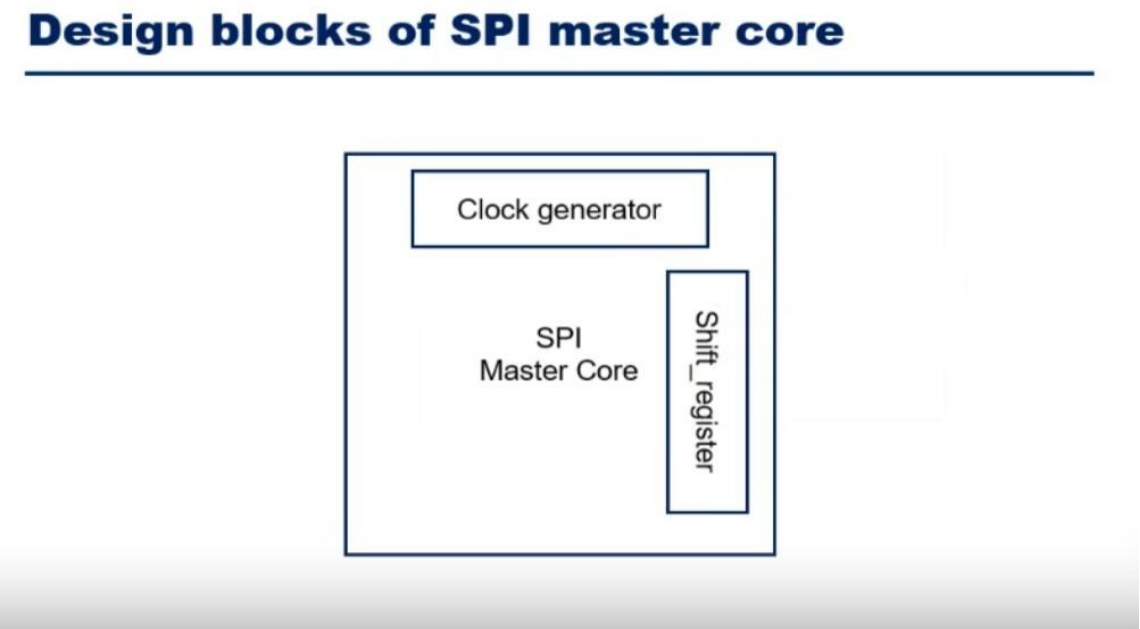




Overall functionality:

- Wishbone Master: This block serves as the interface for communication between the SPI Master Core and the external system. It controls the Wishbone bus transactions, handling read and write operations. It allows the core to read from and write to various registers.
- SPI Master Core (including Clock Generation and Shift Register): This is the heart of the SPI master functionality. It includes the clock generation block, which generates the clock signal required for SPI communication. The clock signal is crucial for synchronizing data transfers with SPI slave devices. The shift register is responsible for serializing and deserializing data, as well as managing data frame formats and timing.
- SPI Slave: While not explicitly mentioned in the sub-blocks, the SPI Master Core also interacts with external SPI Slaves, enabling communication between the master and slave devices. The SPI Slave devices can include sensors, displays, memory chips, or any other peripherals that use the SPI communication protocol.

Sub-blocks block diagram:



Functionality:

- SPI Clock Generation (Sub-Block): The clock generation sub-block generates the clock signals necessary for SPI communication, including the serial clock (sclk). It ensures that the clock signals are synchronized with the Wishbone bus clock and provides the required timing for SPI data transmission.
- SPI Shift Register (Sub-Block): The SPI shift register sub-block is responsible for serializing and deserializing data as it is transmitted over the SPI bus. It handles the transmission and reception of data, including the management of control signals such as MOSI (Master Out Slave In), MISO (Master In Slave Out), and tip (Transaction in Progress). The shift register manages the state of the SPI transaction, including the data format (e.g., data width, MSB or LSB first) and communication parameters (e.g., clock polarity).

WISHBONE Interface Signals:

Port	Width	Direction	Description
wb_clk_i	1	Input	Master clock
wb_rst_i	1	Input	Synchronous reset, active high
wb_adr_i	5	Input	Lower address bits
wb_dat_i	32	Input	Data towards the core
wb_dat_o	32	Output	Data from the core
wb_sel_i	4	Input	Byte select signals
wb_we_i	1	Input	Write enable input
wb_stb_i	1	Input	Strobe signal/Core select input
wb_cyc_i	1	Input	Valid bus cycle input
wb_ack_o	1	Output	Bus cycle acknowledge output
wb_err_o	1	Output	Bus cycle error output
wb_int_o	1	Output	Interrupt signal output

SPI External Connections:

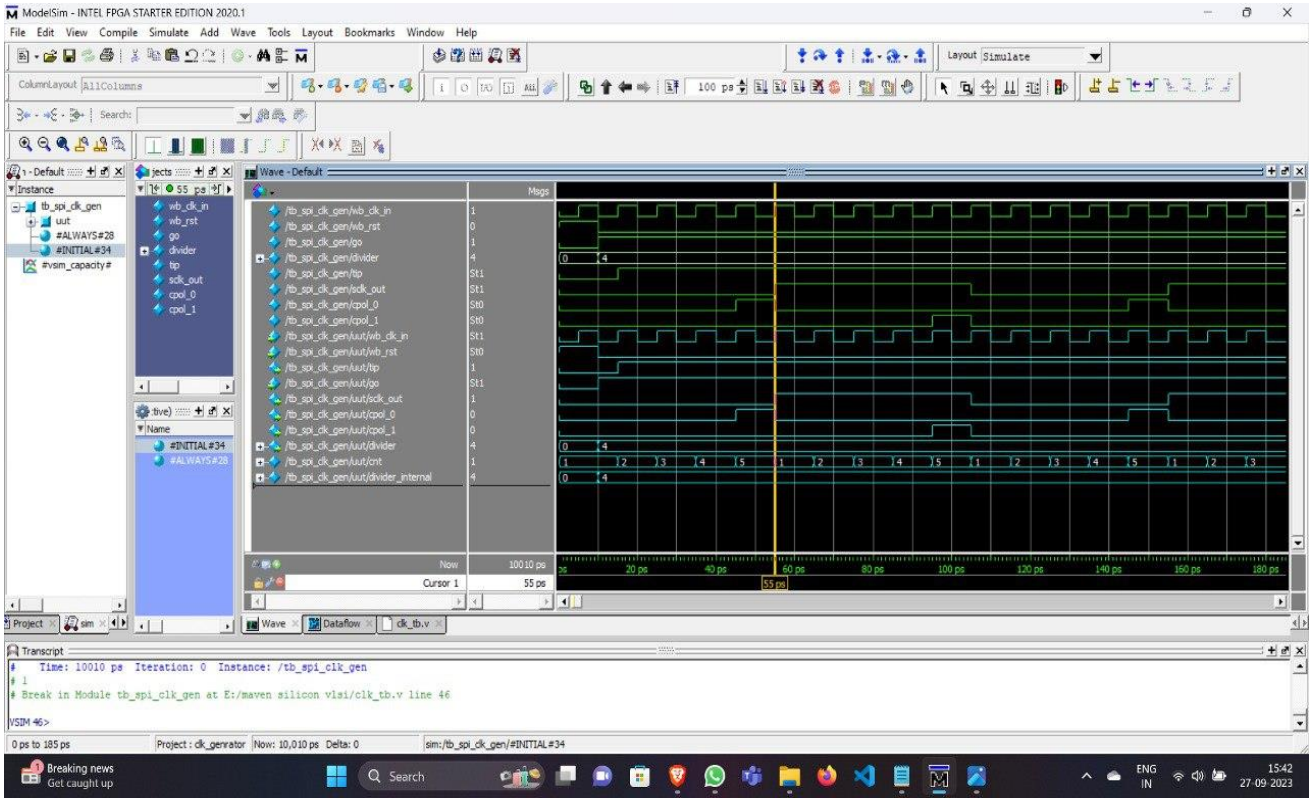
Port	Width	Direction	Description
/ss_pad_o	8	Output	Slave select output signals
sclk_pad_o	1	Output	Serial clock output
mosi_pad_o	1	Output	Master out slave in data signal output
miso_pad_i	1	Input	Master in slave out data signal input

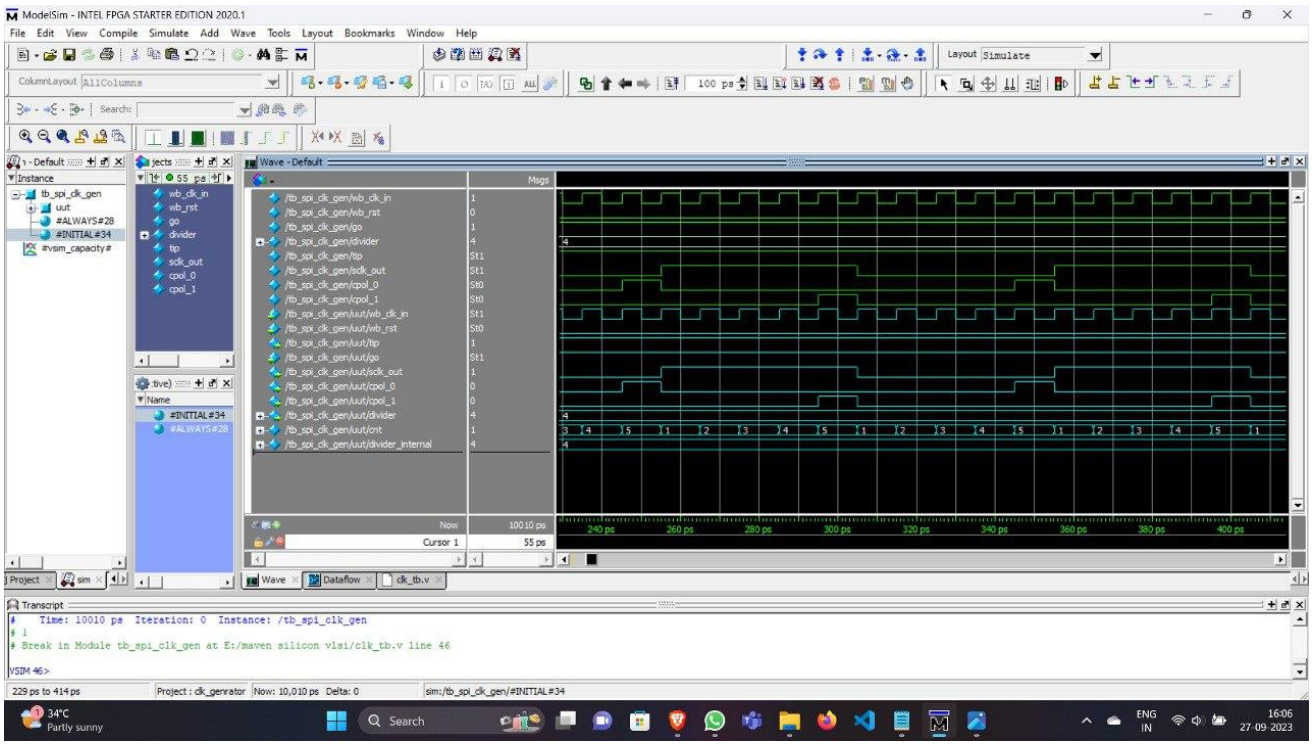
Core Register List:

Name	Address	Width	Access	Description
Rx0	0x00	32	R	Data receive register 0
Rx1	0x04	32	R	Data receive register 1
Rx2	0x08	32	R	Data receive register 2
Rx3	0x0c	32	R	Data receive register 3
Tx0	0x00	32	R/W	Data transmit register 0
Tx1	0x04	32	R/W	Data transmit register 1
Tx2	0x08	32	R/W	Data transmit register 2
Tx3	0x0c	32	R/W	Data transmit register 3
CTRL	0x10	32	R/W	Control and status register
DIVIDER	0x14	32	R/W	Clock divider register
SS	0x18	32	R/W	Slave select register

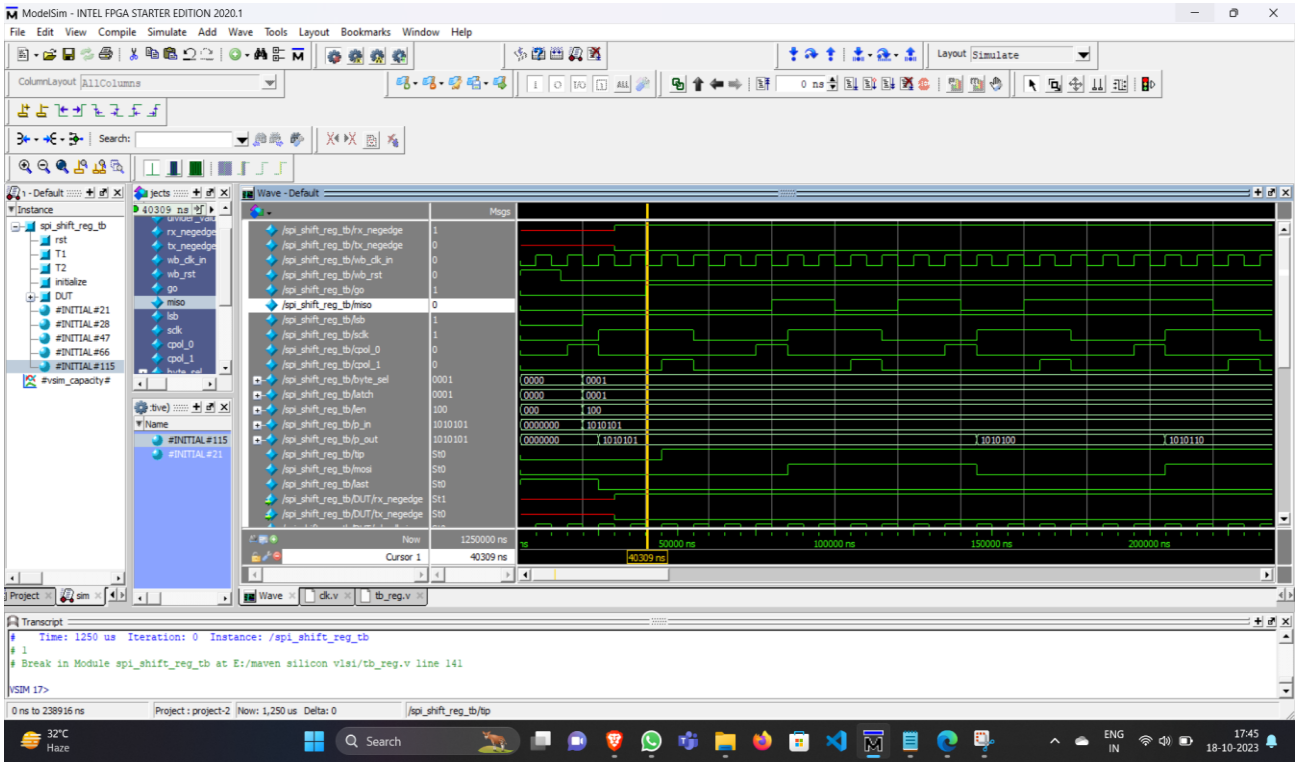
Output Waveforms of Sub-blocks of SPI Master core:

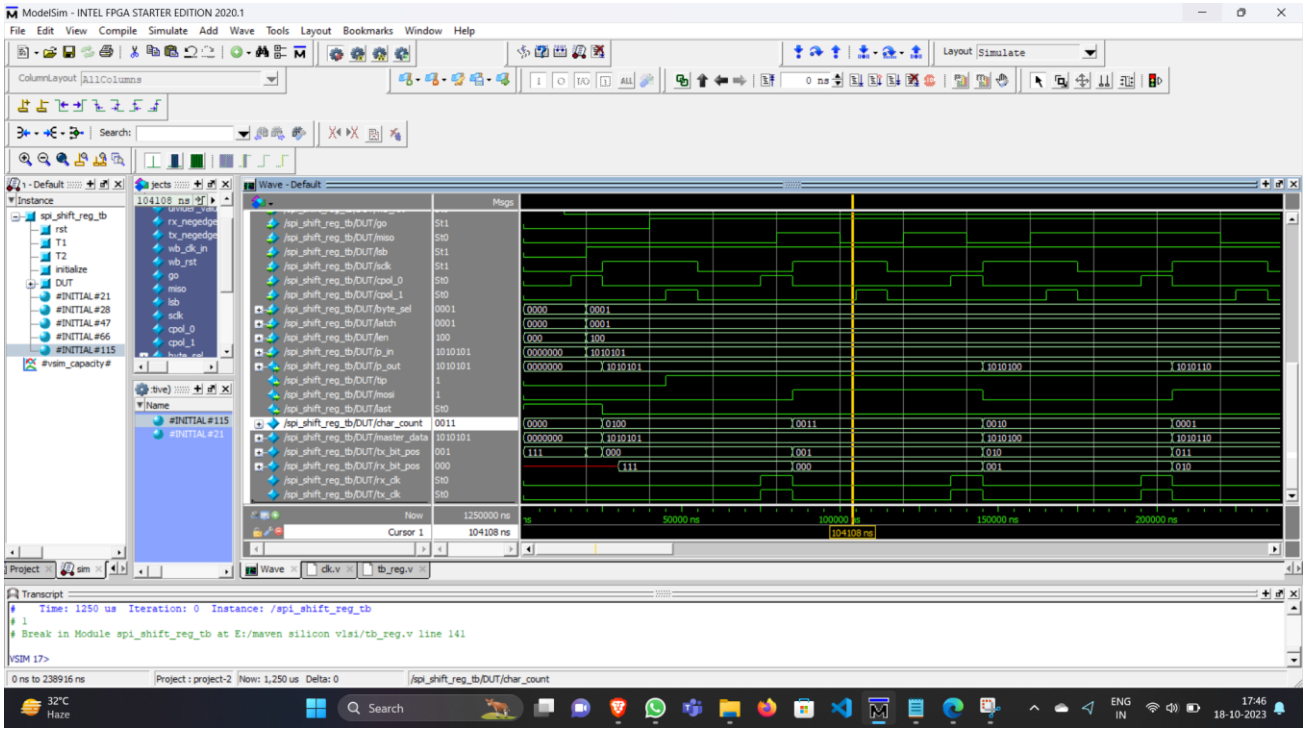
Clock Generator Waveform:





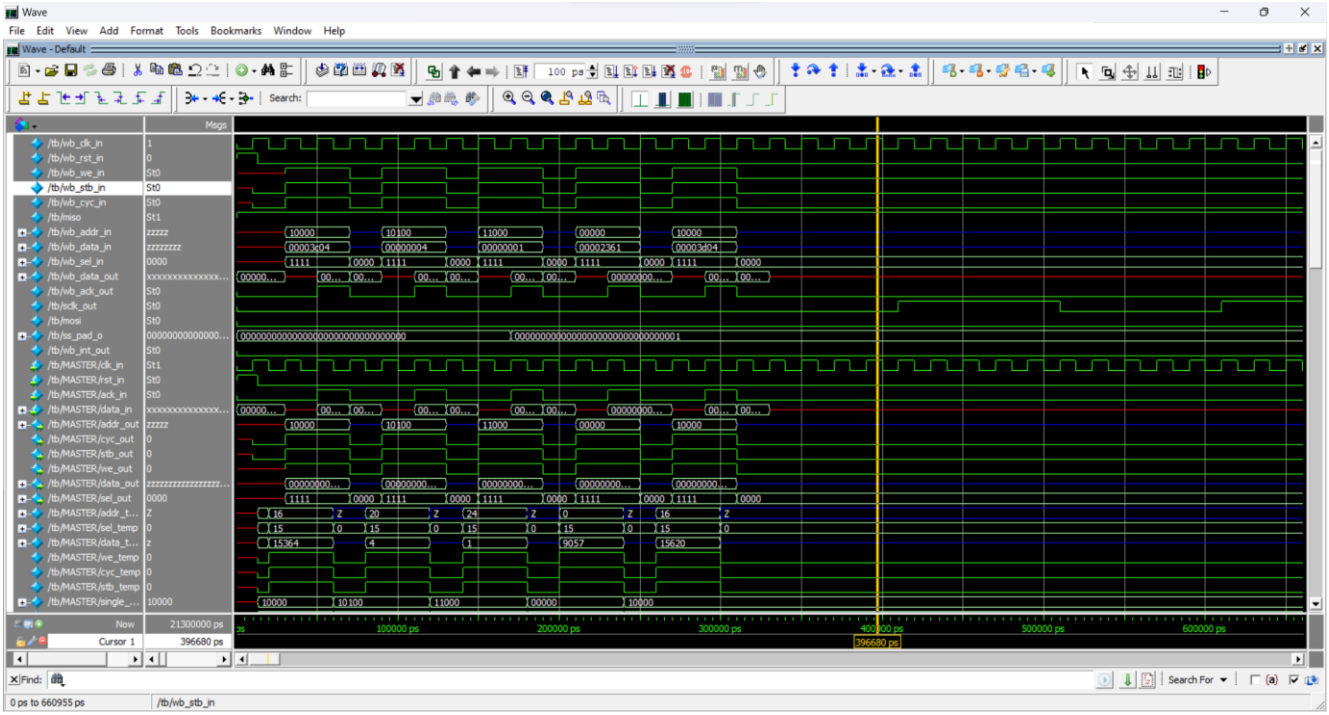
Shift Register Waveform:

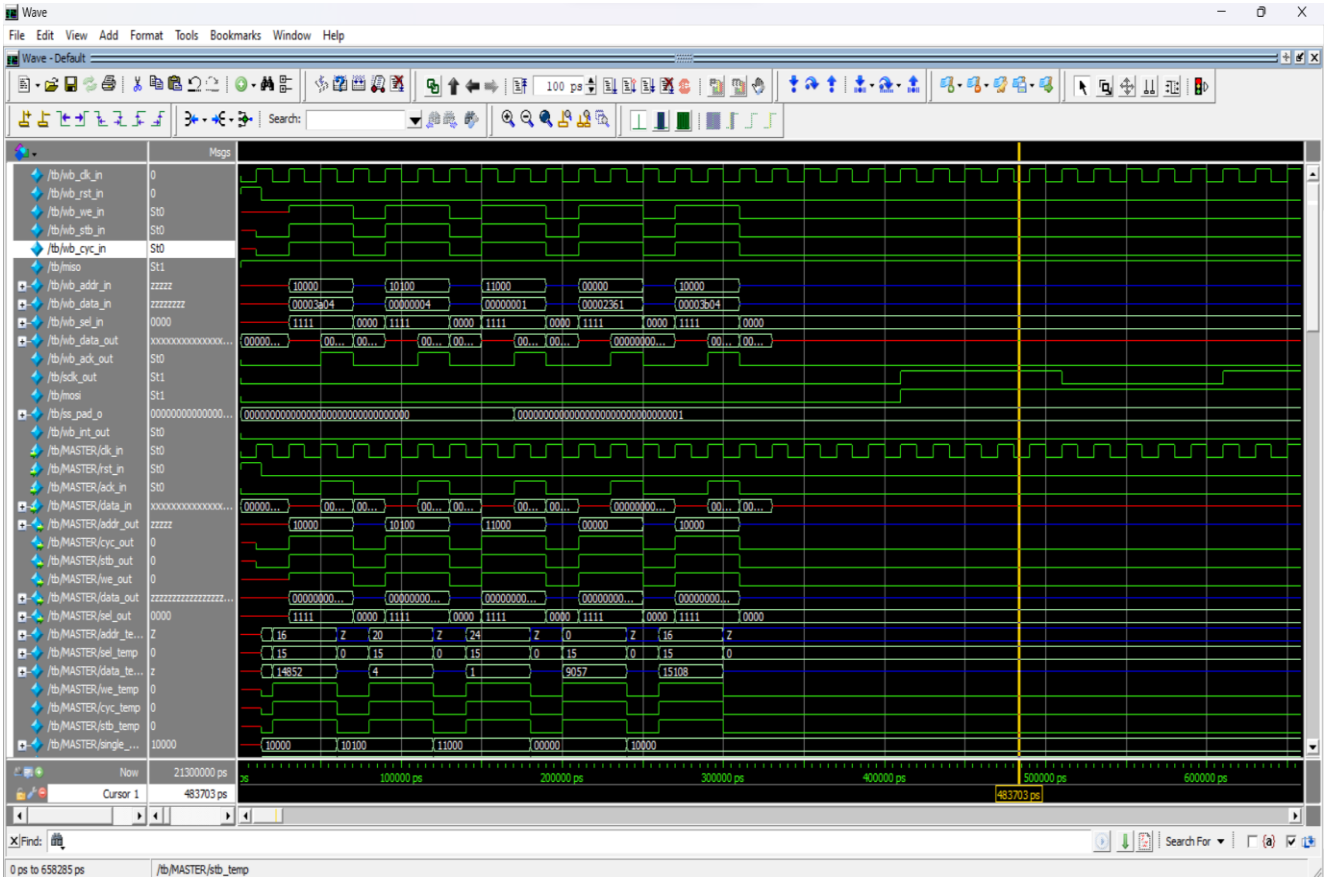




Output Waveforms of Top module of SPI Master core:

CASE 1 and 2 waveforms:





Results:

- Successful data exchange with SPI Slaves.
- Analysis of SPI signals including clock generation, data serialization, and control signals.
- Data integrity and correctness verification.

Conclusion:

In conclusion, the lab experiment revealed the efficient operation of the SPI Master Core and its sub-blocks. The core successfully communicated with SPI Slave devices, managed data transfer, and maintained signal integrity. This experiment enhanced our understanding of SPI communication protocols and the SPI Master Core's role in enabling these communications.