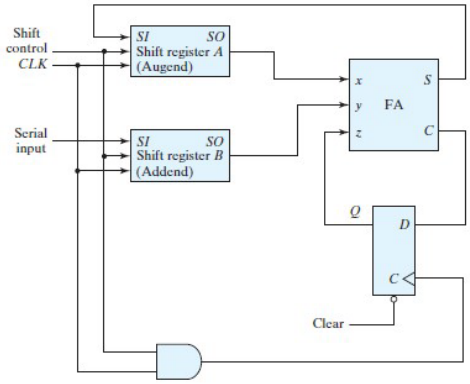
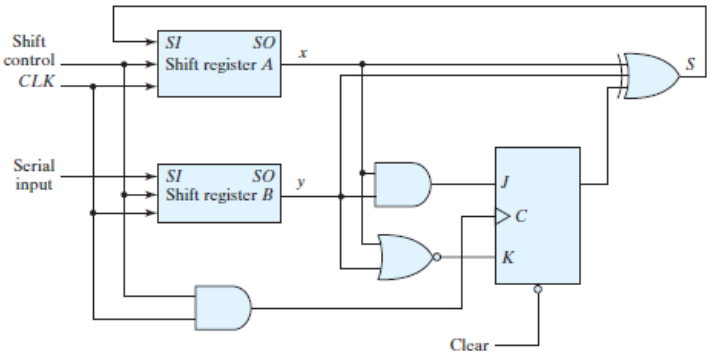
EE2001-Tutorial 7
Date: 15th March 2018
Registers and Counters

1) Two ways for implementing a serial adder (A + B) is shown. It is necessary to modify the circuits to convert them to serial subtractors (A - B).
(a) Using the left-sided circuit, show the changes needed to perform A + 2's complement of B. (b) Using the right-sided circuit, show the changes needed by modifying the corresponding state table from an adder to a subtractor circuit.



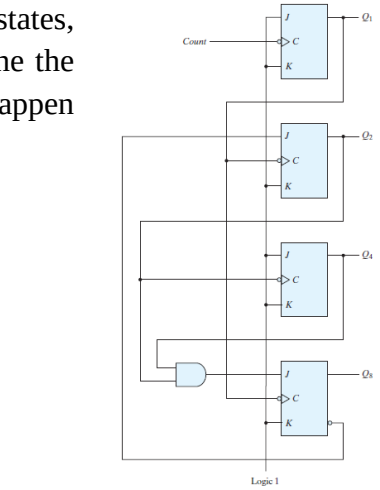


2) (i) Design a serial 2's complementer with a shift register and a flip-flop. The binary number is shifted out from one side and it's 2's complement shifted into the other side of the shift register.
(ii) A binary ripple counter uses flip-flops that trigger on the positive-edge of the clock. What will be the count if (a) the normal outputs of the flip-flops are connected to the clock and (b) the complement outputs of the flip-flops are connected to the clock?

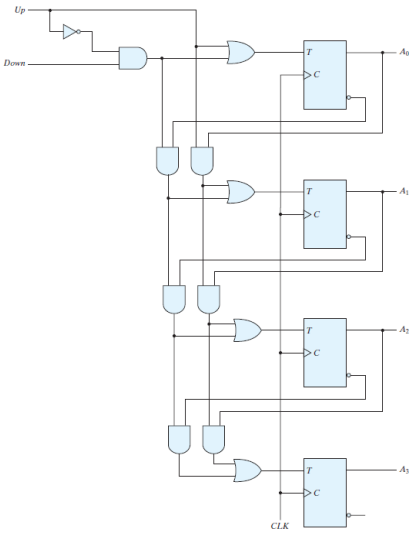
3) (i) Draw the logic diagram of a four-bit binary ripple countdown counter using
(a) flip-flops that trigger on the positive-edge of the clock and
(b) flip-flops that trigger on the negative-edge of the clock.
(ii) Show that a BCD ripple counter can be constructed using a four-bit binary ripple counter with asynchronous clear and a NAND gate that detects the occurrence of count 1010.

4) (i) How many flip-flop will be complemented in a 10-bit binary ripple counter to reach the next count after the following counts?
(a) 1001100111
(b) 1111000111
(c) 0000001111
(ii) A flip-flops has a 3 ns delay from the time the clock edge occurs to the time the output is complemented. What is the maximum delay in a 10-bit binary ripple counter that uses these flip-flops? What is the maximum frequency at which the counter can operate reliably?

5) The BCD ripple counter shown has four flip-flops and 16 states, of which only 10 are used. Analyze the circuit and determine the next state for each of the other six unused states. What will happen if a noise signal sends the circuit to one of the unused states?

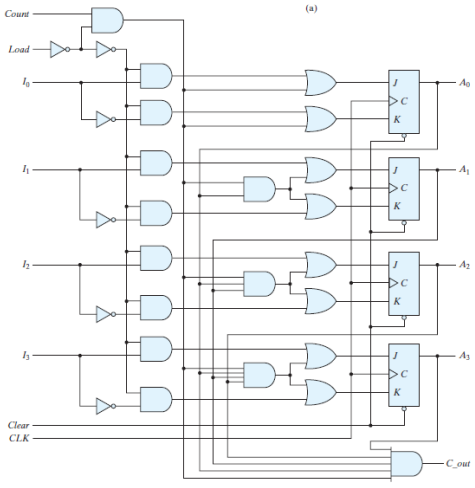


6) (i) Design a four-bit binary synchronous counter with D flip-flops.
(ii) What operation is performed in the given up–down counter when both the up and down
inputs are enabled? Modify the circuit so that when both inputs are equal to 1, the counter does not change state.

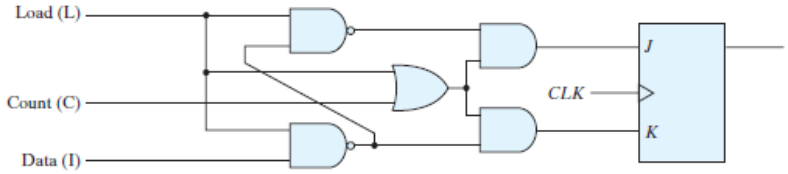


7) Obtain the input equations for a BCD counter that uses
(a) JK flip-flops,
(b) D flipflops
(c) T- flipflops.
Compare the three designs to determine which one is the most efficient.

8) Enclose the given binary counter with parallel load in a block diagram showing all inputs and outputs.
(a) Show the connections of four such blocks to produce a 16-bit counter with parallel load.
(b) Construct a binary counter that counts from 0 through binary 127.



9) The binary counter with parallel load has two control inputs—Load (L) and Count (C)—and a data input, (I_i).
(a) Derive the flip-flop input equations for J and K of the first stage in terms of L, C, and I.
(b) The logic diagram of the first stage of an equivalent circuit is shown above. Verify if this circuit is equivalent to the one in (a).



10) (i) For the binary counter with parallel load circuit, give three alternatives for a mod-12 counter (i.e., the count evolves through a sequence of 12 distinct states)
(a) Using an AND gate and the load input.
(b) Using the output carry.
(c) Using a NAND gate and the asynchronous clear input.
(ii) Design a timing circuit that provides an output signal that stays on for exactly twelve clock cycles. A start signal sends the output to the 1 state, and after twelve clock cycles the signal returns to the 0 state.