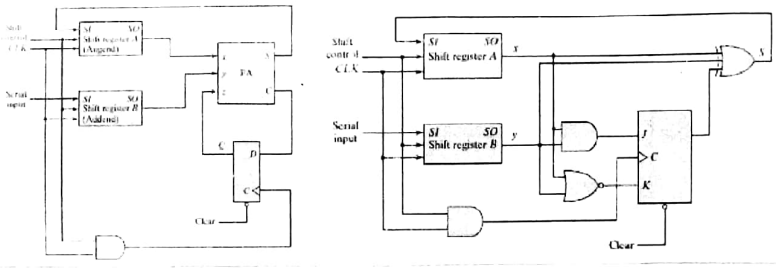
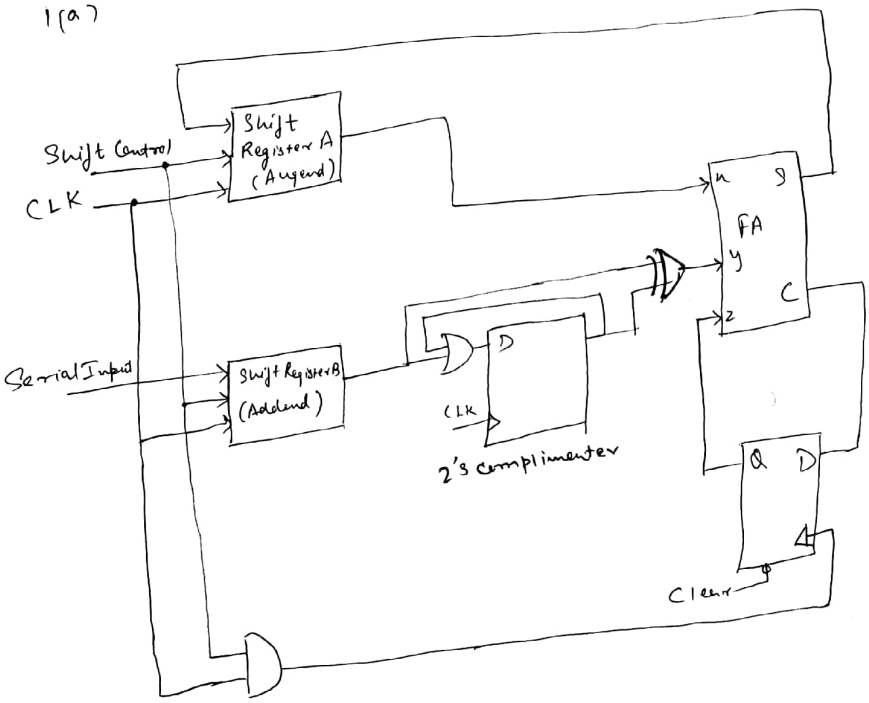
EE2001-Tutorial 7
Date: 13th March 2018
Registers and Counters

1) Two ways for implementing a serial adder (A + B) is shown. It is necessary to modify the circuits to convert them to serial subtractors (A - B).
(a) Using the left-sided circuit, show the changes needed to perform A + 2's complement of B. (b) Using the right-sided circuit, show the changes needed by modifying the corresponding state table from an adder to a subtractor circuit.



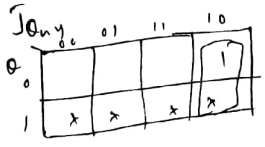
1(a)



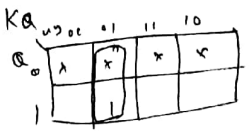
Both A and 2's compliment of B are fed in FA. If carry is there then it is fed back as z through D-FF.

(b) Complimenting B register output

Q	u	y	Q(t+1)	JQ	KQ
0	0	0	0	0	x
0	0	1	0	0	x
0	1	0	1	1	x
0	1	1	0	0	x
1	0	0	1	x	0
1	0	1	0	x	1
1	1	0	1	x	0
1	1	1	1	x	0



$JQ = u\bar{y}$



$KQ = \bar{u}y$

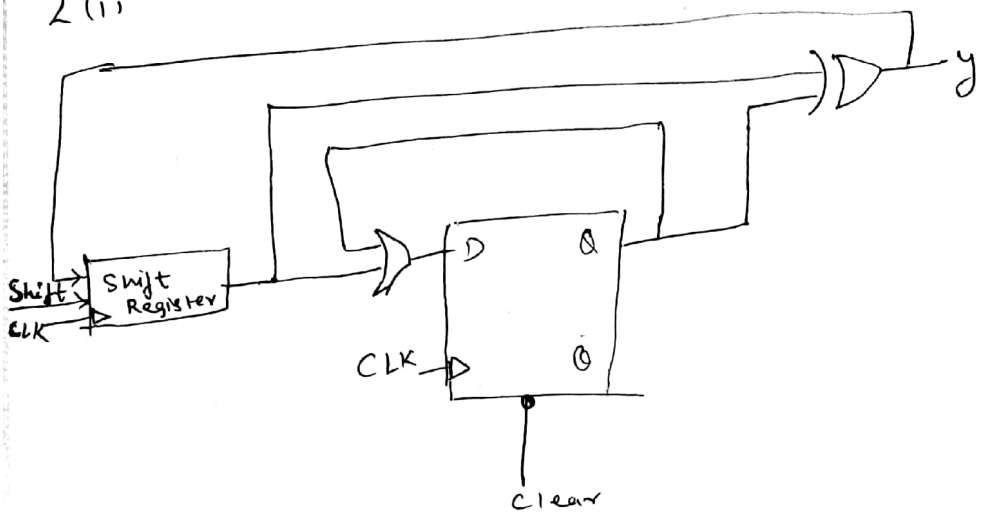
The next state Q(t+1) is decided by $\bar{y}$ and u

Assuming the J-K flipflop is set initially. It will behave as a subtractor circuit.

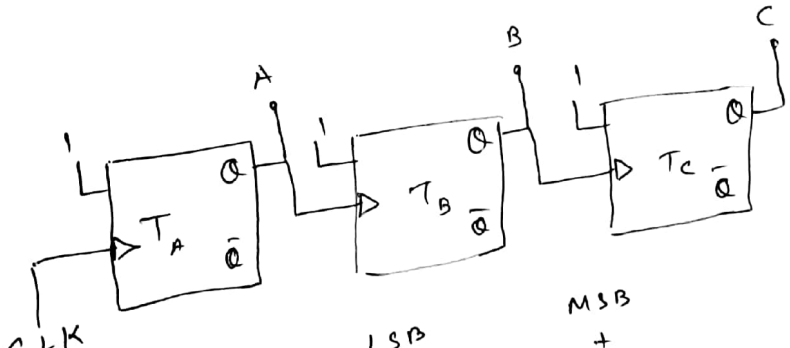
2) (i) Design a serial 2's complementer with a shift register and a flip-flop. The binary number is shifted out from one side and it's 2's complement shifted into the other side of the shift register.

(ii) A binary ripple counter uses flip-flops that trigger on the positive-edge of the clock. What will be the count if (a) the normal outputs of the flip-flops are connected to the clock and (b) the complement outputs of the flip-flops are connected to the clock?

2 (i)



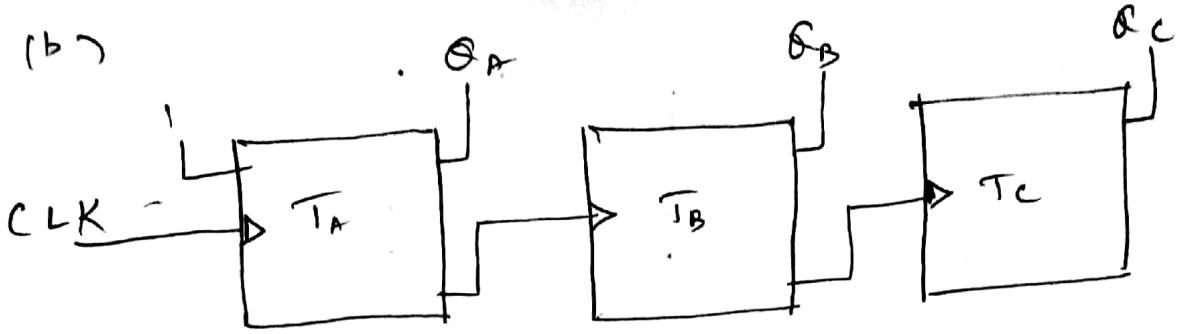
(ii) (a) It is an Downcounter



LSB A	B	MSB C	LSB A^+	B^+	MSB C^+
1	1	1	0	1	1
0	1	1	1	0	1
1	0	1	0	0	1
0	0	1	1	1	0
1	1	0	0	1	0
0	1	0	1	0	0
1	0	0	0	0	0

UP Counter.

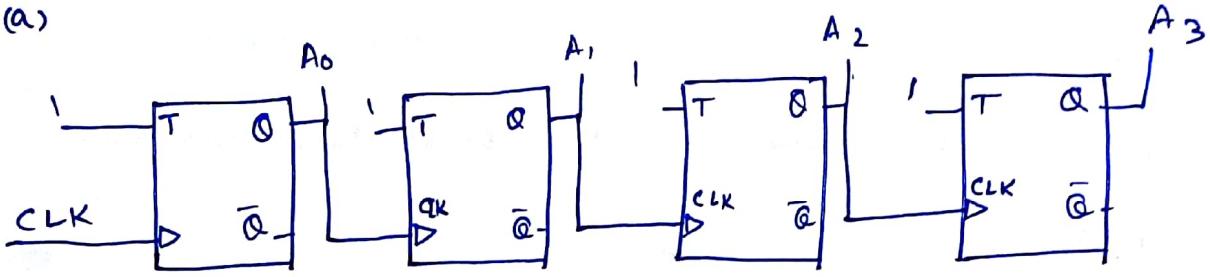
(b)



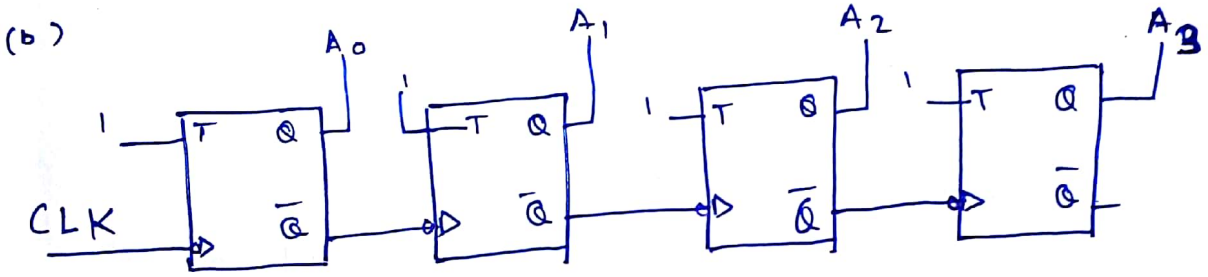
LSB A	B	MSB C	LSB A^+	B^+	MSB C^+
0	0	0	1	0	0
1	0	0	0	1	0
0	1	0	1	1	0
1	1	0	0	0	1
0	0	1	1	0	1
1	0	1	0	1	1
0	1	1	1	1	1

3) (i) Draw the logic diagram of a four-bit binary ripple countdown counter using
(a) flip-flops that trigger on the positive-edge of the clock and
(b) flip-flops that trigger on the negative-edge of the clock.
(ii) Show that a BCD ripple counter can be constructed using a four-bit binary ripple counter with asynchronous clear and a NAND gate that detects the occurrence of count 1010.

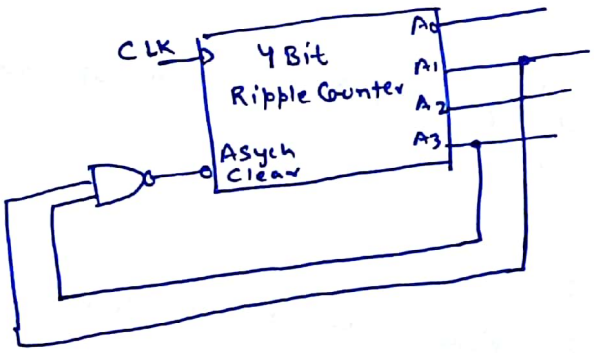
(i) (a)



(b)



(ii)



A_3	A_2	A_1	A_0
1	0	1	0

Only for the case 1010 the ripple counter is getting cleared. Once the count reaches from 0000 to 1001 it remains as it is. After 1001, 1010 is reached so the counter is cleared off.

4) (i) How many flip-flop will be complemented in a 10-bit binary ripple counter to reach the next count after the following counts?

(a) 1001100111

(b) 1111000111

(c) 0000001111

(ii) A flip-flops has a 3 ns delay from the time the clock edge occurs to the time the output is complemented. What is the maximum delay in a 10-bit binary ripple counter that uses these flip-flops? What is the maximum frequency at which the counter can operate reliably?

(a) Add 1 to the sequence so that first four bits will be toggled.

```
  1 0 0 1 1 0 0 1 1 1
                  +
                  1
  ---------------------
  1 0 0 1 1 0 1 0 0 0
  ---------------------
```

Four FF will be complemented

(b)

```
  1 1 1 1 0 0 0 1 1 1
                +   1
  ---------------------
  1 1 1 1 0 0 1 0 0 0
  ---------------------
```

Four FF will be complemented

(c)

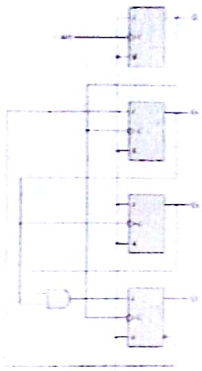
```
  0 0 0 0 0 0 1 1 1 1
                  1
  ---------------------
  0 0 0 0 0 1 0 0 0 0
  ---------------------
```

Five FF will be complemented

(ii) Maximum Delay = $3ns \times 10 = 30ns$

Maximum Frequency at which counter can operate reliably = $\frac{1}{30ns} = 33.33MHz$

5) The BCD ripple counter shown has four flip-flops and 16 states, of which only 10 are used. Analyze the circuit and determine the next state for each of the other six unused states. What will happen if a noise signal sends the circuit to one of the unused states?



5. BCD ripple counter counts from 0 – 9

No. of flip flop = 4

Total States = 16

Unused States = 16 − 10 = 6

	CLK	Q_8	Q_4	Q_2	Q_1
BCD Ripple Counter	1	0	0	0	0
	2	0	0	0	1
	3	0	0	1	0
	4	0	0	1	1
	5	0	1	0	0
	6	0	1	0	1
	7	0	1	1	0
	8	0	1	1	1
	9	1	0	0	0
	10	1	0	0	1
Unused States	11	1	0	1	0
	12	1	0	1	1
	13	1	1	0	0
	14	1	1	0	1
	15	1	1	1	0
	16	1	1	1	1

Analysis from given Circuit

* Q_1 changes state after each CP
* Q_2 toggles everytime Q_1 goes from 1 to 0 till $Q_8 = 0$
* when $Q_8 = 1$, Q_2 remain 0
* Q_4 compliments everytime Q_2 goes from 1 to 0
* Q_8 remains at 0 as long as Q_2 or $Q_4 = 0$ ($\because$ AND gate)
* when both Q_2 & Q_4 becomes 1, Q_8 toggles ~~from~~ when Q_1 goes from 1 to 0.
* Q_8 is cleared on next transition of Q_1.

PS				NS							
Q_8	Q_4	Q_2	Q_1	Q_8^+	Q_4^+	Q_2^+	Q_1^+	Q_8^{++}	Q_4^{++}	Q_2^{++}	Q_1^{++}
1	0	1	0	1	0	1	1	0	1	0	0
1	0	1	1	0	1	0	0	0	1	0	1
1	1	0	0	1	1	0	1	0	1	0	0
1	1	0	1	0	1	0	0	0	1	0	1
1	1	1	0	1	1	1	1	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	1

If a noise signal sends the circuit to one of the unused state then after 1 or 2 clock cycles the counter will resume from either 0100 or 0101 or 0000 or 0001 depending upon unused state.

EE2001-Tutorial 7
Date: 15th March 2018
Registers and Counters

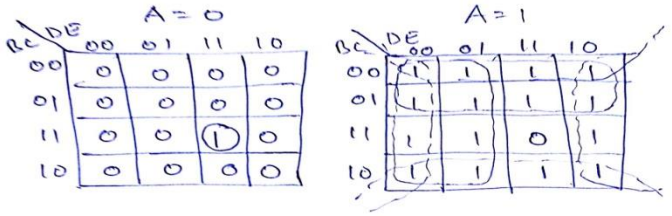
6)(i) Design a four-bit binarysynchronous counter with Dflip-flops.

Answer:

STATE TABLE:

Present state	Input	Next State	D- Flipflop inputs			
ABCD	E	A+B+C+ D+	D3	D2	D1	D0
0000	0	0000	0	0	0	0
0000	1	0001	0	0	0	1
0001	0	0001	0	0	0	1
0001	1	0010	0	0	1	0
0010	0	0010	0	0	1	0
0010	1	0011	0	0	1	1
0011	0	0011	0	0	1	1
0011	1	0100	0	1	0	0
0100	0	0100	0	1	0	0
0100	1	0101	0	1	0	1
0101	0	0101	0	1	0	1
0101	1	0110	0	1	1	0
0110	0	0110	0	1	1	0
0110	1	0111	0	1	1	1
0111	0	0111	0	1	1	1
0111	1	1000	1	0	0	0
1000	0	1000	1	0	0	0
1000	1	1001	1	0	0	1
1001	0	1001	1	0	0	1
1001	1	1010	1	0	1	0
1010	0	1010	1	0	1	0
1010	1	1011	1	0	1	1
1011	0	1011	1	0	1	1
1011	1	1100	1	1	0	0
1100	0	1100	1	1	0	0
1100	1	1101	1	1	0	1
1101	0	1101	1	1	0	1
1101	1	1110	1	1	1	0
1110	0	1110	1	1	1	0
1110	1	1111	1	1	1	1
1111	0	1111	1	1	1	1
1111	1	0000	0	0	0	0

K-map for A+

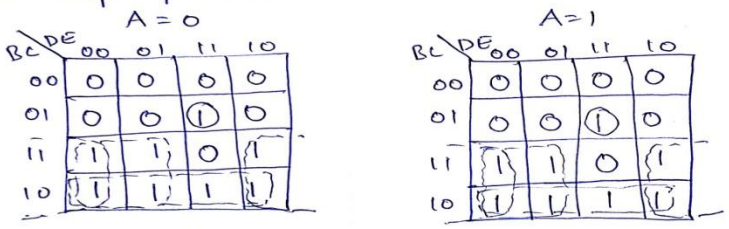


$A^+ = A'BCDE + A(B'+C'+D'+E')$

$= A'BCDE + A(BCDE)'$

$= A \oplus (BCDE)$

K-map for B+

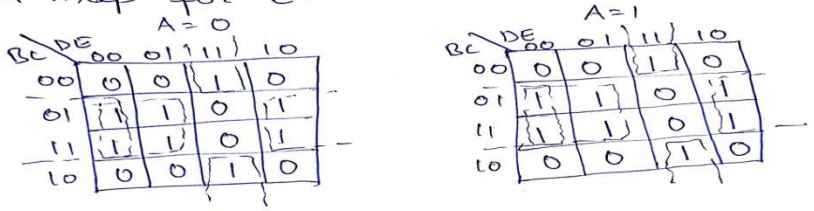


$B^+ = B'CDE + BC' + BD' + BE'$

$= B'CDE + B(CDE)'$

$= B \oplus (CDE)$

K-map for C+



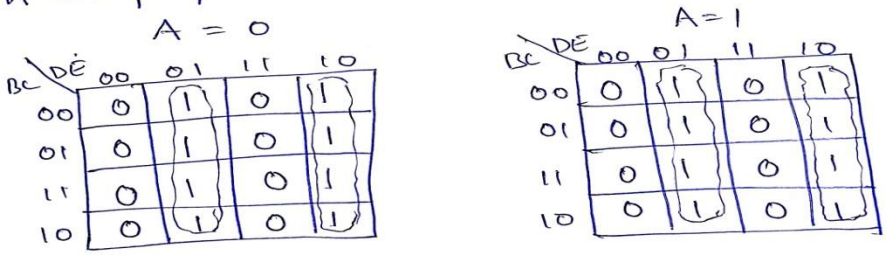
$C^+ = CD' + CE' + C'DE$

$= C(D'+E') + C'DE$

$= C(DE)' + C'DE$

$= C \oplus (DE)$

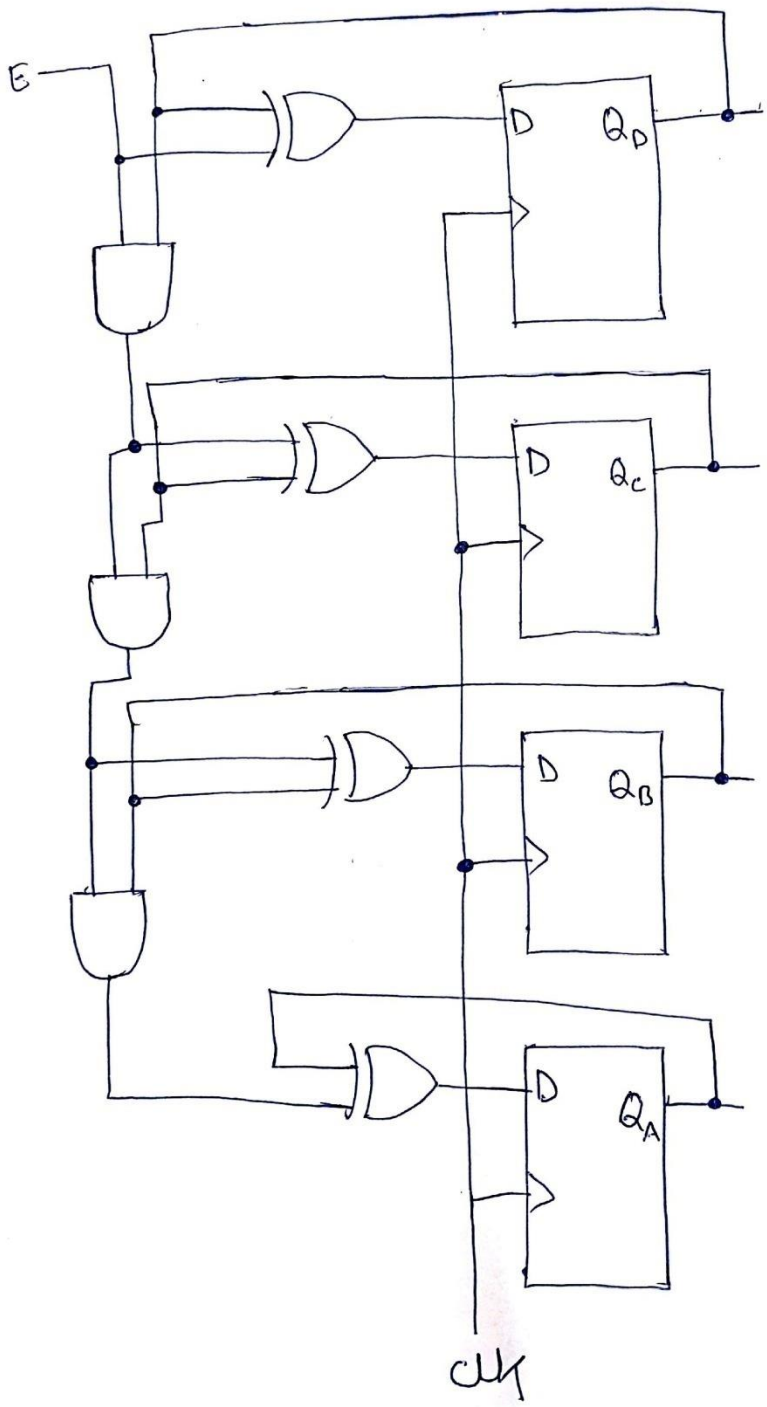
K-map for D+



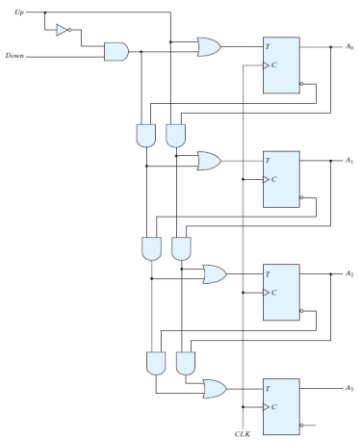
$D^+ = D'E + DE'$

$= D \oplus E$

Circuit Diagram:-

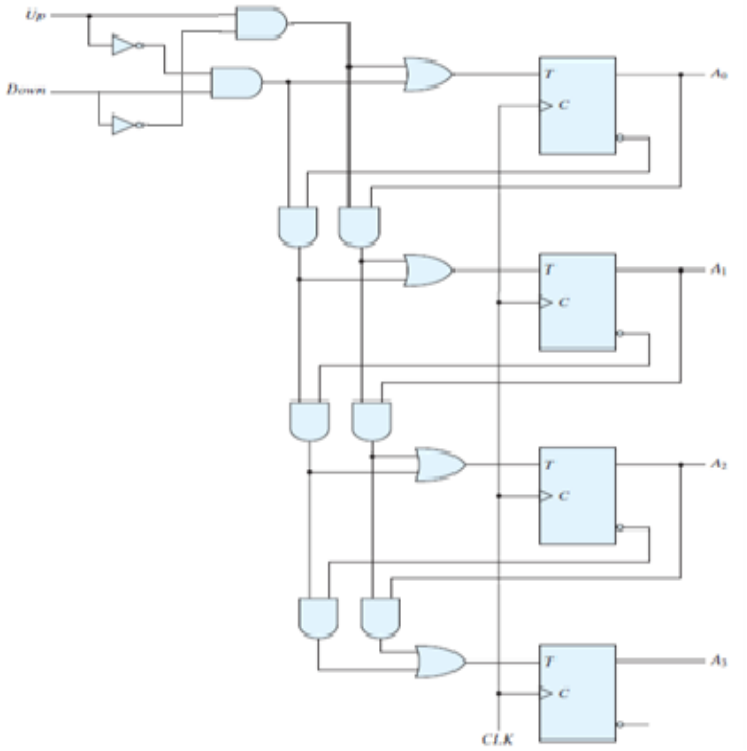


(ii) What operation is performedin the given up–down counterwhen both the up and down
inputs are enabled? Modify thecircuit so that when both inputsare equal to 1, the counter doesnot change state.



Answer: When both up and down inputs are enabled , up-counter operation is performed.

Modified circuit diagram so that both inputs are equal to 1, counter does not change state is given below:



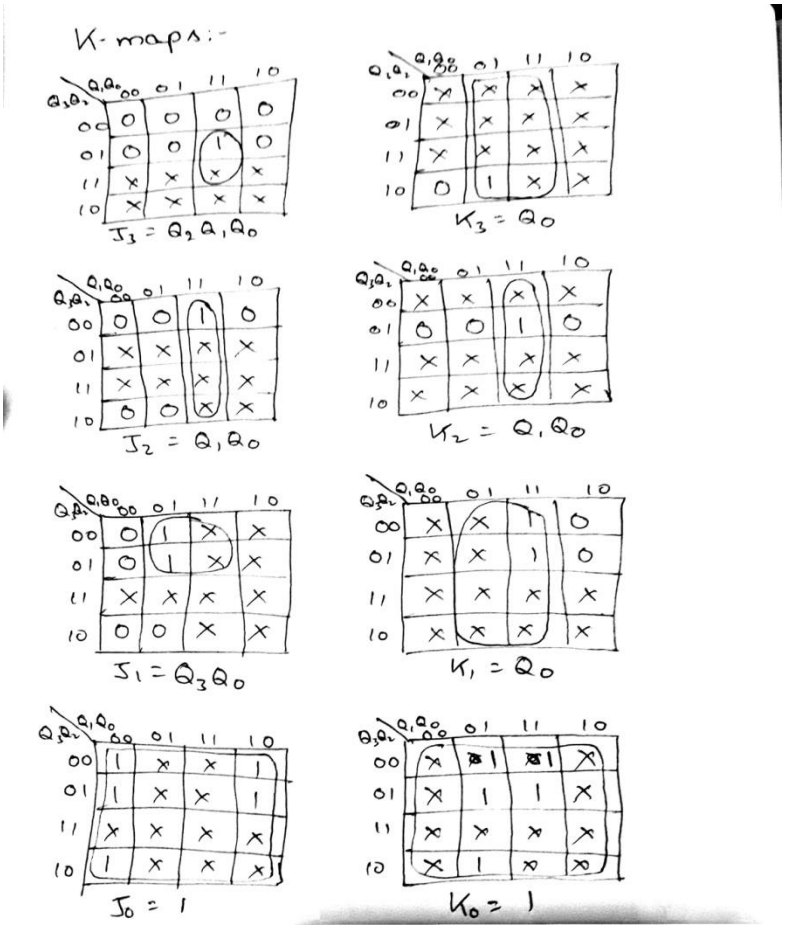
7)Obtain the input equations for a BCD counter that uses
(a) JK flip-flops,
(b) D flipflops
(c) T- flipflops.
Compare the three designs to determine which one is themost efficient.

Answer:

a) JK flip-flops

State table:

Present state	Next state	Output	Flip-flop inputs							
Q3 Q2 Q1 Q0	Q3 Q2 Q1 Q0	y	J3	K3	J2	K2	J1	K1	J0	K0
0000	0001	0	0	X	0	X	0	X	1	X
0001	0010	0	0	X	0	X	1	X	X	1
0010	0011	0	0	X	0	X	X	0	1	X
0011	0100	0	0	X	1	X	X	1	X	1
0100	0101	0	0	X	X	0	0	X	1	X
0101	0110	0	0	X	X	0	1	X	X	1
0110	0111	0	0	X	X	0	X	0	1	X
0111	1000	0	1	X	X	1	X	1	X	1
1000	1001	0	X	0	0	X	0	X	1	X
1001	0000	1	X	1	0	X	0	X	X	1



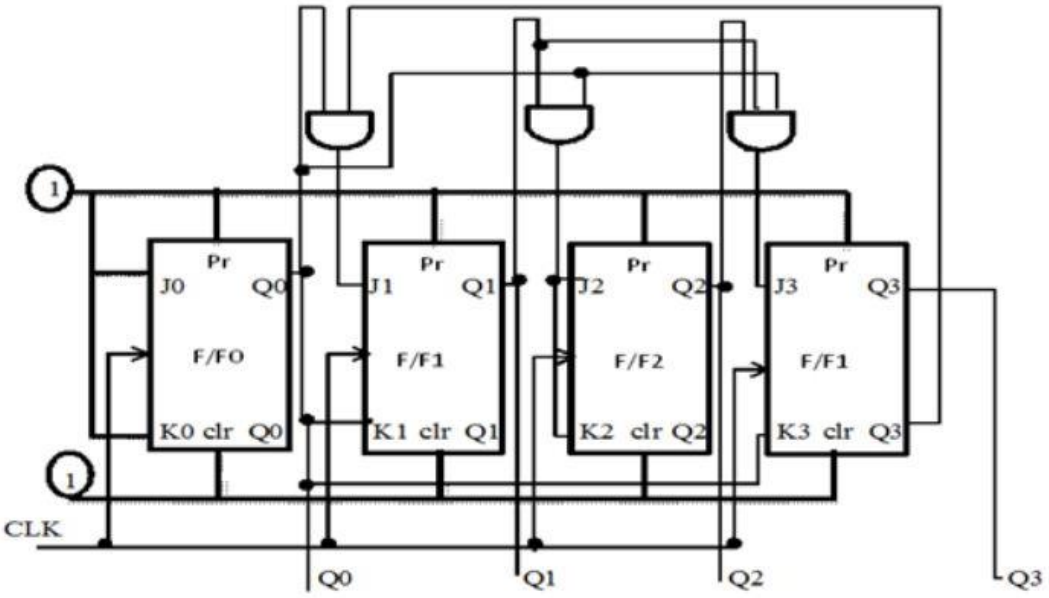
Input Equations:

J0 = 1 K0 = 1

J1 = Q3Q0 K1 = Q0

J2 = Q1Q0 K2 = Q1Q0

J3 = Q2Q1Q0 K3 = Q0

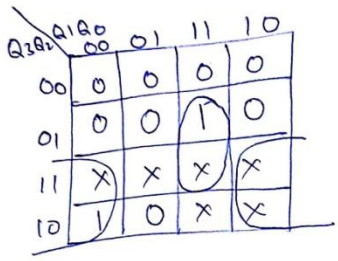


b) D- Flip-flops:

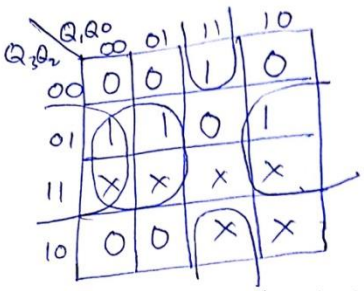
From the above state table in (a)

D3 = Q3+ , D2 = Q2+, D1 = Q1+, D0 = Q0+ (Next state Q3 Q2 Q1 Q0)

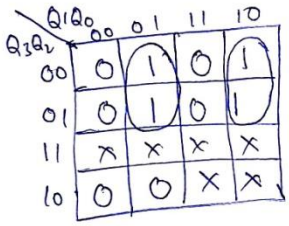
K-maps:-



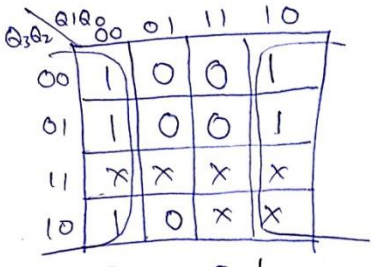
$D3 = Q_3Q_0' + Q_2Q_1Q_0$



$D2 = Q_2Q_1' + Q_2Q_0' + Q_2'Q_1Q_0$



$D1 = Q_3'Q_1'Q_0 + Q_3'Q_1Q_0'$

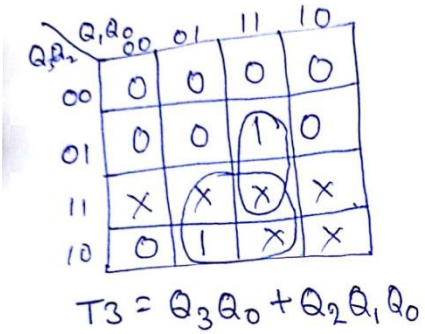


$D0 = Q_0'$

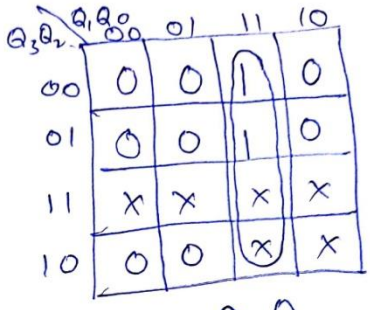
c) T- Flip-flops

Present state	Next state	Output	T- Flip flop inputs			
Q3 Q2 Q1 Q0	Q3 Q2 Q1 Q0	y	T3	T2	T1	T0
0000	0001	0	0	0	0	1
0001	0010	0	0	0	1	1
0010	0011	0	0	0	0	1
0011	0100	0	0	1	1	1
0100	0101	0	0	0	0	1
0101	0110	0	0	0	1	1
0110	0111	0	0	0	0	1
0111	1000	0	1	1	1	1
1000	1001	0	0	0	0	1
1001	0000	1	1	0	0	1

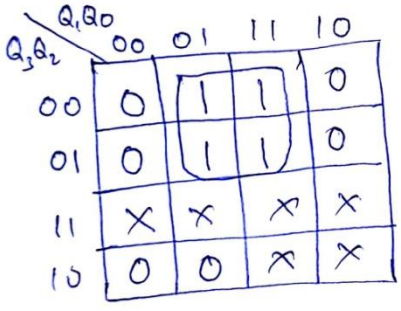
K-maps



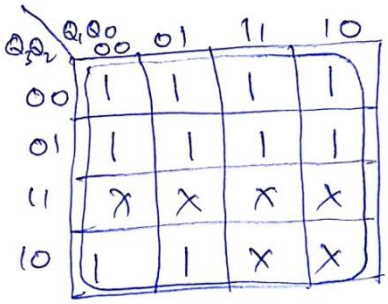
$T3 = Q_3Q_0 + Q_2Q_1Q_0$



$T2 = Q_1Q_0$



$T1 = Q_3'Q_0$



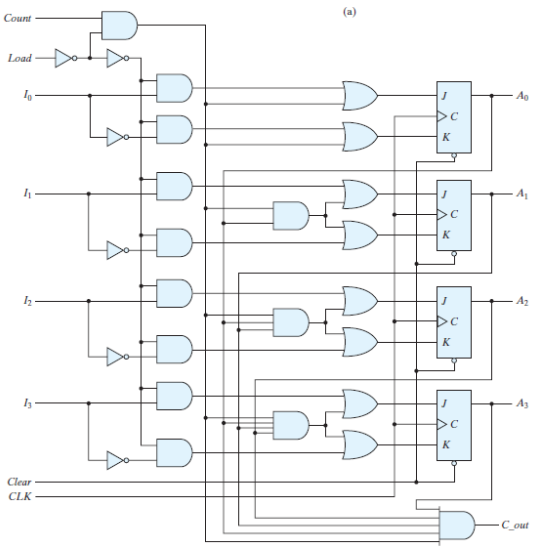
$T0 = 1$

Note: BCD counter using JK flip flop uses 3 AND gates while BCD counter using D-flipflops uses 7 AND gates and 3 OR gates and BCD counter using T- flipflops uses 4 AND gates and 1 OR gate hence BCD counter using JK flip flops is most efficient.

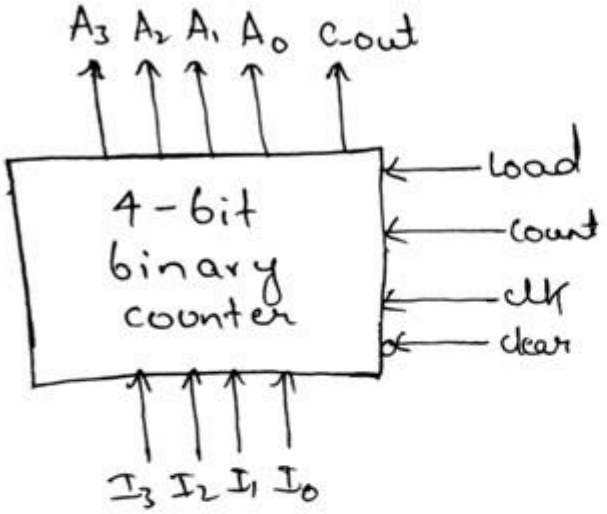
8)Enclose the given binarycounter with parallel load ina block diagram showingall inputs and outputs.

(a) Show the connectionsof four such blocks toproduce a 16-bit counterwith parallel load.

(b) Construct a binarycounter that counts from 0through binary 127.



Answer:

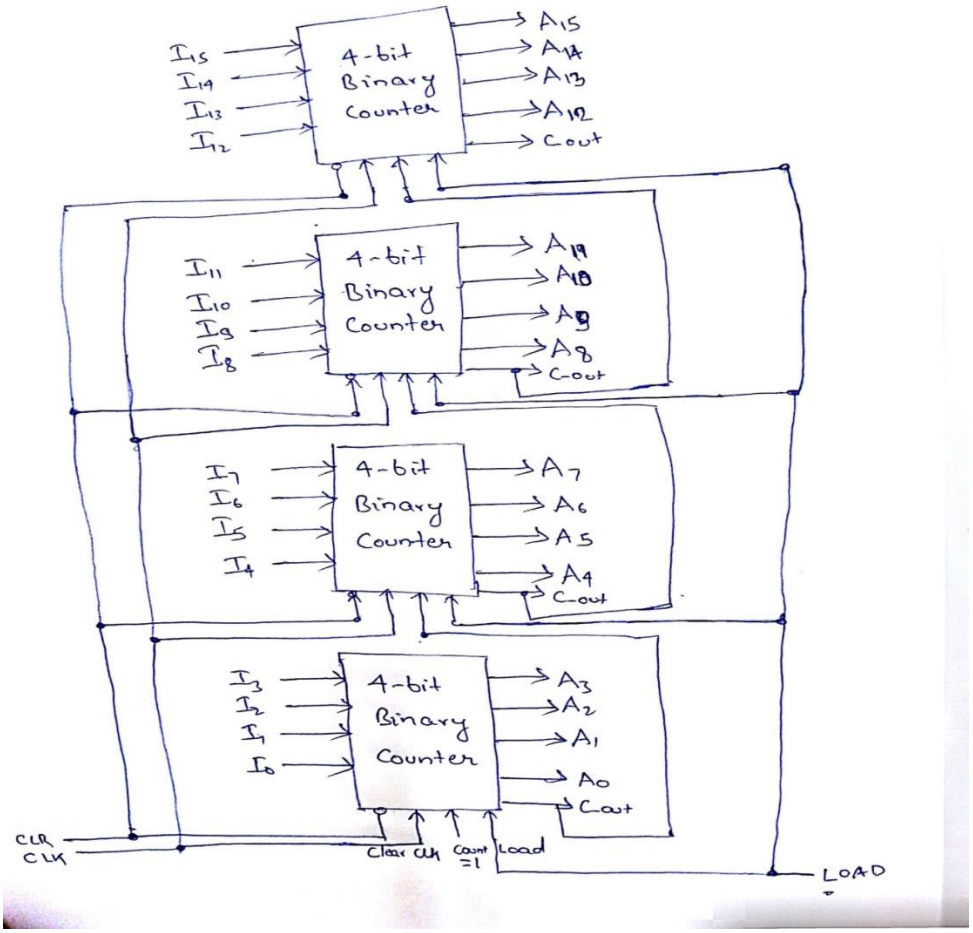


Load	Count	
1	X	Loads the parallel data
0	1	counts
0	0	No change

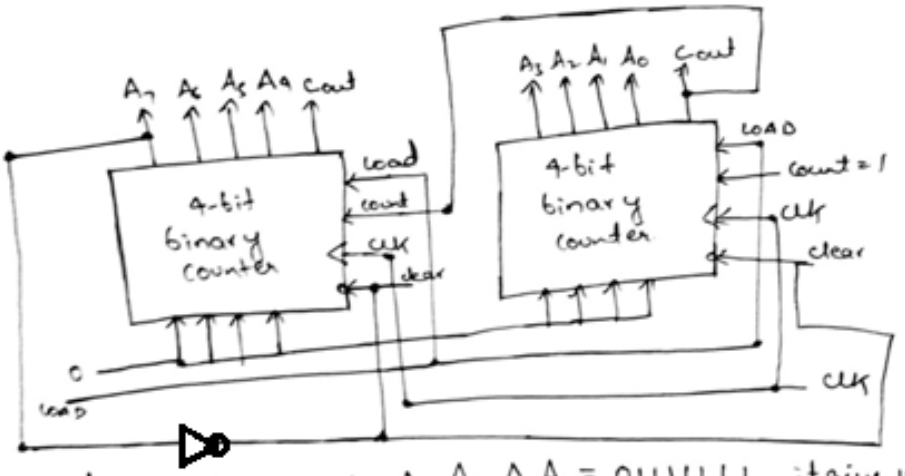
When $A_3A_2A_1A_0$ becomes 1111, C_out goes from 0 to 1.

∴ In 16-bit binary counter, we string all 4 load and clear together so that when load = 1, it will load 16 bit parallel data and when clear = 0, it will give all outputs $A_{15}A_{14}\ldots A_0$ to 00..00. C_out of predecessor counter is connected count of successive unit so that when predecessor reaches it's maximum, successive start counting.

a)



b)



when $A_7A_6A_5A_4A_3A_2A_1A_0 = 01111111$, it give 127, so as soon as A_7 goes from 0 to 1, it will enable clear and all output will go to 0.

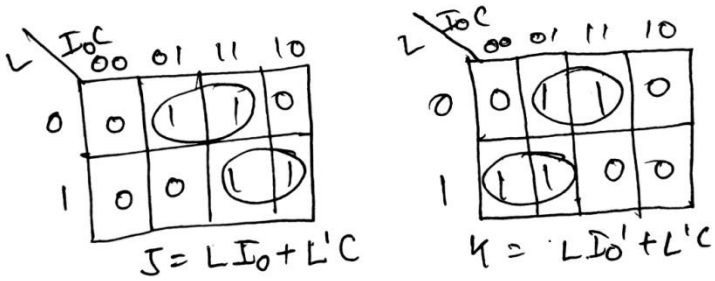
Binary counter that counts from 0 through 127

9) The binary counter with parallel load has two control inputs—Load (L) and Count (C)—and a data input, (I_i).
(a) Derive the flip-flop input equations for J and K of the first stage in terms of L, C, and I.

Answer:

When load L = 1 regardless of C, it will load data I ie when I=0, J=0 and K=1.
When load L=0 and C = 1, it will count i.e J=1 and K =1.
When load L = 0 and C=0, output will remain same so J=0 and K=0.
For the first stage:

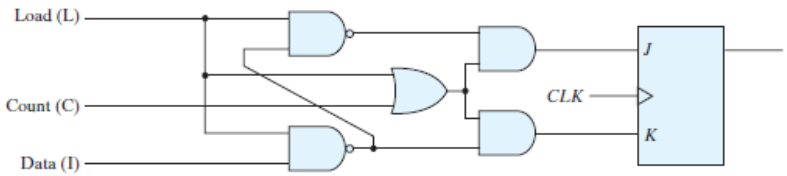
L	I_o	C	J	K
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	1	1
1	0	0	0	1
1	0	1	0	1
1	1	0	1	0
1	1	1	1	0



From the above truth table:

$$J_0 = LI_0 + L'C$$
$$K_0 = LI_0' + L'C$$

(b) The logic diagram of the first stage of an equivalent circuit is shown above. Verify if this circuit is equivalent to the one in (a).



Answer:

$$J = (L(LI)')'(L + C) = (L' + LI)(L + C) = LI + L'C + LIC = LI + L'C$$
$$K = (LI)'(L + C) = (L' + I')(L + C) = LI' + L'C$$

10) (i) For the binary counter with parallel load circuit, give three alternatives for a mod-12 counter (i.e., the count evolves through a sequence of 12 distinct states)

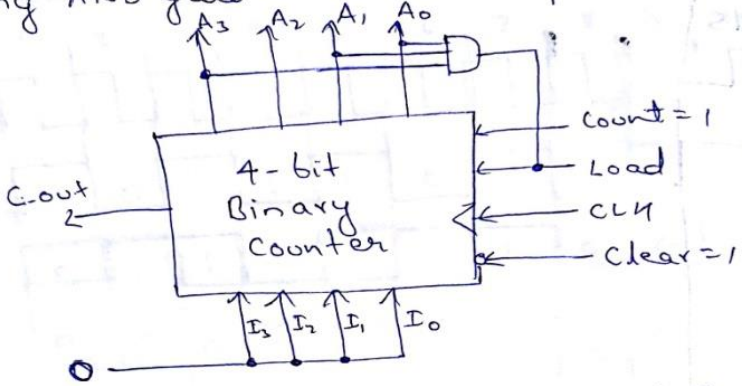
(a) Using an AND gate and the load input

(b) Using the output carry.

(c) Using a NAND gate and the asynchronous clear input.

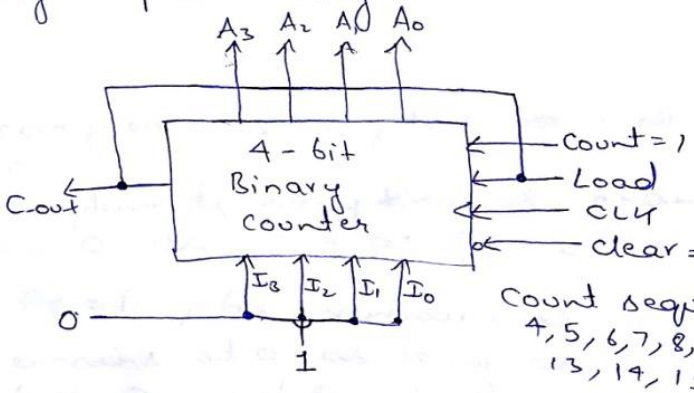
Answer:

a) Using AND gate and load input



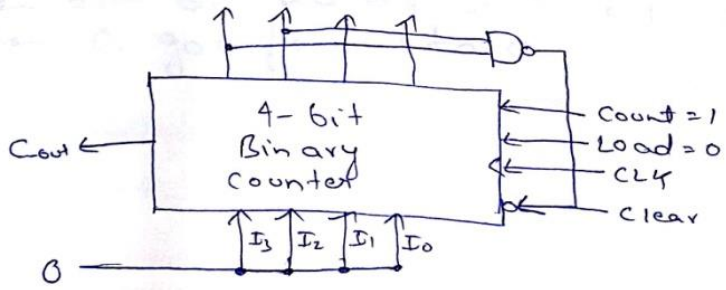
Count sequence: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11

b) Using output carry



Count sequence: 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15.

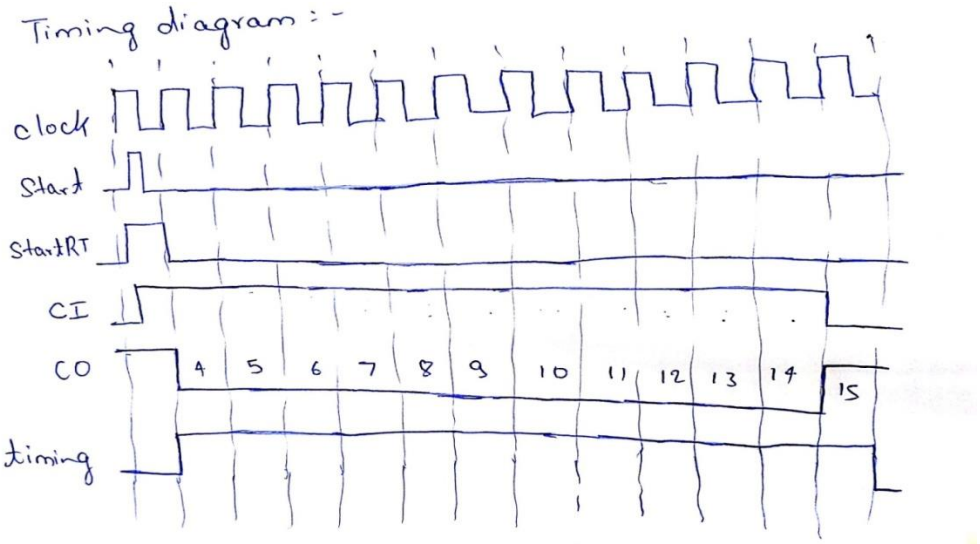
c)

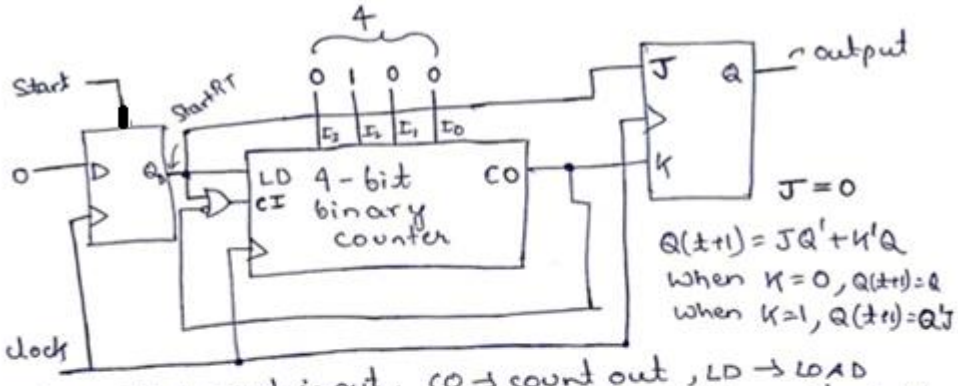


Count sequence: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11

(ii) Design a timing circuit that provides an output signal that stays on for exactly twelve clock cycles. A start signal sends the output to the 1 state, and after twelve clock cycles the signal returns to the 0 state.

Answer:





Here CI → count input, CO → count out, LD → LOAD

When we give start signal to D flip flop, it will set it to 1 and hence LD and CI will become 1. In next clock cycle as 0 is given input to D flip flop, Q_0 will become 0 making LD = 0, CO = 0 and CI = 1 which will start counter to count from 4 to 15. When counter reaches to 15, CO will become 1.

Since at starting CO = 1 when start signal is given and Q_0=1 i.e both J and K become 1 and it sends output from 0 to 1 state. In next clock cycles K = 0, making JK flip flop output to remain at 1 till it reaches 12 clock cycles after that CO=1 which will give Q = 0