EE2001-Tutorial 6
Date: 6th March 2018
More on Synchronous Sequential Logic including Register
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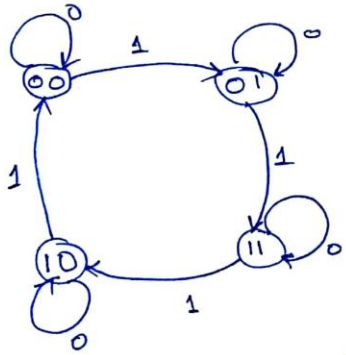
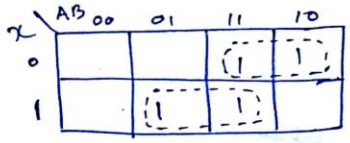
1) (i) Design a sequential circuit with two D flip-flops A and B, and one input x_{in}. When x_{in} = 0, the state of the circuit remains the same. When x_{in} = 1, the circuit goes through the state transitions from 00 to 01, to 11, to 10, back to 00, and repeats.

ANS 1(i) State Diagram.

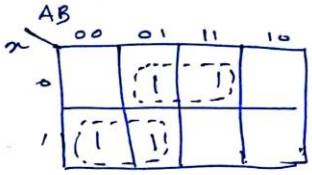


A(t+1)

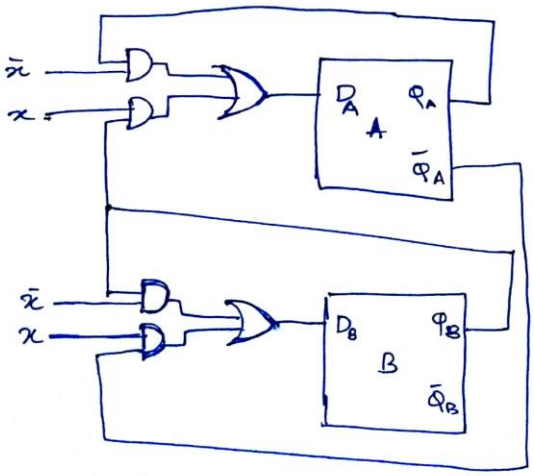


$A(t+1) = \bar{x}A + xB$

B(t+1)

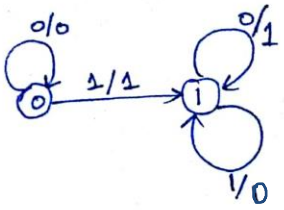


$B(t+1) = \bar{x}B + x\bar{A}$



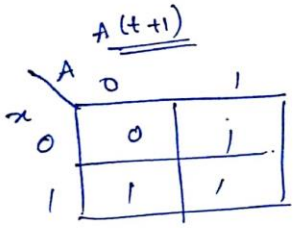
(ii) Design a one-input, one-output serial 2's complementer. The circuit accepts a string of bits from the input and generates the 2's complement at the output. The circuit can be reset asynchronously to start and end the operation.

(ii)



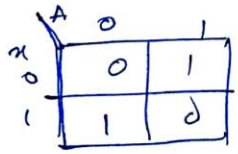
Rule used

→ Untill first '1', continue the bits; after that - reverse the bits



$A(t+1) = A + x$

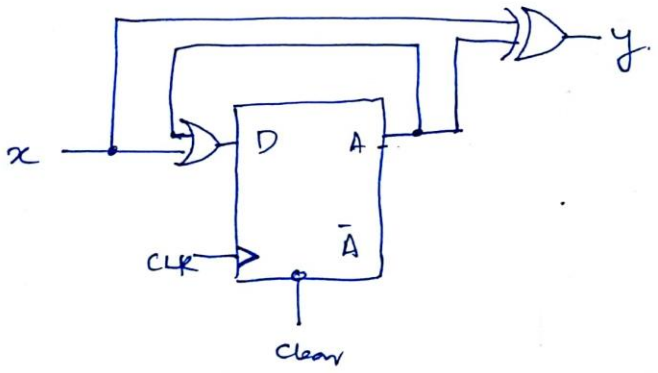
y



$y = A\bar{x} + \bar{A}x$

$= A \oplus x$

Circuit:



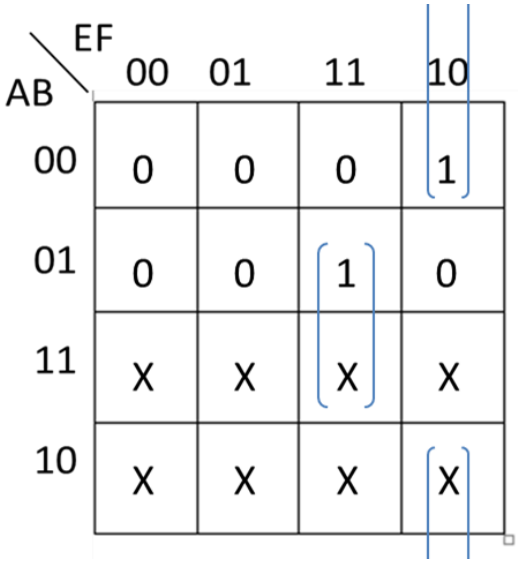
2) Design a sequential circuit with two JK flip-flops A and B and two inputs E and F. If E = 0, the circuit remains in the same state regardless of the value of F . When E = 1 and F = 1, the circuit goes through the state transitions from 00 to 01, to 10, to 11, back to 00, and repeats. When E = 1 and F = 0, the circuit goes through the state transitions from 00 to 11, to 10, to 01, back to 00, and repeats.

State Table:

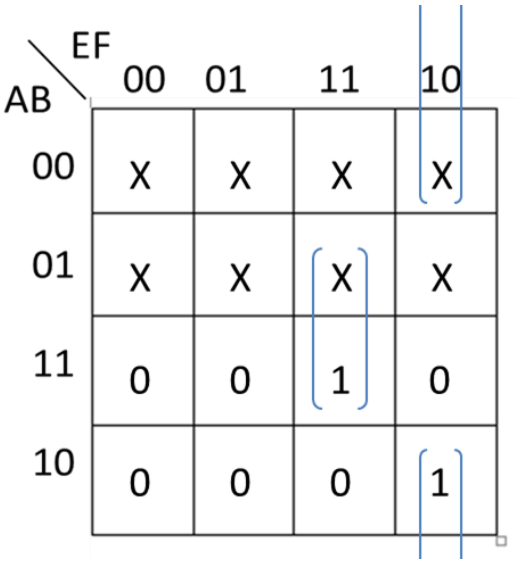
Present state		Inputs		Next state		Flip-flop inputs			
A	B	E	F	A	B	J_A	K_A	J_B	K_B
0	0	0	0	0	0	0	X	0	X
0	0	0	1	0	0	0	X	0	X
0	0	1	0	1	1	1	X	1	X
0	0	1	1	0	1	0	X	1	X
0	1	0	0	0	1	0	X	X	0
0	1	0	1	0	1	0	X	X	0
0	1	1	0	0	0	0	X	X	1
O	1	1	1	1	0	1	X	X	1
1	0	0	0	1	0	X	0	0	X
1	0	0	1	1	0	X	0	0	X
1	0	1	0	0	1	X	1	1	X
1	0	1	1	1	1	X	0	1	X
1	1	0	0	1	1	X	0	X	0
1	1	0	1	1	1	X	0	X	0
1	1	1	0	1	0	X	0	X	1
1	1	1	1	0	0	X	1	X	1

JK Flip-flop:

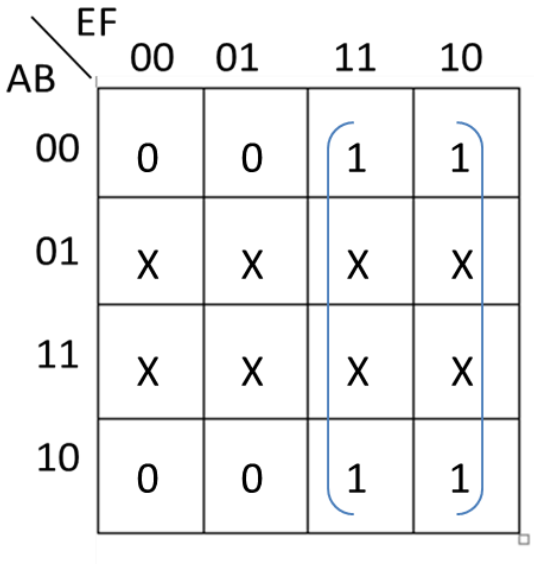
Q_n	J	K	Q_{n+1}
0	0	X	0
0	1	X	1
1	X	1	0
1	X	0	1



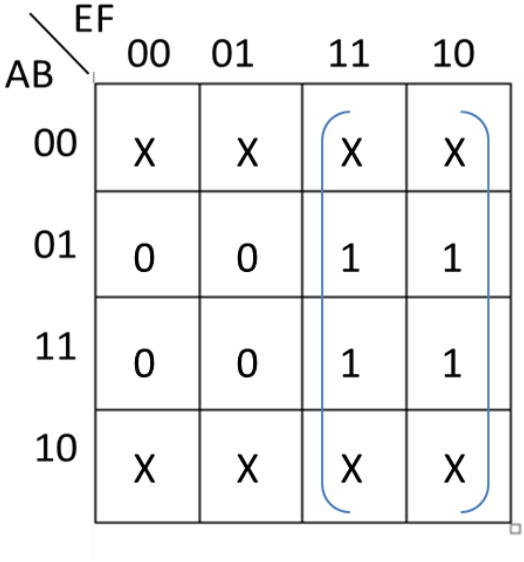
$J_A = E\,(BF+B'F')$



$k_A = E\,(BF+B'F')$

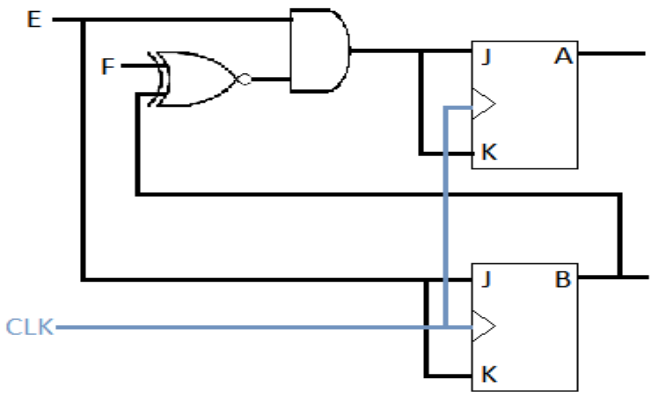


$J_B = E$

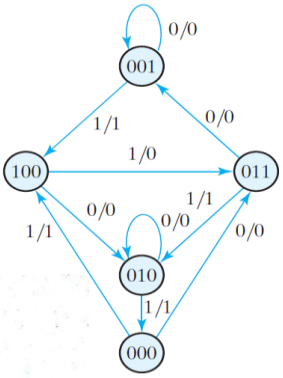


$k_B = E$

Circuit Diagram:



3) A sequential circuit has three flip-flops A, B, C ; one input x_{in}; and one output y_{out}. The state diagram is shown. The circuit is to be designed by treating the unused states as don't-care conditions. Analyze the circuit obtained from the design to determine the effect of the unused states. (a) Use D flip-flops in the design. (b) Use JK flipflops in the design.



3.

	Present state			Input	Next state			Output
	A	B	C	x	A	B	C	y
0	0	0	0	0	0	1	1	0
1	0	0	0	1	1	0	0	1
2	0	0	1	0	0	0	1	0
3	0	0	1	1	1	0	0	1
4	0	1	0	0	0	1	0	0
5	0	1	0	1	0	0	0	1
6	0	1	1	0	0	0	1	0
7	0	1	1	1	0	1	0	1
8	1	0	0	0	0	1	0	0
9	1	0	0	1	0	1	1	0

Unused ⇒ Don't Care

$$d(A,B,C,x) = \sum(10,11,12,13,14,15)$$

(i) Using D-Flip flops:

$$D_A = \bar{A}\bar{B}x$$

$$D_B = A + \bar{C}\bar{x} + BCx$$

$$D_C = Ax + C\bar{x} + \bar{A}\bar{B}\bar{x}$$

$$y = \bar{A}x$$

Unused State table.

Present State			Input	Next State			Output
A	B	C	x	A	B	C	y
1	0	1	0	0	1	1	0
1	0	1	1	0	1	1	0
1	1	0	0	0	1	0	0
1	1	0	1	0	1	1	0
1	1	1	0	0	1	1	0
1	1	1	1	0	1	1	0

All unused states transit to Used states (011, 010).

So circuit is self correcting.

(ii) With J-K flip flops

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

$J_A = \bar{B}x$

$J_B = A + \bar{C}x$

$J_C = Ax + B\bar{A}\bar{B}x$

$K_A = 1$

$K_B = \bar{C}x + C\bar{x}$

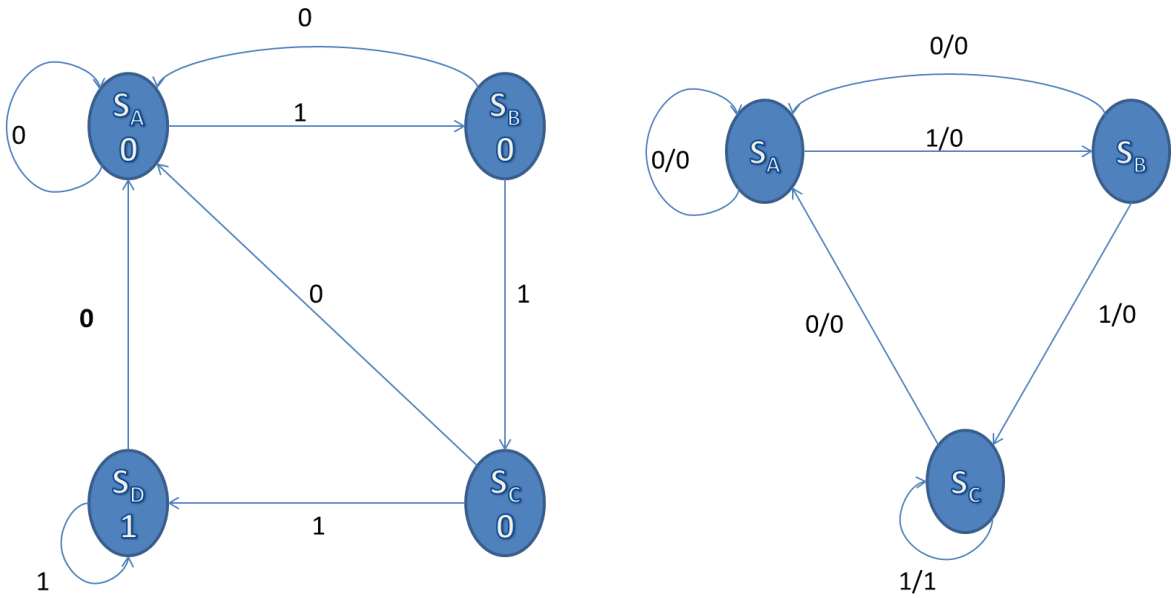
$K_C = x.$

$y = \bar{A}x.$

Here $K_A = 1$; which sets $Q_A = 0$

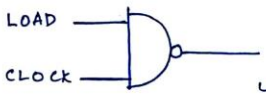
The circuit is self correcting.

4) Develop the state diagram for a state machine that detects a sequence of three or more consecutive 1's in a string of bits coming through an input line.



5) Include a 2-input NAND gate in the given register shown and connect the gate output to the C inputs of all the flip-flops. One input of the NAND gate receives the clock pulses from the clock generator, and the other input of the NAND gate provides a parallel load control. Explain the operation of the modified register. Explain why this circuit might have operational problems.

5.



↳ To C inputs of flip-flops.

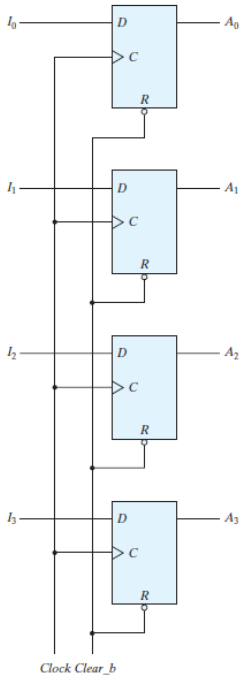
When LOAD = 0 ;
output is HIGH ; irrespective of CLOCK signal.

When LOAD = 1
output is $\overline{\text{CLOCK}}$

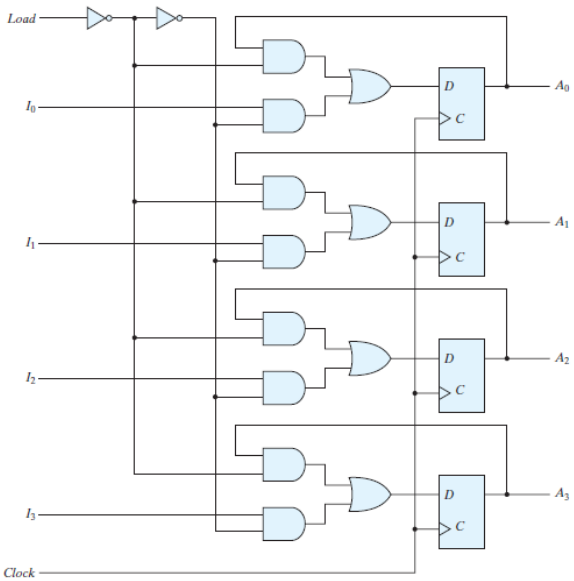
[Since the flip flops are Edge triggered, the HIGH logic at C doesn't matter.]

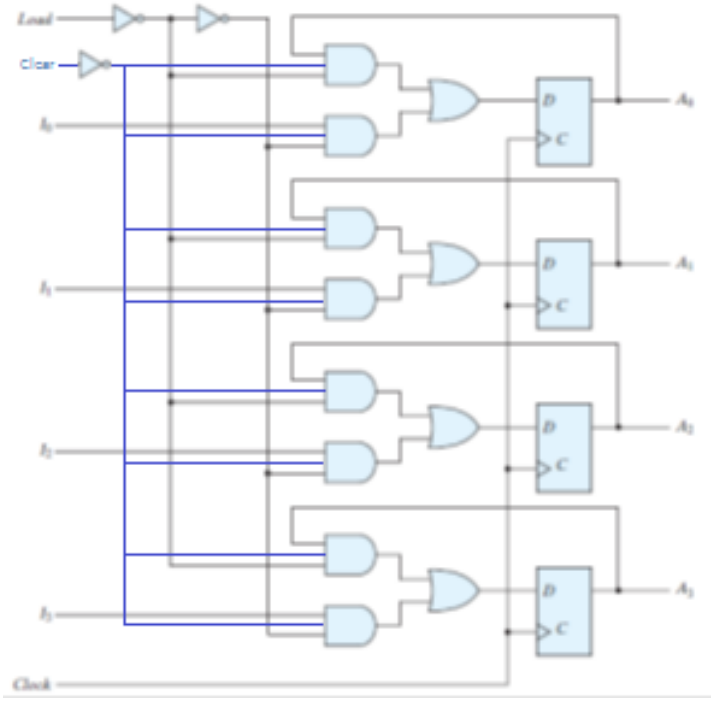
Possible Operational Problems :

(1). The additional delay introduced by the Gated clock affects the synchronicity of this register with other elements which are working in tandem.



6) Include a synchronous clear input to the given register. The modified register will have a parallel load capability and a synchronous clear capability. The register is cleared synchronously when the clock goes through a positive transition and the clear input is equal to 1.





7) (i) What is the difference between serial and parallel transfer? Explain how to convert serial data to parallel and parallel data to serial. What type of register is needed?
(ii) The contents of a four-bit register is initially 0110. The register is shifted six times to the right with the serial input being 1011100. What is the content of the register after each shift?

7 (i) **Serial transfer :**

→ Transfers 1 bit data with the clock

→ To transfer N bits ; $\lceil N \times$ Clock Period $\rceil$ time is taken.

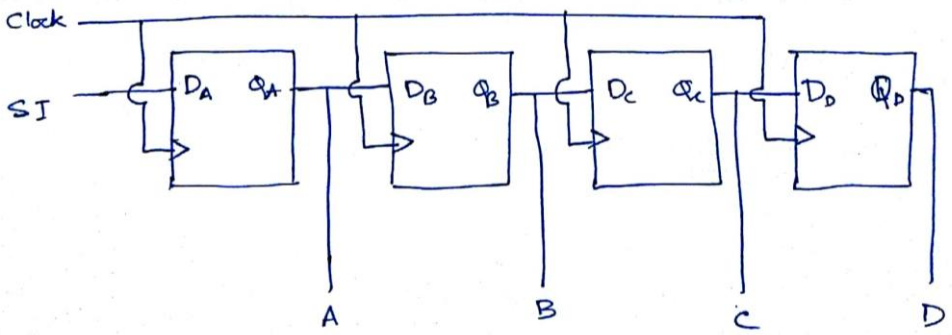
Parallel transfer.

→ Transfers multiple bits with clock

→ To transfer N bits ; $\left\lceil \frac{N \times \text{Clock Period}}{K} \right\rceil$ time is taken ; { K ⇒ No. of parallel lines }

SERIAL - IN PARALLEL OUT

4 - bit Example.

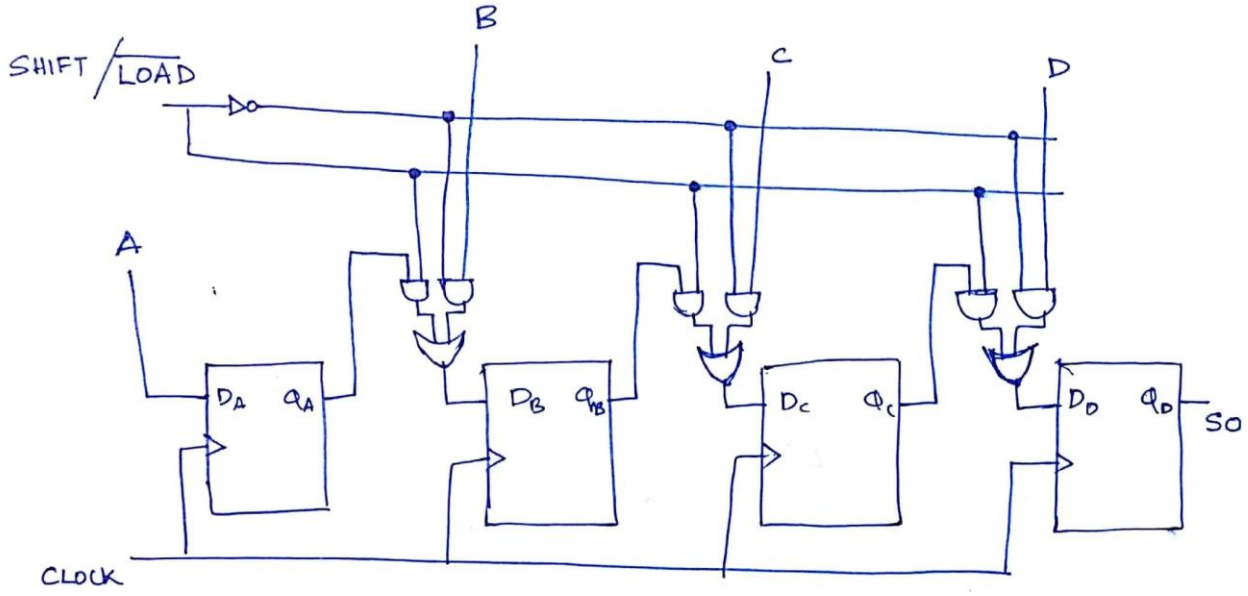


PARALLEL IN SERIAL OUT

(4-bit example)

Set $\overline{LOAD} = 0$ to load the parallel data

Set SHIFT/$\overline{LOAD}$ = 1 to transfer data serially.

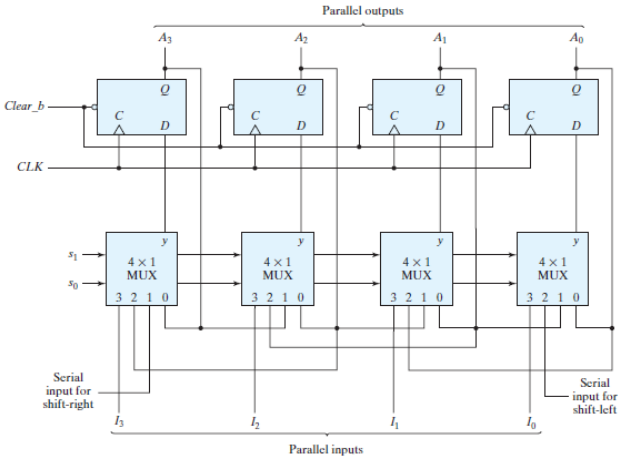


D-flips flops are used to make these registers

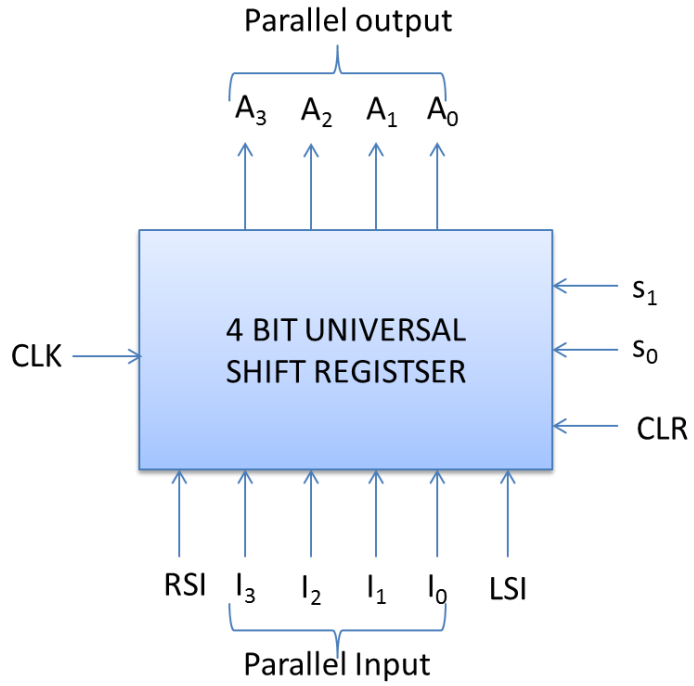
(ii)

	A	B	C	D
Initial stage :	0	1	1	0
1st pulse :	1	0	1	1
2nd pulse :	0	1	0	1
3rd pulse :	1	0	1	0
4th pulse :	1	1	0	1
5th pulse :	1	1	1	0
6th pulse :	0	1	1	1

8) The given four-bit universal shift register is enclosed within one IC component package.
(a) Draw a block diagram of the IC showing all inputs and outputs. Include two pins for the power supply.
(b) Draw a block diagram using two of these ICs to produce an eight-bit universal shift register.

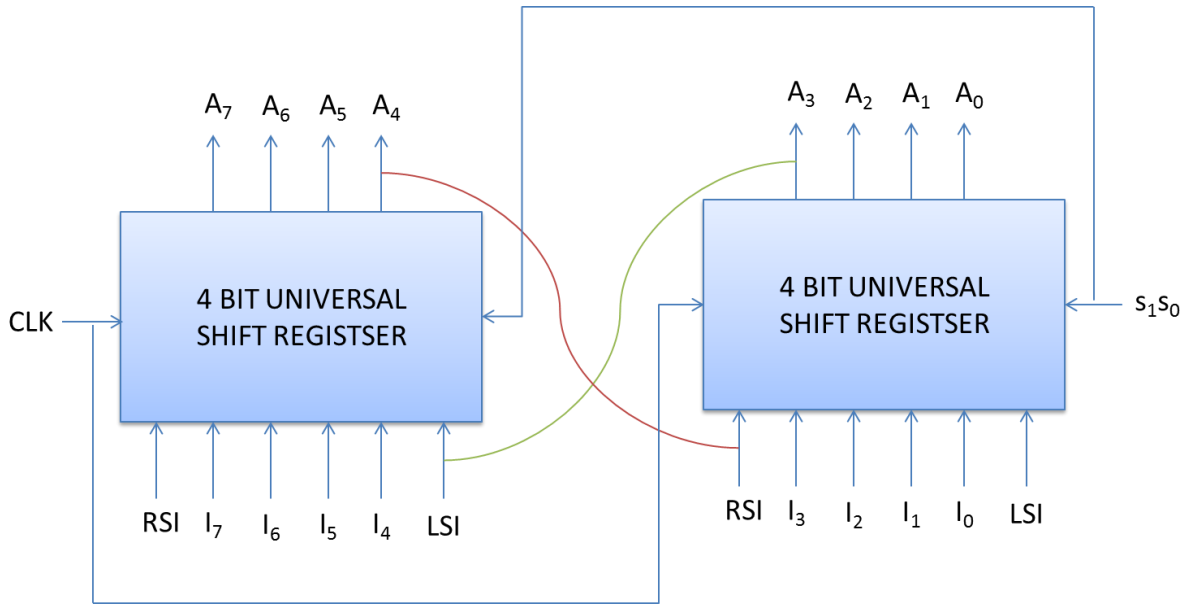


Block diagram:

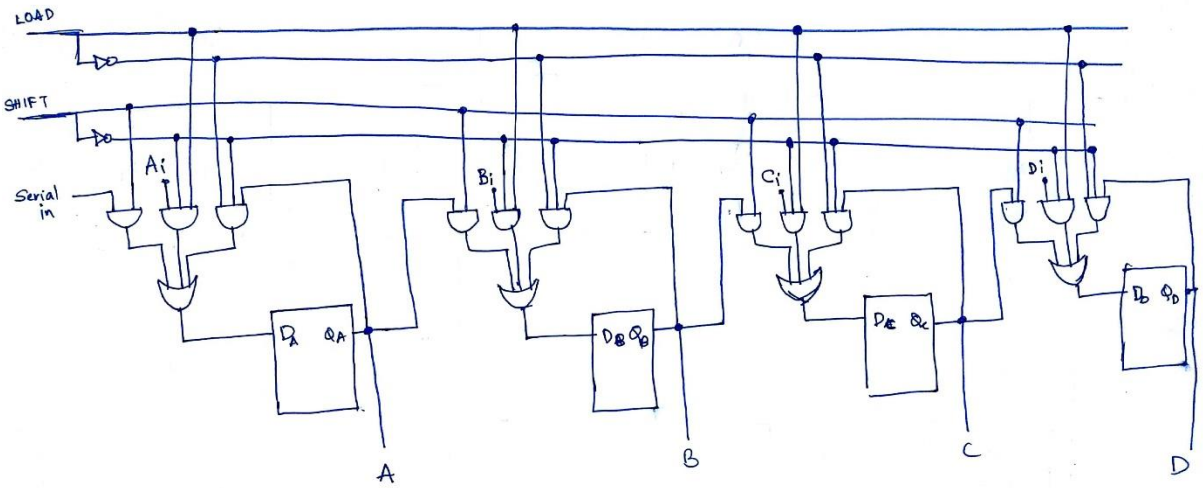


S1	S0	Register operation
0	0	No change
0	1	Shift right with RSI
1	0	Shift left with LSI
1	1	Parallel load

8-bit universal shift register using two 4-bit shift registers:



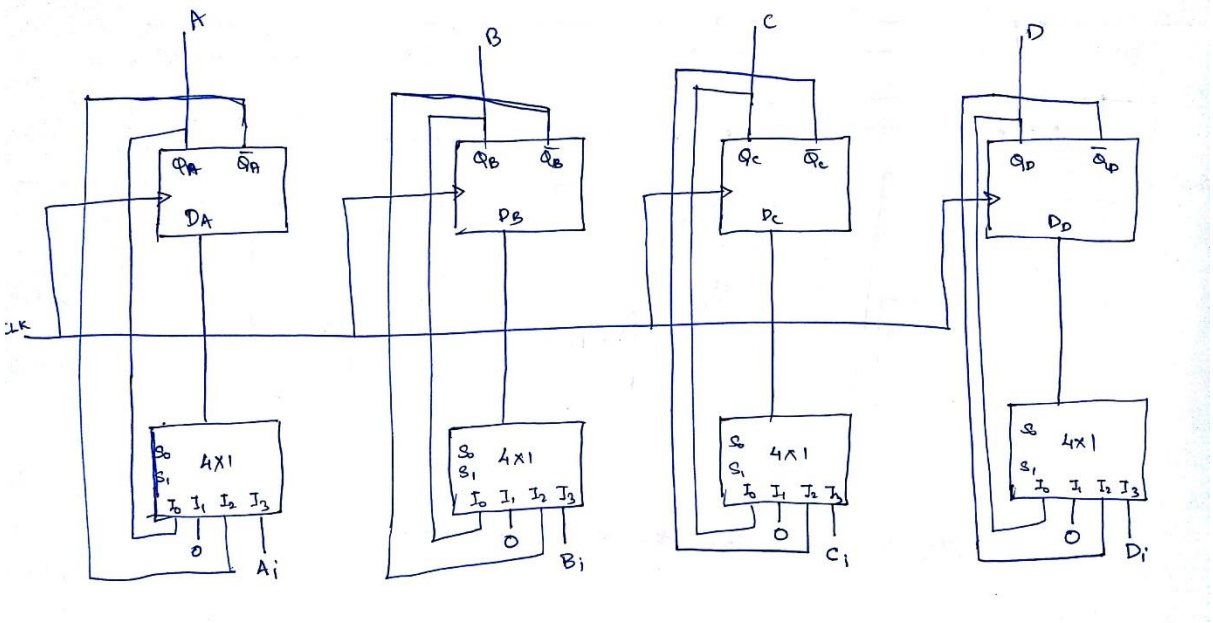
9) (i) Design a four-bit shift register with parallel load using D flip-flops. There are two control inputs: shift and load. When shift = 1, the content of the register is shifted by one position. New data are transferred into the register when load = 1 and shift = 0. If both control inputs are equal to 0,the content of the register does not change.



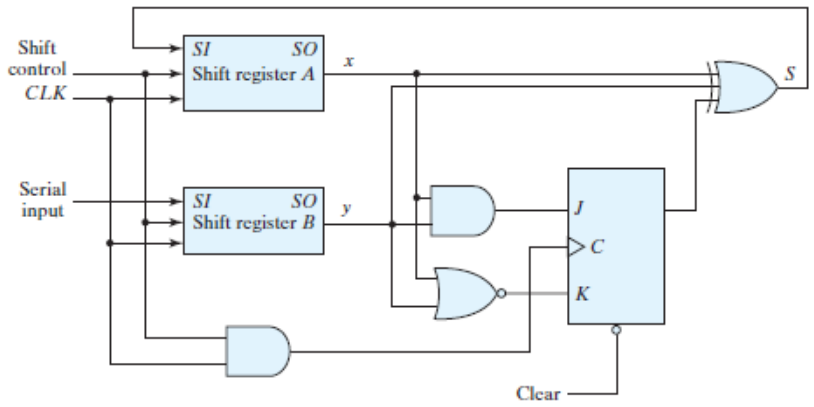
(when SHIFT =1, irrespective of LOAD bit, System will operate in Serial shift mode)

(ii) Draw the logic diagram of a four-bit register with four D flip-flops and four 4 × 1 multiplexers with mode selection inputs s1 and s0. The register operates according to the following function table.

s_1	s_0	Register Operation
0	0	No change
1	0	Complement the four outputs
0	1	Clear register to 0 (synchronous with the clock)
1	1	Load parallel data



10) The given serial adder uses two four-bit registers. Register A holds the binary number 0101 and register B holds 0111. The carry flip-flop is initially reset to 0. List the binary values in register A and the carry flip-flop after each shift.



Shift Register A				Shift Register B				JK flip-flop				
A3	A2	A1	A0	B3	B2	B1	B0	Q_n	J	K	Q_{n+1}	S
0	1	0	1	0	1	1	1	0	1	0	1	0
0	0	1	0	-	0	1	1	1	0	0	1	0
0	0	0	1	-	-	0	1	1	1	0	1	1
1	0	0	0	-	-	-	0	1	0	1	0	1
1	1	0	0									

Verification:

A + B = 0101 + 0111 = 1100(A value) with 0 carry (flip-flop output)