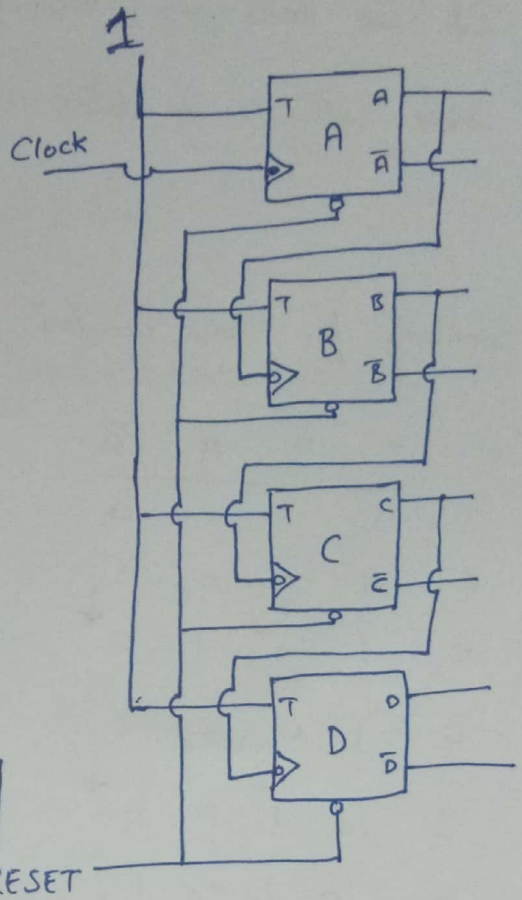
Date: 4/3/19

EE2001 : Digital Systems

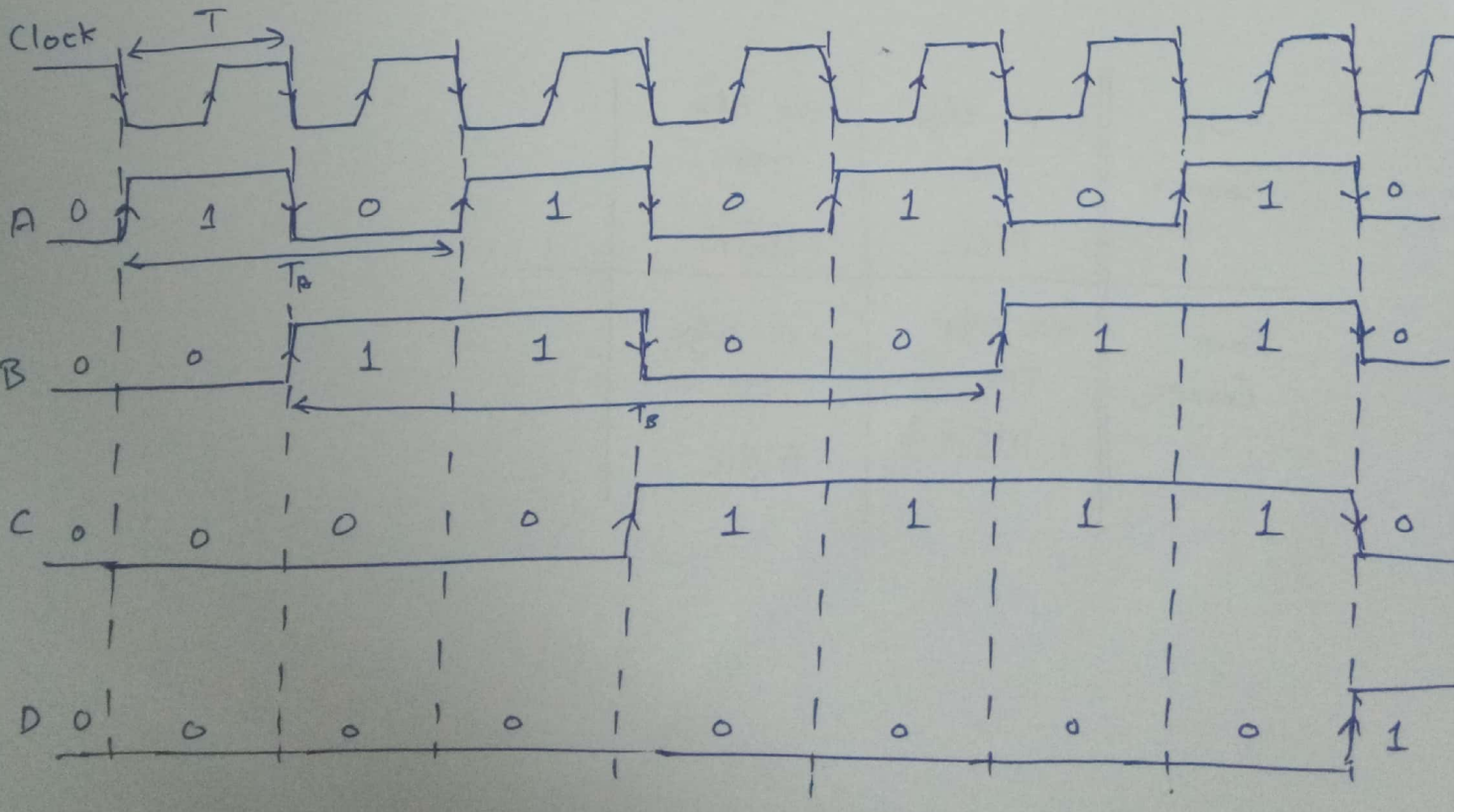
Ripple Counter (Asynchronous Counters)

C	B	A	C^+	B^+	A^+
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0



[B changes only when A goes from 1→0
C " " " B " " 1→0]

trailing edge



→ $T_A = 2T$, $T_B = 4T$, $T_C = 8T$, $T_D = 16T$

→ If we take into account the delay from clock → output, there will be a delay b/w transition of A & transition of B, " " " " " B & " " C...

→ Similarly for down counter

	C	B	A	$\bar{A}$
7	1	1	1	0
6	1	1	0	1
5	1	0	1	0
4	1	0	0	1
3	0	1	1	0
2	0	1	0	1
1	0	0	1	0
0	0	0	0	1

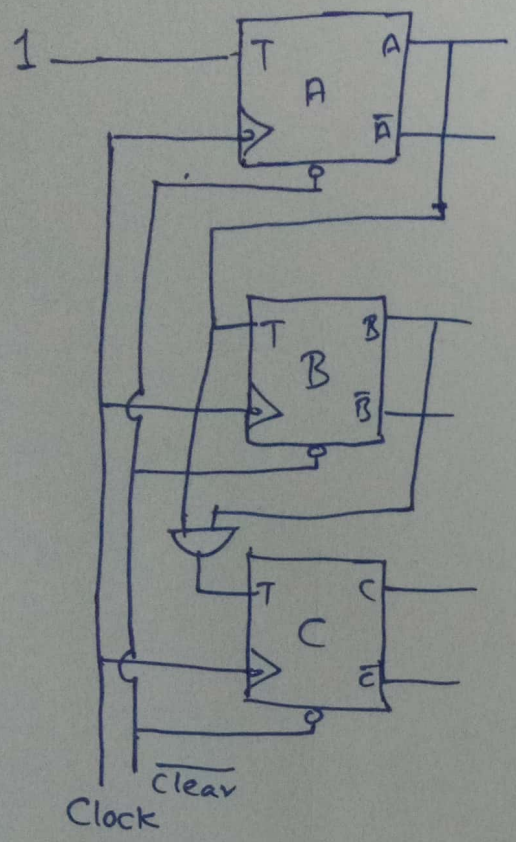
→ Use +ve edge TFF and tap A

(or)

Use -ve edge TFF and tap $\bar{A}$

→

Up Counter	-ve edge TFF A|B|C	+ve edge TFF $\bar{A}\|\bar{B}\|\bar{C}$
Down Counter	+ve edge TFF A|B|C	-ve edge TFF $\bar{A}\|\bar{B}\|\bar{C}$



$T_B = A$

$T_C = A \cdot B$

$T_D = A \cdot B \cdot C$

Synchronous Up Counter