EE2001: Tutorial 4 Solutions

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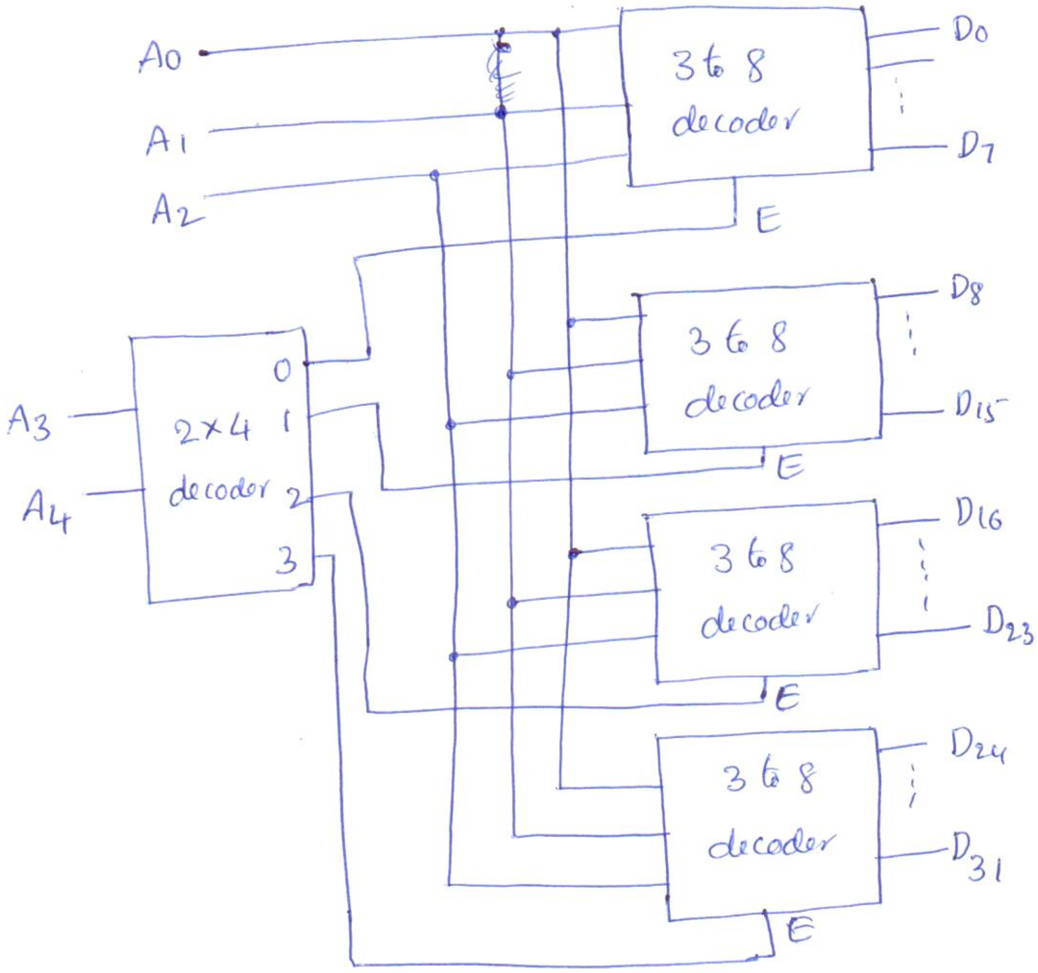
1 (i) Construct a 5-to-32 line decoder with four 3-to-8 line decoders with enable and a 2-to-4 line decoder. Use block diagrams for the Components.

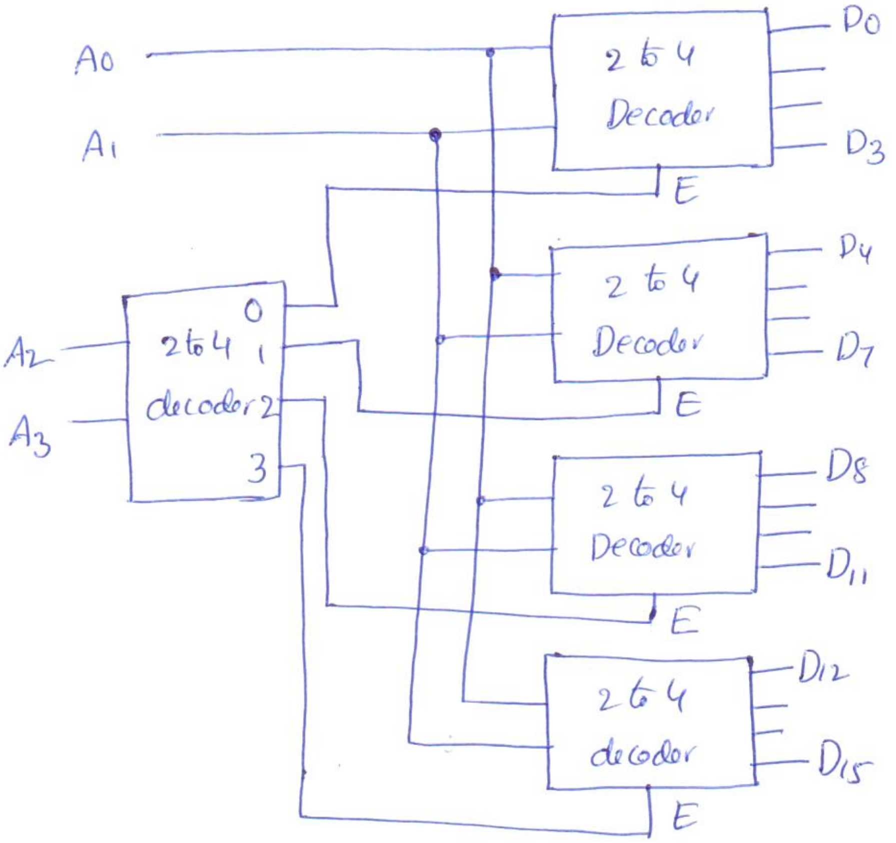
ii) Construct a 4-to-16 line decoder with five 2-to-4 line decoders with enable.

Sol:

i)



ii)



2) A Combinational circuit is specified by the following three Boolean functions:

$F_1(A,B,C) = \Sigma(1,4,6)$

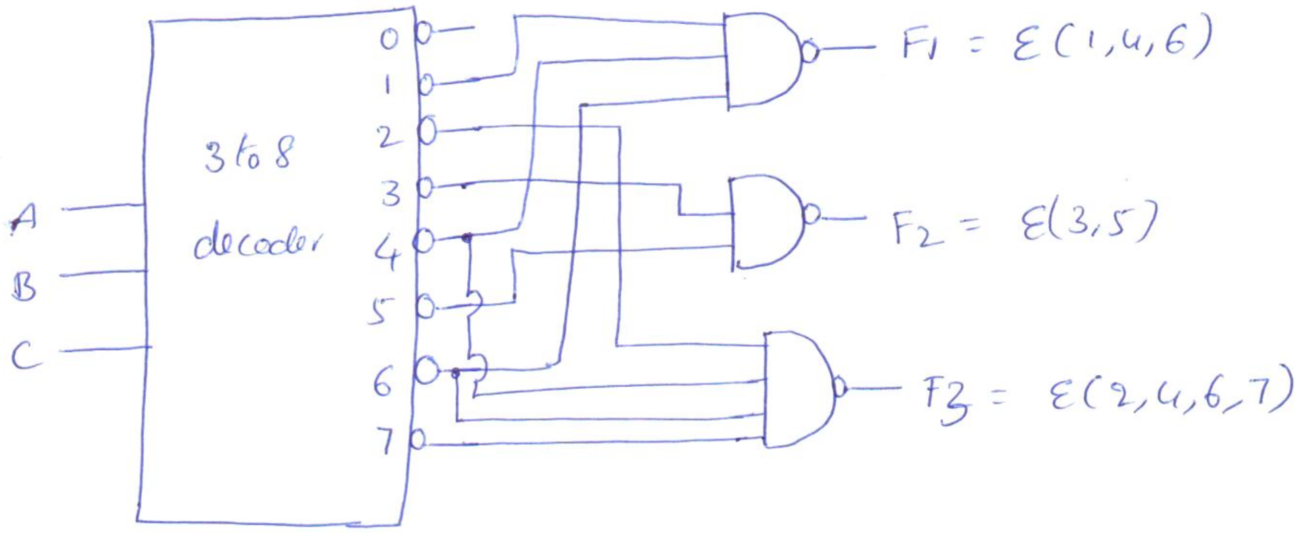
$F_2(A,B,C) = \Sigma(3,5)$

$F_3(A,B,C) = \Sigma(2,4,6,7)$

Implement the circuit with a decoder constructed with NAND gates and NAND or ~~N~~AND gates connected to the decoder outputs. Use a block diagram for the decoder. Minimize the number of inputs in the external gates.

Sol: 3 inputs $\Rightarrow 2^3 = 8$ outputs

- So, we require 3-to-8 decoder.
- Decoder with NAND gates results in active low output.



3) Using a decoder and external gates, design the combinational circuit defined by the following three Boolean functions:

a) $F_1 = x'yz' + xz$

$F_2 = xy'z' + x'y$

$F_3 = x'y'z' + xy$

b) $F_1 = (y' + x)x$

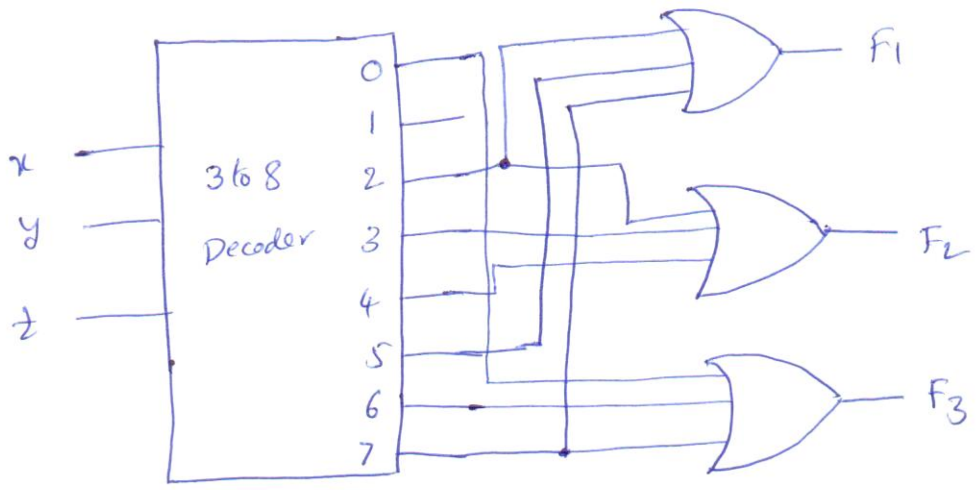
$F_2 = y'z' + x'y + yz'$

$F_3 = (x+y)z$

a) $F_1 = x'yz' + xz = x'yz' + xyz + xy'z = \Sigma(2,5,7)$

$F_2 = xy'z' + x'y = xy'z' + x'yz + x'yz' = \Sigma(2,3,4)$

$F_3 = x'y'z' + xy = x'y'z' + xyz + xyz' = \Sigma(0,6,7)$



b) $F_1 = (y'+x)z = y'z + xz = xy'z + x'y'z + xyz + xy'z$

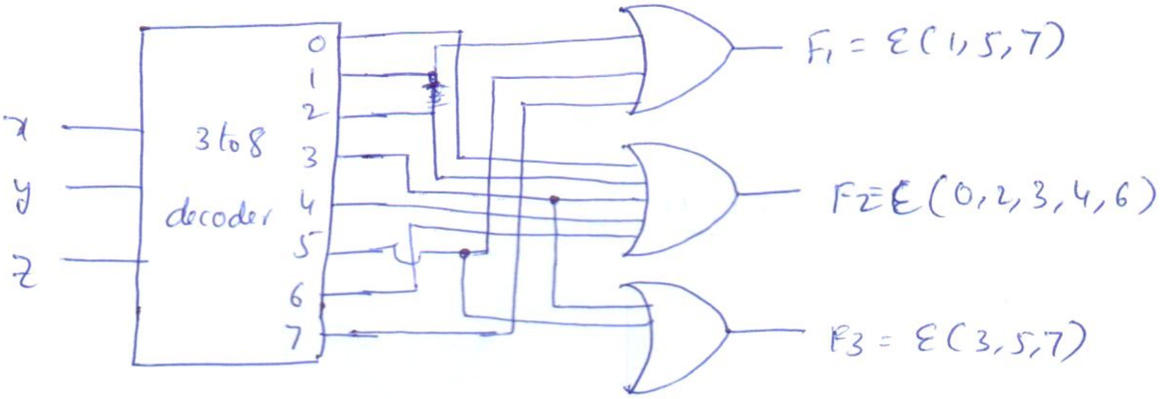
$= \Sigma(1,5,7)$

$F_2 = y'z' + x'y + yz' = xy'z' + x'y'z' + x'yz + x'yz' + xyz' + x'yz'$

$= \Sigma(0,2,3,4,6)$

$F3 = (x+y)z = xz + yz = xyz + xy'z + xyz + x'yz$

$= \Sigma(3,5,7)$



4) i) Design a four input priority encoder with input D_0 having the highest priority and input D_3 the lowest priority.

ii) Specify the truth table of an octal-to-binary priority encoder. Provide an output V to indicate that atleast one of the inputs is present. The input with the highest subscript number has the highest priority. What will be the value of the four outputs if inputs D_2 and D_6 are 1 at the same time?

Sol: Truth table for 4 input ~~pripd~~ priority encoder, $D_0 > D_1 > D_2 > D_3$

Inputs				Outputs		
D_3	D_2	D_1	D_0	X	Y	V
0	0	0	0	X	X	0
X	X	X	1	0	0	1
X	X	1	0	0	1	1
X	1	0	0	1	0	1
1	0	0	0	1	1	1

K- map for X

$D_3D_2 \backslash D_1D_0$	00	01	11	10
00	X			
01	1			
11	1			
10	1			

$x = D_1' D_0'$

K- map for Y

$D_3D_2 \backslash D_1D_0$	00	01	11	10
00	X			1
01				1
11				1
10	1			1

$Y = D_2' D_0' + D_1 D_0'$

$V = D_0 + D_1 + D_2 + D_3$

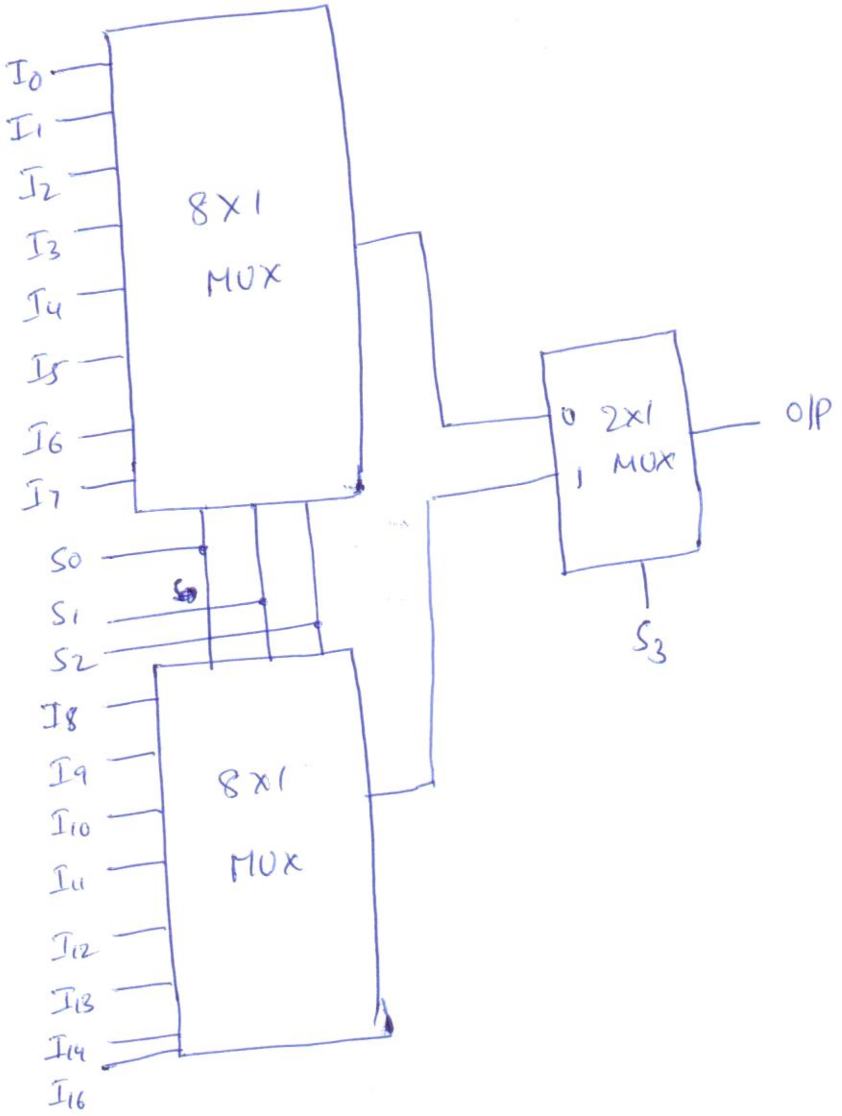
iv) octal - to - binary priority encoder: $D_7 > D_6 > D_5 > D_4 > D_3 > D_2 > 1$

Inputs								Outputs			
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	x	y	z	V
0	0	0	0	0	0	0	0	X	X	X	0
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	1	X	0	0	1	1
0	0	0	0	0	1	X	X	0	1	0	1
0	0	0	0	1	X	X	X	0	1	1	1
0	0	0	1	X	X	X	X	1	0	0	1
0	0	1	X	X	X	X	X	1	0	1	1
0	1	X	X	X	X	X	X	1	1	0	1
1	X	X	X	X	X	X	X	1	1	1	1

Since D_6 has highest priority than D_2, the output will be $XYZV = 1101$

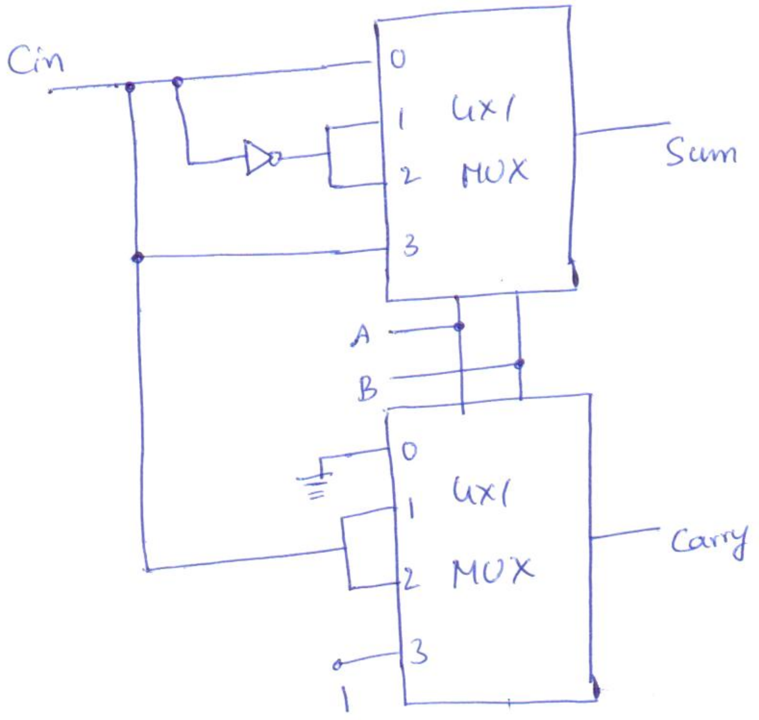
5 i) Construct a 16×1 multiplexer with two 8×1 and one 2×1 multiplexers. Use block diagrams.

ii) Implement a full adder with two 4×1 multiplexers.



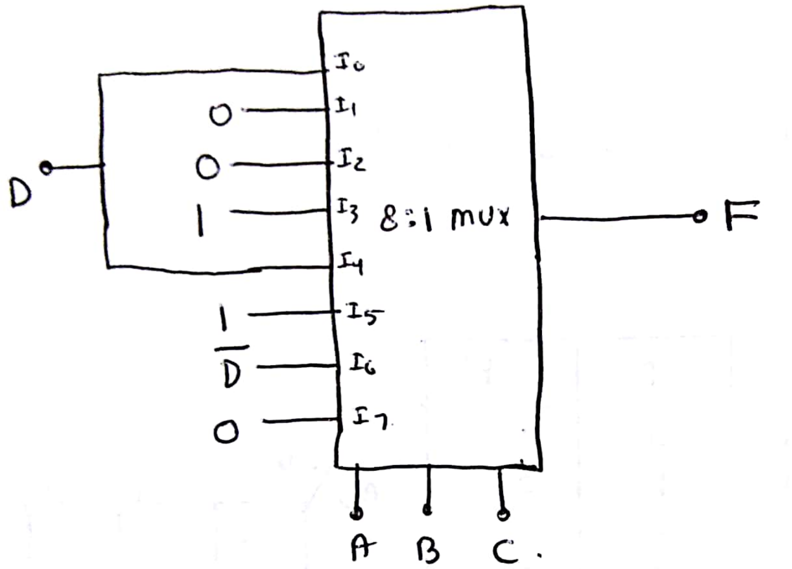
ii) Truth table for fulladder

A	B	Cin	Sum	Cout
0	0	0	0	0 } → 0
0	0	1	← Cin 1	0
0	1	0	1	0 } → Cin
0	1	1	← $\overline{Cin}$ 0	1
1	0	0	1	0 } → Cin
1	0	1	← $\overline{Cin}$ 0	1
1	1	0	0	1 } → 1
1	1	1	← Cin 1	1

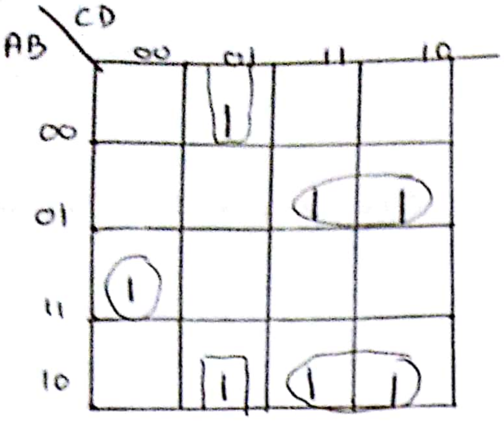


PROBLEM : 6

(a) According to the question, the circuit is as follows :



A	B	C	D	F.
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

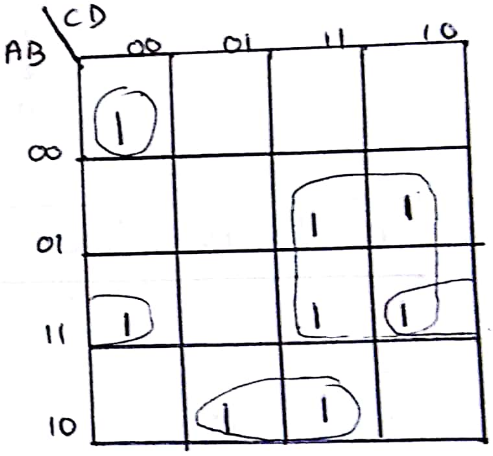


AB \ CD	00	01	11	10
00		1		
01			1	1
11	1			
10		1	1	1

$F = \bar{A}BC + A\bar{B}C + AB\bar{C}\bar{D} + \bar{B}\bar{C}D$

(b) Similarly,

A	B	C	D	F
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1



AB \ CD	00	01	11	10
00	1			
01			1	1
11	1		1	1
10		1	1	

$$\boxed{F = BC + A\bar{B}D + \bar{A}\bar{B}\bar{C}\bar{D} + AB\bar{D}}$$

PROBLEM : 7

(a) $F_1(A,B,C,D) = \Sigma(1,3,4,11,12,13,14,15)$

AB \ CD	00	01	11	10
00		1	1	
01	1			
11	1	1	1	1
10			1	

⇒ * AB = 00

F=1 for CD = 01 and 11

ie. $\boxed{F = D}$ will do.

* AB = 01.

F=1 for CD = 00

$\boxed{F = \bar{C}\bar{D} \equiv \overline{(C+D)}}$

* AB = 11

F = 1 for all CD = x x.

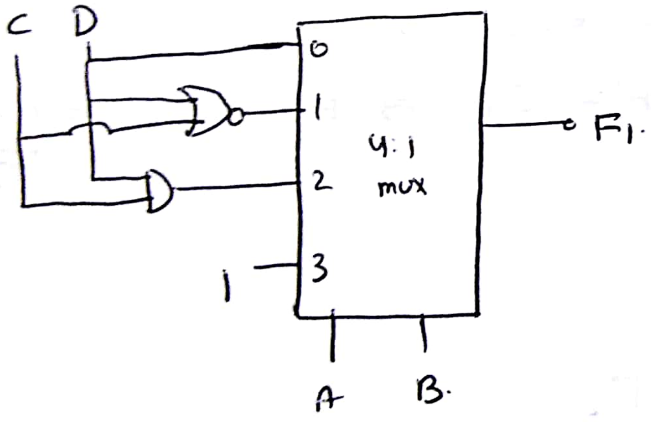
$\boxed{F=1}$

* AB = 10.

F =1 for CD = 11

⇒ $\boxed{F = CD.}$

ans:



b) $F_2(A,B,C,D) = \Sigma(1,2,5,7,8,10,11,13,15)$

AB \ CD	00	01	11	10
00		1		1
01		1	1	
11		1	1	
10	1		1	1

* AB = 00

F = 1 when CD = 01, 10

$\Rightarrow F = C \oplus D$ will do

* AB = 01

F = 1 when CD = 01, 11

$\Rightarrow F = D$ will do.

* AB = 11

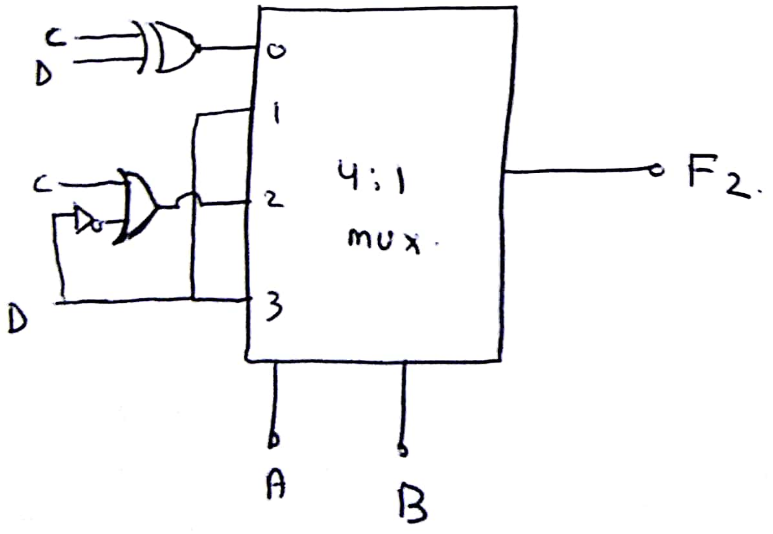
F = D will do (same as AB = 01 case)

* AB = 10.

F = 1 when CD = 00, 11, 10

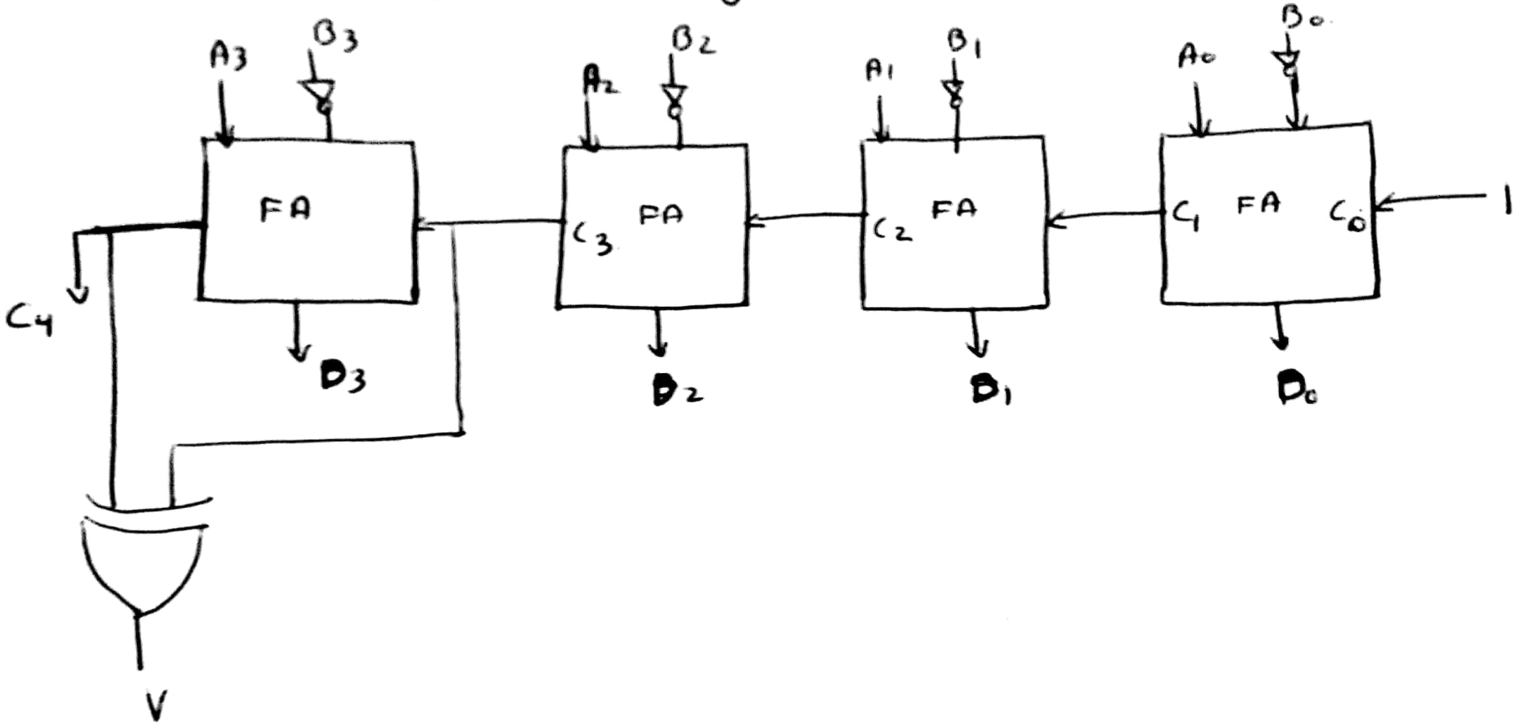
or F = 0 when CD = 01

$F' = \bar{C} D \Rightarrow F = \overline{(\bar{C} D)} = C + \bar{D}$



PROBLEM : 8

4-bit ripple carry subtractor



V=1 ⇒ overflow, result invalid

V=0 ⇒ result is valid

PROBLEM : 9

A single bit comparator (SBC) with i/p A & B.

$A > B \Rightarrow A = 1,\ B = 0 \Rightarrow A\overline{B}$

$A < B \Rightarrow A = 0,\ B = 1 \Rightarrow \overline{A}B$.

$A = B \Rightarrow A = B = 0$ or $A = B = 1 \Rightarrow A \odot B$ (XNOR)

For n bit case, we need another signal, E.

	A	B	A>B	A=B	A<B
If E=1	0	0	0	1	0
	0	1	0	0	1
	1	0	1	0	0
	1	1	0	1	0
If E=0	X	X	0	0	0

A>B.

E \ AB	00	01	11	10
0	0	0	0	0
1	0	0	0	1

$A > B \equiv EA\overline{B}$

A < B.

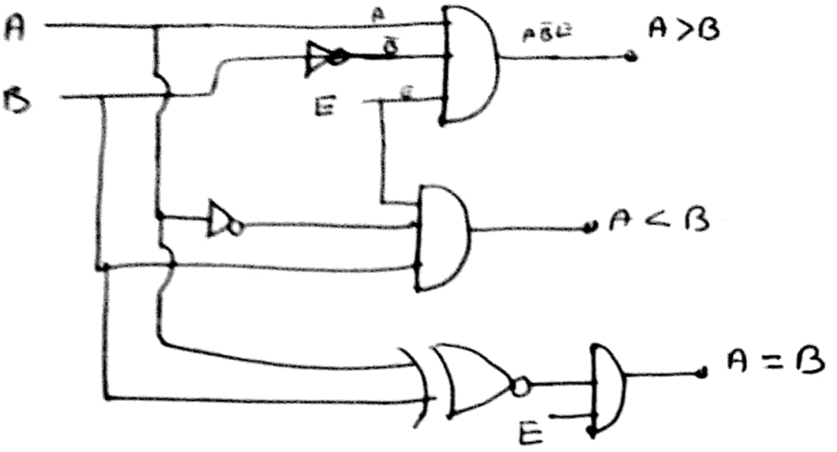
E \ AB	00	01	11	10
0	0	0	0	0
1	0	1	0	0

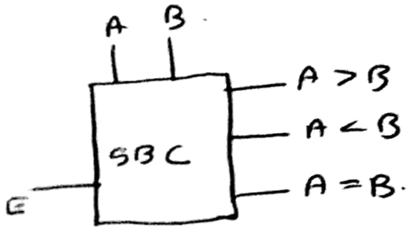
$A < B \equiv E\overline{A}B$

A = B.

E \ AB	00	01	11	10
0	0	0	0	0
1	1	0	1	0

$A = B \equiv E\, A \odot B$

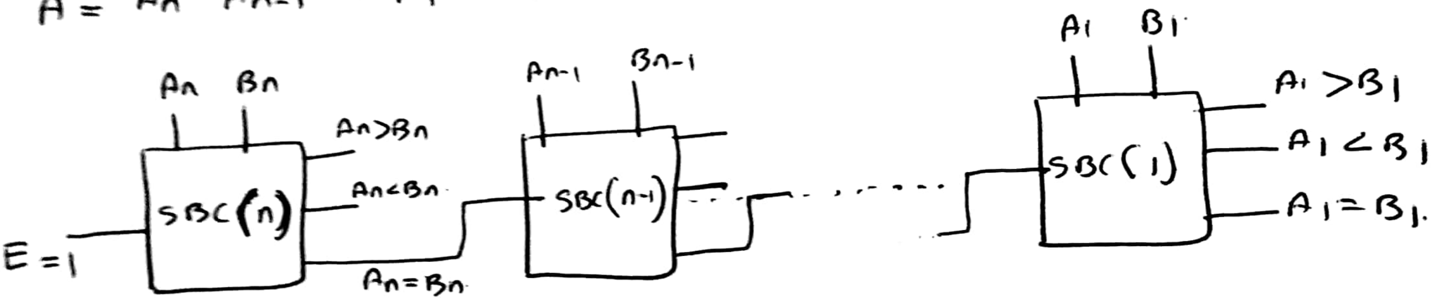


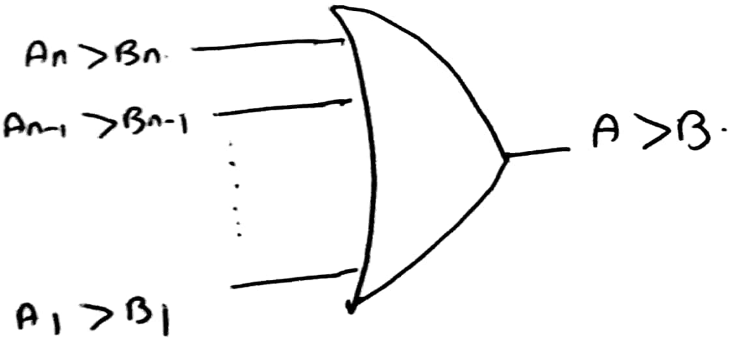


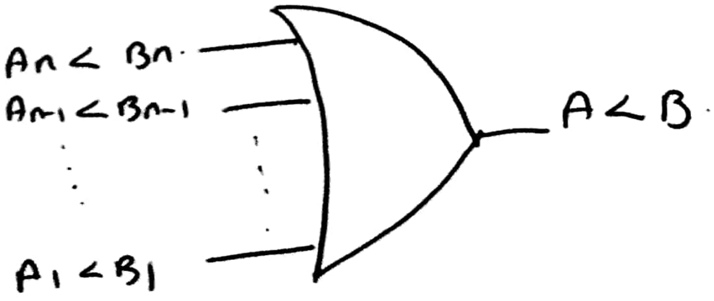
E=1 for single bit comparator. Useful for n-bit (n>1) comparisons.

For n-bit comparison:

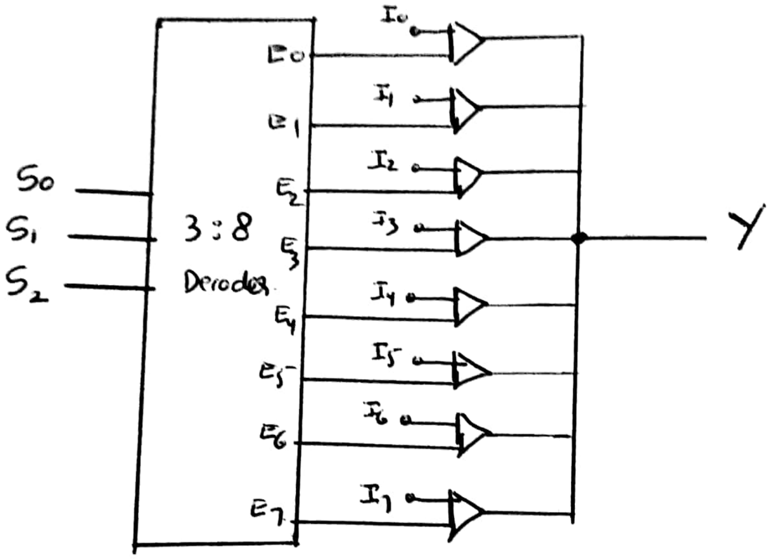
A = An An-1 -- A1 and B = Bn Bn-1 ··· B1.







PROBLEM : 10



Note : S_0, S_1, S_2 here acts as select lines

E_0 → E_7 will enable the tristate gates .

I_0 → I_7 will act as inputs to the mux .