EE2001: Tutorial 3 Solutions

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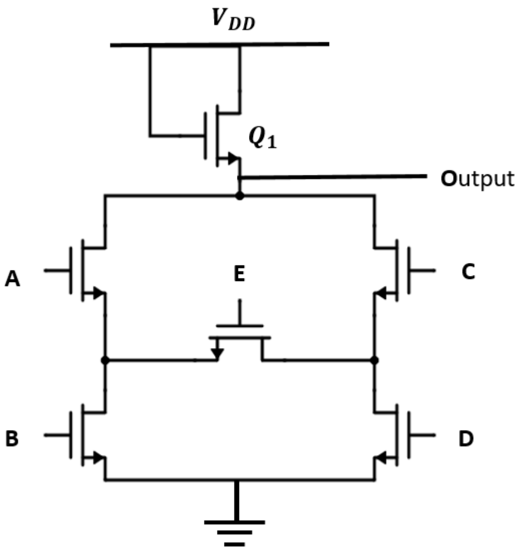
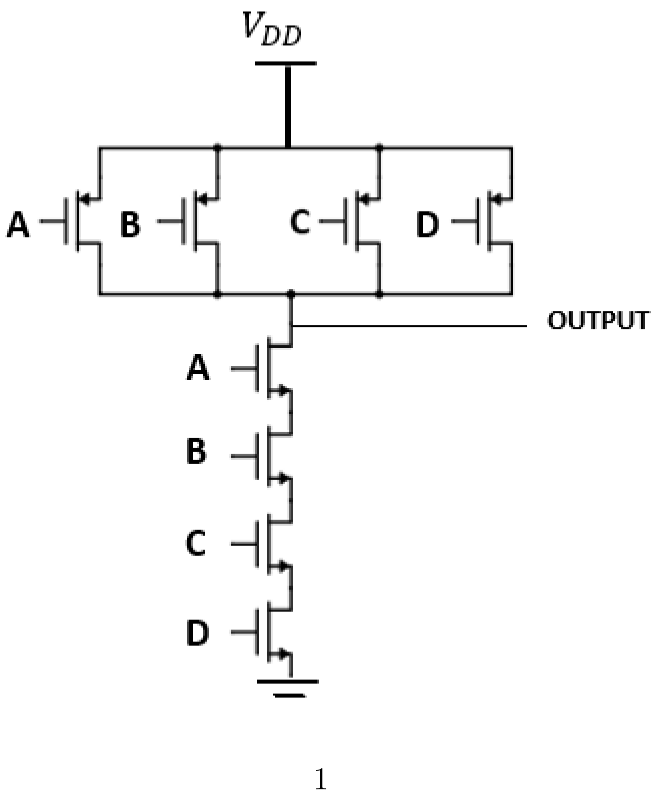
1. (i)



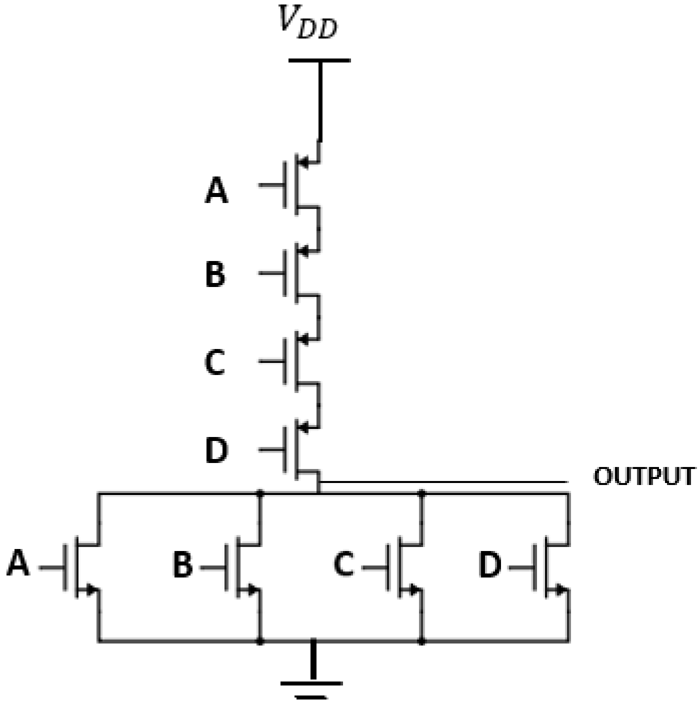
As the gate and drain terminals of the Q_1 transistor are shorted, it acts as resistor. MOS transistor is bilateral. So we have two similar paths AED and CEB (other than AB and CD), that connect the output to ground.
Output $Y = (AB + CD + AED + CEB)'$

(ii)



Output $Y = (ABCD)'$

(iii)



Output $Y = (A + B + C + D)'$

2. (a) $M = 0$

$$\begin{array}{lr} A & 0111 \\ B & 0110 \\ \hline S & 01101 \end{array}$$

$$C = C_4 = 0 \qquad C_3 = 1 \qquad V = C_4 \oplus C_3 = 1$$

(b) $M = 0$

$$\begin{array}{lr} A & 1000 \\ B & 1001 \\ \hline S & 10001 \end{array}$$

$$C = C_4 = 1 \qquad C_3 = 0 \qquad V = C_4 \oplus C_3 = 1$$

(c) $M = 1$

$$\begin{array}{lr} A & 1100 \\ B' & 0111 \\ C_0 & 1 \\ \hline S & 10100 \end{array}$$

$$C = C_4 = 1 \qquad C_3 = 1 \qquad V = C_4 \oplus C_3 = 0$$

(d) $M = 1$

$$\begin{array}{lr} A & 0101 \\ B' & 0101 \\ C_0 & 1 \\ \hline S & 01011 \end{array}$$

$$C = C_4 = 0 \qquad C_3 = 1 \qquad V = C_4 \oplus C_3 = 1$$

(e) $M = 1$

$$\begin{array}{lr} A & 0000 \\ B' & 1110 \\ C_0 & 1 \\ \hline S & 01111 \end{array}$$

$$C = C_4 = 0 \qquad C_3 = 0 \qquad V = C_4 \oplus C_3 = 0$$

3. Carry lookahead generator consists of two level forms of logic AND and OR. So this adder is a four level realization. Total delay is:

$$10(XOR) + 5(AND) + 5(OR) + 10(XOR) = 30ns$$

4. (a)

$$\begin{aligned} (C_i'G_i' + P_i')' &= (C_i'G_i')'P_i \\ &= (C_i + G_i)P_i \\ &= C_iP_i + G_iP_i \\ &= C_i(A_i + B_i) + A_iB_i(A_i + B_i) \\ &= C_iA_i + C_iB_i + A_iB_i \\ &= C_{i+1} \end{aligned}$$

$$\begin{aligned}(P_iG_i') \oplus C_i &= (A_i + B_i)(A_iB_i)' \oplus C_i \\ &= (A_i + B_i)(A_i' + B_i') \oplus C_i \\ &= A_i \oplus B_i \oplus C_i \\ &= S_i\end{aligned}$$

(b) Output of NOR gate = $(A_o + B_0)' {=} P_o'$
Output of $NAND$ gate = $(A_oB_0)' {=} G_o'$

$$S_o = (P_oG_o') \oplus C_o$$

$$C_1 = (C_o'G_o' + P_o')$$

5. (a)

$$\begin{aligned}(G_i + P_iC_i) &= (G_i + P_i)(G_i + C_i) \\ &= (G_i'P_i')'(G_i'C_i')' \\ &= (G_i'P_i' + G_i'C_i')'\end{aligned}$$

(b)

$$C_2 = (G_1'P_1' + G_1'C_1')'$$

$$\begin{aligned}C_3 &= (G_2'P_2' + G_2'C_2')' \\ &= (G_2'P_2' + G_2'(G_1'P_1' + G_1'C_1')')'\end{aligned}$$

$$\begin{aligned}C_4 &= (G_3'P_3' + G_3'C_3')' \\ &= (G_3'P_3' + G_3'(G_2'P_2' + G_2'C_2')')' \\ &= (G_3'P_3' + G_3'(G_2'P_2' + G_2'(G_1'P_1' + G_1'C_1')')')'\end{aligned}$$

6. (i) BCD to 9's complement circuit diagram

BCD				9's complement			
A	B	C	D	W	X	Y	Z
0	0	0	0	1	0	0	1
0	0	0	1	1	0	0	0
0	0	1	0	0	1	1	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	0	0
0	1	1	0	0	0	1	1
0	1	1	1	0	0	1	0
1	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0

AB \ CD	00	01	11	10
00	1	1	0	0
01	0	0	0	0
11	X	X	X	X
10	0	0	X	X

$$W = A'B'C'$$

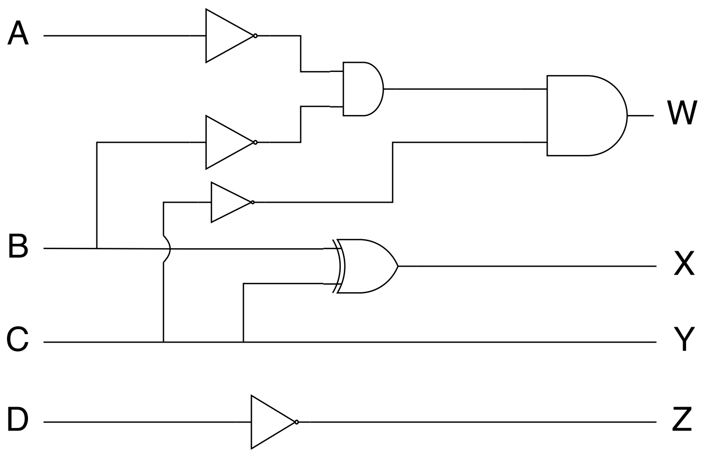
AB \ CD	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	X	X	X	X
10	0	0	X	X

$$X = B'C + BC' = B \oplus C$$

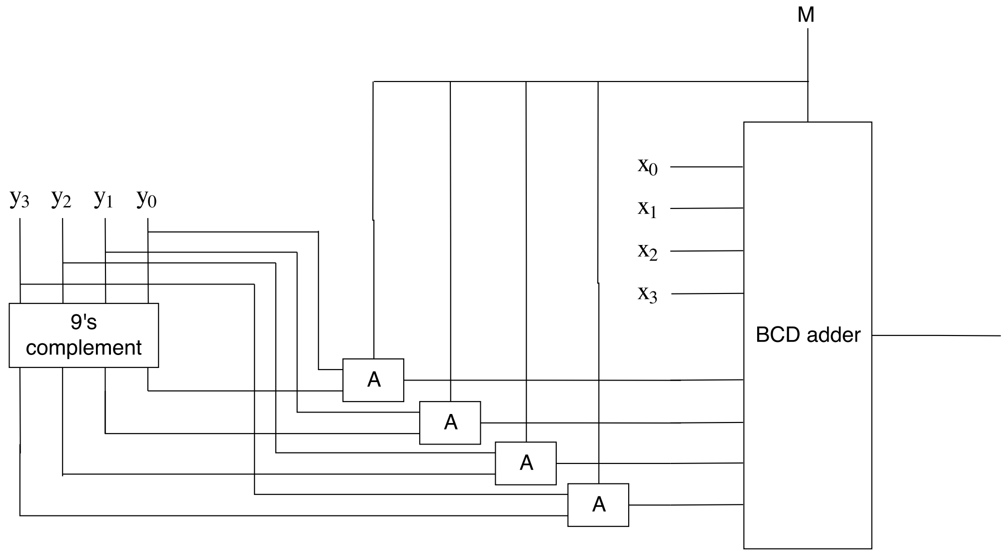
$$Y = C$$

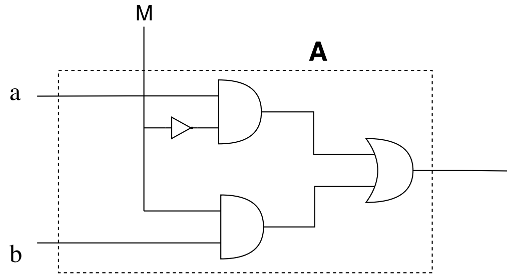
$$Z = D'$$

Circuit diagram



(ii) Consider X, Y to be two BCD numbers.
X=$x_3x_2x_1x_0$ and Y=$y_3y_2y_1y_0$

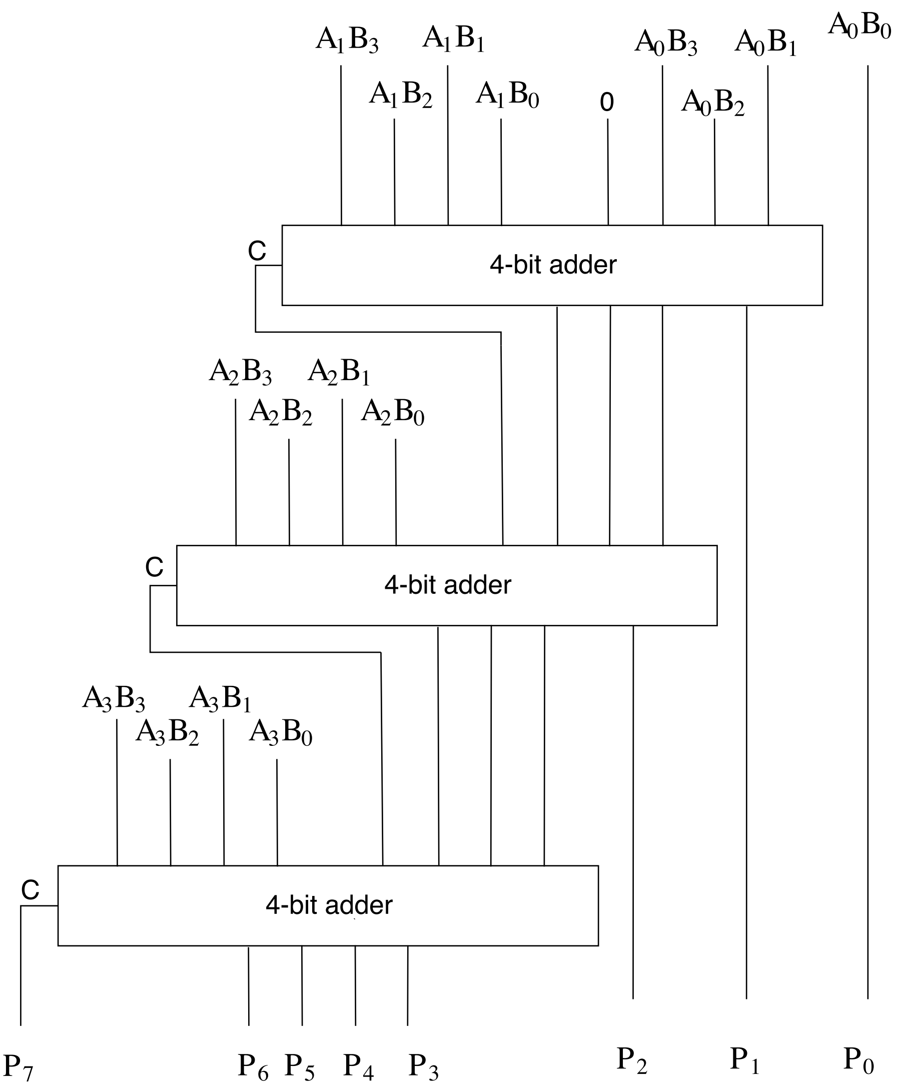




M is to select mode.
M = 0 for BCD adder and M = 1 for BCD subtractor.

7. (i) Binary multiplier using AND gates and binary adders

$$
\begin{array}{cccccccc}
 & & & & B_3 & B_2 & B_1 & B_0 \\
 & & & & A_3 & A_2 & A_1 & A_0 \\
\hline
 & & & & A_0B_3 & A_0B_2 & A_0B_1 & A_0B_0 \\
 & & & A_1B_3 & A_1B_2 & A_1B_1 & A_1B_0 & \\
 & & A_2B_3 & A_2B_2 & A_2B_1 & A_2B_0 & & \\
 & A_3B_3 & A_3B_2 & A_3B_1 & A_3B_0 & & & \\
\hline
P_7 & P_6 & P_5 & P_4 & P_3 & P_2 & P_1 & P_0
\end{array}
$$



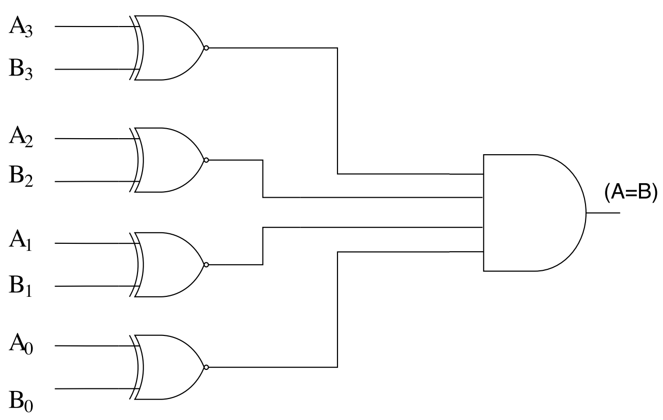
(ii) 4 bit comparator

Consider $A=A_3A_2A_1A_0$ and $B=B_3B_2B_1B_0$

$(A=B) = 1$ if $A_i=B_i$ for all $i = 0, 1, 2, 3$

$= 0$ otherwise

This can be implemented using XNOR and AND gates.



$$(A=B)= (A_3 \odot B_3)\ (A_2 \odot B_2)\ (A_1 \odot B_1)\ (A_0 \odot B_0)$$

8. Given X=$x_1x_2x_3x_4$ and Y=$y_1y_2y_3y_4$

(i) If $G_3 = 1$, $S_3 = 0$ then $G_4 = 1$, $S_4 = 0$.
If $G_3 = 0$, $S_3 = 1$ then $G_4 = 0$, $S_4 = 1$.
If $G_3 = 0$, $S_3 = 0$, then compare x_4 and y_4.

G_3	S_3	x_4	y_4	G_4	S_4
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	0	0
0	1	0	0	0	1
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	0	1
1	0	0	0	1	0
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	1	0
1	1	0	0	X	X
1	1	0	1	X	X
1	1	1	0	X	X
1	1	1	1	X	X

G_3S_3 \ x_4y_4	00	01	11	10
00	0	0	0	1
01	0	0	0	0
11	X	X	X	X
10	1	1	1	1

$$G_4 = G_3 + S_3' x_4 y_4'$$

G_3S_3 \ x_4y_4	00	01	11	10
00	0	1	0	0
01	1	1	1	1
11	X	X	X	X
10	0	0	0	0

$$S_4 = S_3 + G_3'x_4'y_4$$

(ii) Generalizing the equations,

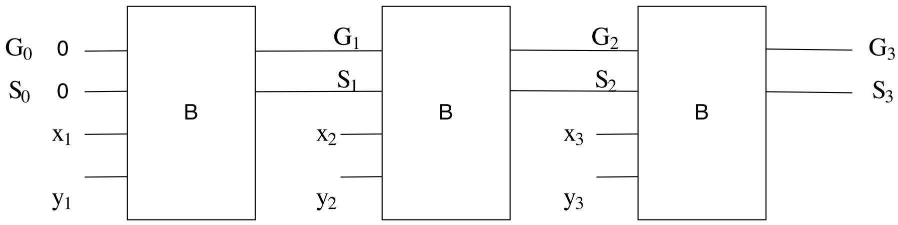
$$G_i = G_{i-1} + S_{i-1}'x_iy_i'$$

$$S_i = S_{i-1} + G_{i-1}'x_i'y_i$$

$$\therefore G_1 = G_0 + S_0'x_1y_1' \qquad S_1 = S_0 + G_0'x_1'y_1$$

$$G_2 = G_1 + S_1'x_2y_2' \qquad S_2 = S_1 + G_1'x_2'y_2$$

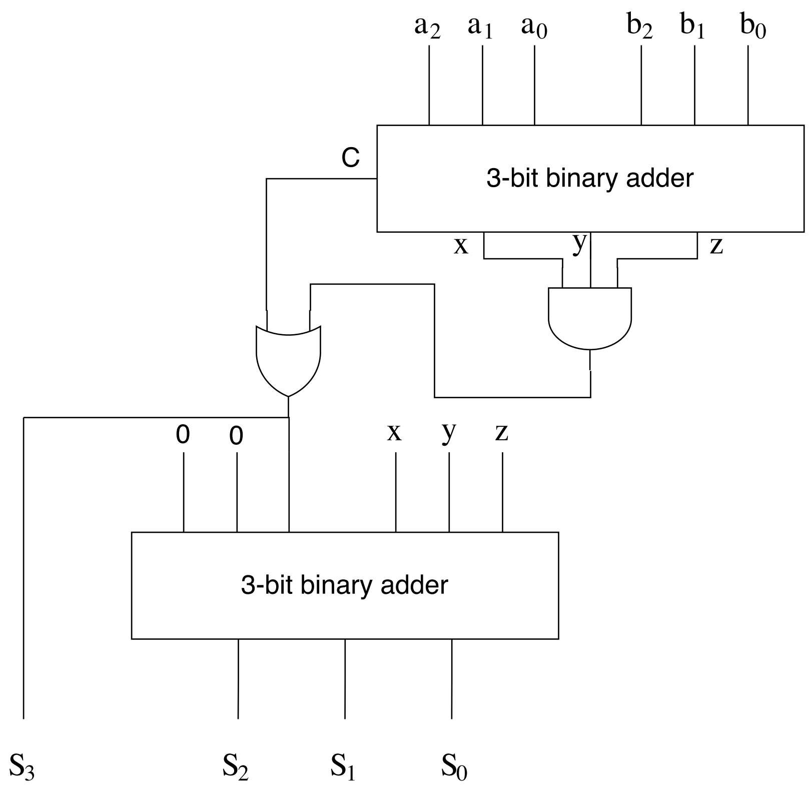
$$G_3 = G_2 + S_2'x_3y_3' \qquad S_3 = S_2 + G_2'x_3'y_3$$



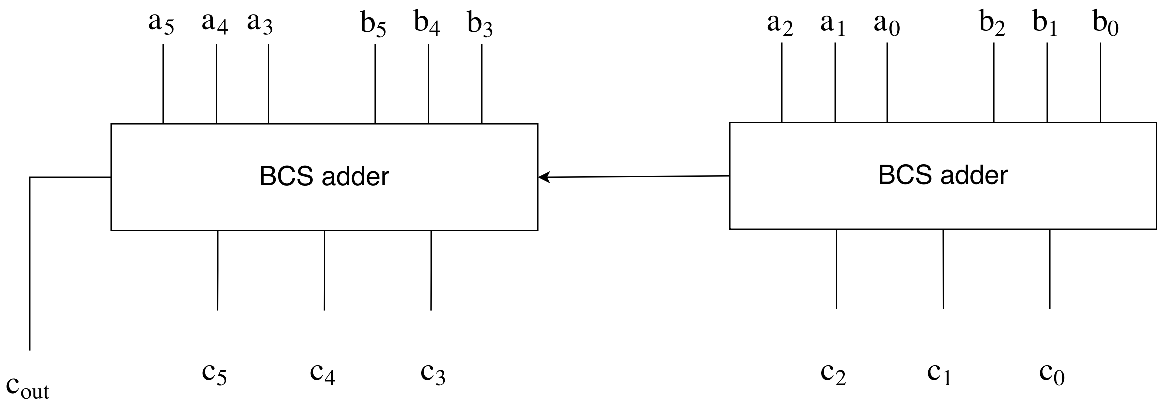
9. (i) Binary coded base-seven (BCS)

Decimal	BCS
0	000 000
1	000 001
2	000 010
3	000 011
4	000 100
5	000 101
6	000 110
7	001 000
8	001 001
...	...
...	...

BCS adder using 3-bit binary adders



(ii) 2-digit BCS adder using two 1-digit BCS adders



10. Seven segment decoder

ABCD	a	b	c	d	e	f	g
0000	1	1	1	1	1	1	0
0001	0	1	1	0	0	0	0
0010	1	1	0	1	1	0	1
0011	1	1	1	1	0	0	1
0100	0	1	1	0	0	1	1
0101	1	0	1	1	0	1	1
0110	1	0	1	1	1	1	1
0111	1	1	1	0	0	0	0
1000	1	1	1	1	1	1	1
1001	1	1	1	1	0	1	1

AB \ CD	00	01	11	10
00	1	0	1	1
01	0	1	1	1
11	0	0	0	0
10	1	1	0	0

$$a = A'C + A'BD + B'C'D' + AB'C'$$

AB \ CD	00	01	11	10
00	1	1	1	1
01	1	0	1	0
11	0	0	0	0
10	1	1	0	0

$$b = A'B' + A'C'D' + A'CD + B'C'$$

AB \ CD	00	01	11	10
00	1	1	1	0
01	1	1	1	1
11	0	0	0	0
10	1	1	0	0

$$c = A'D + A'B + B'C'$$

AB \ CD	00	01	11	10
00	1	0	1	1
01	0	1	0	1
11	0	0	0	0
10	1	1	0	0

$$d = A'CD' + A'B'C + B'C'D' + AB'C' + A'BC'D$$

AB \ CD	00	01	11	10
00	1	0	0	1
01	0	0	0	1
11	0	0	0	0
10	1	0	0	0

$$e = A'CD' + B'C'D'$$

AB \ CD	00	01	11	10
00	1	0	0	0
01	1	1	0	1
11	0	0	0	0
10	1	1	0	0

$$f = A'BC' + A'C'D' + A'BD' + AB'C'$$

AB \ CD	00	01	11	10
00	0	0	1	1
01	1	1	0	1
11	0	0	0	0
10	1	1	0	0

$$g = A'CD' + A'B'C + A'BC' + AB'C'$$