EE2001 Quiz-1 Digital System Design (Theory) Feb 18 2019

Duration	50 minutes
Submit your answers in the order of questions	2 points penalty for wrong order
Wrong/No Roll Number or Name	Zero points for the Quiz
Wrong/No Instructor Name	2 points will be deducted from the total

Roll Number	ee18b122
Name	AKILESH KANNAN
Instructor's Name	Prof - Ananth Krishnan

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Question:	1	2	3	Total
Points:	6	3	3	12
Score:				

This exam has 3 questions, for a total of 12 points.

1. (6 points) Design a minimal gate level implementation and draw a minimal gate level circuit diagram for finding the square of a given positive decimal number N, with following conditions

   - Input to the circuit is the unsigned binary form of decimal number N
   - N is represented in binary by 2.1 bits as $(N)_{10} = (ab.c)_2$ where a,b, and c are bits. So, N is represented by 2 bits (a and b) for integer part and 1 bit (c) for fractional part. For example, if $ab.c = 10.1$, so, $a = 1, b = 0$ and $c = 1$, then, $(N)_{10}$ will correspond to the decimal equivalent of $(ab.c)_2$. Hence, a, b, and c will be the inputs to the circuit.
   - $(0.0)_{10} \leq (N)_{10} \leq (3.0)_{10}$ or simply $(0.0 \leq N \leq 3.0)$
   - the output of the circuit should be the Binary equivalent of $(N^2)_{10}$ {For example, if, $(N)_{10} = (2.0)_{10}$, then, the output should be binary form of $(N^2)_{10}$. In this case, the output would be binary form of $(4.00)_{10}$}.
   - The binary output should be represented by sufficient number of bits for Accurately representing, both the integer and fractional parts.
   - only AND, OR and NOT gates are to be used.

2. (3 points) Draw the minimal NOR gate based implementation of the following function.
   $F(A,B,C,D) = \sum m(0,3,5,7,8,9,10,12,13) + \sum d(1,6,11,14)$

3. (3 points) A majority circuit is a combinational circuit, whose output is equal to 1, when the input variables have more 1s than 0s. The output is zero otherwise. Design a three-input majority function using 4 : 1 MUX.

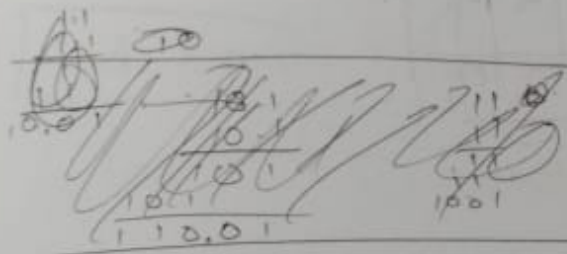
TRUTH TABLE for the squaring operation

INPUTS			INTEGRAL OUTPUTS				FRACTIONAL	
a	b	c	x	y	z	w	x	q
0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1
0	1	0	0	0	0	1	0	0
0	1	1	0	0	1	0	0	1
1	0	0	0	1	0	0	0	0
1	0	1	0	1	1	0	0	1
1	1	0	1	0	0	1	0	0
1	1	1	x	x	x	x	x	x

DON'T CARE

Given number here < 3,0 (11.0).

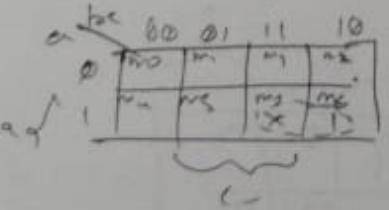
So a=b=c=1 is a DON'T CARE case



Taking 4 digits for integral & 2 bits for fractional as max integral bits : 4 (for 9 : 1001.0)

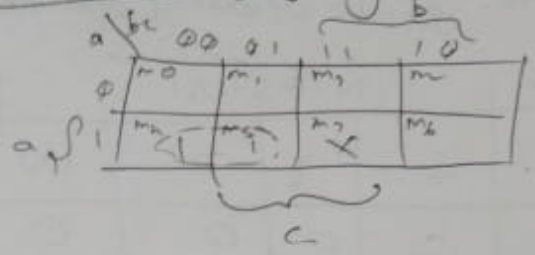
Max frac. bits for 0.11 = (0.01)

Predictor for x



x = ab

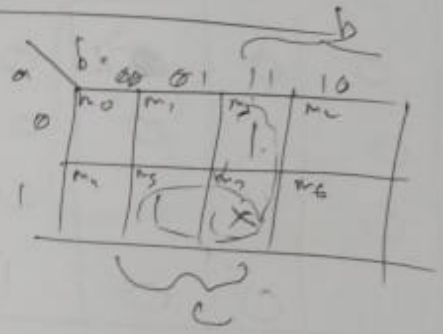
Reduction for y



m_4, m_5 ●

$= a b'$

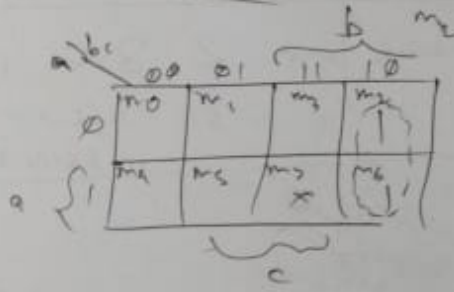
Reduction for z



$z = ac + bc$

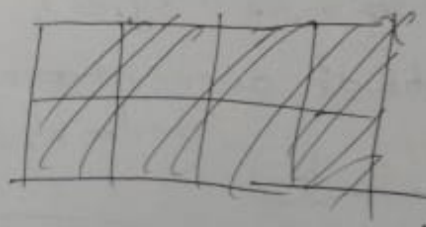
$= (a+b) \cdot c$

Reduction for w



$w = bc'$

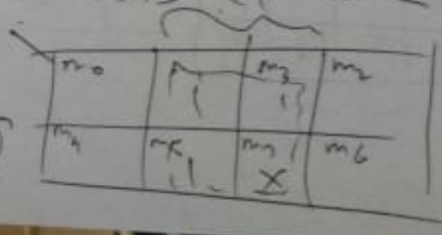
for P



$P = 0$

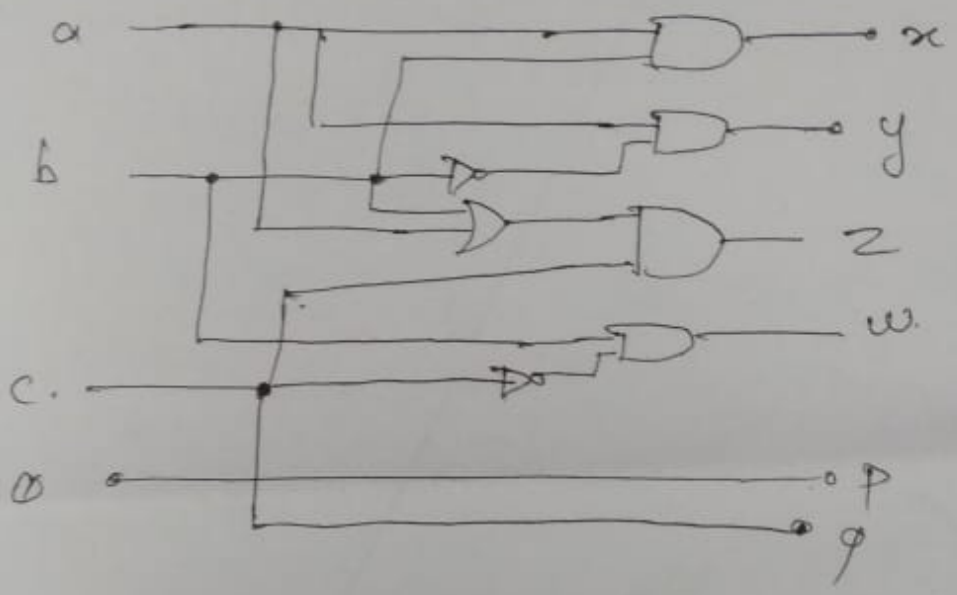
for all. m/p

for q:



$q = c$

⇒ the circuit implementation is.

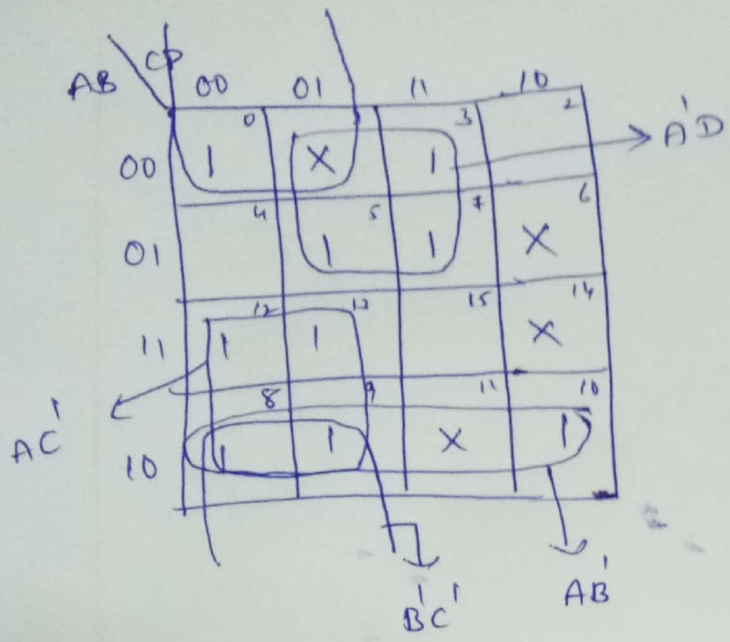


Expressions :

$(ab.c)^2 = (xyzw.pq)_2$

$x = ab$
$y = ab'$
$z = (a+b).c$
$w = bc'$
$p = 0$
$q = c$

2)

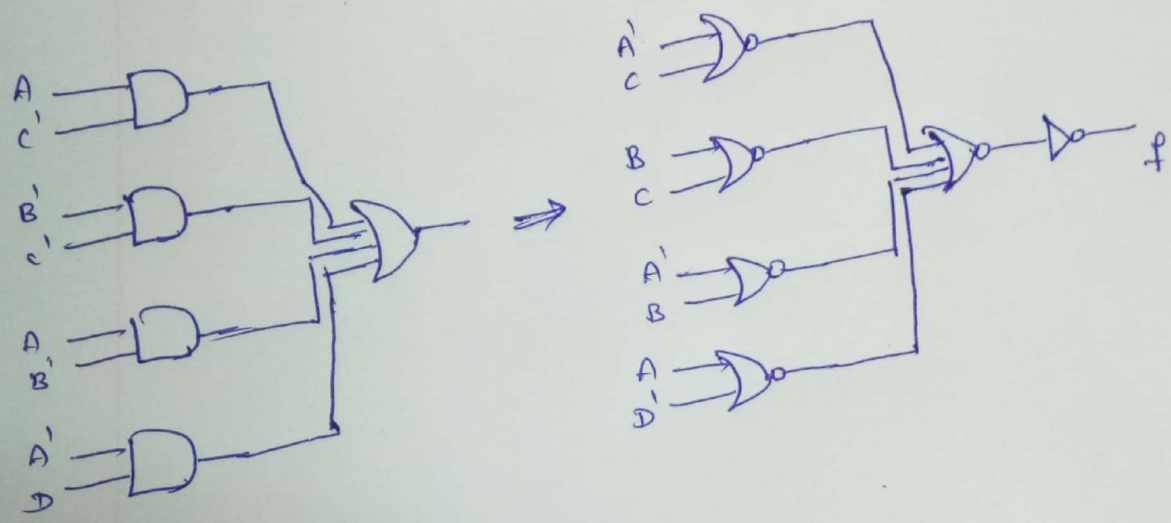


K-MAP – 1 MARK

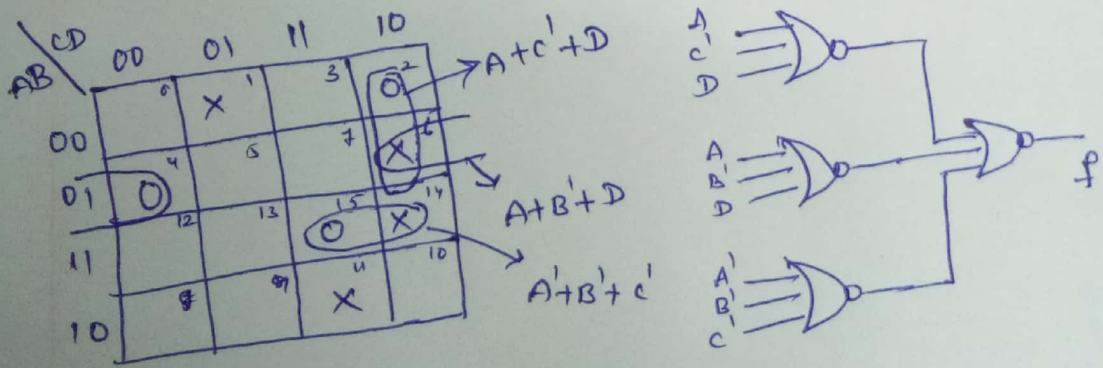
EXPRESSION – 1 MARK

CIRCUIT DIAGRAM – 1 MARK

$$F = AC' + BC' + AB' + A'D$$



[or]



$$f = (A + C' + D)(A + B' + D)(A' + B' + C')$$

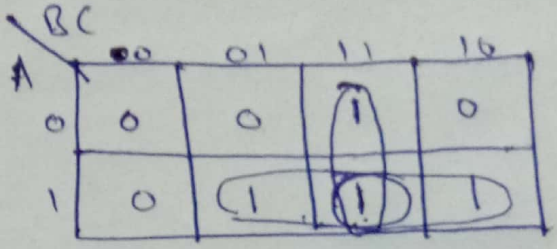
→ Let the 3 inputs be A, B, C, & Output be Y

Truth table (for the given i/p, o/p map)

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

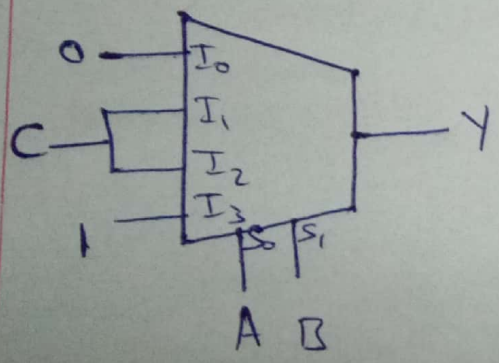
K-Map

(OR)



→ Identifying the truth table /k-Map – (1 Mark)

Realization with 4:1 Mux – (2 Marks)



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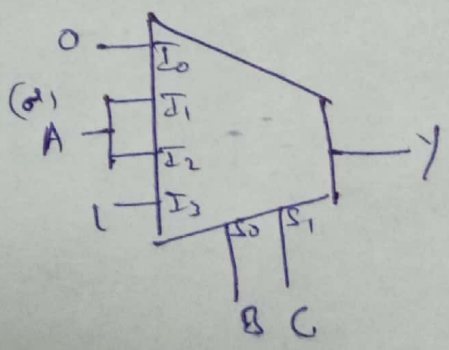

(or)