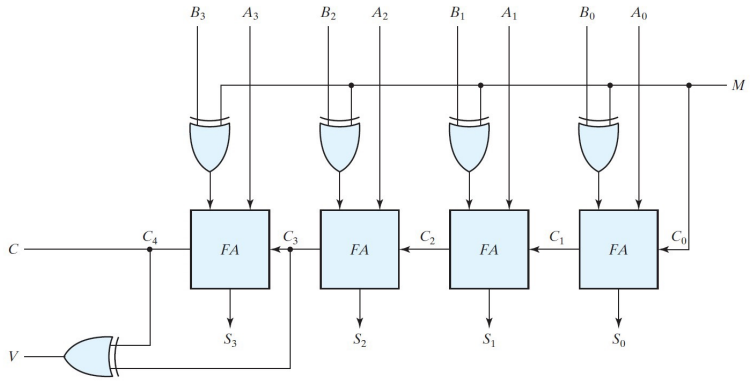
EE2001-Tutorial 3
Date: 6th February 2018
MOS Implementation and Combinational Logic

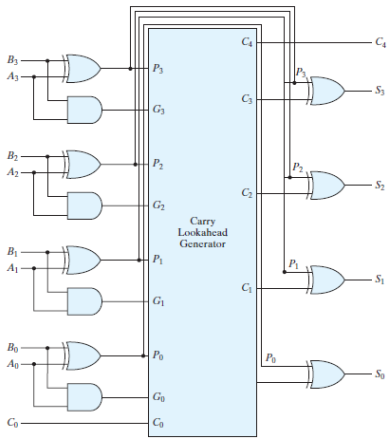
1) (i) The MOS transistor is bilateral, i.e., source and drain are interchangeable. Using this property, derive a circuit that implements the following Boolean function using six nMOS transistors.
Y = (AB+CD+AED+CEB)'
(ii) Show the circuit of a four-input NAND gate using CMOS transistors.
(iii) Show the circuit of a four-input NOR gate using CMOS transistors.

2) The adder–subtractor circuit has the values for mode input M and data inputs A and B as given below. In each case, determine the values of the four SUM outputs, the carry C and overflow V.



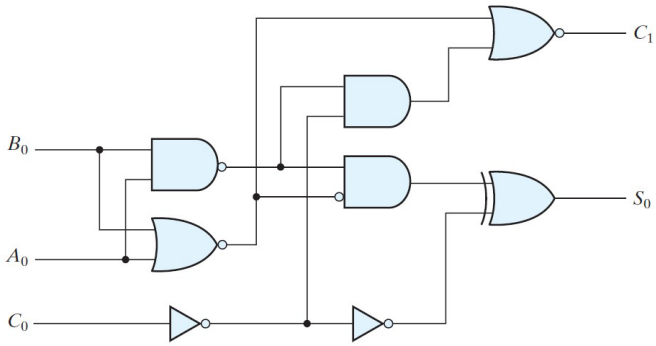
	M	A	B
(a)	0	0111	0110
(b)	0	1000	1001
(c)	1	1100	1000
(d)	1	0101	1010
(e)	1	0000	0001

3) Assume that the exclusive-OR gate has a propagation delay of 10 ns and that the AND or OR gates have a propagation delay of 5 ns. What is the total propagation delay time in the four-bit adder given below.



4) Define the carry propagate and carry generate as $P_i = A_i + B_i$ and $G_i = A_iB_i$ respectively. Show that the output carry and output sum of a full adder becomes
$C_{i+1} = (C_i' G_i' + P_i')'$ and $S_i = (P_iG_i')$ XOR C_i

The logic diagram of the first stage of a four-bit parallel adder as implemented in IC type74283 is shown. Identify the Pi and Gi terminals and show that the circuit implements a full-adder circuit.

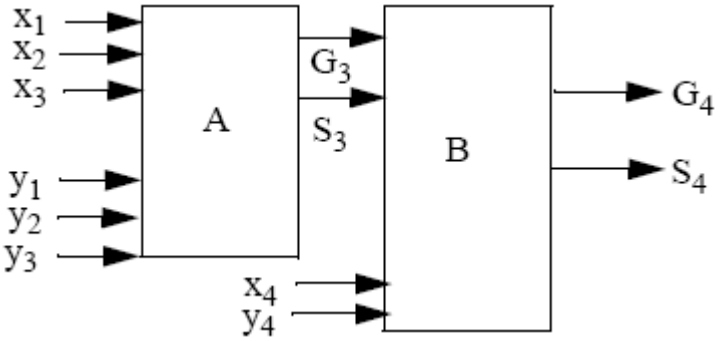


5) Show that the output carry in a full adder circuit can be expressed in the AND-OR-INVERT form $C_{i+1} = G_i + P_iC_i = (G_i'P_i' + G_i'C_i')'$
IC type 74182 is a lookahead carry generator circuit that generates the carries with AND-OR-INVERT gates. The circuit assumes that the input terminals have the complements of the G's, the P's, and of C_1. Derive the Boolean functions for the lookahead carries C_2, C_3, and C_4 in this IC.

6) (i) Design a combinational circuit that generates the 9's complement of a BCD digit.
(ii) Construct a BCD adder–subtractor circuit using the result of (i).

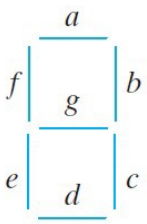
7) (i) Using AND gates and binary adders, design a binary multiplier that multiplies two unsigned four-bit numbers.
(ii) Design a combinational circuit that compares two 4-bit numbers to check if they are equal. The circuit output is equal to 1 if the two numbers are equal and 0 otherwise.

8) In the figure below, the logic package A compares the magnitudes of two three bit numbers, $X_3=x_1x_2x_3$ and $Y_3= y_1y_2y_3$, where x_1 and y_1 are the most significant bits. Package A has two outputs G_3 and S_3, such that $G_3=1$ iff $X_3>Y_3$; $S_3=1$ iff $X_3<Y_3$; and $G3=S3=0$ iff $X_3=Y_3$. A logic unit B serves together with package A as a comparator for two four bit numbers, $X_4=x_1x_2x_3x_4$ and $Y_4=y_1y_2y_3y_4$ as given in the figure.
(i) Find expressions for G_4 and S_4 in terms of inputs to B.
(ii) Also find corresponding expressions for designing package A by means of units of type B.



9) (i) Like binary coded decimal (BCD) number system, we can define a binary coded base-seven (BCS) number system. A BCS adder is a circuit that adds two BCS digits and produces a sum (and carry) digit(s) also in BCS number system. Using two 3-bit binary adders, construct such a BCS adder.
(ii) Using two such BCS adders construct a 2-digit BCS adder.

10) An ABCD-to-seven-segment decoder is a combinational circuit that converts a decimal digit in BCD to an appropriate code for the selection of segments in an indicator used to display the decimal digit in a familiar form. The seven outputs of the decoder (a, b, c, d, e, f, g) select the corresponding segments in the display, as shown in (a). The numeric display chosen to represent the decimal digit is shown in (b). Using a truth table and Karnaugh maps, design the BCD-to-seven-segment decoder using a minimum number of gates. The six invalid combinations should result in a blank display.



(a) Segment designation

(b) Numerical designation for display