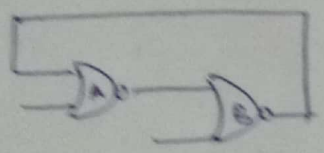
21/07

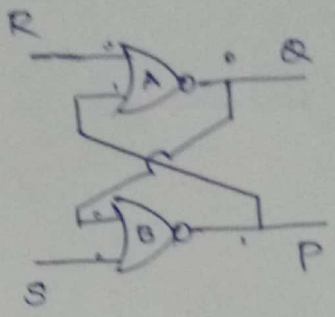
THURSDAY

DIGITAL SYSTEMS

LATCHES AND FLIP FLOPS



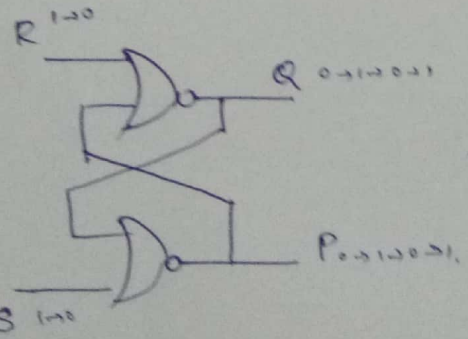
Redrawn as



(cross coupled NOR GATES)

S	R	Q(t)	$Q^+(t+\epsilon)$	$P^+(t+\epsilon)$	
0	0	0	0	1	(Check for stability)
0	0	1	1	0	→ No change
1	0	0	1	0	→ Set condition (Setting Q^+ to '1')
1	0	1	1	0	
0	1	0	0	1	→ Reset condition (Resets Q^+ to '0')
0	1	1	0	1	
1	1	0	?	?	Prohibited condition (Never make S & R 1 at the same instant)
1	1	1			

THIS LATCH IS CALLED AS SET-RESET (SR) LATCH.

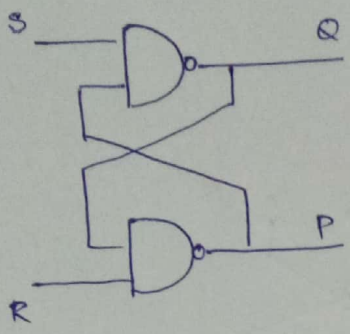


→ NOT A STABLE STATE

Race - condition

→ Settles due to difference in delay to either Q→0 or Q→1

USING NAND GATES.



	S	R	Q	Q^+	P^+
No-change	1	1	0	0	1
	1	1	1	1	0
Set condition	0	1	0	1	0
	0	1	1	1	0
Reset condition	1	0	0	0	1
	1	0	1	0	1
Prohibited condition	0	0	0	?	?
	0	0	1		

Active low set & Reset.