

## Instruction Type & Formats :-

① R type (Register) ADD ~~rd~~ rs1 rs2  $\Leftrightarrow$   $rd \leftarrow rs1 + rs2$

Where rd - destination Register

rs1, rs2 - Source registers

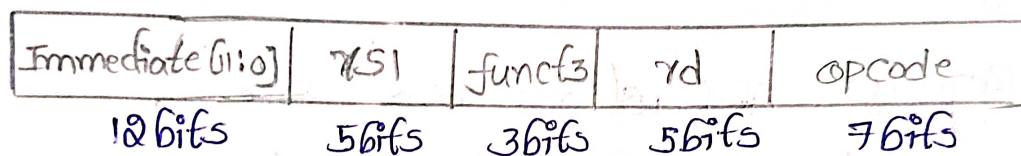
funct7	rs2	rs1	funct3	rd	opcode
7bits	5bits	5bits	3bits	5bits	7bits

funct7 & funct3 are additional opcodes.

② I-type (Immediate)

load: Memory  $\longrightarrow$  Register

ex: lw rd, Immediate(rs)  $\Rightarrow$  rd = Mem[rs + Immediate]

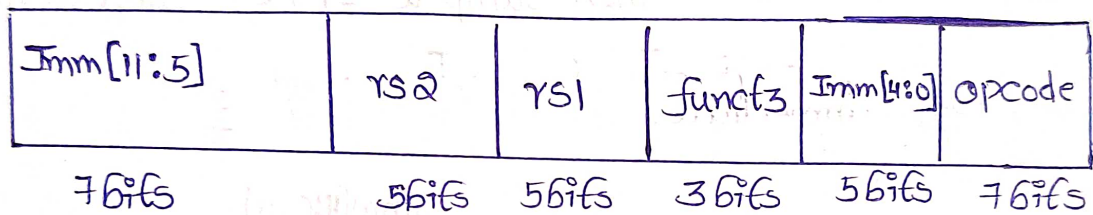


funct3 & opcode Helps to identify this instructions.

s-type (store)

store - Register  $\rightarrow$  Memory

sw rs2, immediate (rs1)



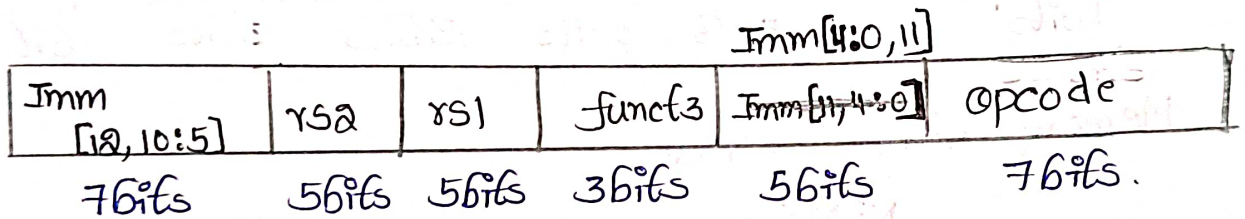
Memory address - rs2

$$\text{MEM}[\text{rs2}] = \text{rs1} + \text{Immediate}$$

## B Type (branch type)

`beq rs1, rs2, L`  $\Rightarrow$  if  $(rs1 == rs2)$   
then Jump to  $(L + PC)^{th}$  instruction

`beq rs1, rs2, Immediate`

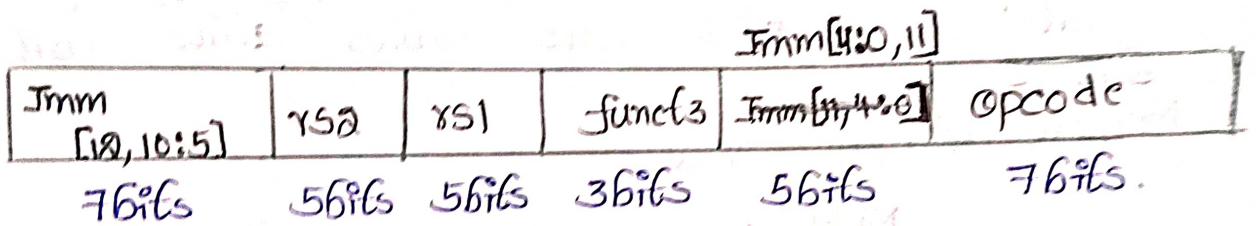


If  $rs1 \neq rs2$ , then immediately  
Start executing  $(PC + Immediate)^{th}$  instruction.

## B Type (branch type)

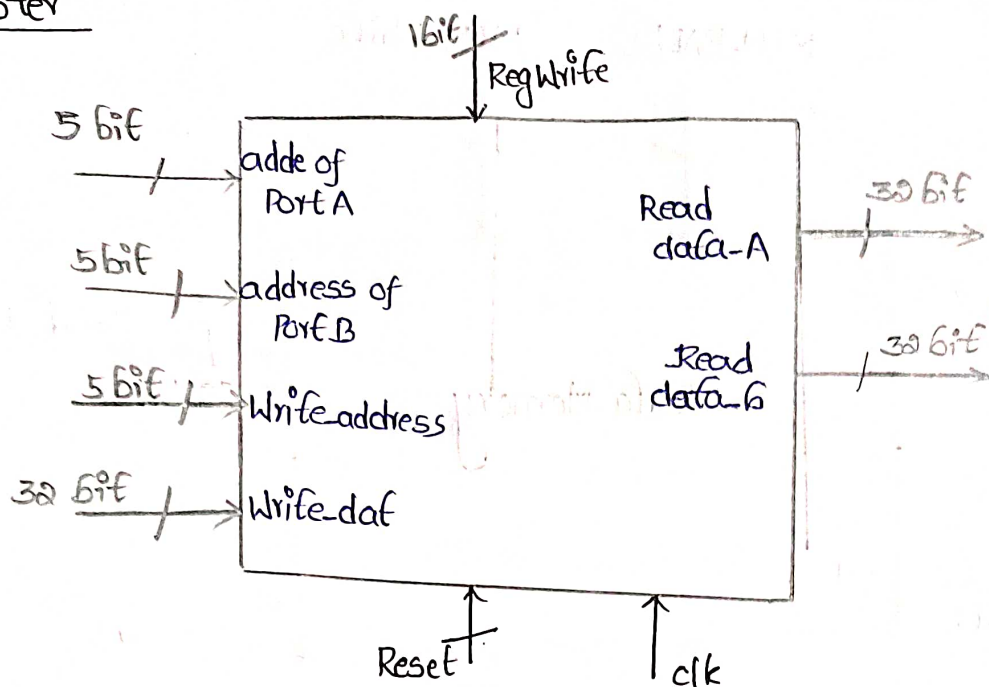
$\text{beq } r_{s1} \ r_{s2} . L \Rightarrow \text{if } (r_{s1} == r_{s2})$   
then Jump to  $(L + PC)^{\text{th}}$  Instruction

$\text{beq } r_{s1}, r_{s2}, \text{Immediate}$

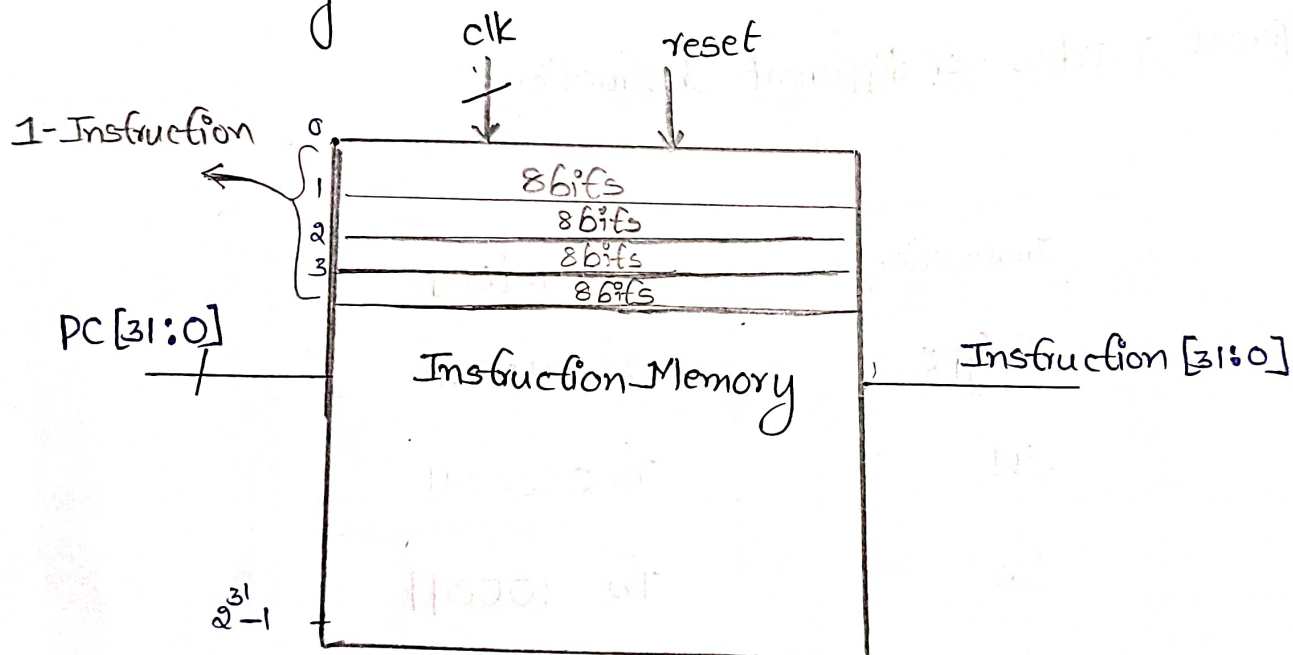


If  $r_{s1} \neq r_{s2}$ , then immediately  
Start executing  $(PC + \text{Immediate})^{\text{th}}$  Instruction.

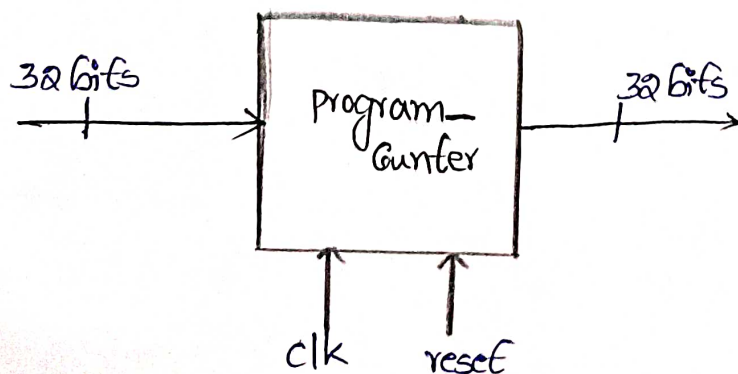
## Register



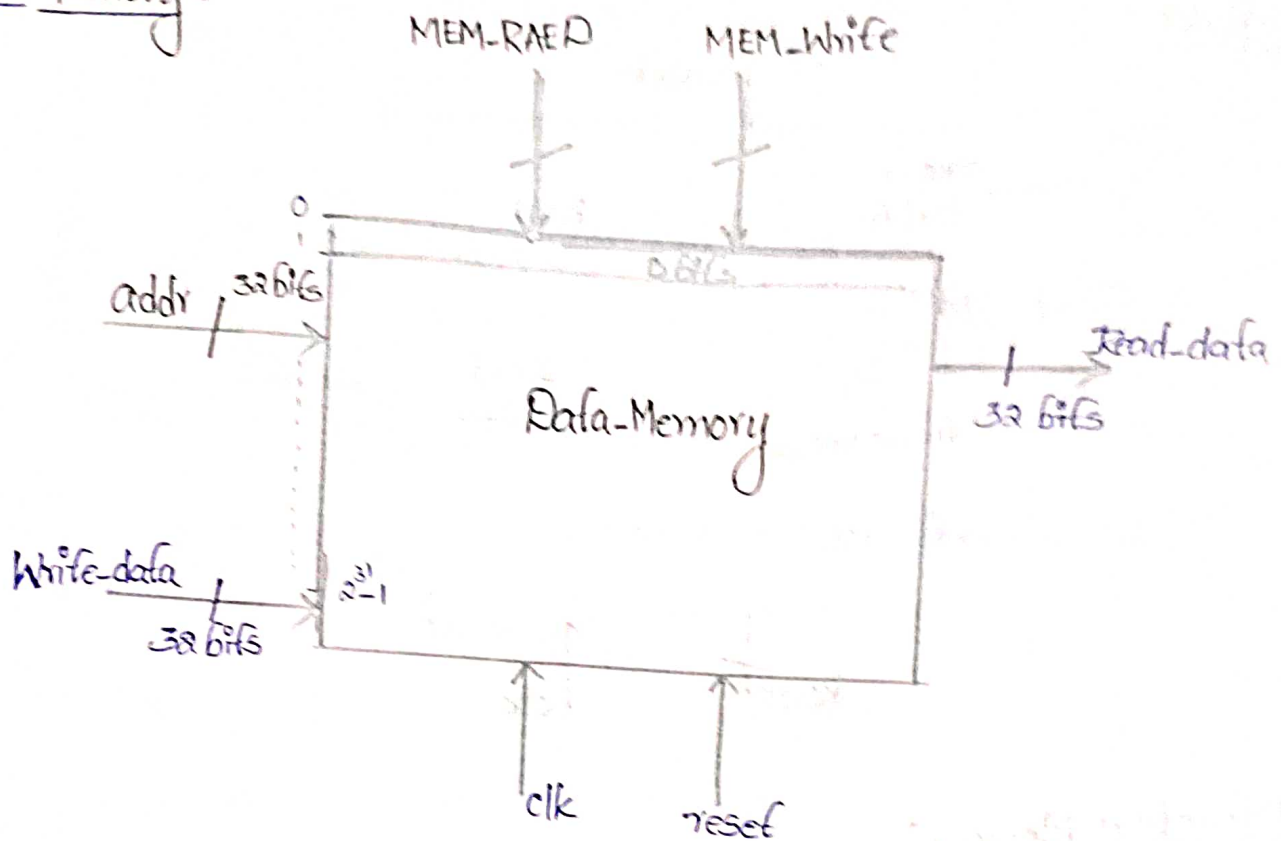
## Instruction Memory



## Program Counter



## Data Memory:

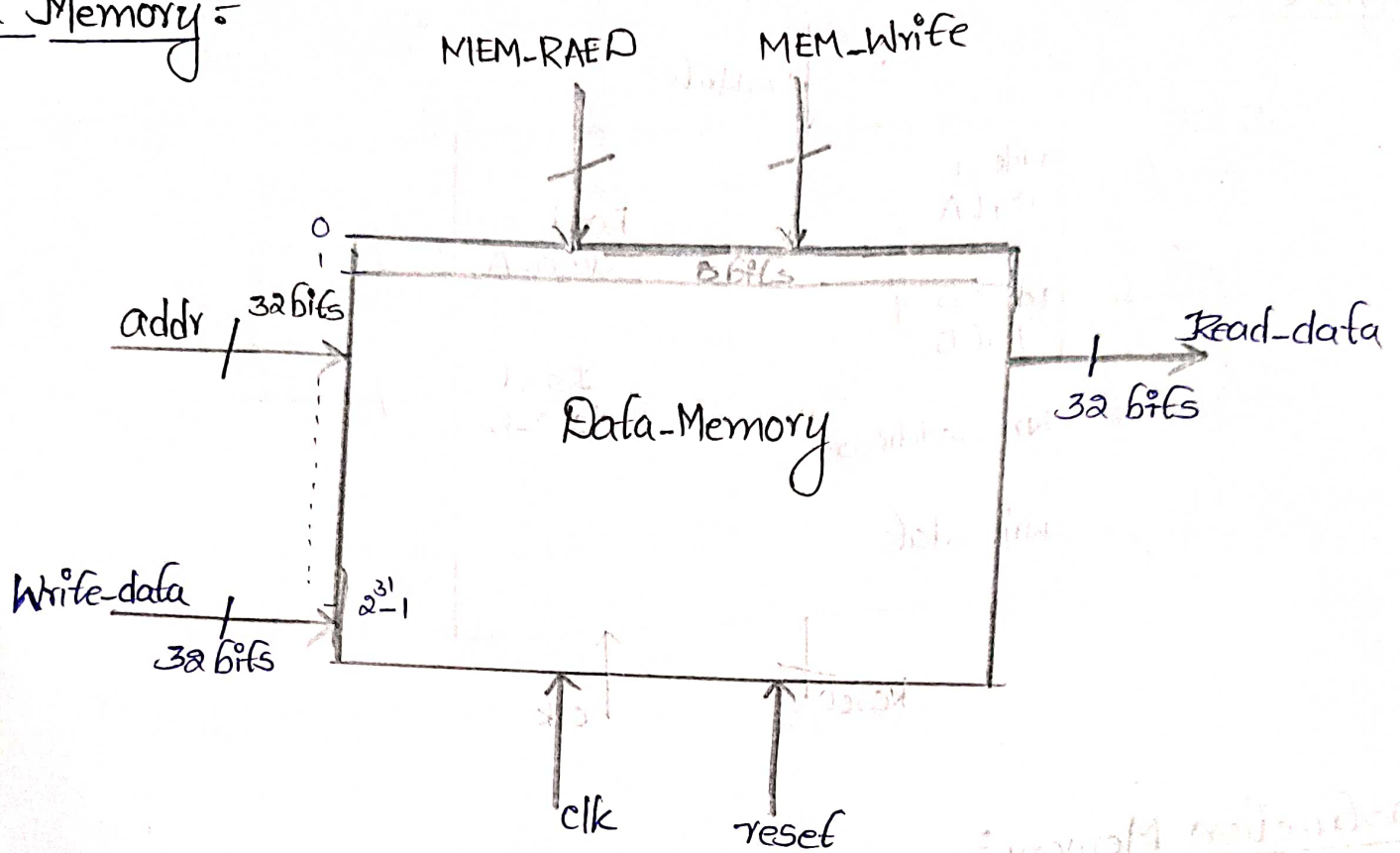


## Different opcodes for different Instructions:

Instruction	opcode [6:0]
R-type	7b 0110011
sw	7b 0000011
lw	7b 0100011
beq	7b 1100011



## Data Memory :



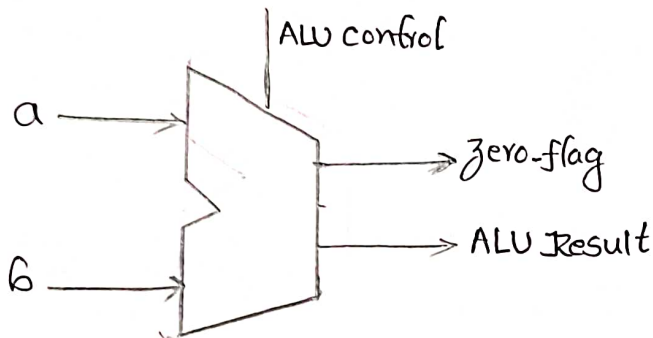
## Different opcodes for different Instructions :

Instruction	opcode [6:0]
R-type	7b 0110011
sw	7b 0000011
lw	7b 0100011
beq	7b 1100011

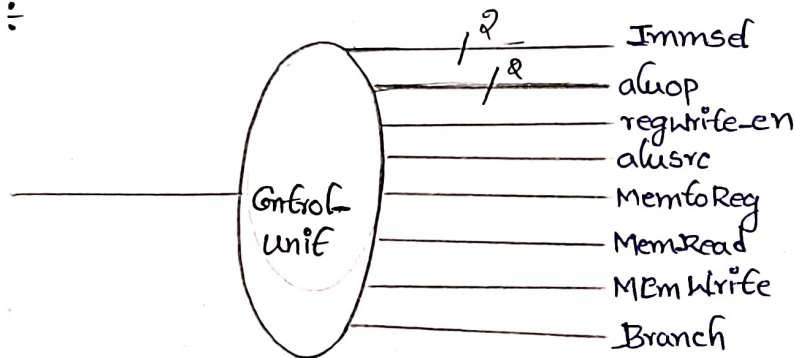


## ALU:

ALU Control lines	Function
0000	AND
0001	OR
0010	ADD
0110	SUB



## Control Unit:



Instruction	ALUSrc ( <small>6bits</small> )	MEM to Reg	Regwrite	MEM Read	MEM write	Branch	ALUop
R-type	0	0	1	0	0	0	10
lw-type	1	1	1	1	0	0	00
sw	1	x	0	0	1	0	00
beq	0	x	0	0	0	1	01

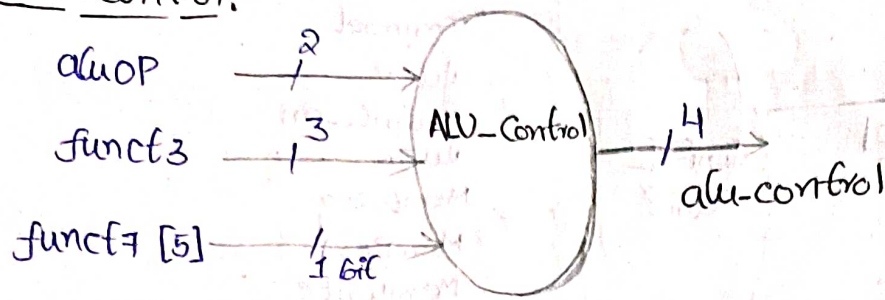
R-type Immset = 0'6xx

lw - Immset = 0'600

store-operation  $\Rightarrow$  Immset = 0'601

Beq-operation  $\Rightarrow$  Immset = 0'610

## alu-control:-



Instruction opcode	ALUop	operation	Funct7 field	Funct3 Field	desired ALU action	ALU Control input
lw	00	load	xxxxxxx	xxx	add	0010
sw	00	store	xxxxxxx	xxx	add	0010
beq	01	branch if equal	xxxxxxx	xxx	sub	0110
R-type	10	add	0000000	000	add	0010
R-type	10	sub	0100000	000	sub	0110
R-type	10	and	0000000	111	and	0000
R-type	10	or	0000000	110	or	0001

Here, for lw, sw, beq

ALUop are different

So, we can make decision on ALUop

But for R-type

ALUop was same

funct7 [5], field

{funct7 field [5], funct3 field} - 0000 - add  
 1000 - sub  
 0111 - and  
 0110 - or