REPORT

The project mainly deals with design and performance analysis of a simple 8:1 multiplexer circuit. The circuit is simulated in Cadence, Microwind and NG spice software's. The 8:1 MUX circuit can be generated either using NAND gates or Transmission gates(CMOS).

The Main aim of the project is to get familiar with the below software's.

CADENCE

Cadence provides a wide range of tools for various stages of the electronic design automation (EDA) process, from schematic capture to layout and verification.

When a Pmos and Nmos transistors are connected as in the below image a 2:1 Mux circuit can be generated.

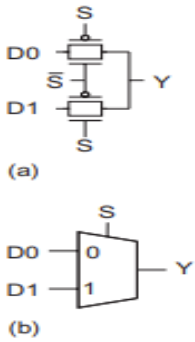
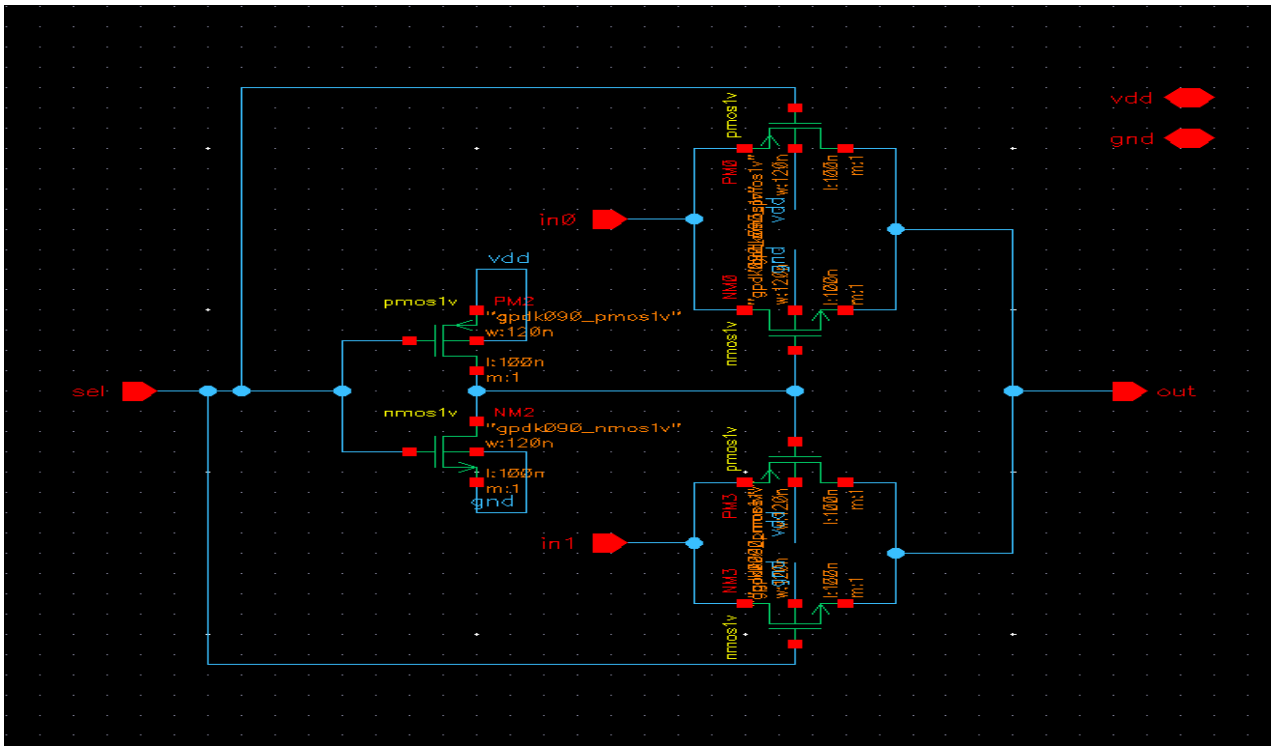


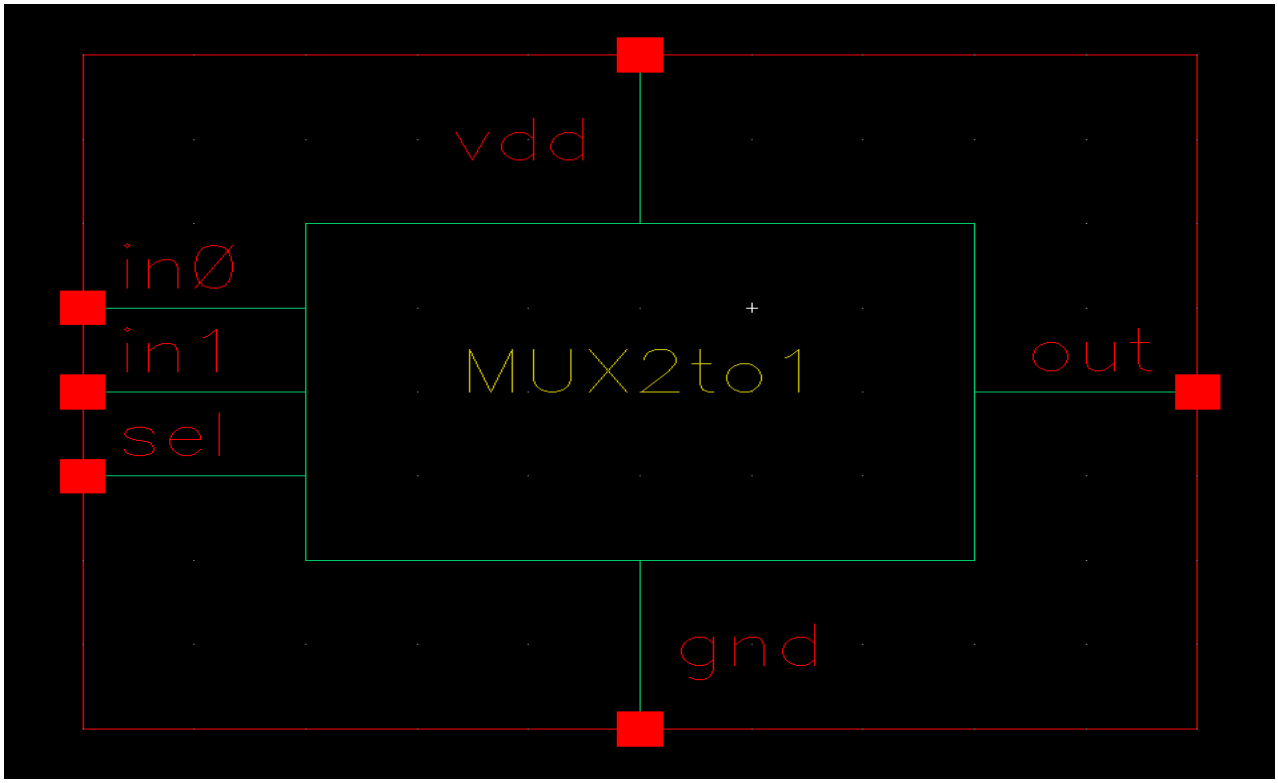
FIGURE 1.28 Transmission gate multiplexer

TABLE 1.6 Multiplexer truth table

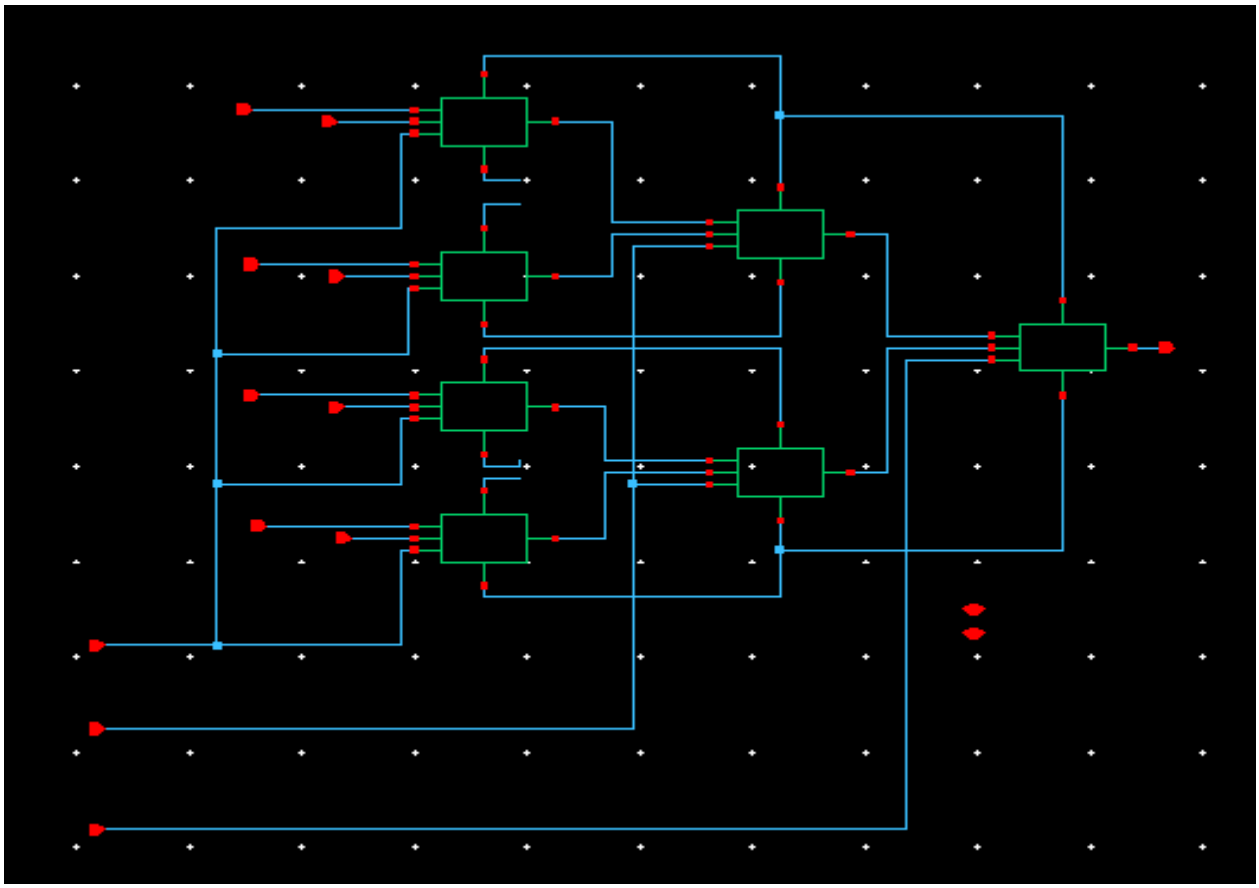
$S / \bar{S}$	D1	D0	Y
0 / 1	X	0	0
0 / 1	X	1	1
1 / 0	0	X	0
1 / 0	1	X	1



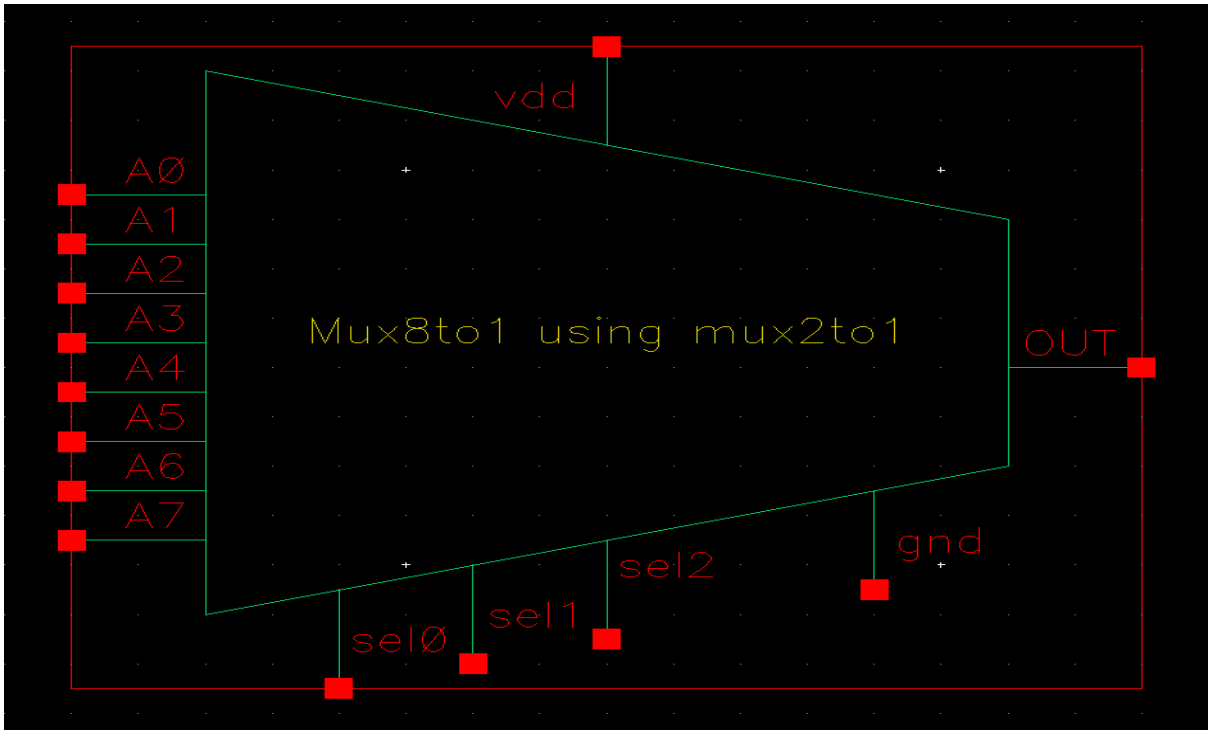
We can convert the above circuit into a symbol



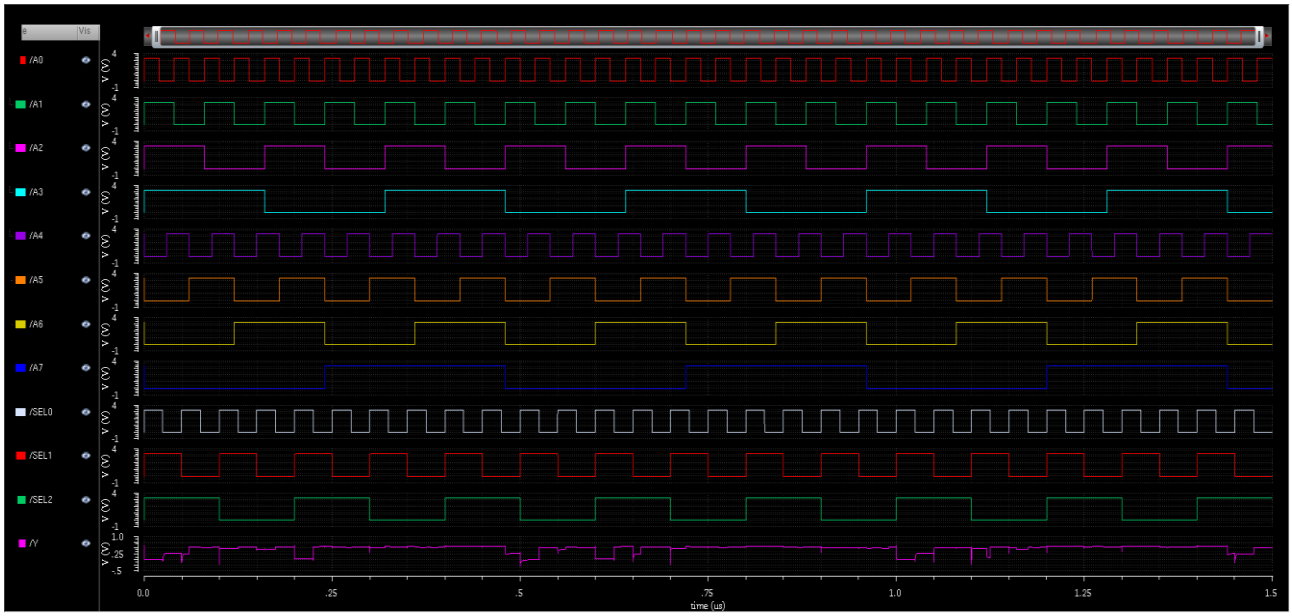
Now, by instantiating we can generate 8:1 MUX.



And when converted into a symbol,



By performing Transient analysis we obtain,

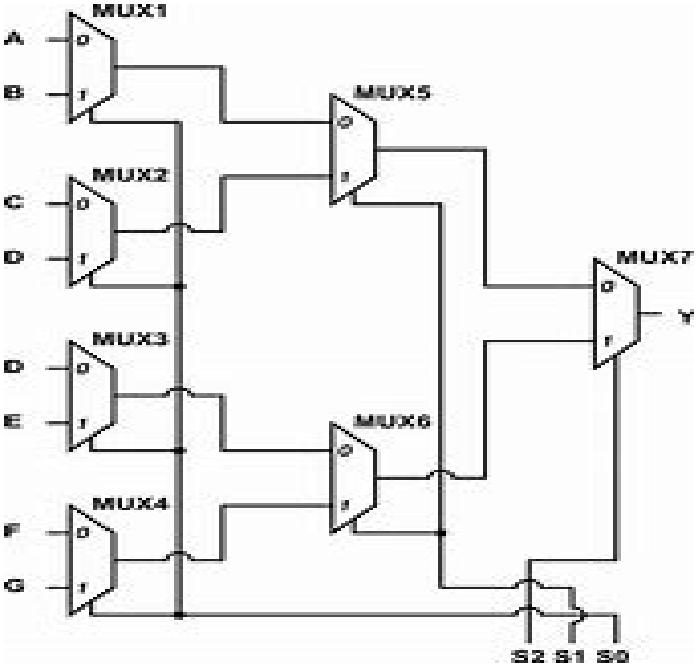


You can observe that they are some impulses that are generated in the output. It is due to transition of multiple inputs at the transition of the select inputs.

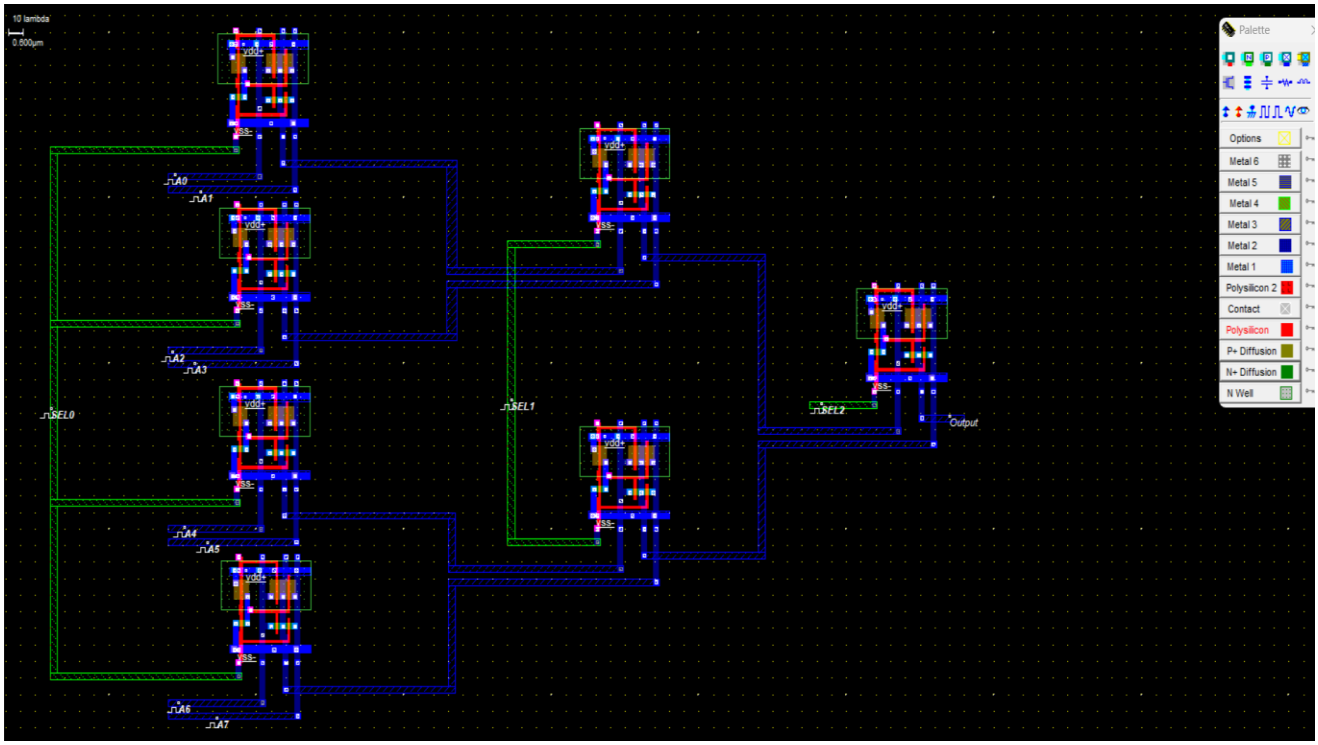
MICROWIND

Microwind provides an integrated environment for designing and simulating digital and analog circuits, including both CMOS and bipolar technologies.

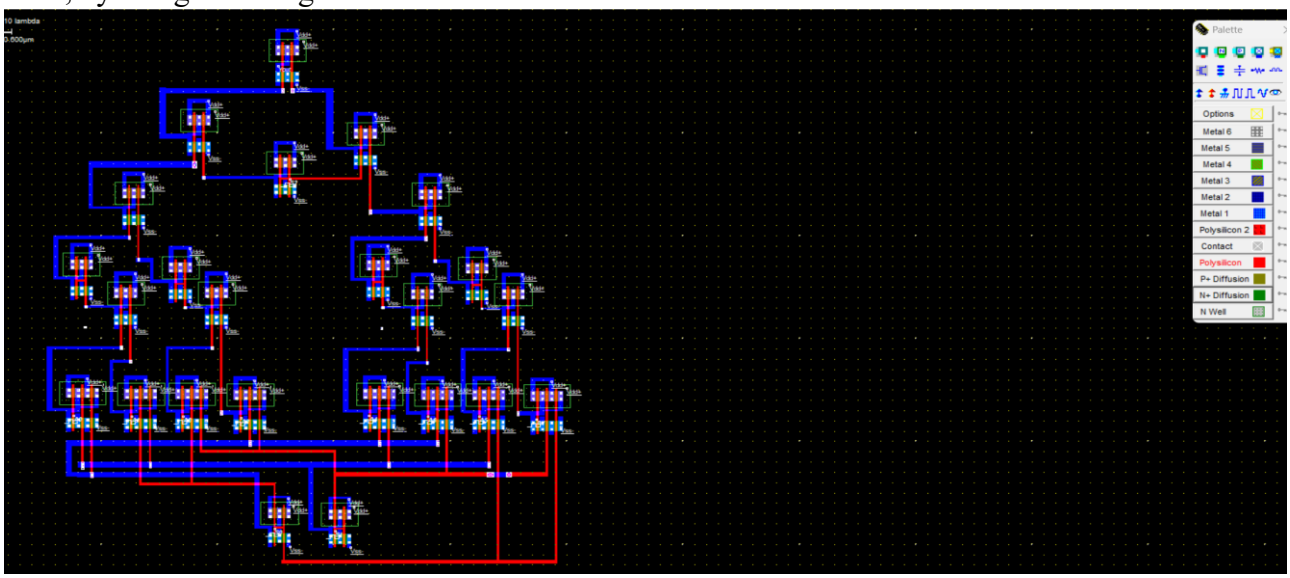
The given multiplexer layout can be generated using the given circuit,



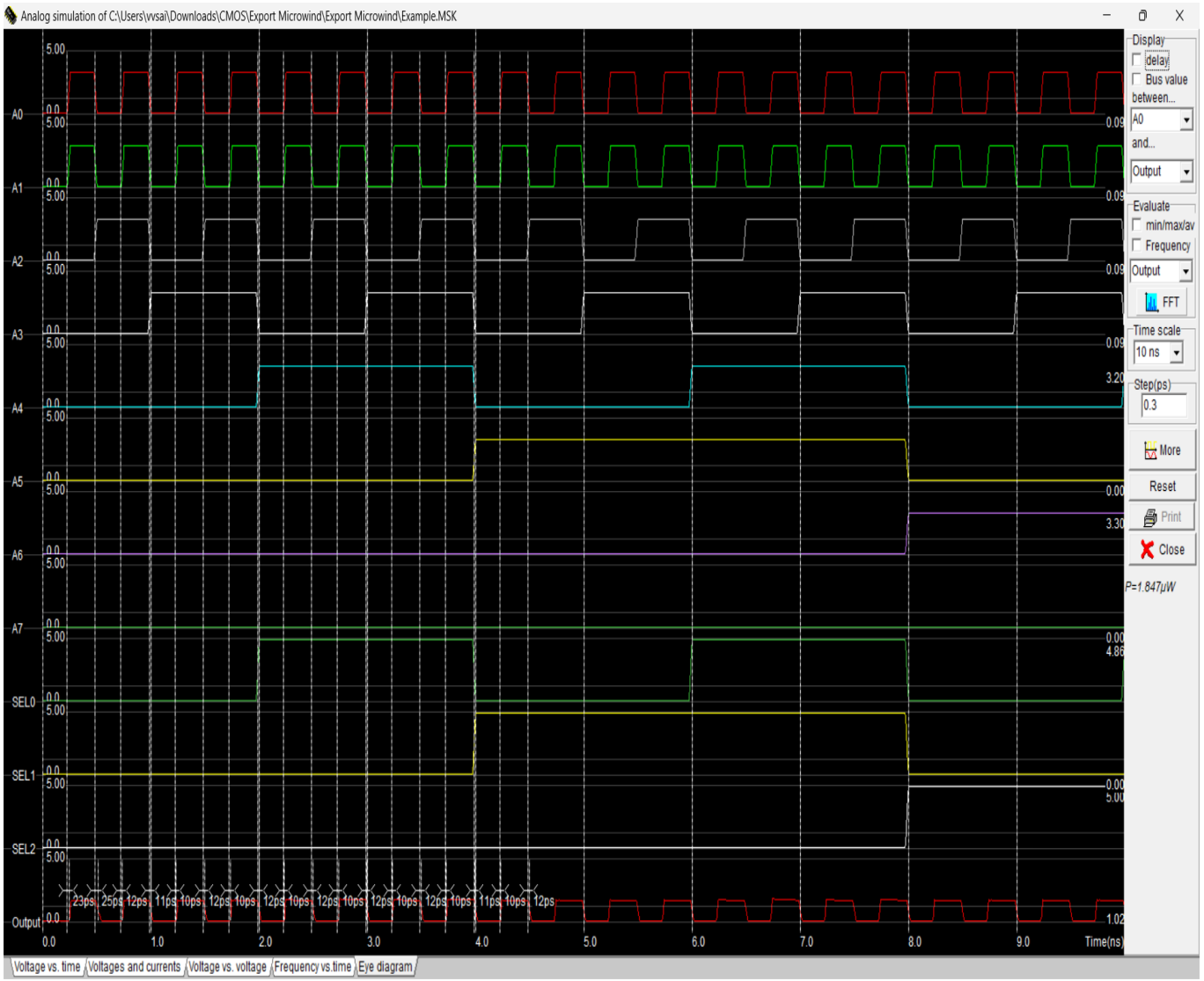
Using 2to1 MUX layout I have generated the 8to1 MUX by satisfying the design rules.



Also, by using NAND gates



The generated output is,

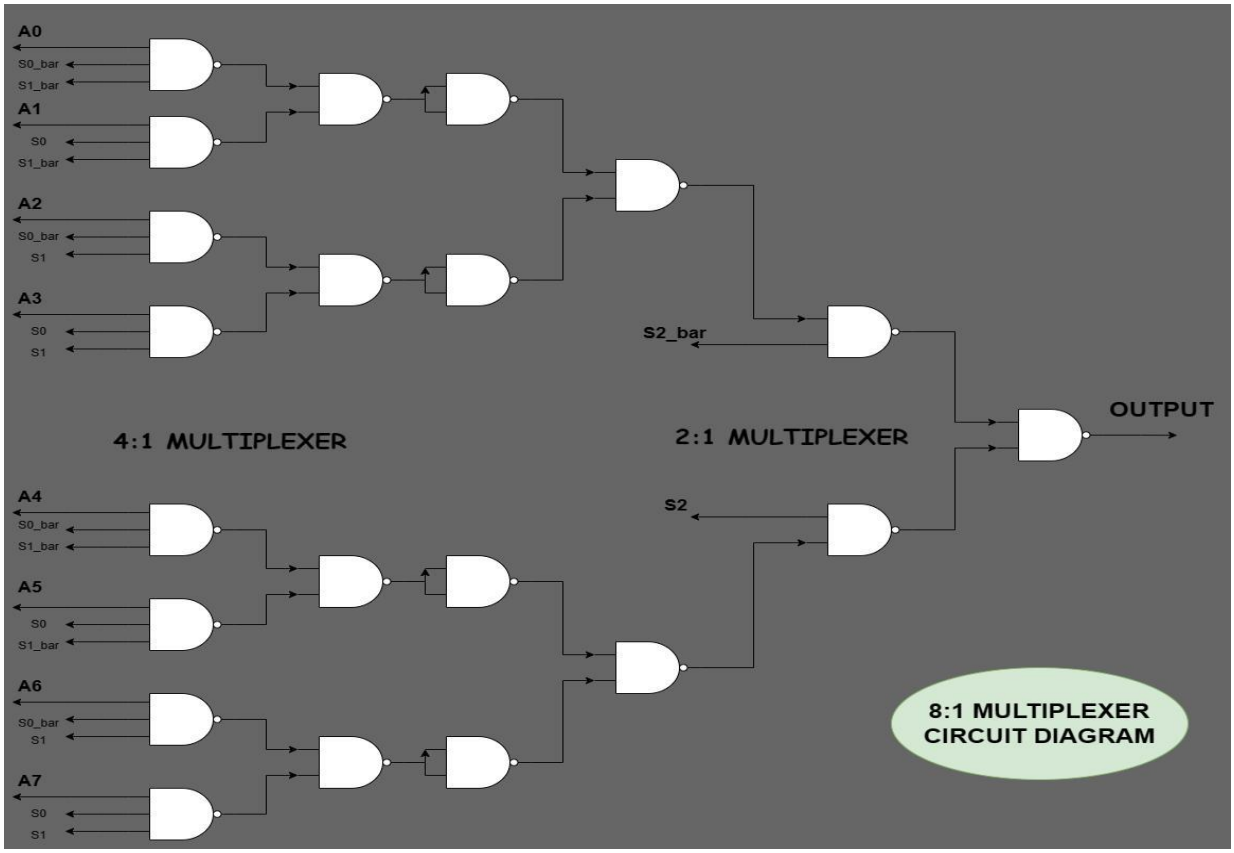


The generated output contains delays. It is due to linear delay model due to RC circuit.

NGspice

NGspice is an open-source circuit simulator, i.e. it is freely available and can be modified as per user requirements or can be integrated into other tools.

The 8:1 MUX is generated using the NAND gates whose circuit diagram is



The Output generated is