

EE619 : VLSI SYSTEM
DESIGN

Course Instructor : Dr. RIK DEY

GROUP NO. 7

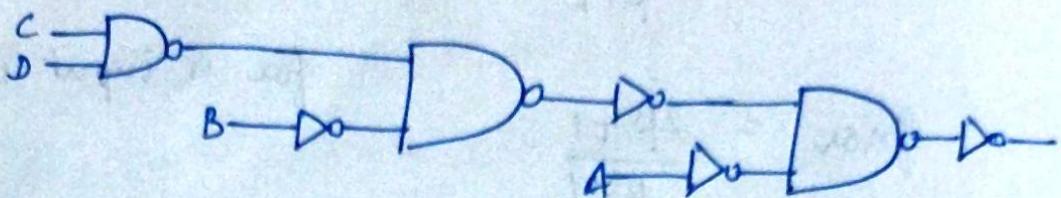
ANANYA → 190126

ADITI → 190055

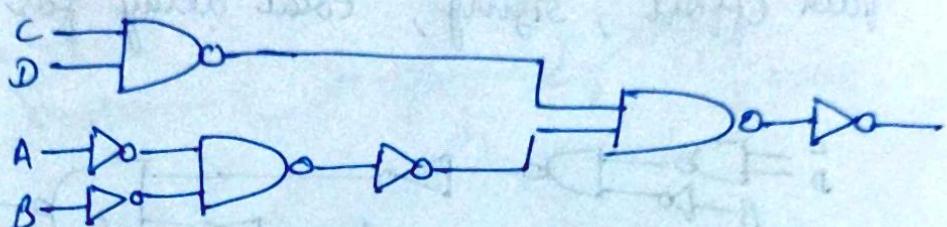
MADIHA FATIMA → 19807465

SAI VEDANT → 210901

① (a) (i)

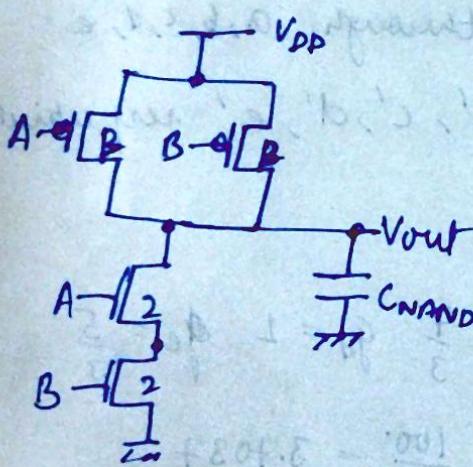


(ii)

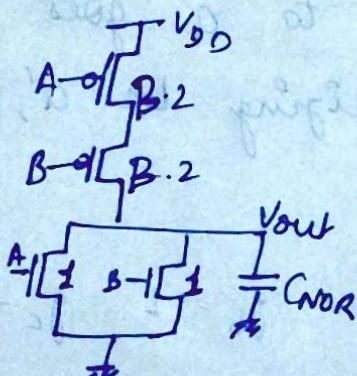


Calculating intrinsic delay & Logic effort

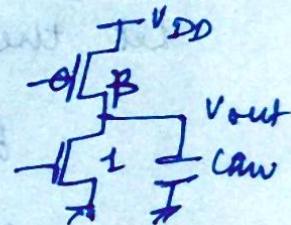
2ip NAND



2ip NOR



inverter



$$P_{inv} = 1$$

$$P = \frac{C_{gate}}{C_{inv}}$$

$$P_{NAND} = \frac{2\beta + 2}{\beta + 1} = 2$$

$$P_{NOR} = \frac{2\beta + 2}{\beta + 1} = 2$$

for n input " " nor
nand $P = n$
 $P = n$

$g = \frac{C_{\text{gate}} \text{ as load}}{C_{\text{inv. as load}}}$

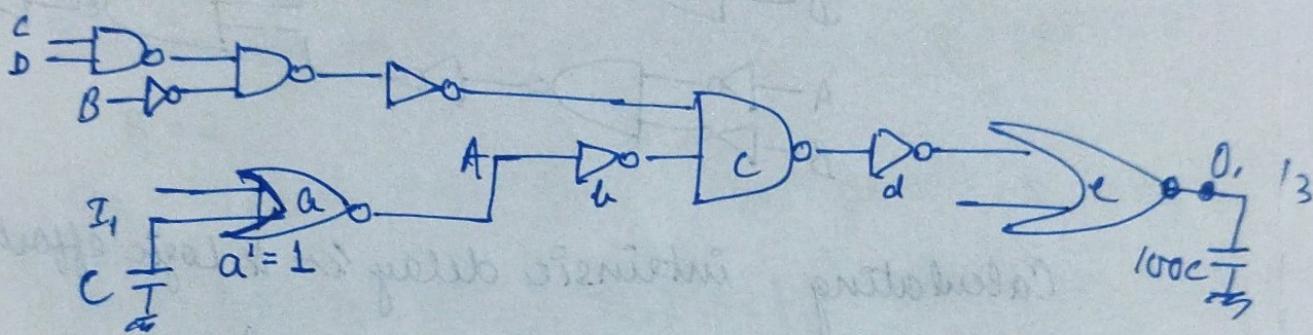
$$g_{\text{NAND}} = \frac{\beta + 2}{\beta + 1}$$

for n input nand $g = \frac{\beta + n}{\beta + 1}$

$$g_{\text{nor}} = \frac{2\beta + 1}{\beta + 1}$$

for n input nor $g = \frac{\beta n + 1}{\beta + 1}$

path effort, sizing, total delay for part (i).



path from I_1 to O_1 goes through a, b, c, d, e
let their sizing be a', b', c', d', e' respectively
 $\beta = 2$

$$g_a = \frac{5}{3} \quad g_b = 1 \quad g_c = \frac{4}{3} \quad g_d = 1 \quad g_e = \frac{5}{3}$$

$$G_1 = g_a g_b g_c g_d g_e = \frac{100}{27} = 3.7037$$

$$\beta = 1$$

$$H = \frac{100c}{c} = 100$$

$$\text{Path Effort} \rightarrow F = G_1 \beta H = \frac{10000}{27} = 370.37$$

$$f_{\text{opt}} = (370.37)^{1/5} = 3.2638$$

(2)

$$f_{opt} = hgb$$

$$f_{opt} = b'/1 * 5/3 * 1 \Rightarrow b' = 1.958$$

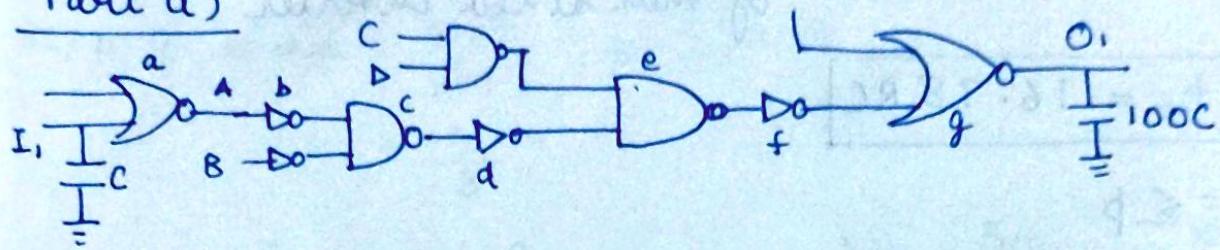
$$f_{opt} = c'/b' * 1 * 1 \Rightarrow c' = 6.391$$

$$f_{opt} = a'/c' * 4/3 * 1 \Rightarrow a' = 15.644$$

$$f_{opt} = e'/d' * 1 * 1 \Rightarrow e' = 51.059$$

$$f_{opt} = \frac{100}{e'} \times \frac{5}{3} = 3.264 \text{ (verified)}$$

Part ii)



Let path from I_1 to O_1 go through a, b, c, d, e, f, g
& their sizing be $a', b', c', d', e', f', g'$ with $a' = 1$

$$\beta = 2$$

$$g_a = 5/3 \quad g_b = g_d = g_f = 1 \quad g_c = g_e = 4/3 \quad g_g = 5/3$$

$$G_1 = \pi g = (5/3)^2 (4/3)^2 \times (1)^3 = 4.9383$$

$$H = \frac{100C}{c} = 100 \quad B = 1$$

$$\text{Path effort } F = G_1 H B = 493.83$$

$$f_{opt} = F^{1/7} = 2.425$$

$$f_{opt} = \frac{5}{3} * 1 * b' \Rightarrow b' = 1.455$$

$$f_{opt} = 1 * 1 * c'/b' \Rightarrow c' = 3.528$$

$$f_{opt} = 4/3 + 1 * d'/c' \Rightarrow d' = 6.416$$

$$f_{opt} = 1 * 1 * e'/d' \Rightarrow e' = 15.559$$

$$f_{opt} = 4/3 + 1 * f'/e' \Rightarrow f' = 28.298$$

$$f_{opt} = 1 * 1 * g'/f' \Rightarrow g' = 68.623$$

$$f_{opt} = 100 * \frac{1}{g'} \times \frac{5}{3} + 1 \quad f_{opt} = 2.428 \text{ (verified!!)}$$

$$\text{i) } P = \sum p = 2p_{\text{NOR}} + 2p_{\text{INV}} + p_{\text{NAND}}$$

$$= 2\{2+1\} + 2\{2+1\} + 2$$

$$P = 8$$

$$t_p = t_{p_0} \{ P + N f_{opt} \}$$

$$= t_{p_0} \{ 8 + 5 \times 3.2638 \}$$

$$\boxed{t_p = 24.319 t_{p_0}}$$

$t_{p_0} = 0.69 R C$ where R & C are resistance & cap. of min sized inverter

$$\boxed{t_p = 16.78 R C}$$

$$\text{ii) } P = \sum p$$

$$= 3p_{\text{INV}} + 2\{p_{\text{NAND}} + p_{\text{NOR}}\}$$

$$= 3 + 2\{2+2\}$$

$$= 11$$

$$t_p = t_{p_0} \{ P + N \times f_{opt} \}$$

$$= t_{p_0} \{ 11 + 7 \times 2.425 \}$$

$$\boxed{t_p = 27.975 t_{p_0}}$$

$t_{p_0} = 0.69 R C$ if R & C are resistance & cap. of min. sized inverter

$$\boxed{t_p = 19.303 R C}$$

$$\text{i) Total Area} = 1 + b' + c' + d' + e'$$

$$= 1 + 1.958 + 6.391 + 15.644 + 51.059$$

$$= \cancel{51.059 \text{ units}} - 76.052 \text{ units}$$

$$\text{ii) Total Area} = 1 + b' + c' + d' + e' + f' + g'$$

$$= 1 + 1.455 + 3.528 + 6.416 + 15.559 + 28.298$$

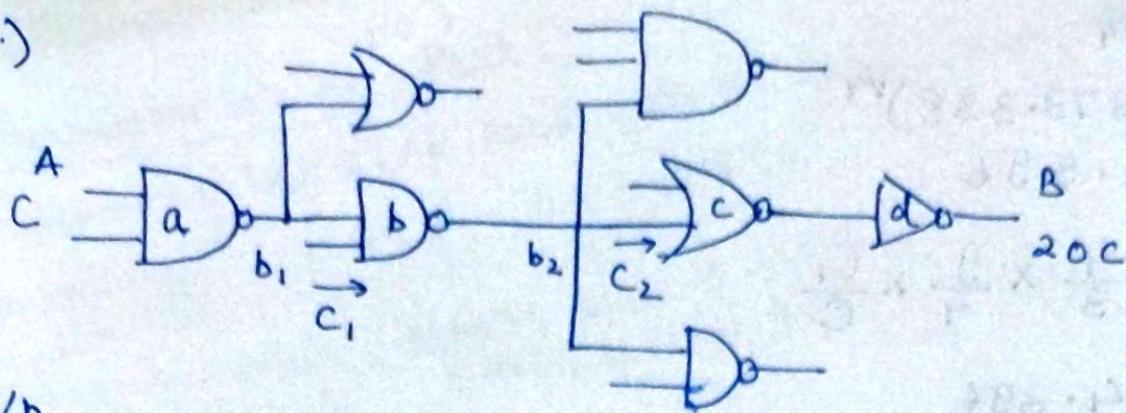
$$+ 68.623$$

$$= 124.879 \text{ units}$$

i) is better implementation in terms of area

b.)

(3)



2i/p

$$g_2 \text{ NAND} = 4/3$$

$$g_2 \text{ NOR} = 5/3$$

3i/p $g_3 \text{ NAND} = \frac{n+\beta}{B+1}$, $\beta=2$, $n=3$

$$= \frac{5}{3}$$

$$b_1 = \frac{g_2 \text{ NAND} + g_2 \text{ NOR}}{g_2 \text{ NAND}} = 1 + \frac{5/3}{4/3} = \frac{9}{4}$$

$$b_2 = \frac{g_2 \text{ NAND} + g_3 \text{ NAND} + g_2 \text{ NOR}}{g_2 \text{ NOR}}$$

$$= \frac{4/3}{5/3} + 1 + 1 = 2 + \frac{4}{5} = \frac{14}{5}$$

$$\boxed{b_1 = 9/4}$$

$$\boxed{b_2 = \frac{14}{5}}$$

Total Path effort $F = GBH$

$$B = 1 * b_1 * b_2 * 1$$

$$= \frac{14}{5} * \frac{9}{4} = 6.3$$

$$\boxed{B = 6.3}$$

$$g_1 = \frac{4}{3} \quad g_2 = \frac{4}{3} \quad g_3 = \frac{5}{3} \quad g_4 = 1$$

$$G_1 = g_1 g_2 g_3 g_4 = \frac{80}{27} \quad \boxed{G_1 = 2.963}$$

$$H = \frac{20C}{C} = 20 \quad \boxed{H = 20}$$

$$\boxed{F = GBH = 373.338}$$

$$f_{opt} = F^{1/4}$$

$$= (373.338)^{1/4}$$

$$= 4.396$$

$$f_{opt} = \frac{4}{3} \times \frac{9}{4} \times \frac{C_1}{C}$$

$$C_1 = \frac{4.396}{3}$$

$$\boxed{C_1 = 1.465 C}$$

$$f_{opt} = \frac{4}{3} \times b_2 \times \frac{C_2}{C_1}$$

$$= \frac{4}{3} \times \frac{14}{5} \times \frac{C_2}{C_1}$$

$$C_2 = 4.396 \times \frac{15}{4 \times 14} \times 1.465 C$$

$$\boxed{C_2 = 1.714 C}$$

$$P = p_1 + p_2 + p_3 + p_4$$

$$= 2 + 2 + 2 + 1 = 7$$

$$\boxed{P = 7}$$

$$t_p = t_{p0} (P + N f_{opt})$$

$$= t_{p0} (7 + 4(4.396))$$

$$= 24.584 t_{p0}$$

$$= 16.963 R C$$

{ when R & C are resistance & capacitance of min-sized inverters }

Sizing: a, b, c, d, a=1

$$f_{opt} = \frac{4}{3} * b_1 * b = \frac{4}{3} \times b_2 * \frac{C}{b} = \frac{5}{3} * 1 * \frac{d}{c}$$

$$\text{Given } b = \frac{C_1}{C} = 1.465 \quad C = 1.714 \quad d = \frac{3}{5} C \times f_{opt}$$

$$= \frac{3}{5} \times 1.714 \times 4.396$$

$$= 4.521$$

Transistor Sizing Part i)

\rightarrow Assuming 1st 2i/p NOR gate as min sized, $\Rightarrow S_1 = 1$

$$\rightarrow b' = \frac{S_2}{\cancel{S_1}} = 1.958 \quad S_2 = 1.958$$

For inverter, NMOS size = 1.958
PMOS size = 3.916

$$\rightarrow C' = S_3 = 6.391$$

for 2i/p NAND NMOS size $\rightarrow 12.782$

$$\text{PMOS} \rightarrow 12.782$$

$$\rightarrow S_4 = 15.644 \quad \text{NMOS} \rightarrow 15.644$$

$$\text{PMOS} \rightarrow 31.288$$

$$\rightarrow S_5 = 51.059 \quad \text{NMOS} \rightarrow 51.059$$

$$\text{PMOS} \rightarrow 204.236$$

1.) a.) Part ii)

\rightarrow Assuming size of 1st stage
2i/p NOR gate as min. sized.

$$\rightarrow S_2 = 1.455 \quad \text{NMOS} \rightarrow 1.455$$

$$\text{PMOS} \rightarrow 2.910$$

$$\rightarrow S_3 = 3.528 \quad \text{NMOS} \rightarrow 7.056$$

$$\text{PMOS} \rightarrow 7.056$$

$$\rightarrow S_4 = 6.416 \quad \text{NMOS} \rightarrow 6.416$$

$$\text{PMOS} \rightarrow 12.832$$

$$\rightarrow S_5 = 15.559 \quad \text{NMOS} \rightarrow 31.118$$

$$\text{PMOS} \rightarrow \cancel{31.118} \quad 31.118$$

$$\rightarrow S_6 = 28.298 \quad \text{NMOS} \rightarrow 28.298$$

$$\text{PMOS} \rightarrow 56.596$$

$$\rightarrow S_7 = \frac{51.059 - 68.626}{68.623} \quad \text{NMOS} \rightarrow 68.623$$

$$\text{PMOS} \rightarrow 274.492$$

1.) b.)

→ Assume 1st 2i/pNAND gate to be min sized. ($NMOS \rightarrow 2$)

$$S_2 = 1.465$$

2i/pNAND →

$$NMOS \rightarrow 1.465 \times 2 = 2.930$$

$$PMOS \rightarrow 2.93$$

$$S_3 = 1.714$$

$$NOR: NMOS \rightarrow 1.714$$

$$PMOS \rightarrow 4 \times 1.714$$

$$= 6.856$$

$$S_4 = \frac{4.521}{5} d = 4.521 \text{ M}^4 \quad NMOS \rightarrow 4.521$$

$$PMOS \rightarrow 9.042$$

$224.1 \leftarrow 20M1$

$0.18.2 \leftarrow 20M9$

$320.5 \leftarrow 20M1$

$320.5 \leftarrow 20M9$

$818.2 \leftarrow 20M1$

$588.31 \leftarrow 20M9$

$24.10 \leftarrow 20M1$

$24.10 \leftarrow 20M9$

$24.10 \leftarrow 20M1$

$24.10 \leftarrow 20M9$

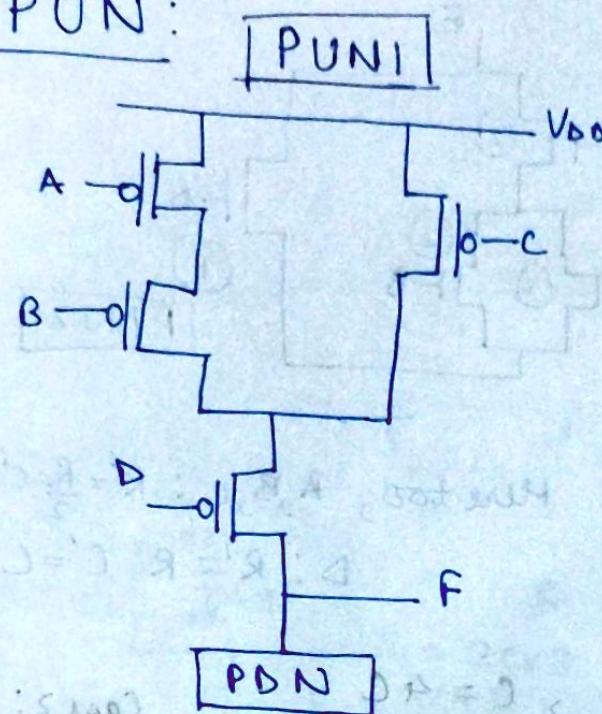
$24.10 \leftarrow 20M1$

$24.10 \leftarrow 20M9$

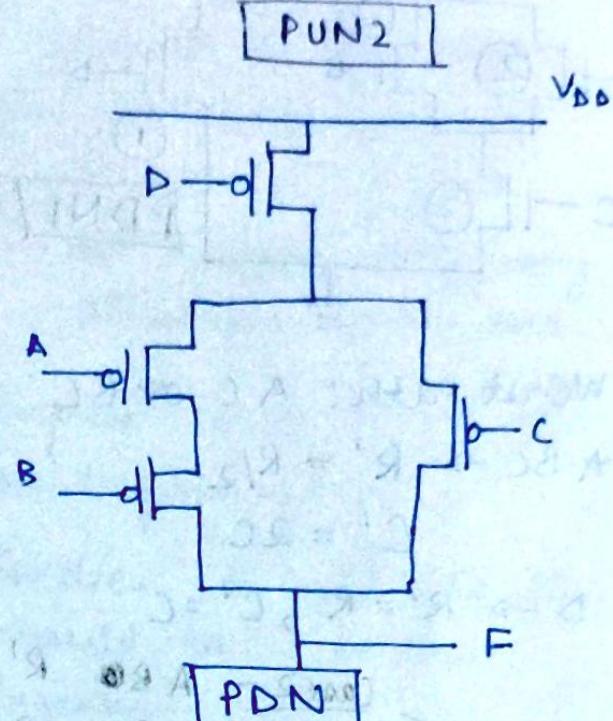
$$2 \cdot a) F = [(A+B)C + D']$$

(5)

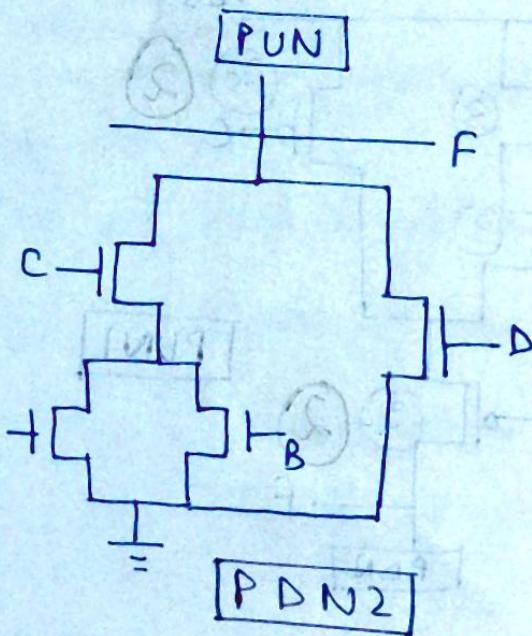
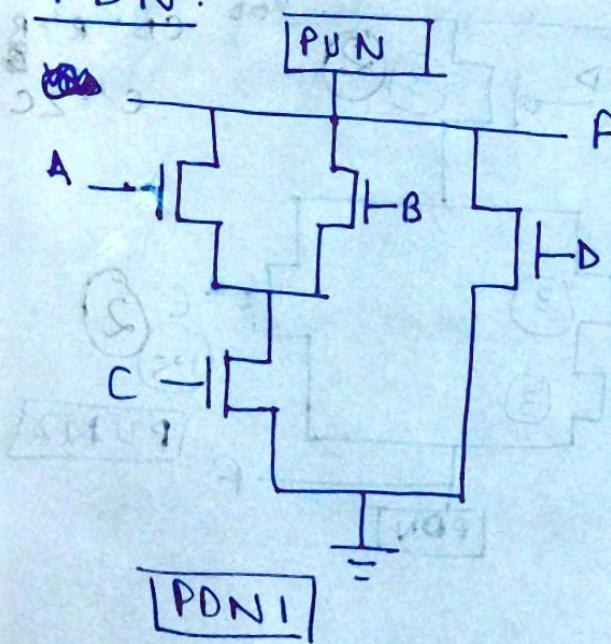
PUN:



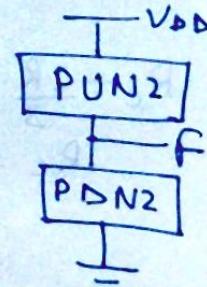
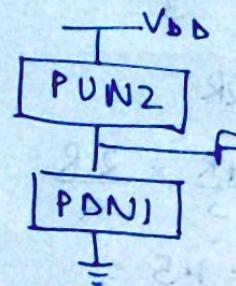
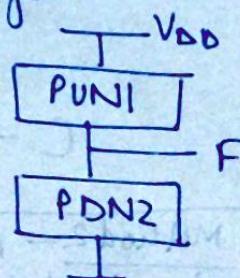
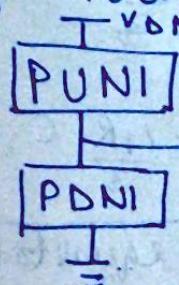
PUN2



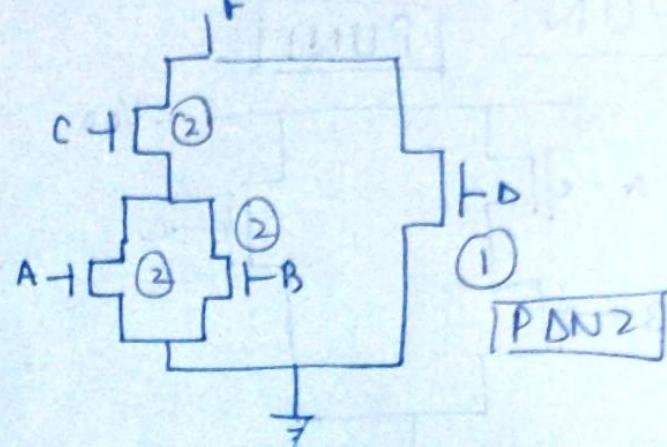
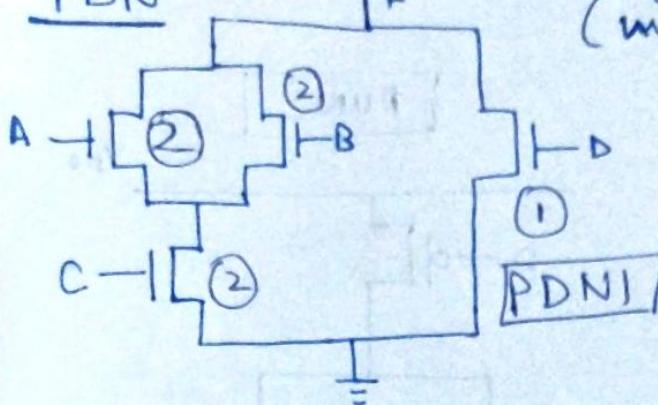
PDN:



4 possible topologies



b.) Worst Case Time Delay = Time delay of min-sized inverter (marked in blue).



Worst Path: A-C or B-C

$$A-B-C \rightarrow R' = R/2$$

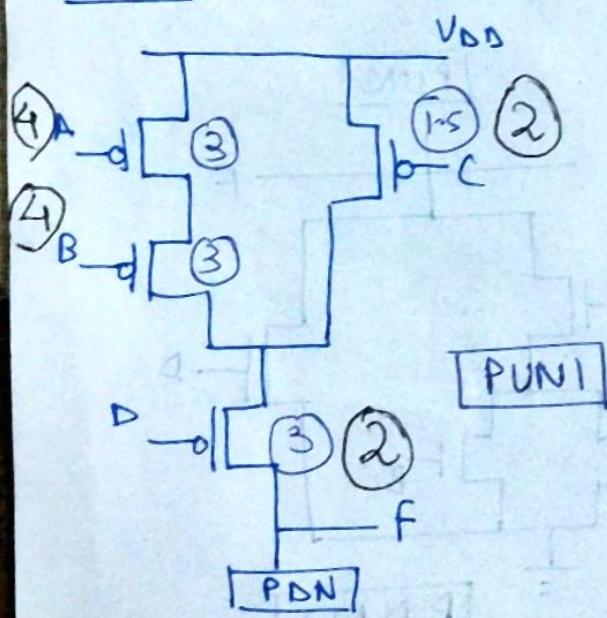
$$C' = 2C$$

$$D \rightarrow R' = R, C' = C$$

$$\text{Here too, } A, B, C : R' = \frac{R}{2}, C' = 2C$$

$$D : R' = R, C' = C$$

PUN — Case 2 - A-B-D $R' = R/2 \rightarrow C = 4C$
C-D $R' = R \rightarrow C = 2C$



Worst Path A-B-D

$$A-B-D \rightarrow R' = \frac{2R}{3}, C' = 3C$$

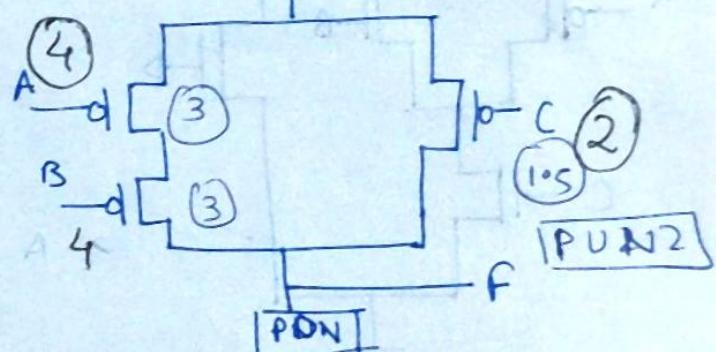
$$R_c + \frac{2R}{3} = 2R$$

$$R_c = \frac{4R}{3} = \frac{2R}{K}$$

$$K = 1.5$$

$$C \rightarrow R' = \frac{4R}{3}, C' = 1.5C$$

Case 2:
A-B $R' = R/2, C' = 4C$
C-D $R' = R, C' = 2C$



Here too,

$$A-B-D : R' = \frac{2R}{3}, C' = 3C$$

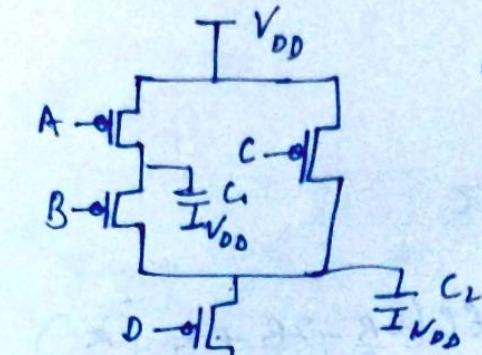
$$C \rightarrow R' = \frac{4R}{3}, C' = 1.5C$$

Method 2 - All sizes equal to that of min sized transistors.

Each PMOS $\rightarrow 2R, C$

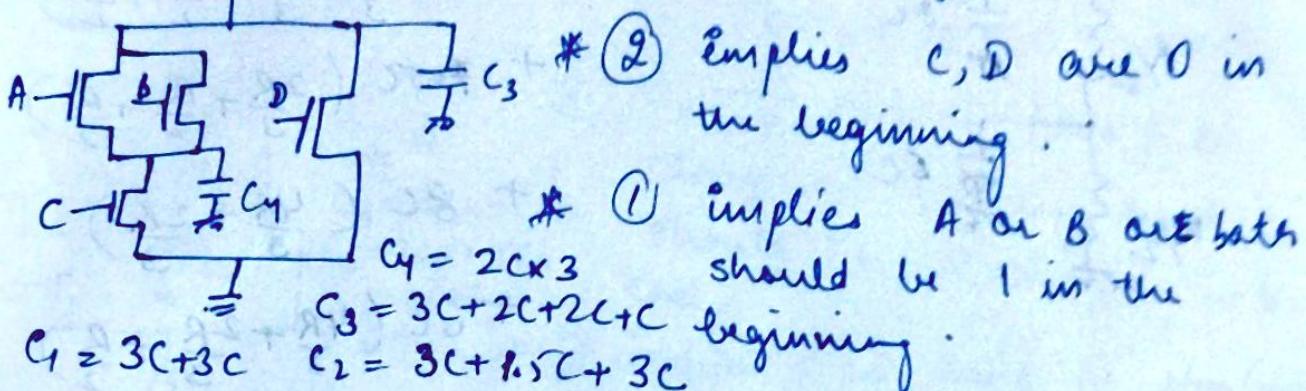
Each NMOS $\rightarrow R, C$

Output goes from high to low SIZING ⑥
topology 2 when output goes from high to low.
 for worst case delay



① C_1, C_2 should be discharged at beginning and charged in the end.

② $C_3, C_4 \rightarrow$ charged in beginning discharged in the end.



~~finally C_3 should be discharged~~ \Rightarrow implies that we should change either change C to 1 or D to 1

If we change D to 1 PUN gets disconnected from output. So we will change C to 1.

\ast Now if we keep B at 1 C_1 will not be able to get charged. so we will keep it at 0.

So input are as follows :-

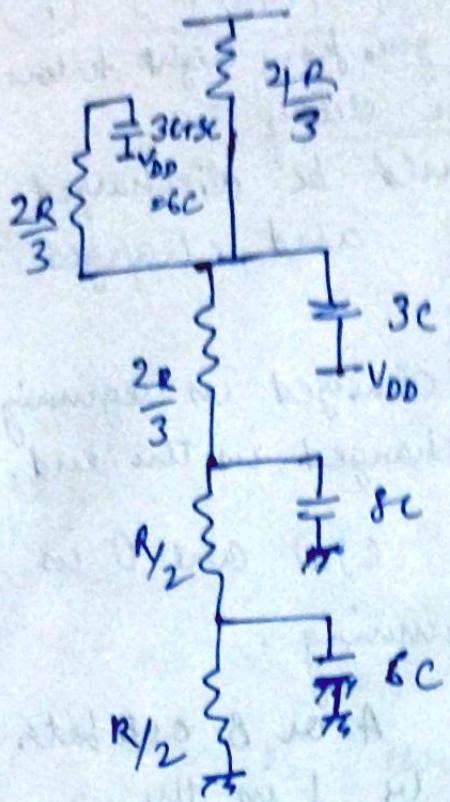
$$A = 1$$

$$B = 0$$

$$C = 0 \rightarrow 1$$

$$D = 0$$

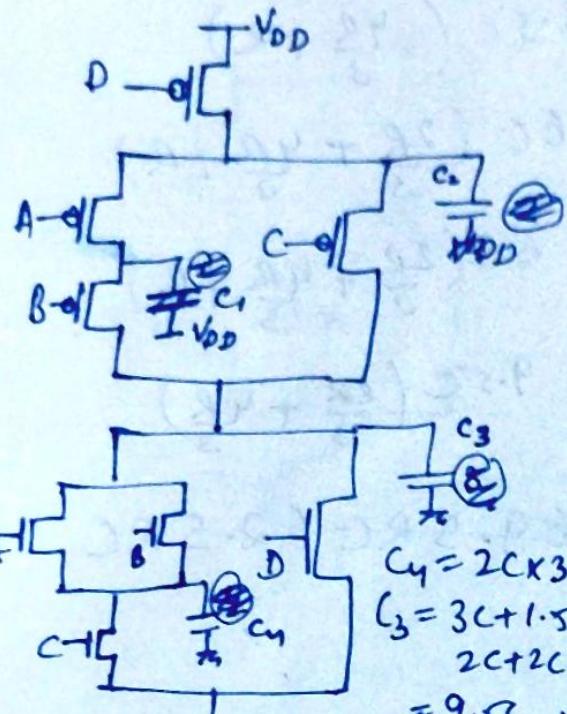
This combination is satisfying ① and ② through longest path possible.



$$\begin{aligned}
 t = & 6C \left(\frac{2R}{3} + \frac{2R}{3} + \frac{R}{2} + \frac{R}{2} \right) \\
 & + 7.5C \left(\frac{2R}{3} + \frac{R}{2} + \frac{R}{2} \right) \\
 & + 8C \left(\frac{4R}{3} + \frac{2R}{3} \right) \\
 & + 6C \left(\frac{4R}{3} + \frac{2R}{3} + \frac{R}{2} \right)
 \end{aligned}$$

$$\begin{aligned}
 t = & \frac{42RC}{3} + \frac{75RC}{6} + 16RC \\
 & + 15RC \\
 & - 57.5RC
 \end{aligned}$$

Topology 2



when output goes from high to low
for worst case delay

① ~~M1~~

① C_1, C_2 should have no charge in beginning & should be charged ~~for~~ in the end.

②

② C_3, C_4 should have full charge in beginning and should be discharged in the end.

$$C_1 = 3C + 3C = 6C$$

$$C_2 = 3C + 3C + 1.5C = 7.5C$$

$$\begin{aligned} C_3 &= 2C \times 3 = 6C \\ C_4 &= 3C + 1.5C + 2C + 2C + C \\ &= 9.5C \end{aligned}$$

* ① implies A, D are 0 in starting
* ② implies A or B or both should be 1 in starting.

* C_2 should be charged in the end so B should be 1 in the end.

* to charge C_1 through longest path B should be ~~0~~ 1, $A = 0$

so

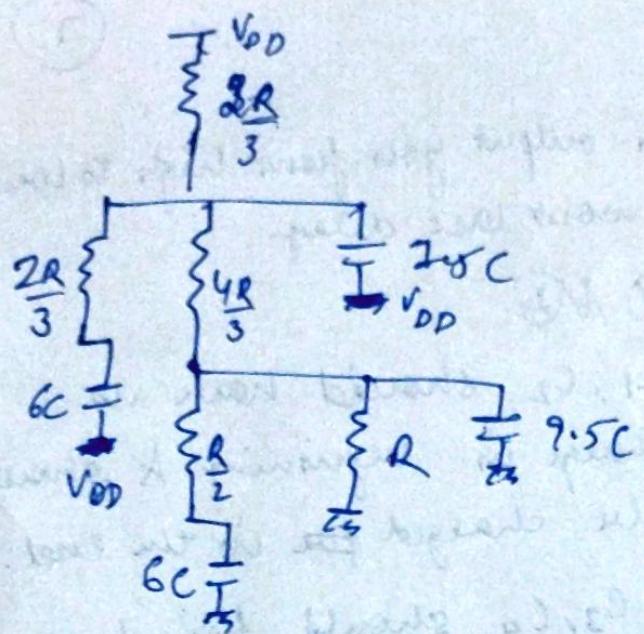
$$A = 0$$

$$B = 1$$

$$C = 0$$

$$D = 0 \rightarrow 1$$

this combination changes or discharges respective capacitors through longest paths.

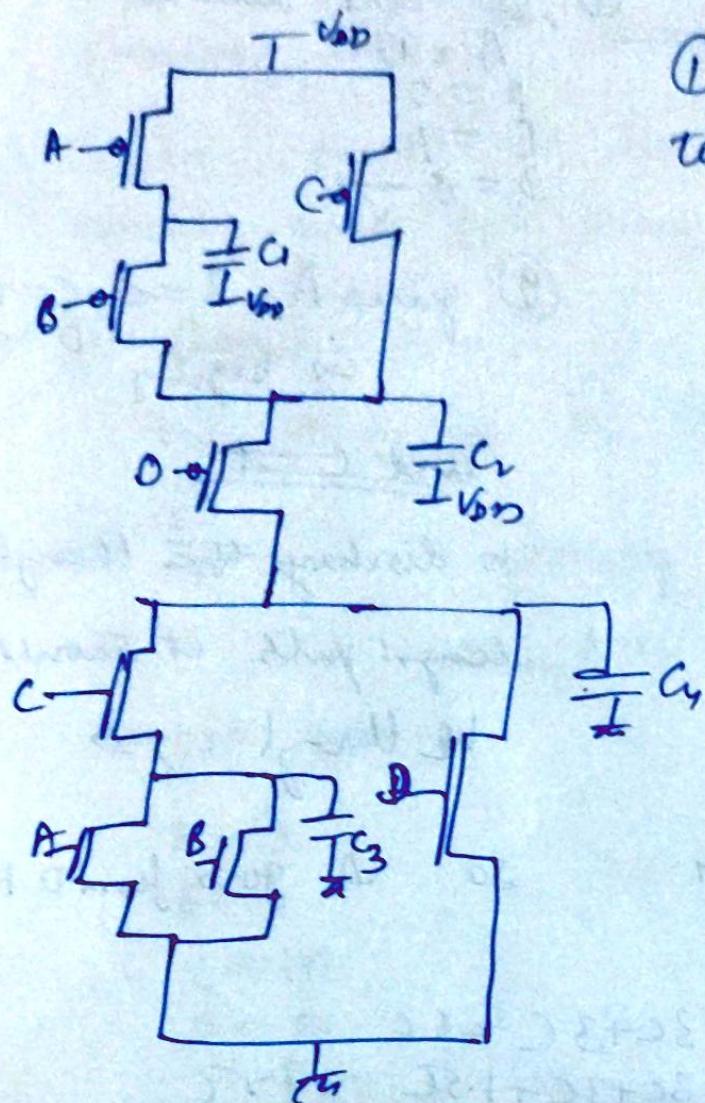


$$\begin{aligned}
 T &= 7.5C \left(\frac{4R}{3} + R \right) \\
 &+ 6C \left(\frac{2R}{3} + \frac{4R}{3} + R \right) \\
 &+ 6C \left(\frac{2R}{3} + \frac{4R}{3} + \frac{R}{2} \right) \\
 &+ 9.5C \left(\frac{2R}{3} + \frac{4R}{3} \right) \\
 &= \cancel{69.5RC} - 62.5RC
 \end{aligned}$$

topology 3

for worst case time delay

(8)



① + ② are same as topology ① & ②

$$D = 0$$

$$C_1 = 3C + 3C =$$

$$B = 0$$

$$A = 0 \rightarrow 1$$

$$C_2 = 3C + 1.5 = 7$$

$$C = 1$$

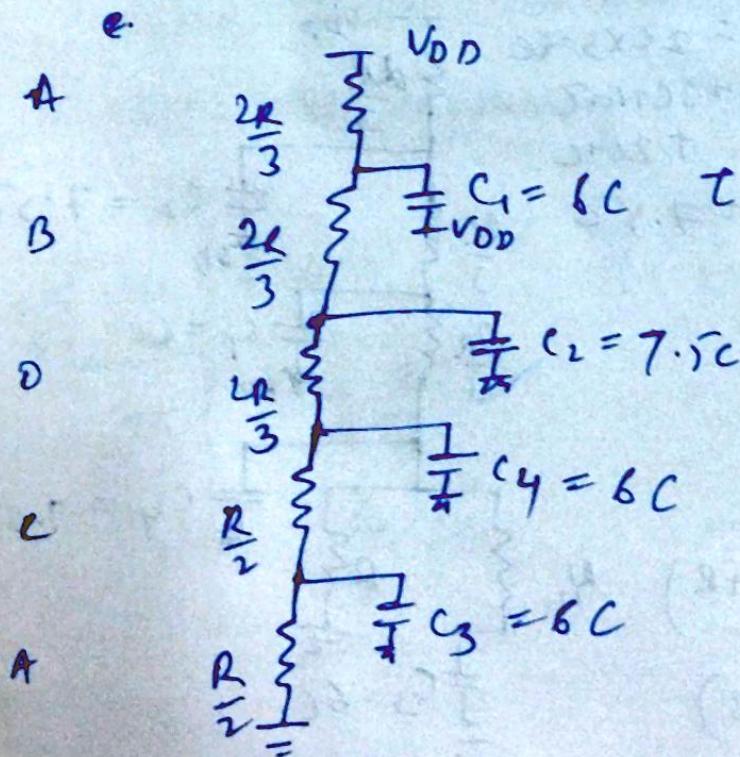
$$C_3 = 2C + 3 = 6$$

$$C_4 = 3C + 2C =$$

② gives $D, A, B = 0$ in beginning.

wence $C = 1$ to keep C_3 charged in begining

A is changed to $\bar{1}$ to disconnect supply and to connect to ground.



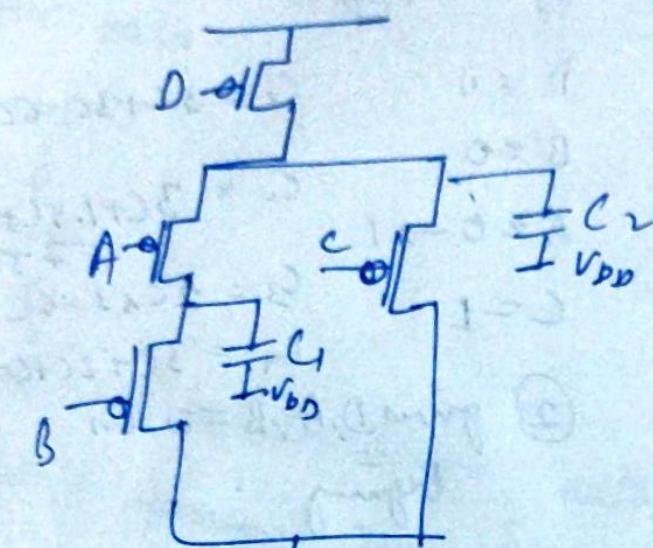
$$\begin{aligned} C_1 &= 6C & T &= 6C\left(\frac{2R}{3} + \frac{2R}{3} + \frac{R}{2} + \frac{R}{2}\right) \\ & & &+ 7.5C\left(\frac{2R}{3} + \frac{R}{2} + \frac{R}{2}\right) \\ C_2 &= 7.5C & &+ 6C\left(\frac{2R}{3} + \frac{2R}{3} + \frac{2R}{3}\right) \\ & & &+ 6C\left(\frac{2R}{3} + \frac{2R}{3} + \frac{2R}{3} + \frac{R}{2}\right) \\ C_3 &= 6C & &= 53.5 RL \\ C_4 &= 6C & & \end{aligned}$$

topology 4

for want can delay
topology 1 (1), 2.

①, ② can same as 1

$$\begin{aligned} A &= 0 \\ B &= 0 \\ C &= 1 \\ D &= 0 \rightarrow 1 \end{aligned}$$

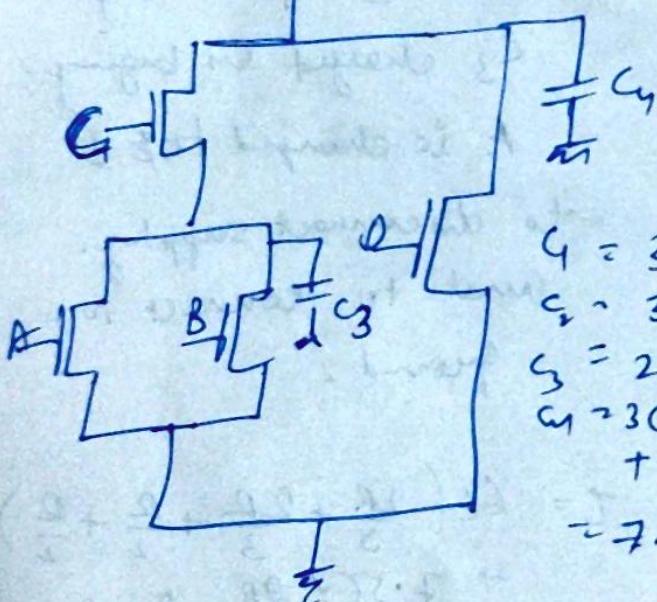


③ gives $A, B = 0, C = 1$
in begin $D = 0$

and C = 1

to discharge ~~C₂~~ through
longest path it should
be through C, D

so D goes from 0 to 1



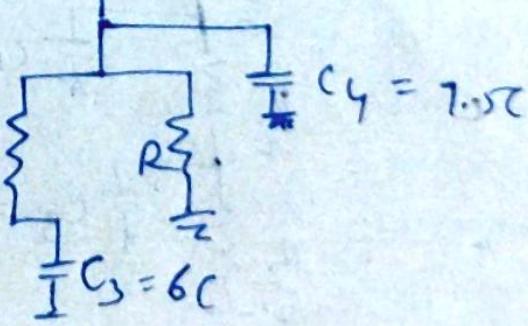
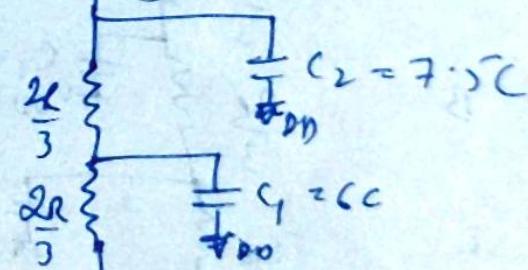
$$G = 3C + 3C = 6C$$

$$C_1 = 3C + 3C + 1.5C = 7.5C$$

$$C_3 = 2C \times 3 = 6C$$

$$\begin{aligned} C_4 &= 3C + 1.5C \\ &\quad + 2C + C \\ &= 7.5C \end{aligned}$$

$$\begin{aligned} &\text{V}_{BD} \\ &\frac{dR}{3} \end{aligned}$$



$$t = 6C \left(\frac{2}{3}R + R \right)$$

$$+ 7.5C \left(2\frac{R}{3} + 2\frac{R}{3} + R \right)$$

$$+ 6C \left(\frac{R}{2} + 2\frac{R}{3} \times 3 \right)$$

$$+ 7.5C \left(\frac{2}{3}R \times 3 \right) = 57.5Rt$$

When output is going from 0 to 1

(g)

topology 1 for worst case delay,-

① C_1, C_2 should be having full charge in starting and 0 charge in end.

② C_3, C_4 should be having zero charge in starting and full charge in the end.

* ① implies $A = 1 \quad B = 0 \quad C = 1 \quad D = 0$ satisfy this condition of beginning.

② for ② to satisfy C should go to zero.
 $A = 1$ also allows C to get discharged through longest path.

$$A = 1$$

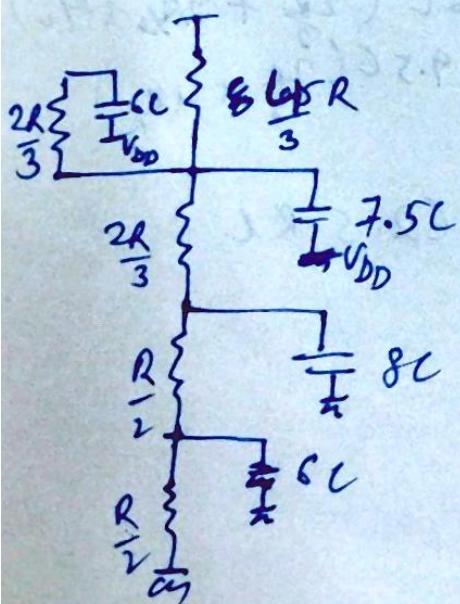
$$B = 0$$

$$C = 1 \rightarrow 0$$

$$D = 0$$

these input combinations satisfy ① & ②.

they are happening through longest paths -



$$\begin{aligned} T &= 6C \left(\frac{2R}{3} + \frac{2R}{3} + \frac{R}{2} + \frac{R}{2} \right) \\ &\quad + 7.5C \left(\frac{2R}{3} + \frac{R}{2} + \frac{R}{2} \right) \\ &\quad + 8C \left(\frac{R}{2} + \frac{R}{2} \right) \\ &\quad + 6C \left(\frac{R}{2} + \frac{2R}{3} + \frac{R}{2} \right) \\ &= 57.5RC \end{aligned}$$

Topology 2

for worst case delay

① and ② are same as that for topology 1.
we have 2 cases

$$A = 0$$

$$B = 1$$

$$C = 0$$

$$D = 1 \rightarrow 0$$

I

$$A = 0$$

$$B = 1$$

$$C = 1 \rightarrow 0$$

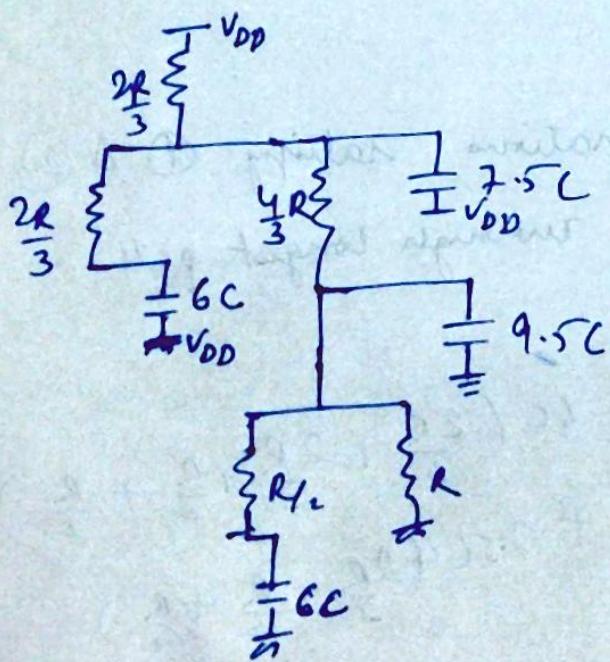
$$D = 0$$

II

in II will ① be not followed, but
things

in I discharging/charging is not done by longest
path but all the capacitors are getting
charged or discharged

so this gives worst case delay.



$$\tau = 7.5C \left(\frac{4R}{3} + R \right)$$

$$+ 6C \left(\frac{2R}{3} + 4R_3 + R \right)$$

$$+ 6C \left(\frac{2R}{3} + 4R_{12} + R_1 \right) + 9.5C \left(\frac{2R}{3} + 4R_3 \right)$$

$$= 62.5RC$$

Topology 3

input will be of similar patterns as that while going from high to low only difference is at the ~~only~~ input that was changing from 0 to 1 will now change from 1 to 0.

$$\begin{aligned} A &= 1 \text{ to } 0 \\ B &= 0 \\ C &= 1 \\ D &= 0 \end{aligned}$$

time constant will be same as there.

$$\tau = 53.5 R C$$

Topology 4

Using same argument as that in Topology 3

$$\begin{aligned} A &= 0 \\ B &= 0 \\ C &= 1 \\ D &= 1 \rightarrow 0 \end{aligned}$$

and same ^{w.c.} time constant as in case of output going from 1 to 0

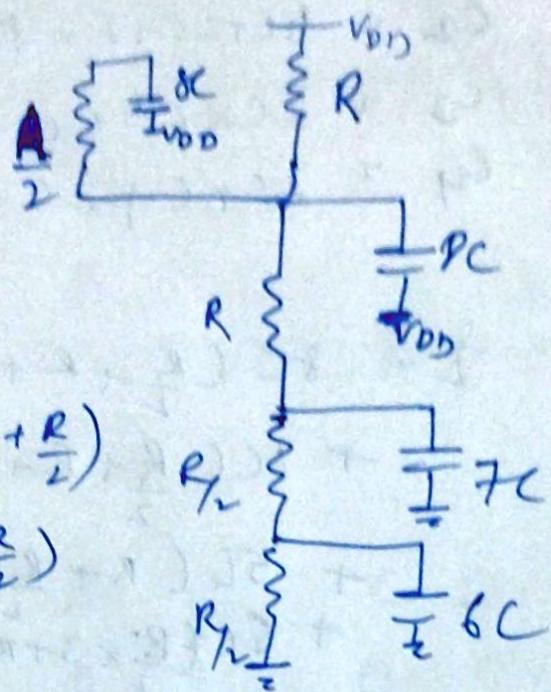
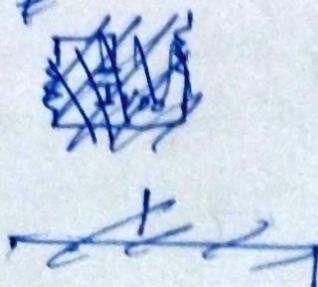
$$\tau = 57.5 R C$$

for Sizing 2

$s/p \rightarrow l^+ l^-$, w.c. delay ~~top~~

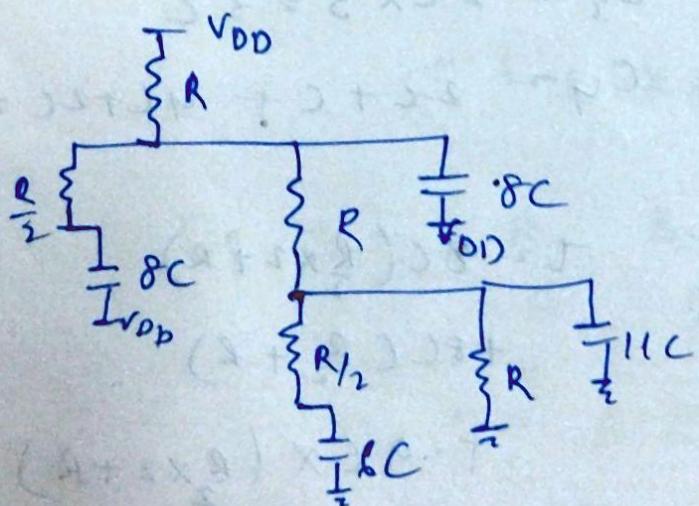
(11)

$$\text{top.1} \quad A = 1 \quad B = 0 \quad C = 0 \rightarrow \cancel{\text{D}} \quad D = 0$$



$$\begin{aligned}
 T &= \frac{RC}{2} \left(R + \frac{R}{2} + \frac{R}{2} + \frac{R}{2} \right) \\
 &\quad + 8C \left(R + \frac{R}{2} + \frac{R}{2} \right) \\
 &\quad + 7C(R+R) \\
 &\quad + 6C \left(R + R + \frac{R}{2} \right) \\
 &= 20RC + 16CR + 14C + 15C = 65RC
 \end{aligned}$$

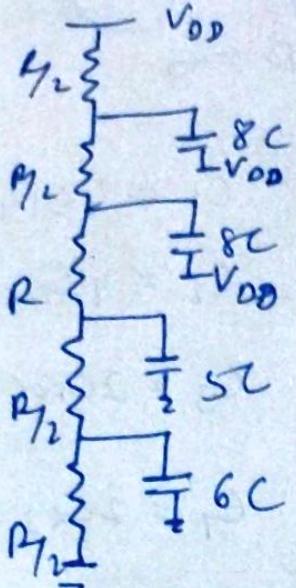
$$\underline{\text{top.2}} \quad A = 0 \quad B = 1 \quad C = 0 \quad D = 0 \rightarrow 1$$



$$\begin{aligned}C_1 &= 4c + 4c = 8c \\C_2 &= 4c + 2c + 2c = 8c \\C_3 &= 4c + 2c + 2c + 2c + c \\&= 11c \\C_4 &= 2c \times 3 = 6c\end{aligned}$$

$$\begin{aligned}
 T &= 8C\left(\frac{R}{2} + R + R\right) + 8C(R + R) \\
 &\quad + 6C\left(\frac{R}{2} + R + R\right) + 11C(2R) \\
 &= 35RC + 16RC + 22RC \\
 &= 73RC
 \end{aligned}$$

topology 3



$$D=0 \quad B=0 \quad A=0 \rightarrow 1 \quad C=1$$

$$C_1 = 4C + 4C = 8C$$

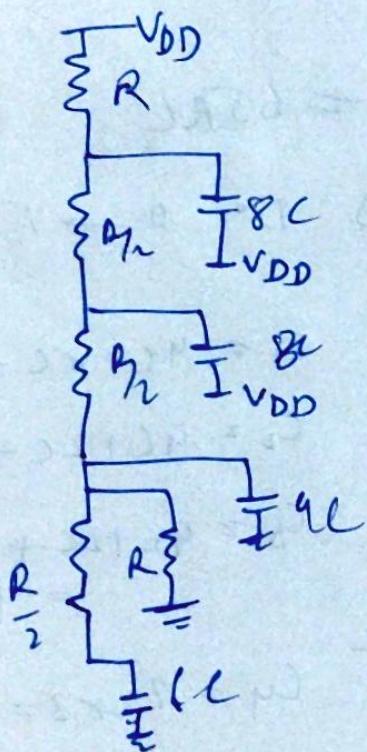
$$C_2 = 4C + 2C + 2 = 8C$$

$$C_3 = 2C \times 3 = 6C$$

$$C_4 = 2C + C + 2C = 5C$$

$$\begin{aligned} T &= 8C \left(\frac{R}{2} + R + \frac{R}{2} + R \right) \\ &+ 8C \left(\frac{R}{2} + R + \frac{R}{2} \right) \\ &+ 5C \left(R + \frac{R}{2} + R/2 \right) \\ &+ 6C \left(\frac{R}{2} \times 3 + R \right) = 15C + 20C + 14C \\ &+ 10C = 61RC \end{aligned}$$

topology 4



$$A=0 \quad B=0 \quad C=1 \quad D=0 \rightarrow 1$$

$$C_1 = 4C + 4C = 8C$$

$$C_2 = 2C + 2C + 4C = 8C$$

$$C_3 = 2C \times 3 = 6C$$

$$C_4 = 2C + C + 4C + 2C = 9C$$

$$T = 8C \left(\frac{R}{2} \times 2 + R \right)$$

$$+ 8C \left(\frac{R}{2} + R \right)$$

$$+ 9C \times \left(\frac{R}{2} \times 2 + R \right)$$

$$+ 8C \left(\frac{R}{2} \times 3 + R \right)$$

$$= 16C + 12C + 18C + 15C$$

$$= 61RC$$

When O/P is going from 0 → 1

(12)

Topologies
Input will be of similar pattern as that while output going from high to low. Only difference is the input that was changing from 0 → 1 will now change from 1 to 0.

so Top 1 :- A B C D
 1 0 1 → 0 0

$$t = 6 \tau_{RL}$$

Top 2 :- A B C D
 0 1 0 0 → 1

$$t = 7 \tau_{RL}$$

Top 3 :- A B C D
 1 → 0 0 1 0

$$t = 6 \tau_{RL}$$

Top 4 :- A B C D
 0 0 1 1 → 0

$$t = 6 \tau_{RL}$$

d.) Best case time delay : high to low trans of S/P

last

→ PUNI & PDNI

Sizing of PMDS - worst case (in blue) {Case 1}

$$\begin{array}{l} ABCD \\ 0010 \end{array} \longrightarrow \begin{array}{l} ABCD \\ 0011 \end{array}$$
$$C = 11RC$$

$$\begin{array}{l} ABCD \\ 1100 \rightarrow 1110 \end{array}$$
$$T = \cancel{R} \cancel{C} 3RC + 3R \times \frac{11}{4} C$$
$$= \frac{25RC}{4}$$

$$\frac{45RC}{4} > 11RC$$

⇒ Best case delay = 11RC for i/p trans.

$$0010 \rightarrow 0011$$

→ PUNI & PDNI : high to low trans of S/P.

$$ABCD : 1100 \rightarrow 1110$$

$$\begin{array}{c} R/2 \times 2 \\ \parallel \\ 2 \times R/2 \\ \parallel \\ R/2 \times 2 \end{array} \quad \frac{1}{2} 12C \quad \frac{R}{4} + \frac{R}{2} = \frac{3R}{4}$$
$$C = 12C \times \frac{3R}{4} = 9RC$$
$$\boxed{C = 9RC}$$

→ PUNI & PDNI — Best case delay
low to high trans of S/P

$$ABCD : 0001 \rightarrow 0000$$

$$\begin{array}{c} 2 \times 2 \times \frac{2}{6} \\ \parallel \\ 2 \times \frac{2}{6} \\ \parallel \\ 2 \times 2 \times \frac{2}{6} \end{array} \quad \left\{ \begin{array}{l} 2R/3 \times 2 \\ 2R/3 \times 2 \end{array} \right\} \quad \text{Req} = \frac{4R}{3}$$
$$\frac{1}{2} 11C \quad T = \frac{22RC}{3}$$

PUN2 & PDN2 O/p : 0 → 1

ABCD : 1110 → 1100

$$C = 2 \times 6RC \times \left(\frac{R}{2}\right) = 12RC$$

Case 2 → sizing shown in black
(4, 4, 2, 2)

→ PUN1 & PDN1 O/p : 0 → 0

ABCD : 0010 → 0010

$$\boxed{C = 9RC}$$

→ PUN2 & PDN2 : O/p 1 → 0

ABCD : 1100 → 1110

$$\boxed{C = \frac{45}{4}RC}$$

→ PUN1 & PDN1 O/p : 0 → 1

ABCD : 0001 → 0000

$$\boxed{C = \frac{27}{4}RC}$$

→ PUN2 & PDN2 O/p : 0 → 1

ABCD : 1110 → 1100

$$\boxed{C = 15RC}$$