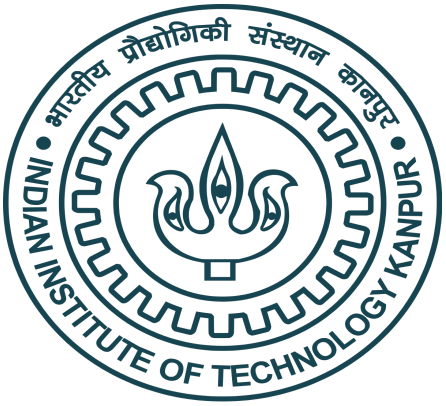

INDIAN INSTITUTE OF TECHNOLOGY, KANPUR

EE-619 VLSI SYSTEM DESIGN

VERILOG PROJECT

GROUP NO: 7

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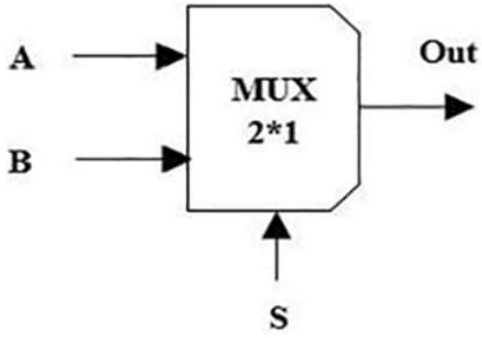
Course Instructor : Dr. Rik Dey

- **Icarus Verilog and gtkwave can be used to simulate all the circuits designed.**
- **All the simulation files are present in the folder itself.**
- **Commands to run the simulations are given along with each part.**

Q1 a)



(a)

S	Out
0	B
1	A

(b)

A	B	S	Out
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

(c)

- Structural modelling of 2-to-1 Multiplexer

  Verilog file: mux2s.v

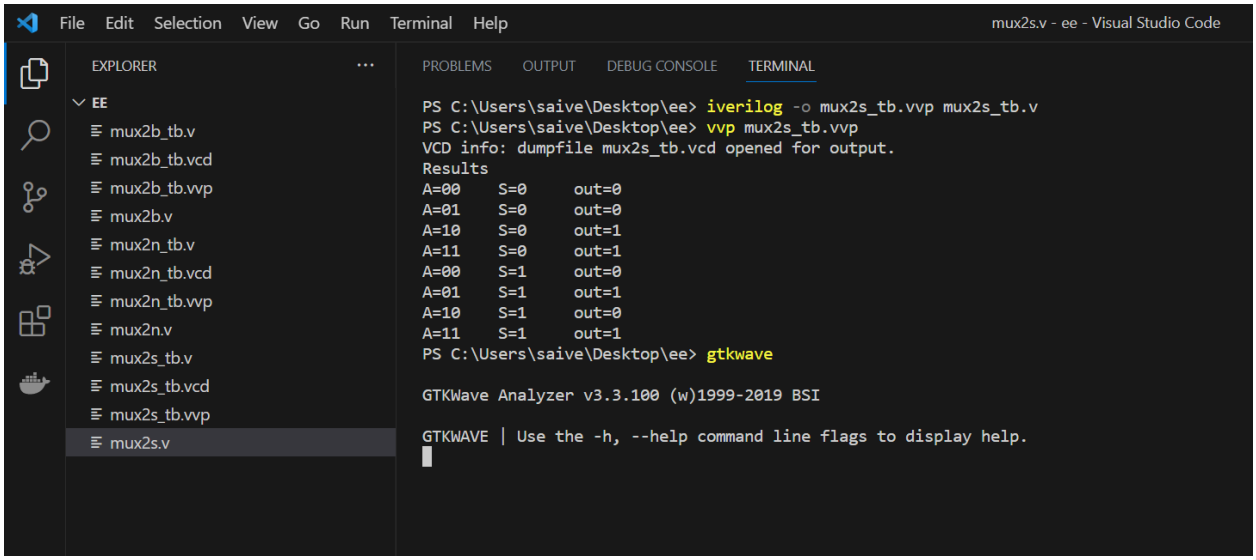
  Testbench: mux2s_tb.v

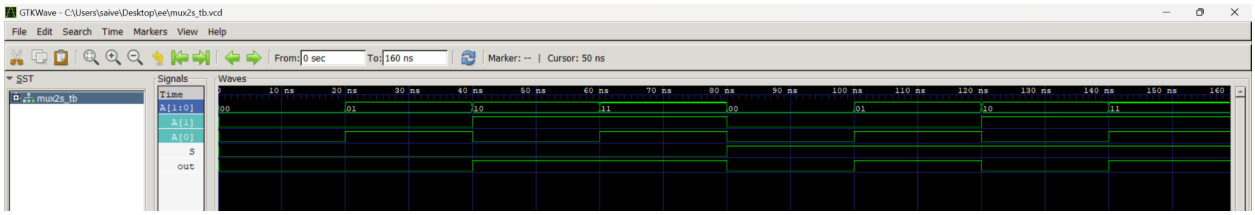
  Command to run testbench:

  $ iverilog -o mux2s_tb.vvp mux2s_tb.v

  $ vpp mux2s_tb.vpp

  gtkwave file: mux2s_tb.vcd





- <u>Behavorial modelling of 2-to-1 Multiplexer</u>

  Verilog file: mux2b.v

  Testbench: mux2b_tb.v

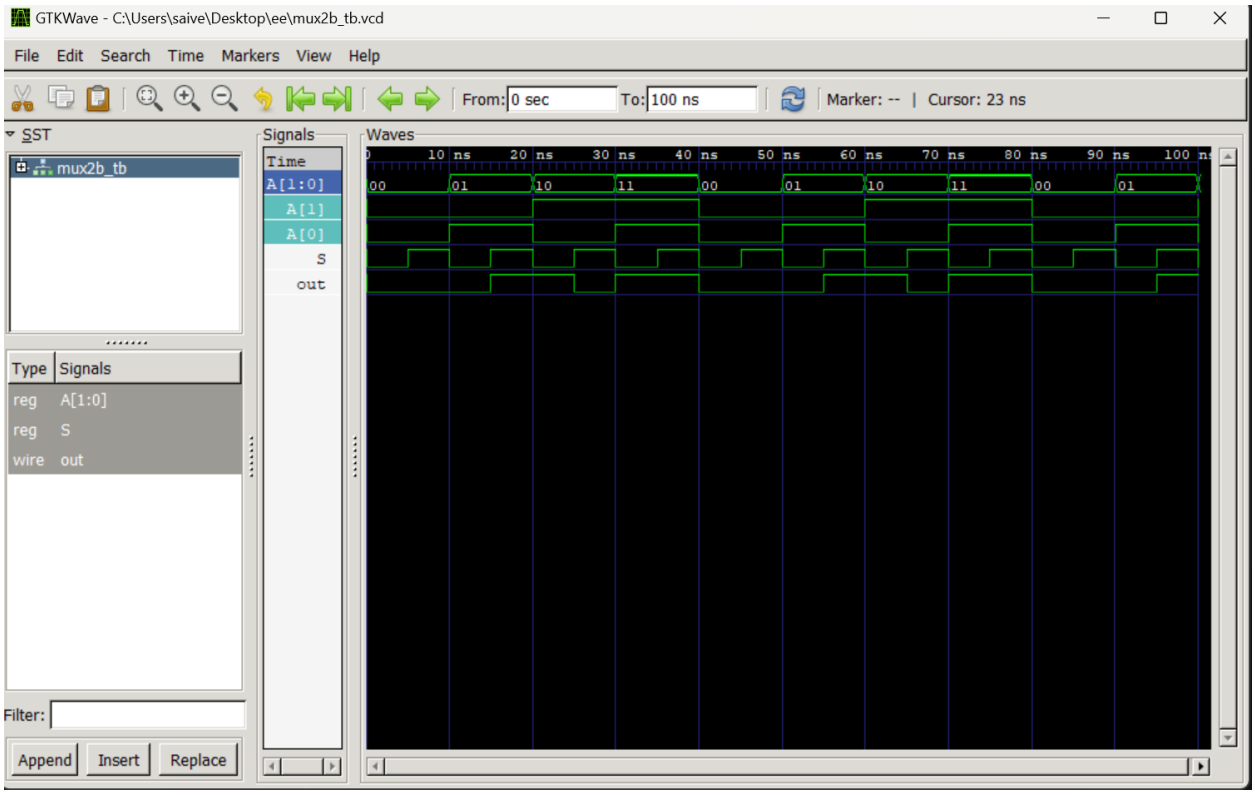
  Command to run testbench:

  $ iverilog -o mux2b_tb.vvp mux2b_tb.v

  $ vpp mux2b_tb.vpp

  gtkwave file: mux2b_tb.vcd

```
PS C:\Users\saive\Desktop\ee> iverilog -o mux2b_tb.vvp mux2b_tb.v
PS C:\Users\saive\Desktop\ee> vvp mux2b_tb.vvp
VCD info: dumpfile mux2b_tb.vcd opened for output.
Results
A=00    S=0     out=0
A=00    S=1     out=0
A=01    S=0     out=0
A=01    S=1     out=1
A=10    S=0     out=1
A=10    S=1     out=0
A=11    S=0     out=1
A=11    S=1     out=1
A=00    S=0     out=0
A=00    S=1     out=0
A=01    S=0     out=0
A=01    S=1     out=1
A=10    S=0     out=1
A=10    S=1     out=0
A=11    S=0     out=1
A=11    S=1     out=1
A=00    S=0     out=0
A=00    S=1     out=0
A=01    S=0     out=0
A=01    S=1     out=1
mux2b_tb.v:18: $finish called at 100 (1ns)
PS C:\Users\saive\Desktop\ee>
```



- 2n-to-1 Multiplexer using 2-to-1 Multiplexer and implementation of 5 variable function

  Verilog file: mux2n.v

  Testbench: mux2n_tb.v

  Command to run testbench:

  $ iverilog -o mux2n_tb.vvp mux2n_tb.v

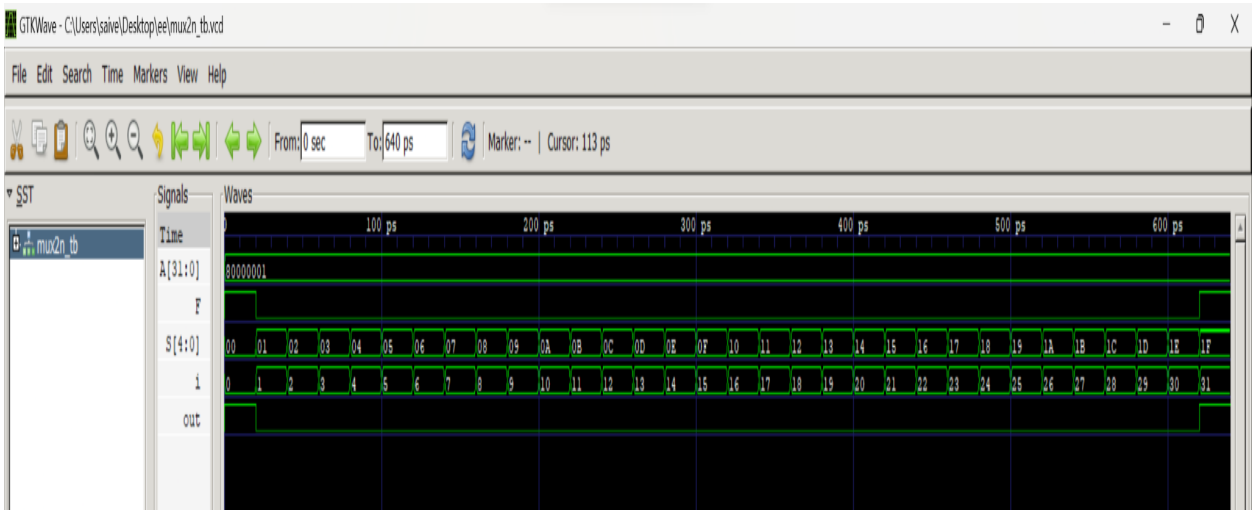
  $ vpp mux2n_tb.vpp

  gtkwave file: mux2n_tb.vcd

  32-to-1 multiplexer was implemented using the 2-to-1 multiplexer designed above. As an example the arbitrary function

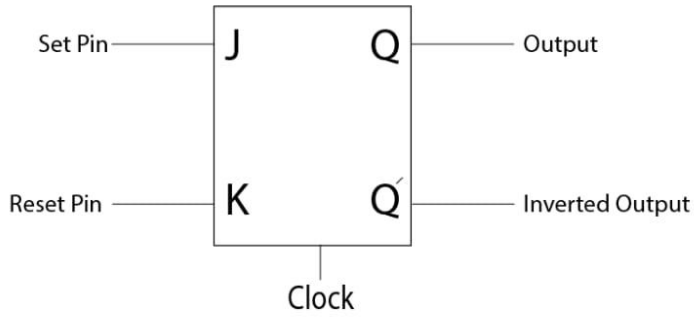
  F=ABCDE+A'B'C'D'E' was implemented in the testbench.

```
PS C:\Users\saive\Desktop\ee> iverilog -o mux2n_tb.vvp mux2n_tb.v
PS C:\Users\saive\Desktop\ee> vvp mux2n_tb.vvp
VCD info: dumpfile mux2n_tb.vcd opened for output.
Results
A=10000000000000000000000000000001      S=00000 out=1   F=1
A=10000000000000000000000000000001      S=00001 out=0   F=0
A=10000000000000000000000000000001      S=00010 out=0   F=0
A=10000000000000000000000000000001      S=00011 out=0   F=0
A=10000000000000000000000000000001      S=00100 out=0   F=0
A=10000000000000000000000000000001      S=00101 out=0   F=0
A=10000000000000000000000000000001      S=00110 out=0   F=0
A=10000000000000000000000000000001      S=00111 out=0   F=0
A=10000000000000000000000000000001      S=01000 out=0   F=0
A=10000000000000000000000000000001      S=01001 out=0   F=0
A=10000000000000000000000000000001      S=01010 out=0   F=0
A=10000000000000000000000000000001      S=01011 out=0   F=0
A=10000000000000000000000000000001      S=01100 out=0   F=0
A=10000000000000000000000000000001      S=01101 out=0   F=0
A=10000000000000000000000000000001      S=01110 out=0   F=0
A=10000000000000000000000000000001      S=01111 out=0   F=0
A=10000000000000000000000000000001      S=10000 out=0   F=0
A=10000000000000000000000000000001      S=10001 out=0   F=0
A=10000000000000000000000000000001      S=10010 out=0   F=0
A=10000000000000000000000000000001      S=10011 out=0   F=0
A=10000000000000000000000000000001      S=10100 out=0   F=0
A=10000000000000000000000000000001      S=10101 out=0   F=0
A=10000000000000000000000000000001      S=10110 out=0   F=0
A=10000000000000000000000000000001      S=10111 out=0   F=0
A=10000000000000000000000000000001      S=11000 out=0   F=0
A=10000000000000000000000000000001      S=11001 out=0   F=0
A=10000000000000000000000000000001      S=11010 out=0   F=0
A=10000000000000000000000000000001      S=11011 out=0   F=0
A=10000000000000000000000000000001      S=11100 out=0   F=0
A=10000000000000000000000000000001      S=11101 out=0   F=0
A=10000000000000000000000000000001      S=11110 out=0   F=0
A=10000000000000000000000000000001      S=11111 out=1   F=1
```



Q1 b)

JK flip-flop symbol



Truth table of JK flip-flop

C	J	K	Q	Q`
HIGH	0	0	Latch	Latch
HIGH	0	1	0	1
HIGH	1	0	1	0
HIGH	1	1	Toggle	Toggle
LOW	0	0	Latch	Latch
LOW	0	1	Latch	Latch
LOW	1	0	Latch	Latch
LOW	1	1	Latch	Latch

- Behavorial modelling of JK Flip Flop

Verilog file: jkb.v

Testbench: jkb_tb.v

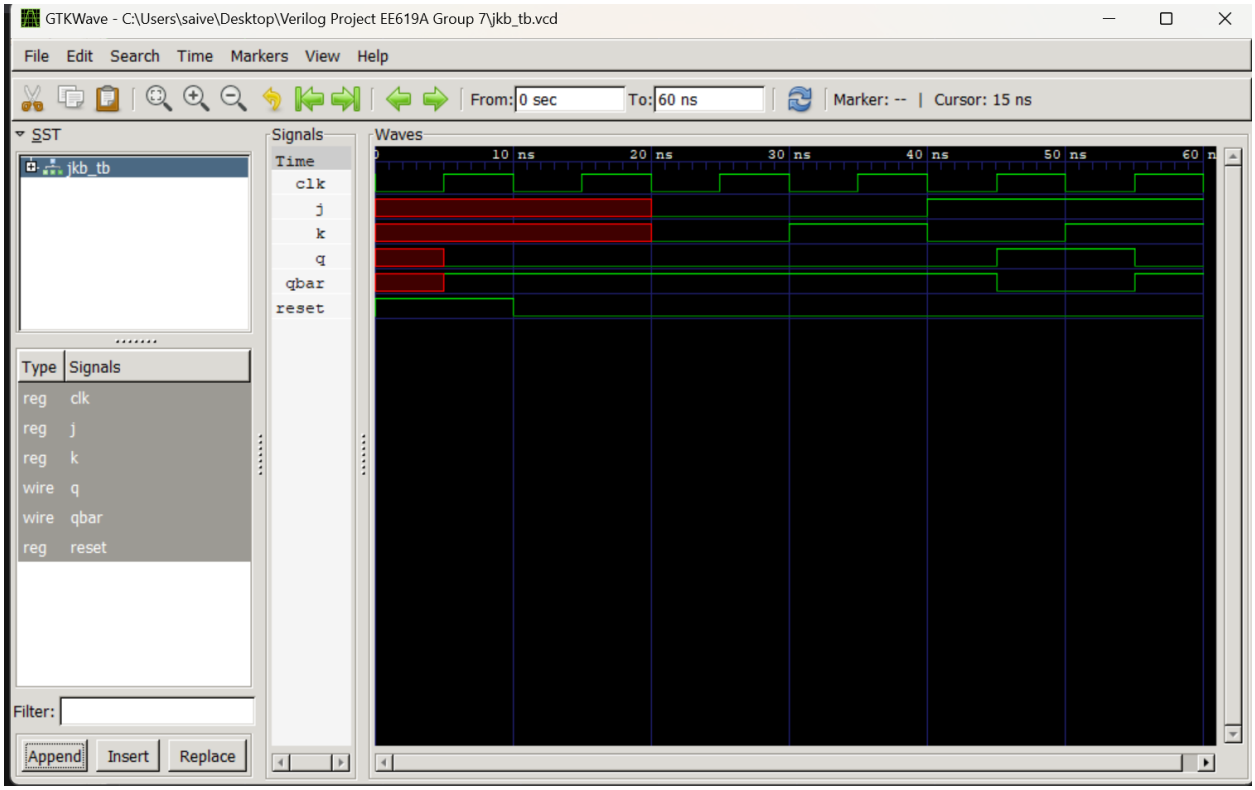
Command to run testbench:

$ iverilog -o jkb_tb.vvp jkb_tb.v

$ vpp jkb_tb.vpp

gtkwave file: jkb_tb.vcd

```
PS C:\Users\saive\Desktop\Verilog Project EE619A Group 7> iverilog -o jkb_tb.vvp jkb_tb.v
PS C:\Users\saive\Desktop\Verilog Project EE619A Group 7> vvp jkb_tb.vvp
VCD info: dumpfile jkb_tb.vcd opened for output.
j=x     k=x     q=0     qbar=1
j=x     k=x     q=0     qbar=1
j=0     k=0     q=0     qbar=1
j=0     k=1     q=0     qbar=1
j=1     k=0     q=1     qbar=0
j=1     k=1     q=0     qbar=1
jkb_tb.v:40: $finish called at 60 (1ns)
PS C:\Users\saive\Desktop\Verilog Project EE619A Group 7>
```



Values that are in Red are Undefined('x' values)

- ## Structural modelling of JK Flip Flop

Verilog file: jks.v

Testbench: jks_tb.v

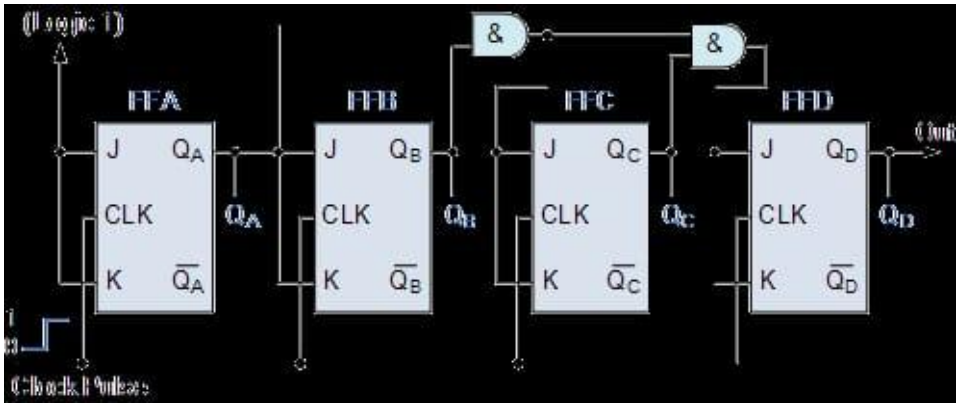
Command to run testbench:

$ iverilog -o jks_tb.vvp jks_tb.v

$ vpp jks_tb.vpp

gtkwave file: jks_tb.vcd

- 4 bit synchronous counter using JK FlipFlop



Rst	CLK	O3	O2	O1	O0
1	↑	0	0	0	0
0	↑	0	0	0	1
0	↑	0	0	1	0
0	↑	0	0	1	1
0	↑	0	1	0	0
0	↑	0	1	0	1
0	↑	0	1	1	0
0	↑	0	1	1	1
0	↑	1	0	0	0
0	↑	1	0	0	1
0	↑	1	0	1	0
0	↑	1	0	1	1
0	↑	1	1	0	0
0	↑	1	1	0	1
0	↑	1	1	1	0
0	↑	1	1	1	1
0	↑	0	0	0	0

Verilog file: count.v

Testbench: count_tb.v

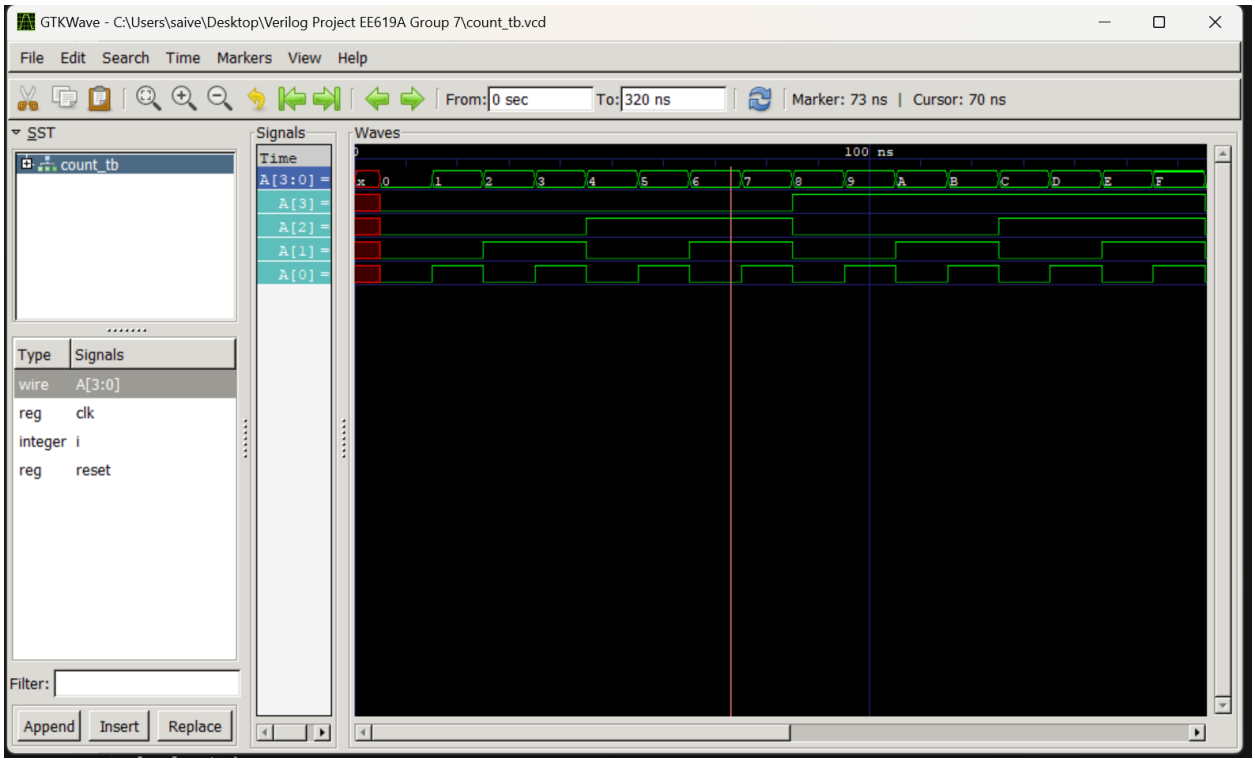
Command to run testbench:

$ iverilog -o count_tb.vvp count_tb.v

$ vpp count_tb.vpp

gtkwave file: count_tb.vcd

```
PS C:\Users\saive\Desktop\Verilog Project EE619A Group 7> iverilog -o count_tb.vvp count_tb.v
PS C:\Users\saive\Desktop\Verilog Project EE619A Group 7> vvp count_tb.vvp
VCD info: dumpfile count_tb.vcd opened for output.
0       0       0       0
0       0       0       1
0       0       1       0
0       0       1       1
0       1       0       0
0       1       0       1
0       1       1       0
0       1       1       1
1       0       0       0
1       0       0       1
1       0       1       0
1       0       1       1
1       1       0       0
1       1       0       1
1       1       1       0
1       1       1       1
0       0       0       0
0       0       0       1
0       0       1       0
0       0       1       1
0       1       0       0
0       1       0       1
0       1       1       0
0       1       1       1
1       0       0       0
1       0       0       1
1       0       1       0
1       0       1       1
1       1       0       0
1       1       0       1
1       1       1       0
1       1       1       1
count_tb.v:31: $finish called at 320 (1ns)
PS C:\Users\saive\Desktop\Verilog Project EE619A Group 7> gtkwave
```



As we can see the Register A is synchronously increasing to 15.