Course title: **Electronic circuit I**

Course code: **EEE 215**

Lecture 6

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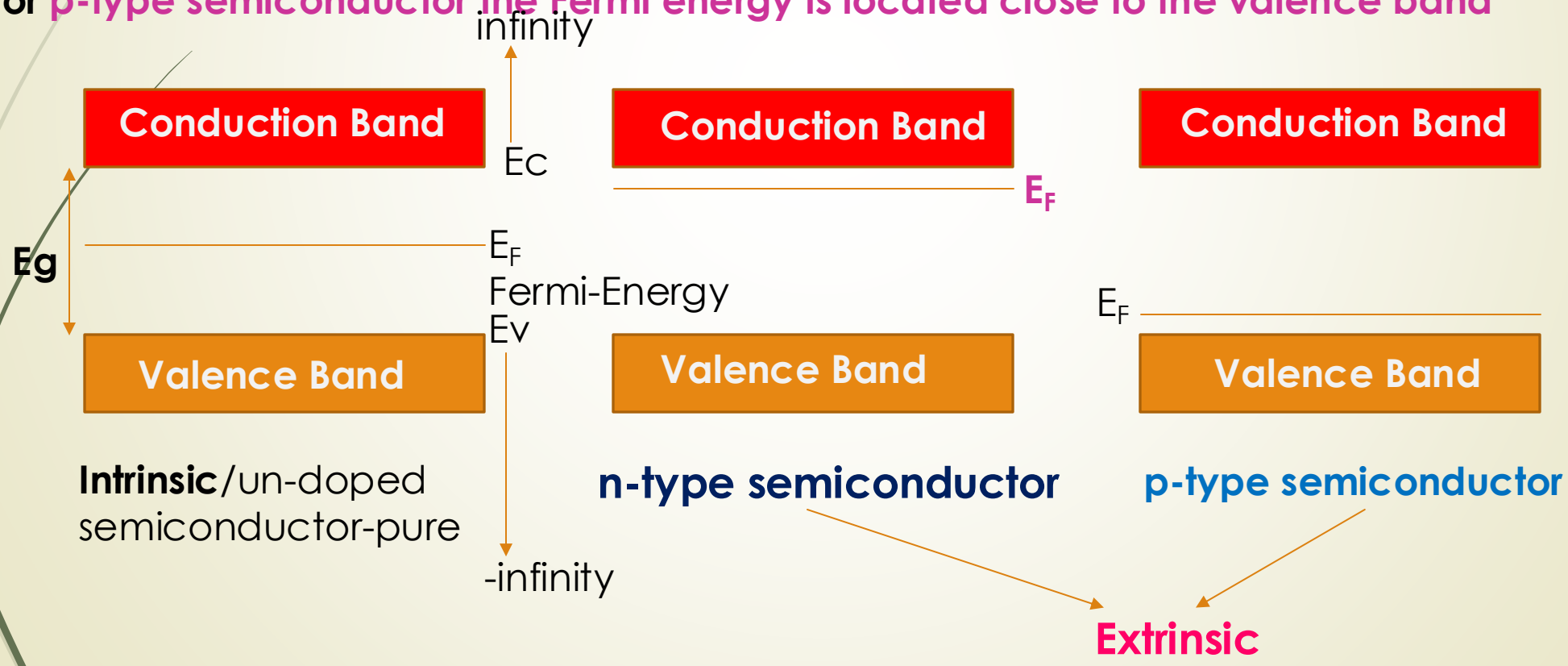
Semester: Fall 2020

Extrinsic Semiconductors

1. n-type

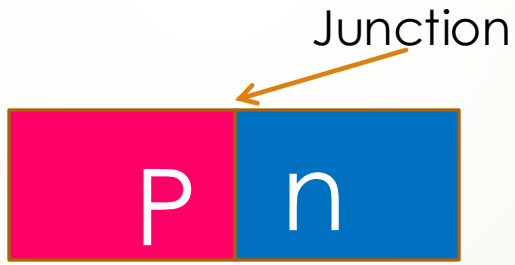
2. p-type

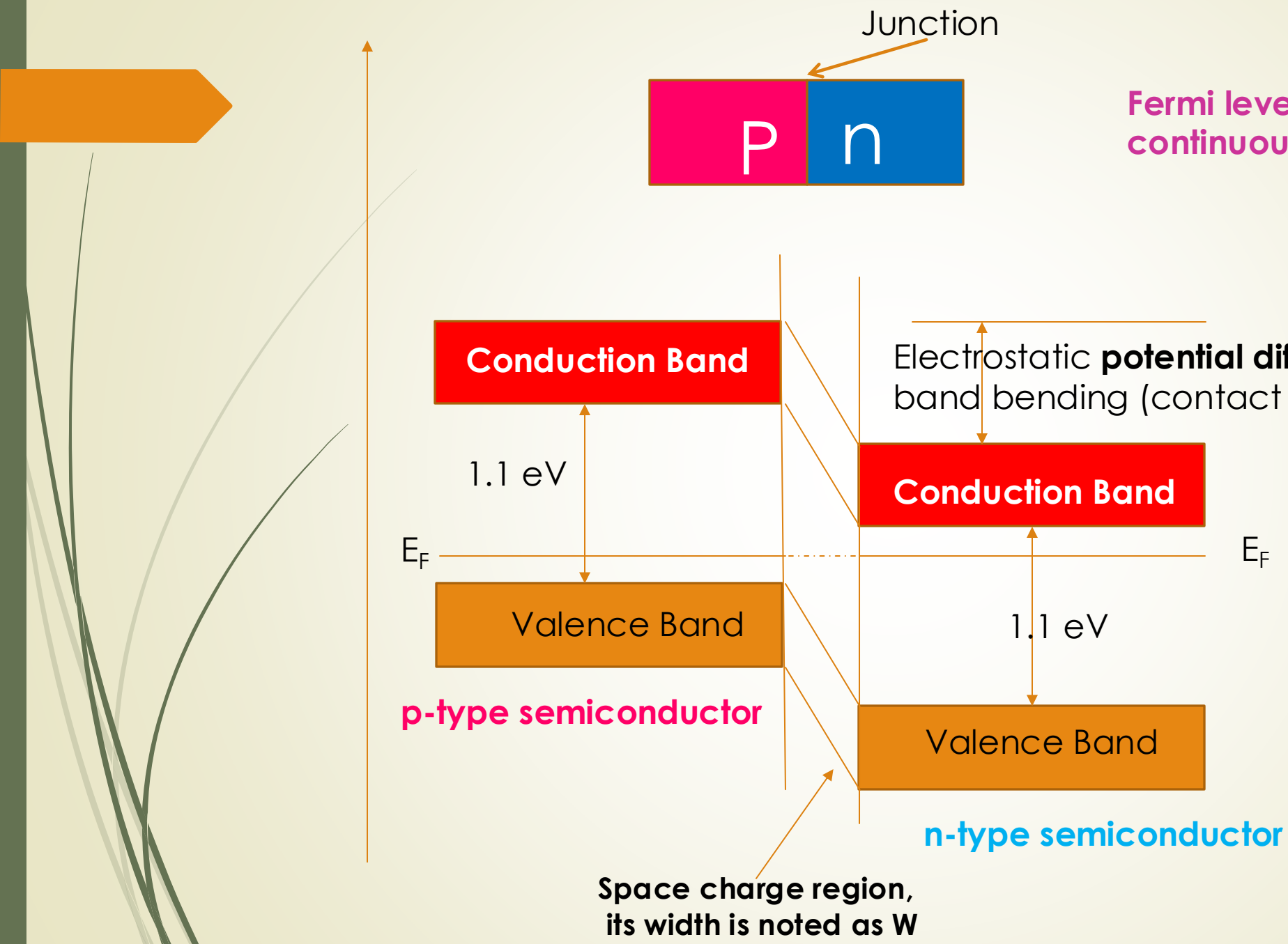
- For intrinsic/un-doped/pure semiconductor the Fermi energy lies at the middle of the conduction band
- For n-type semiconductor the Fermi energy, E_F is located close to the conduction band
- For p-type semiconductor the Fermi energy is located close to the valence band



p-n Junction is the most fundamental device building block

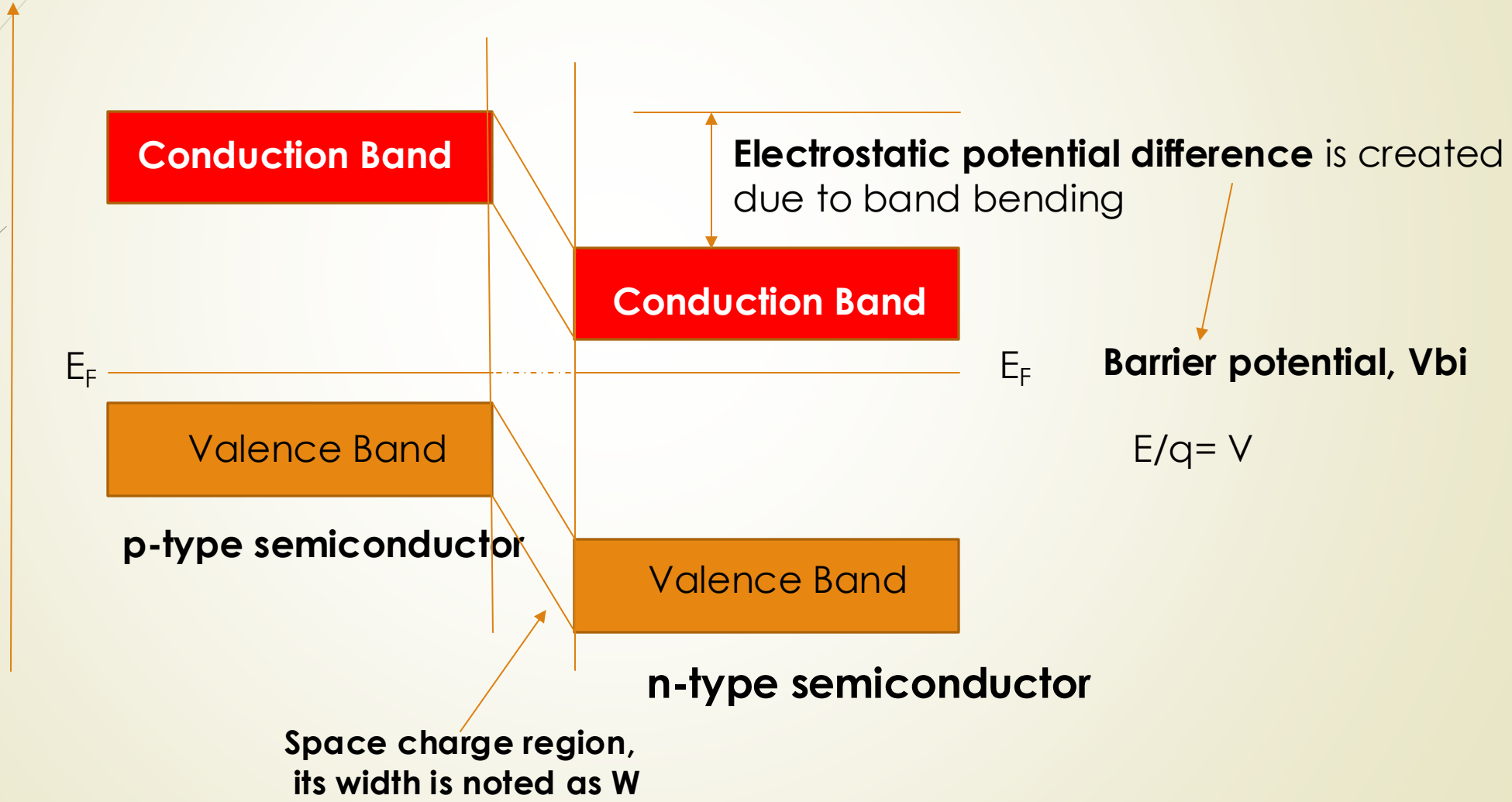
- When p-type Semiconductor is suitably in contact with n-type semiconductor, the p-n junction is formed.




Junction
P
n
Fermi level will be continuous
Conduction Band
1.1 eV
E_F
Valence Band
p-type semiconductor
Electrostatic potential difference is created due to band bending (contact or barrier potential) Vb
Conduction Band
E_F
1.1 eV
Valence Band
n-type semiconductor
E/q=V
Vq=E
Space charge region,
its width is noted as W

p-n junction: when p type is suitably in contact with n type how does the energy diagram look?

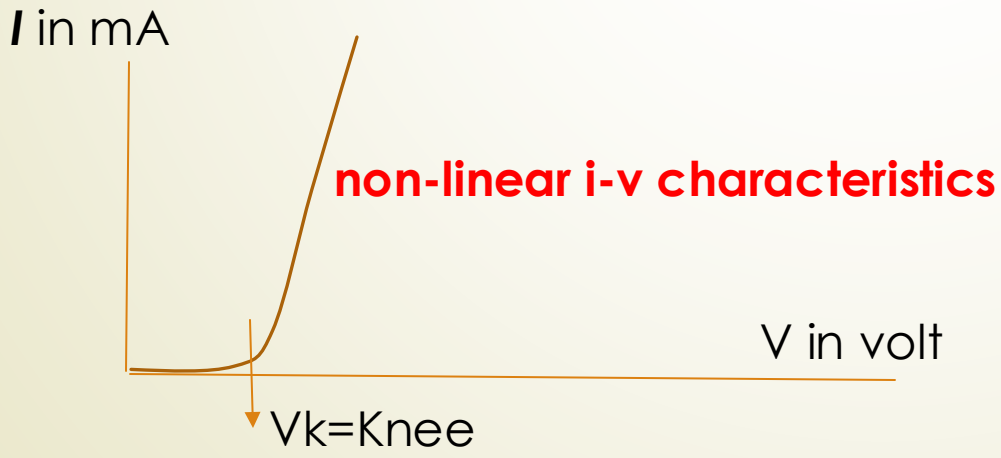
1. **Fermi level should be continuous throughout the junction**
2. **and therefore there will be band bending at the junction**

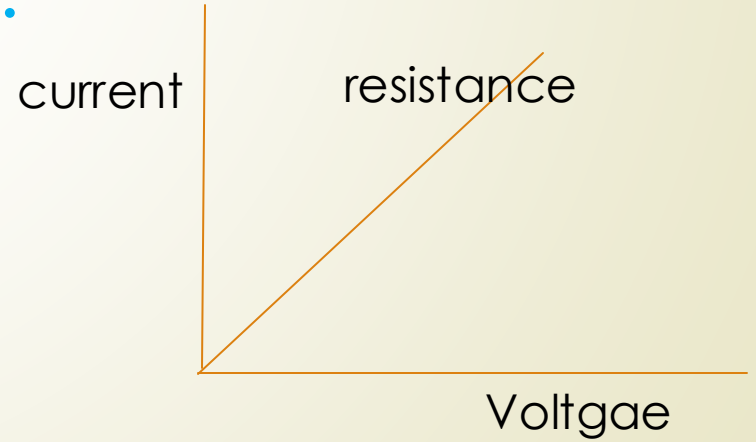


Semiconductor diode:

Diodes are the most simplest and fundamental non-linear circuit elements.

- A **diode** is a **two-terminal electronic component**, Just like resistors, but unlike the resistor which has linear relationship between the current flowing through it and the voltage appearing across it, **the diode has non-linear i-v characteristics.**

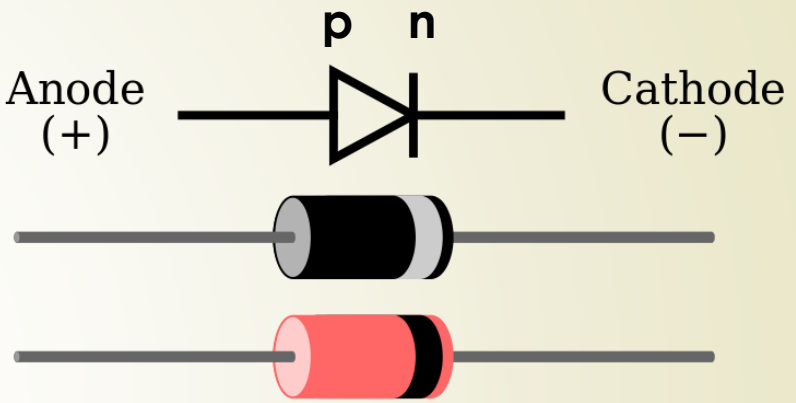


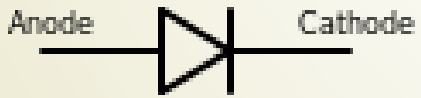


Semiconductor diode:

A **diode** shows

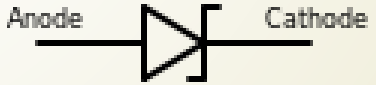
- low (ideally zero) resistance to current flow in forward direction,
- and high (ideally infinite) resistance in the reverse.
- The discovery of crystals' rectifying abilities was made by German physicist Ferdinand Braun in 1874. Today most diodes are made of silicon (Si), but other semiconductors such as selenium or germanium (Ge) are sometimes used.
- **A semiconductor diode, the most common type today, is a crystalline piece of semiconductor material with a p–n junction connected to two electrical terminals.**





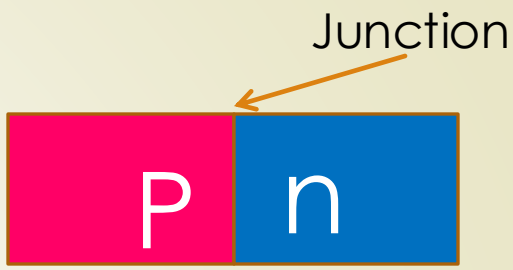
Conventional Diode

Photo diode symbol



Zener diode symbol

A diode is formed by the formation of p-n junction:



When a p-type semiconductor is suitably in contact with a n-type semiconductor, the contact surface is called p-n junction.

It is important to note that simply butting an n-type semiconductor against a p-type semiconductor does not form a junction. The irregular surface atomic forces at such a physical discontinuity at the interface simply prevent junction formation. It is essential that the crystalline background forces are uniform across the junction, i.e., the basic internal crystal regularity is maintained across the junction.

A semiconductor junction is commonly formed by doping a semiconductor so that the impurity concentration varies from n-type to p-type. The electrical junction forms about the 'metallurgical' junction where the transition from one doping type to the other occurs.

The p-n junction may be produced by any one of the following

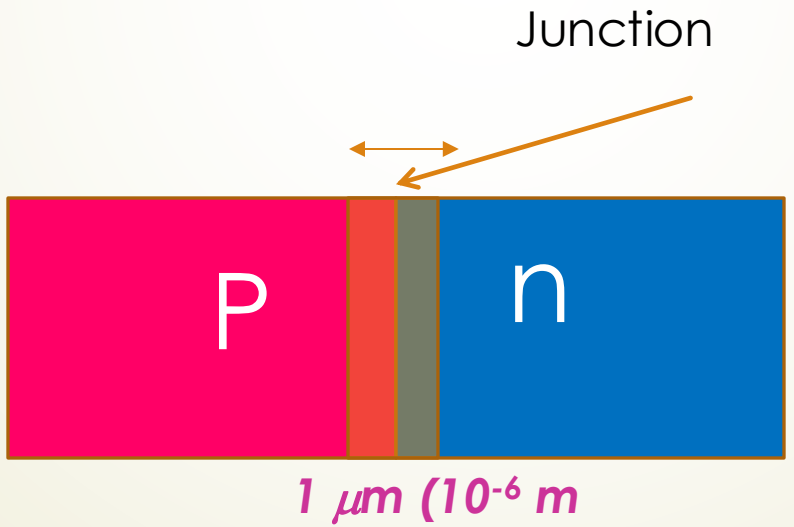
i. Grown junction
ii. Alloy junction
iii. Diffused junction
iv. Epitaxial growth, v. point contact junction

Physical properties of p-n junction:

During the formation of p-n junction, following **two phenomena take place:**

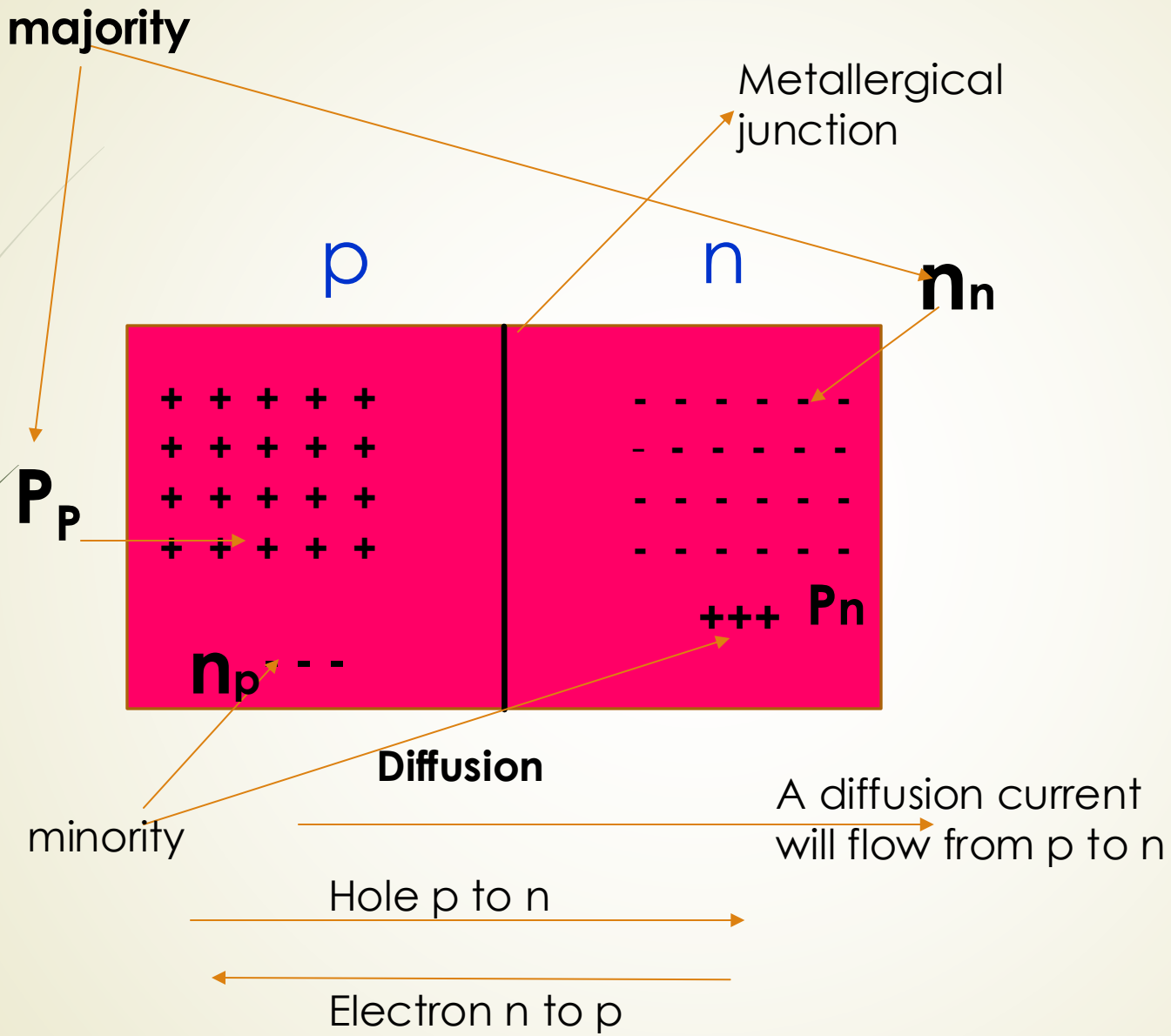
i. ***A thin depletion layer (or region) is set up on both sides of the junction*** *and is so called because it is depleted or devoid of free charge carriers. Its typical width is about 1 μm (10^{-6} m).*

ii. ***A junction or barrier potential V_B*** *is developed across the junction whose value is about* ***0.3 V for Ge*** *and* ***0.7 V for Si.***



High concentration to **low** concentration

diffusion



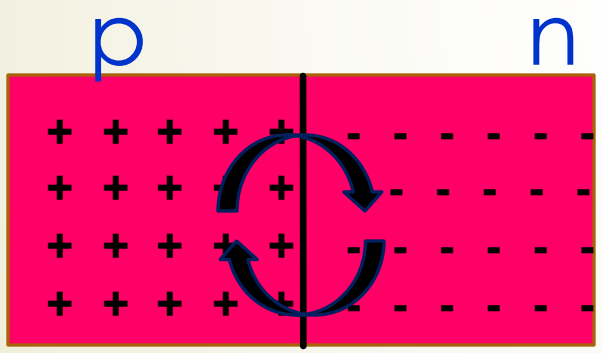
Two current

1. Diffusion current (high to low concentration)
2. Drift current (it depends on electric field)

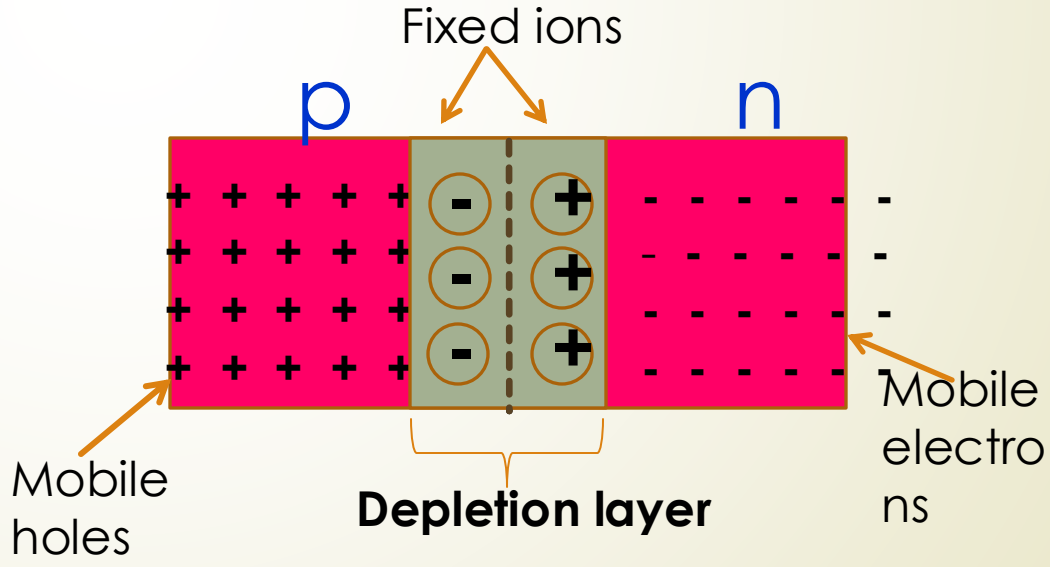
Formation of depletion region:

After a p-n junction is formed, a difference in concentration of carriers creates a density gradient of carriers across junction which will result is majority carrier diffusion .

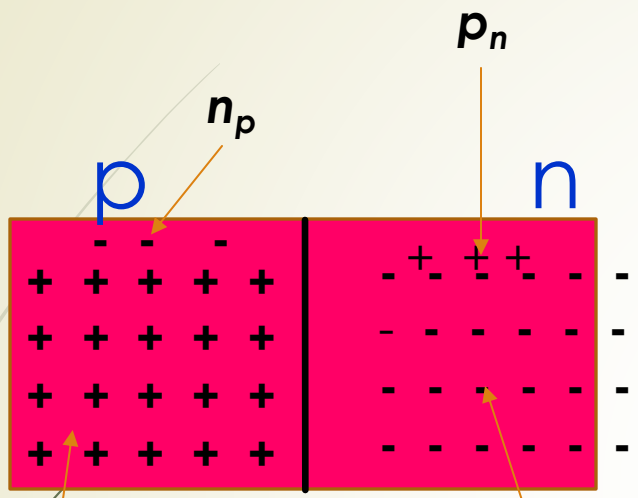
i. ***The holes diffuse from p to n region while electrons from n to p. This recombination of carrier will cause a lack of free carrier at the junction leaving behind the fixed/immobile ions .***
ii. ***This region of uncovered positive and negative ion is called depletion region/layer.***
iii. ***Since this layer contain no free charge it behaves like insulator.***



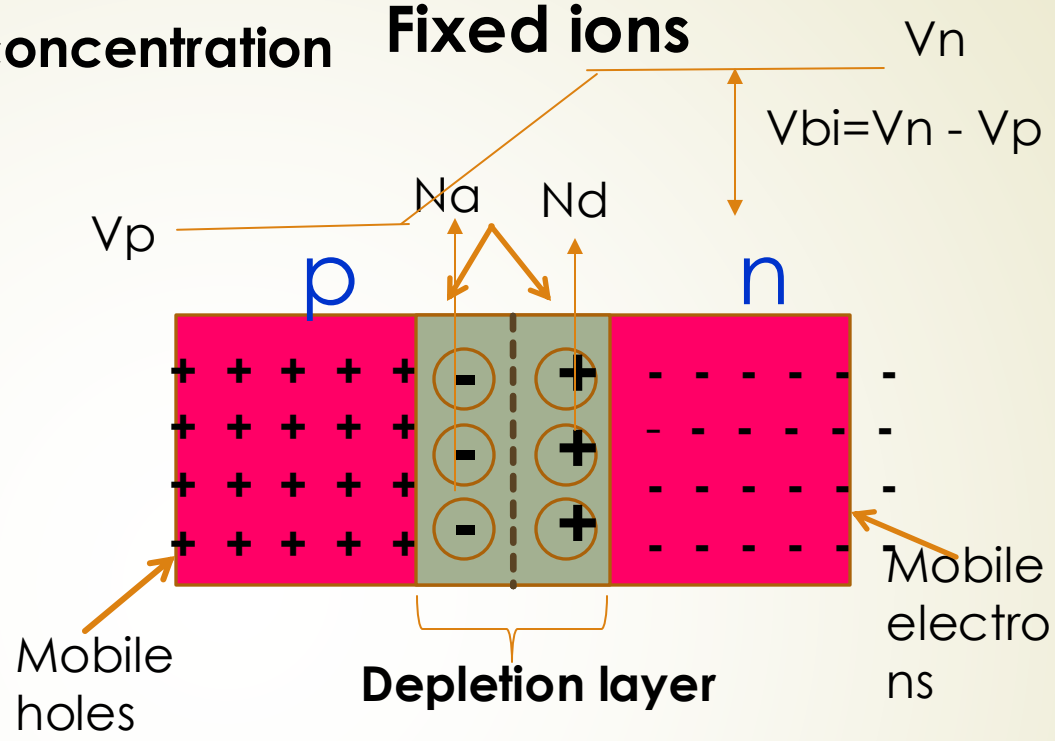
Diffusion



High concentration to low concentration



Fixed ions



ni=pi

Pure-Si

N-type

P-type

Hole will diffuse from p to n

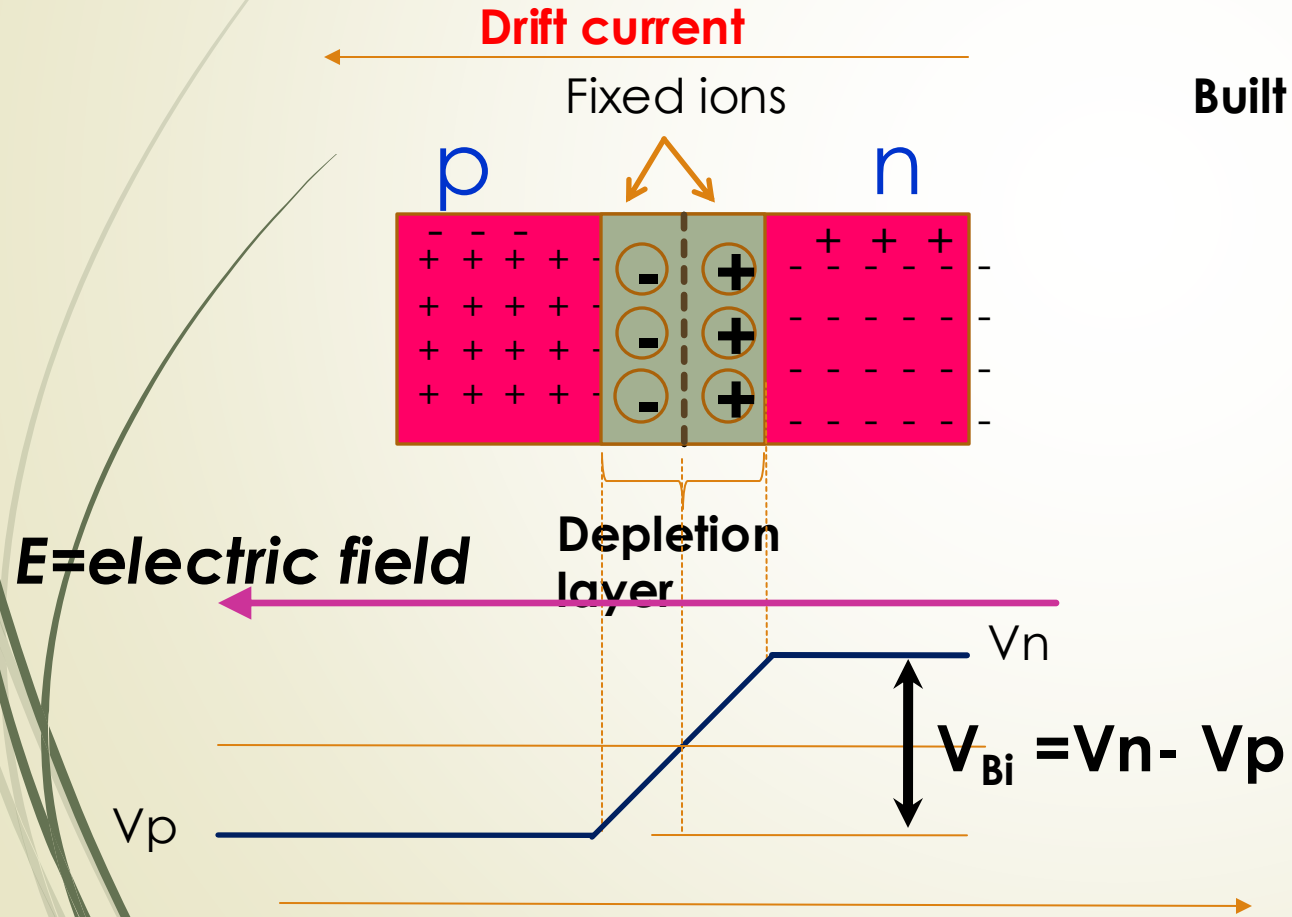
Electron will diffuse from n to p

There is diffusion current from p to n

Formation of junction or barrier voltage:

Since the depletion layer contain only fixed rows of oppositely charged carriers,

i. ***due to this charge separation an electric potential V_B is established across the junction***
ii. ***This potential difference further opposes the diffusion of majority carriers across the junction***
iii. ***The width of depletion region/layer depends on doping level. For heavy doping, depletion layer is physically thin.***



Built in Electric Field $= \frac{change - in - potential}{change - in - distance}$

$$E = -\frac{dV}{dx}$$

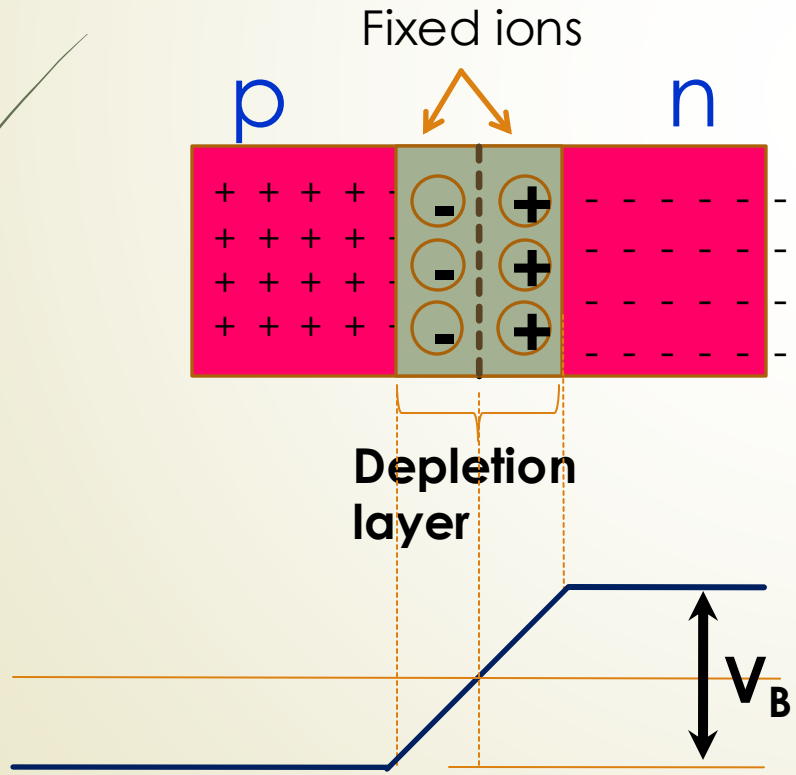
Velocity= mobility X electric field

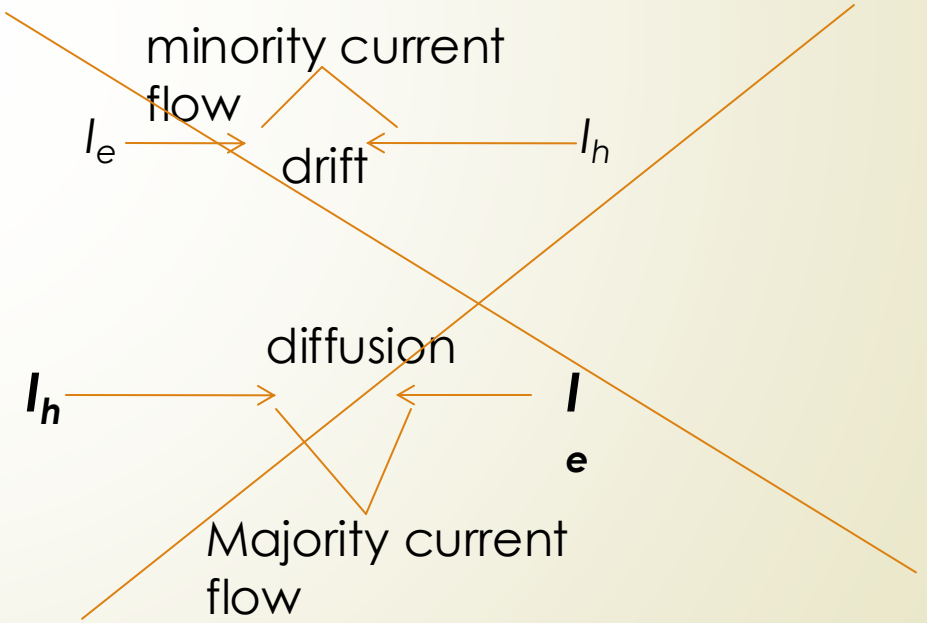
Formation of junction or barrier voltage:

Since the depletion layer contain only fixed rows of oppositely charged carriers,

i. ***due to this charge separation an electric potential V_B is established across the junction***
ii. ***This potential difference further opposes the diffusion of majority carriers across the junction***
iii. ***The width of depletion region/layer depends on doping level. For heavy doping, depletion layer is physically thin.***

Under no bias net current flow across the junction = zero





J= I/A current density

Drift and diffusion:

There are two mechanisms by which holes and electrons move through the silicon crystal-**drift** and **diffusion**.

Diffusion: is associated with random motion due to thermal agitation. Carriers diffuse from the higher region of concentration to lower concentration. This diffusion process gives rise to a net flow of charge, or diffusion current.

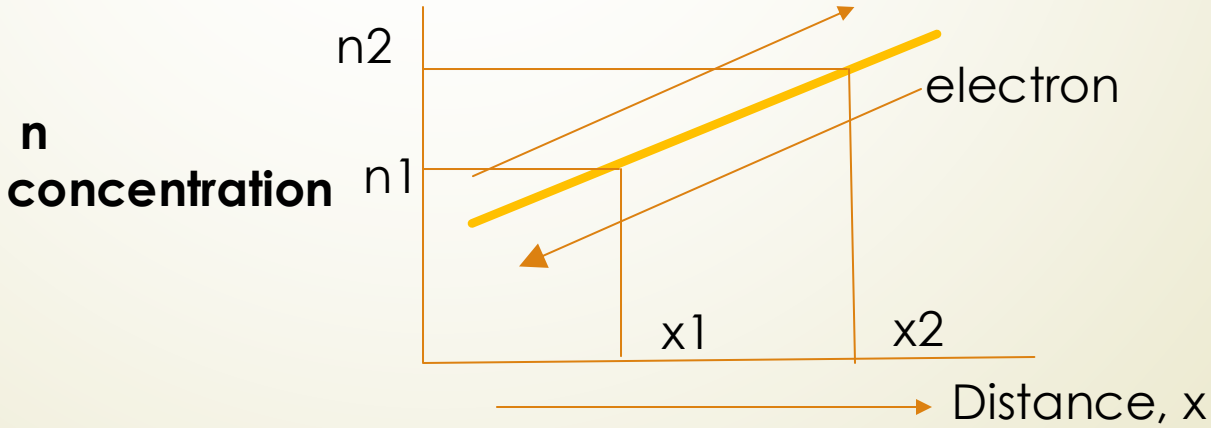
Diffusion current density

$$J_n = qD_n \frac{dn}{dx}$$

Eeeeeee
eeeeee

Where D_p = 12 cm^2/s, is **the hole diffusion coefficient**, D_n = 34 cm^2/s, is the **electron diffusion coefficient**.

$$J_p = -qD_p \frac{dp}{dx}$$



Drift:

The other mechanism in semiconductors is drift. Carrier drift when an electric field is applied across a piece of semiconductor. Free electrons and holes are accelerated by the applied electric field and acquire velocity component called drift velocity,

$v_{drift} = \mu_{p,n} E$, where $\mu_{p,n}$ is the mobility of holes/electrons

The hole-drift current density is $J_{p\text{-}drift} = qp\mu_p E$

The electron-drift current density is $J_{n\text{-}drift} = qn\mu_n E$

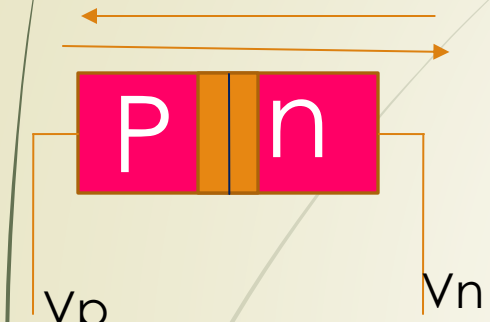
The total drift current density is $J_{drift} = q(p\mu_p + n\mu_n)E$

The Einstien relation

$$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = V_T = \frac{KT}{q} = thermal\ voltage = 25mV, at 300K$$

Quantitative relation between barrier potential and doping concentration on each side of the junction:

We know the drift and diffusion component **of hole** current just **cancel out each other at equilibrium**



$$q[\mu_p pE - D_p \frac{dp}{dx}] = 0 \qquad (1)$$

$$\frac{\mu_p}{D_p} E = \frac{1}{p}\frac{dp}{dx}$$

We know, $E = -\frac{dV}{dx}$

$$-\frac{q}{KT}\frac{dV}{dx} = \frac{1}{p}\frac{dp}{dx} \qquad (4)$$

ing Einstein relation, $\frac{n_n}{n_p} = e^{qV_B/kT}$

After integrating, $-\frac{q}{KT}\int_{V_p}^{V_n} dV = \int_{P_p}^{P_n} \frac{1}{p}\,dp$ or, $-\frac{q}{KT}(V_n - V_p) = \ln\frac{P_n}{P_p}$ (5)

$$V_B = \frac{kT}{q}\ln\frac{n_n}{n_p}$$

V_n-V_p=V_B= contact potential,

$$V_B = \frac{kT}{q}\ln\frac{P_p}{P_n}, \quad \text{or,} \quad \frac{P_p}{P_n} = e^{qV_B/kT} \qquad (6)$$

We know, $p_p n_p = n_i^2 = p_n n_n$ concentration

We can extend equation 6 for also electron

$$\frac{P_p}{P_n} = \frac{n_n}{n_p} = e^{qV_0/kT}$$

$$V_B = \frac{kT}{q}\ln\frac{N_a}{n_i^2/N_d} = \frac{kT}{q}\ln\frac{N_a N_d}{n_i^2}$$

Hole diffusion and hole drift

P n

$$q[\mu_p pE - D_p \frac{dp}{dx}] = 0 \qquad (1)$$

$$\frac{\mu_p}{D_p} E = \frac{1}{p}\frac{dp}{dx} \qquad (2)$$

$$E = -\frac{\mathrm{dV}}{\mathrm{dx}} \qquad (3)$$

$$-\frac{q}{KT}\frac{dV}{dx} = \frac{1}{p}\frac{dp}{dx} \qquad (4)$$

$$-\frac{q}{KT}\int_{V_p}^{V_n} dV = \int_{P_p}^{P_n} \frac{1}{p}\,dp \qquad \text{or,} -\frac{q}{KT}(V_n - V_p) = \ln\frac{P_n}{P_p} \qquad (5)$$

$$\mathrm{V_B} = \frac{kT}{q}\ln\frac{P_p}{P_n}, \qquad \text{or,} \frac{P_p}{P_n} = e^{qV_B/kT} \qquad (6)$$

$$V_B = \frac{kT}{q} \ln \frac{n_n}{n_p}$$

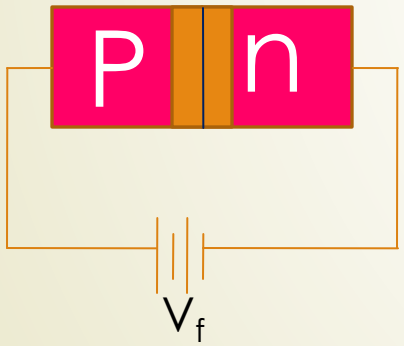
$$\frac{n_n}{n_p} = e^{qV_B / kT}$$

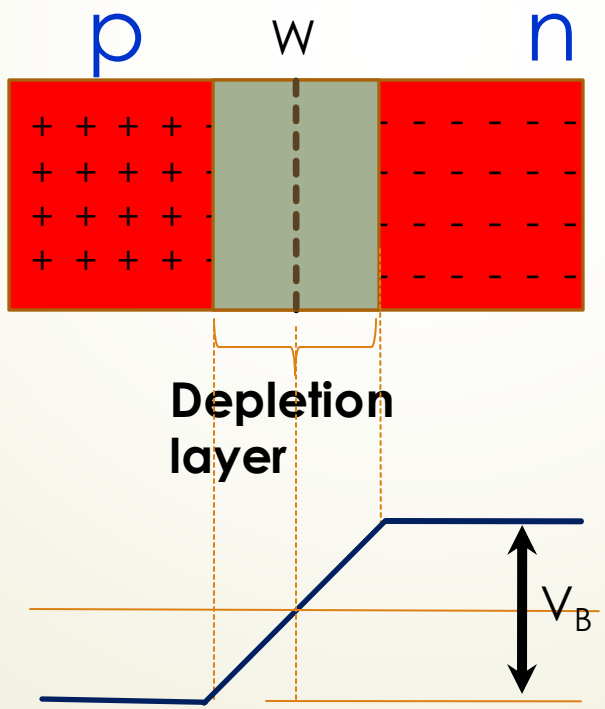
$$V_B = \frac{kT}{q} \ln \frac{N_a}{n_i^2 / N_d} = \frac{kT}{q} \ln \frac{N_a N_d}{n_i^2}$$

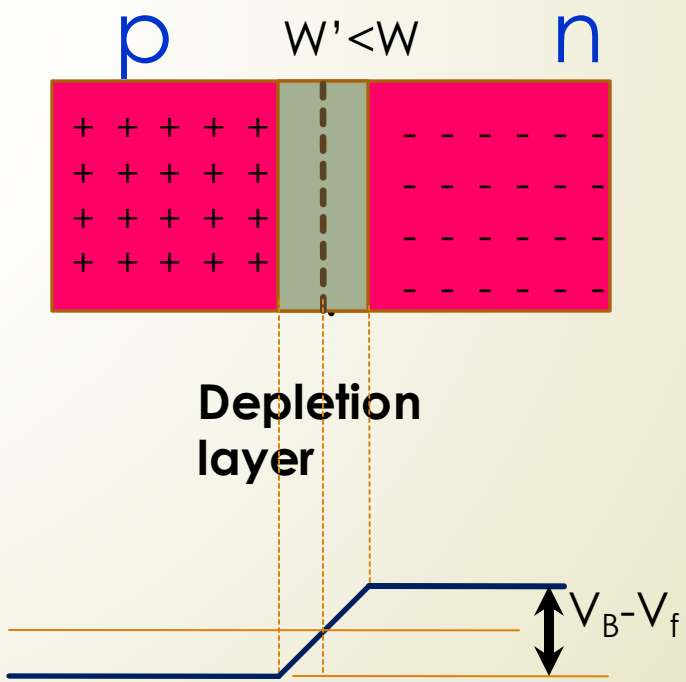
Forward biased condition of p-n junction semiconductor diode:

i. *A forward biased 'on' condition is obtained by applying a positive potential to the p-side of the junction and negative potential to the n-side.*

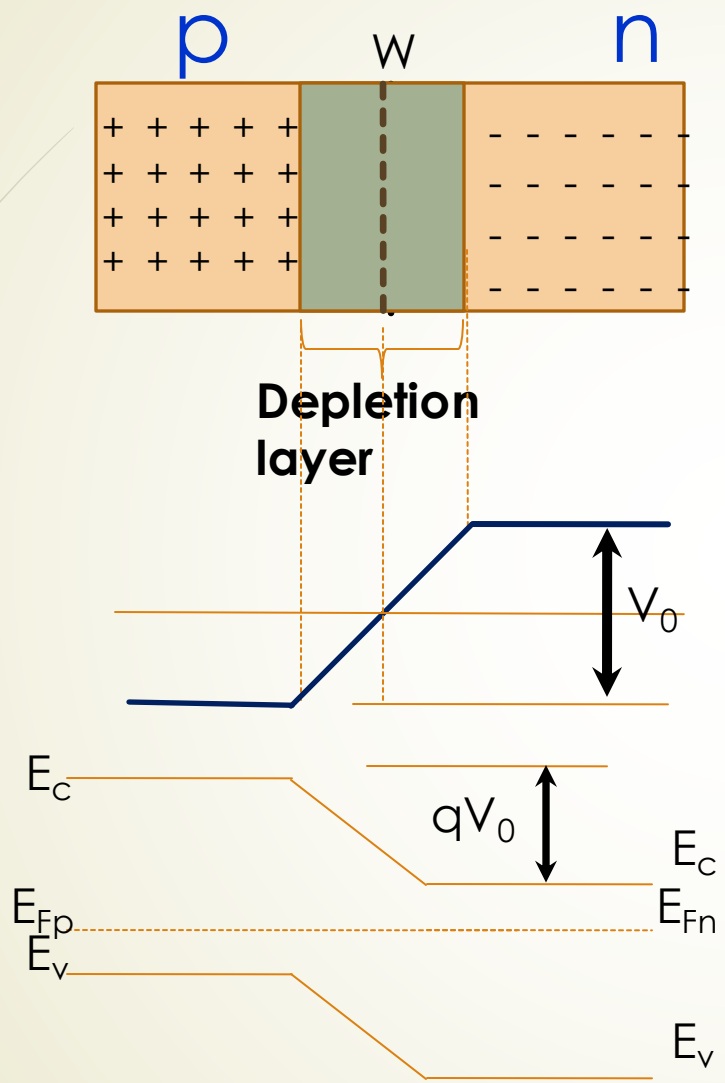
ii. *The application forward bias will cause the electrons and holes driven towards the junction where they recombine and will reduce the width of the depletion region . The resulting minority carrier flow of electrons from p to n will not change, but the reduction of depletion layer will create large amount of current flow across junction.*

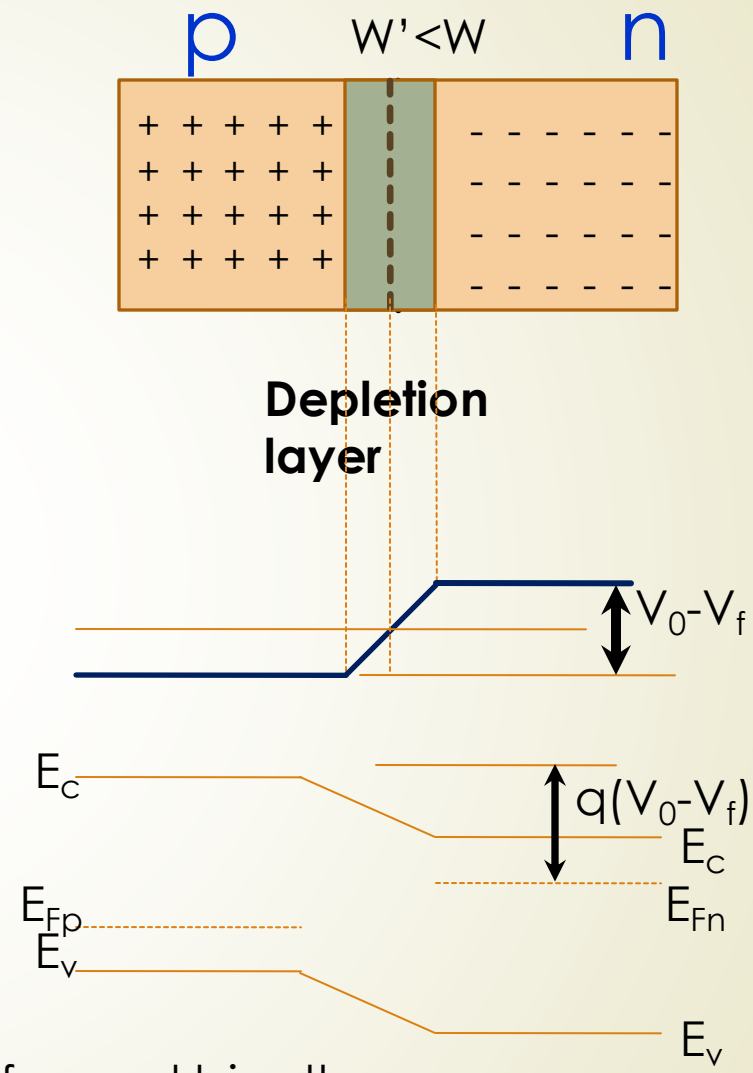






Effect of forward biased on the energy band diagram of p-n junction semiconductor diode:

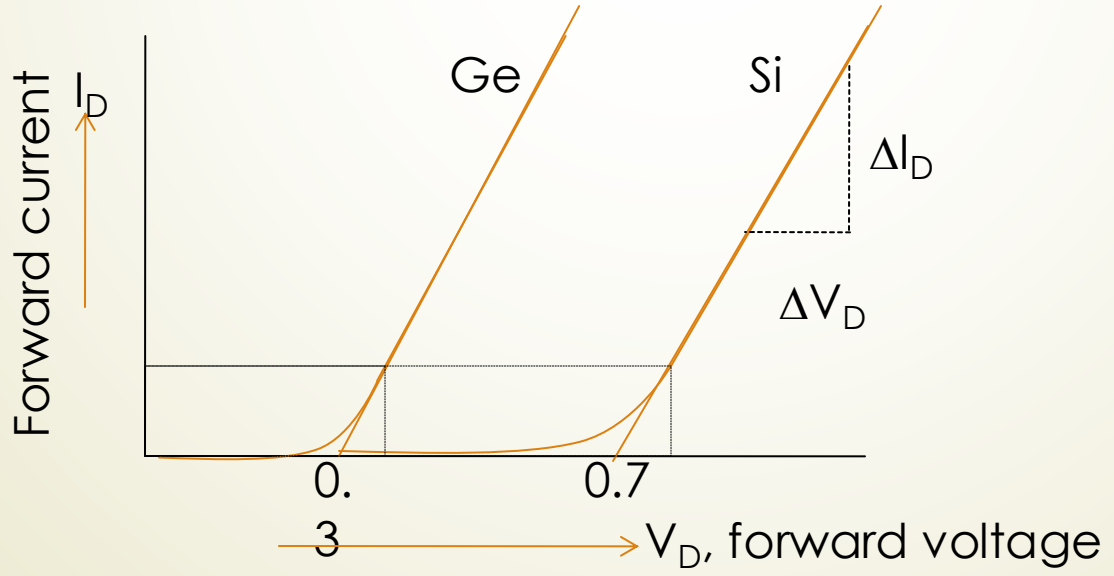




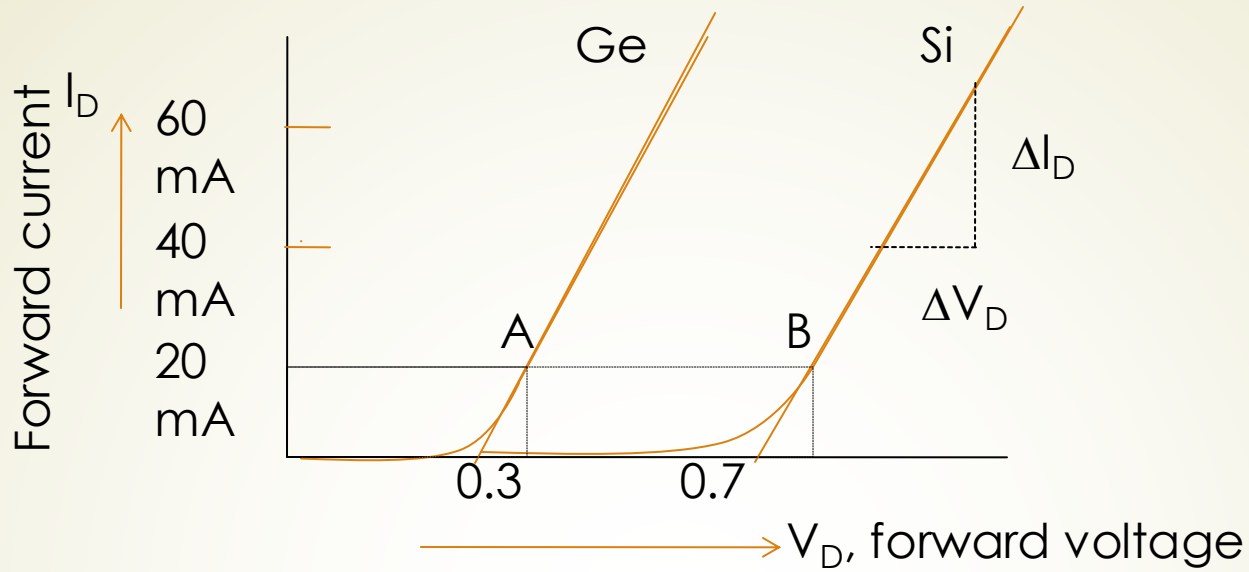
With forward bias the electrostatic potential is lowered from the equilibrium contact potential to V_0-V_f.

Forward V/I characteristics of p-n junction semiconductor diode:

i. *When diode is forward bias and the applied voltage is increased from zero, hardly any current flow the device in the beginning.*
ii. *It is so because the external voltage is opposed by the internal barrier voltage V_B which is 0.7 for Si and 0.3 for Ge.*
iii. *As soon as V_B is neutralized It is seen that the forward current rises exponentially with the applied forward voltage.*
iv. *This voltage is known as threshold voltage V_{th}, cut-in voltage or knee voltage.*
v. *When $V<V_{th}$, negligible current flow*
vi. *When $V>V_{th}$, current rise exponentially*



Forward biased junction resistance:



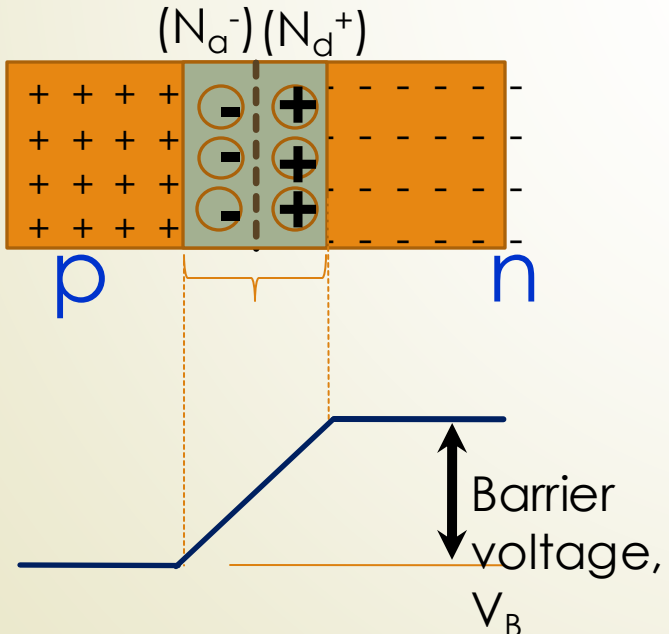
Obviously the forward-biased junction has very low resistance,
For point B in Si,
Static forward resistance is $R_F = \frac{0.76V}{20mA}$

In practice static resistance is not used instead ***dynamic resistance*** or ***ac resistance*** is used. It is given by the reciprocal of the slop of the forward characteristics.

$$\frac{1}{R_{ac}} = \frac{\Delta I_D}{\Delta V_D}$$

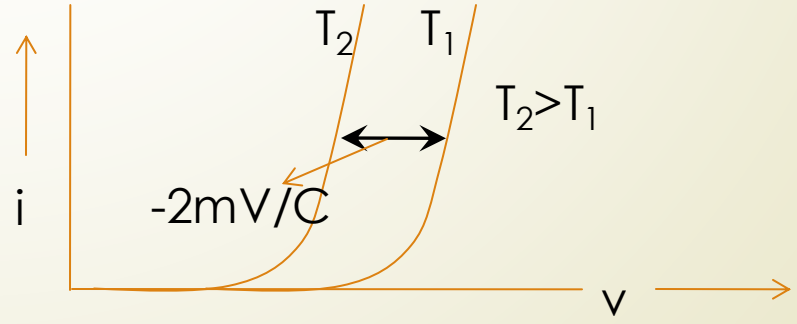
Effect of temperature on barrier voltage:

i. *Barrier voltage depends on doping density, electronic charge and temperature.*
ii. *For a given junction the first two factors are fixed, therefore V_B (barrier voltage) is mainly dependent on temperature.*
iii. *With increase in temperature results in increase of minority carriers leading to their increased drift across the junction.*
iv. *As a result equilibrium occurs at slightly reduced barrier potential.*
v. *It is found that for both Ge and Si VB is decreased about 2mV/°C*



$$\Delta V_B = -0.002.\Delta T$$

$$\Delta T = Change \text{ in } Temperature \text{ in } {}^{o}\text{C}$$



Problem:

Q. Calculate the barrier potential of Si junction at (a) 100 °C and (b) at 0 °C if its value at 25 °C is 0.7 V.

Problem:

Q. Calculate the barrier potential of Si junction at (a)100 °C and (b) at 0 °C if its value at 25 °C is 0.7 V.

$$\Delta T = Change \text{ in } Temperature \text{ in } ^{\circ}\text{C}$$

$$= -25$$

$$\Delta V_B = -0.002 \times \Delta T$$

$$V_{B1} - V_{B2} = -0.002 \times 75 = -0.15$$

$$V_{B2} = 0.55$$

$$\Delta V_B = -0.002 \times \Delta T$$

$$V_{B1} - V_{B2} = -0.002 \times -25 = 0.05$$

$$V_{B2} = 0.75$$

Reverse biased p-n junction:

i. ***A reversed biased 'off' condition is obtained by applying a negative potential to the p-side of the junction and positive potential to the n-side.***

ii. *The application forward bias will cause the electrons and holes driven towards the junction where they recombine and will reduce the width of the depletion region . The resulting minority carrier flow of electrons from p to n will not change, but the reduction of depletion layer will create large amount of current flow across junction.*

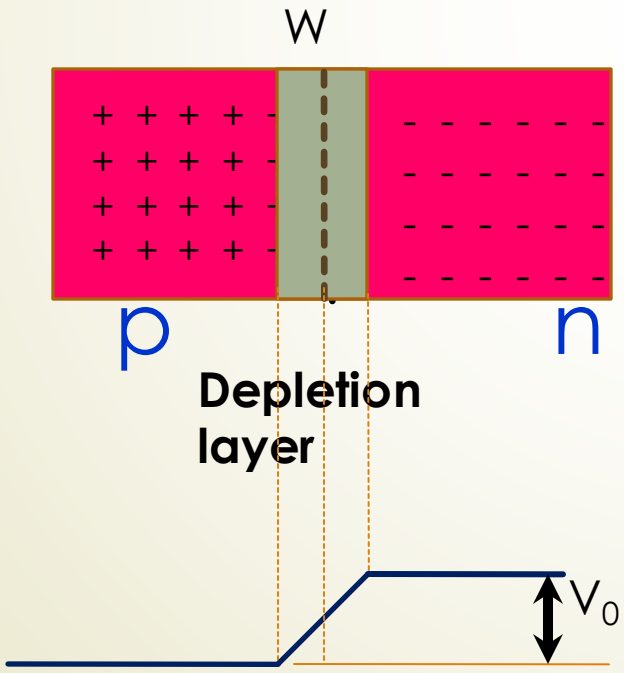
Reverse biased p-n junction:

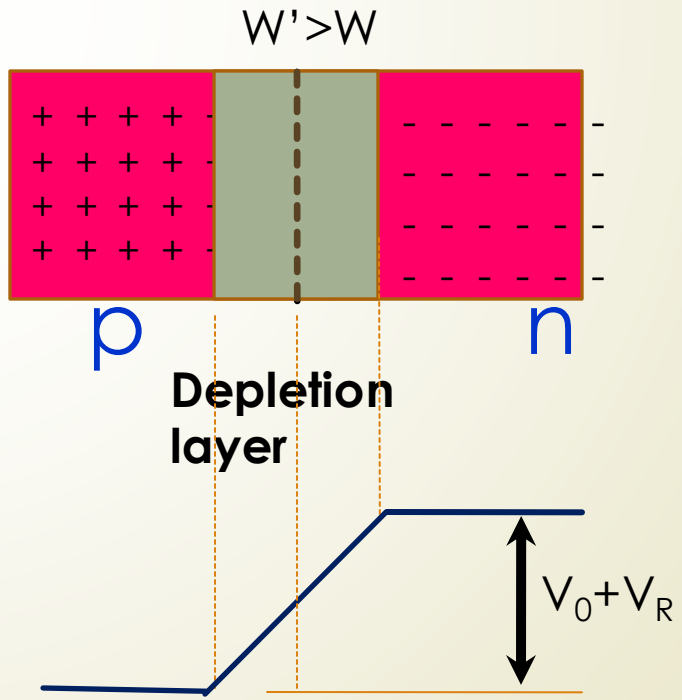
i. ***A reversed biased 'off' condition is obtained*** *by applying a negative potential to the p-side of the junction and positive potential to the n-side.*

ii. *The application forward bias will cause the electrons and holes attracted by the positive and negative battery terminals. Both electrons and holes move away from junction and away from each other*

iii. *No current flows and junction offers high resistance*

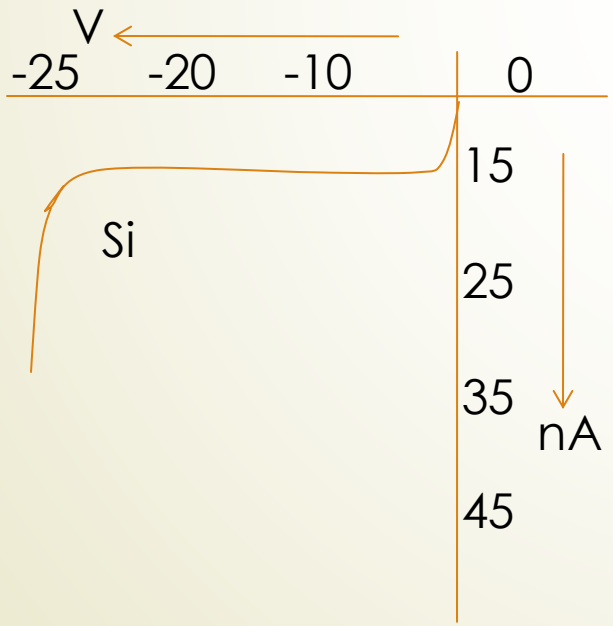
iv. *Under this condition depletion width increases and also barrier potential increases.*

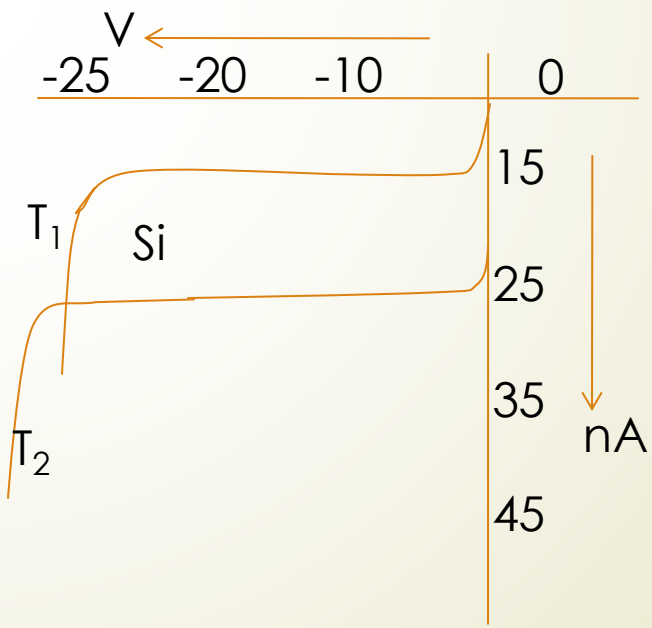




Reverse saturation current:

i. Although under reverse bias no current flows due to majority of carriers
ii. There is small amount of current (a few Pico-amp—micro-amp) flows due minority charge carriers generated by thermal agitation.
iii. This current is called reverse saturation current, I_s.
iv. Since minority carriers are thermally generated, the reverse current is extremely temperature dependent.
v. I_s is found doubled for every 10 degree C rise in temperature in Ge and for every 6 degree C rise in temperature for Si.





Equation of diode/ diode Shockley's equation:

The general characteristics of a semiconductor diode can be defined by the following equations for the forward and reverse biased region

$$I_D = I_S (e^{V_D / nV_T} - 1)$$

I_D= diode current
I_s= Reverse saturation current
V_D= applied forward bias across junction
n= ideality factor; function of operating condition or physical construction, its value is generally considered 1.
V_T= thermal voltage

$$V_T = \frac{kT}{q}$$

K= is the bothzmann constant 1.38×10^{-23} J/K
q= magnitude of electronic charge 1.6×10^{-19} C
T= absolute temperature in Kelvin

Equation of diode/ diode Shockley's equation:

The general characteristics of a semiconductor diode can be defined by the following equations for the forward and reverse biased region

$$I_D = I_S (e^{V_D / nV_T} - 1) \qquad (1.1)$$

For forward bias or positive value of V_D, equation 1.1 will become

$$I_D \cong I_S e^{V_D / nV_T} \qquad (1.2)$$

For negative value of V_D, equation 1.1 will become

$$I_D \cong -I_S \qquad (1.3)$$

At zero voltage $I_D = I_S (e^0 - 1) = 0 \qquad (1.4)$

We know for forward bias or positive value of V_{D1}, diode current will become

$$I_{D1} \cong I_S e^{V_{D1}/nV_T}$$

If forward bias value is V_{D1}, diode current will become

$$I_{D1} \cong I_S e^{V_{D1}/nV_T}$$

The combination of the two equation will become

$$\frac{I_{D2}}{I_{D1}} = e^{\frac{V_{D2}-V_{D1}}{nV_T}}$$

$$V_{D2} - V_{D1} = nV_T \ln \frac{I_{D2}}{I_{D1}}$$

$$V_{D2} - V_{D1} = 2.3nV_T \log \frac{I_{D2}}{I_{D1}}$$

For a decade change in current diode voltage drop changes by $2.3nV_T$

Junction resistance/dynamic resistance:

We have found the dynamic resistance graphically. However, there is a basic definition:

The derivative of a function at a point is equal to the slop of the tangent line drawn at that point

Lets take the derivative of equation 1.1

$$\frac{d}{dV_D} I_D = \frac{d}{dV_D} I_S (e^{V_D / nV_T} - 1) \qquad (1.1)$$

$$\frac{d}{dV_D} I_D = \frac{1}{nV_T} (I_D + I_S), \qquad \text{in general } I_D >> I_S$$

$$\frac{d}{dV_D} I_D = \frac{1}{nV_T} I_D$$

$$\frac{dV_D}{dI_D} = r_d = \frac{nV_T}{I_D}$$

Substituting n=1 and V_T=26 mV $\quad r_d = r_j = \frac{26mV}{I_D}$

Dynamic rsistance $\quad r_{ac} = \frac{26mV}{I_D} + r_B$

Where r_B is the body resistance

$$\frac{d}{dV_D} I_D = \frac{d}{dV_D}[I_S(e^{V_D/nV_T} - 1)]$$

$$= \frac{d}{dV_D}[I_S e^{V_D/nV_T} - I_s] = \frac{I_s}{nV_T} e^{V_D/nV_T} = \frac{1}{nV_T}[I_s e^{V_D/nV_T}]$$

$$= \frac{1}{nV_T}[I_s e^{V_D/nV_T} - I_s + I_s]$$

$$== \frac{1}{nV_T}[I_s(e^{V_D/nV_T} - 1) + I_s]$$

$$\frac{d}{dV_D} I_D = \frac{1}{nV_T}(I_D + I_S), \qquad \text{in general } I_D >> I_S$$

$$\frac{d}{dV_D} I_D = \frac{1}{nV_T} I_D$$

nA

mA

In order to solve the diode circuits: We need to replace the diodes by its equivalent models:

1. **Ideal Model**

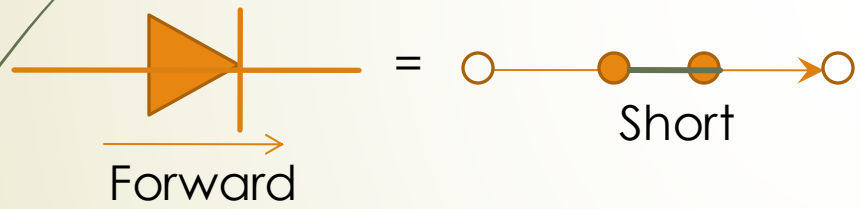
2. **Real Model**

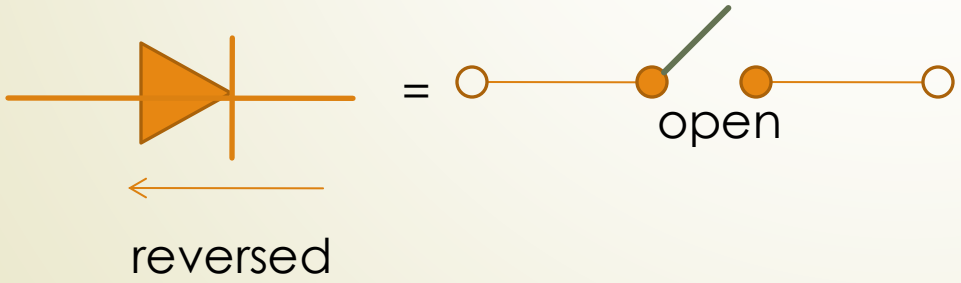
Ideal diode:

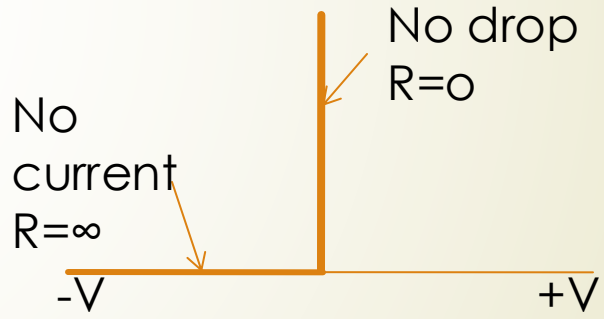
The terminal characteristics of an ideal diode can be interpreted as follows:

i. If a negative voltage is applied to diode, no current flows, the diode behaves as an open circuit. Diode in this mode is said to be reversed bias. It has zero current in the reverse direction and said to be **Cut-off.**

ii. If positive voltage is applied, zero voltage drop appear across diode and the diode behaves as short circuit. A forward/positive bias diode is said to be **Turned on**.



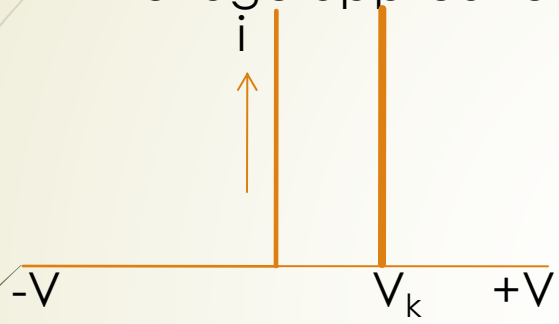




Real diode:

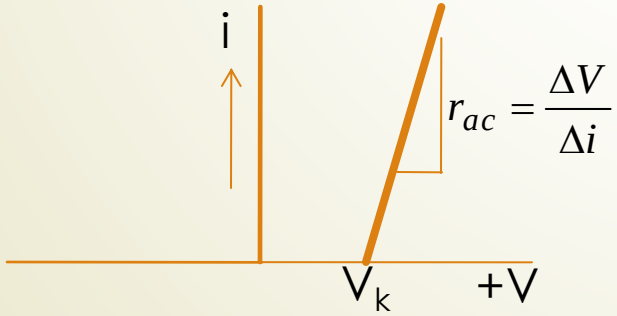
A real diode does not offer zero resistance in forward direction neither it offers infinite resistance in reverse direction

(a) First factor is that forward current does not start flowing until the voltage applied to the diode exceeds the knee voltage V_k



Simplified model

(b) Second factor is that forward dynamic or ac resistance (r_{ac}) offered by the circuit. If we take r_{ac} into account, the forward characteristics becomes

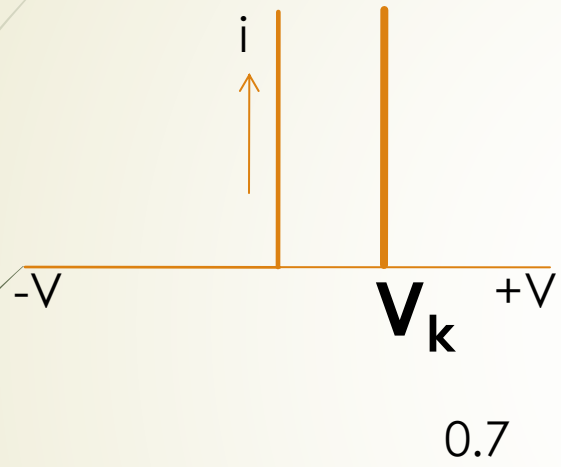


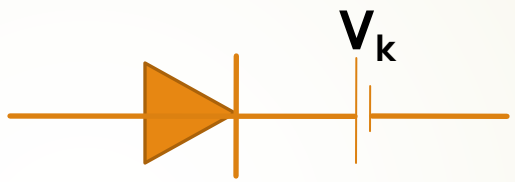
Piecewise linear model

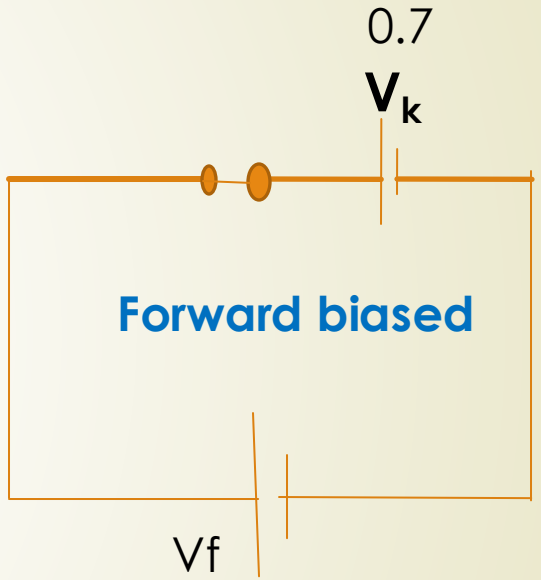
Real diode: 1. Simplified model

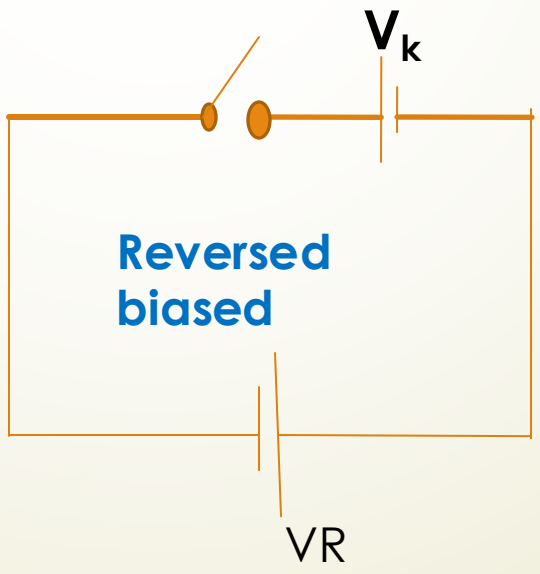
A real diode does not offer zero resistance in forward direction neither it offers infinite resistance in reverse direction

(a) First factor is that forward current does not start flowing until the voltage applied to the diode exceeds the knee voltage V_k





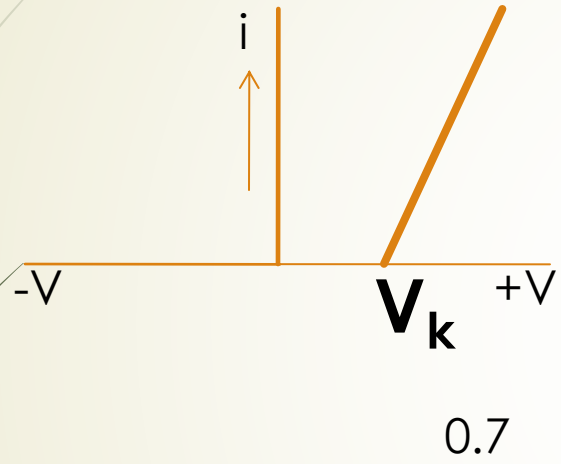


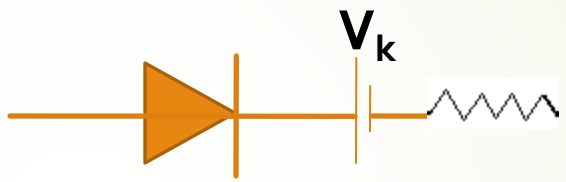


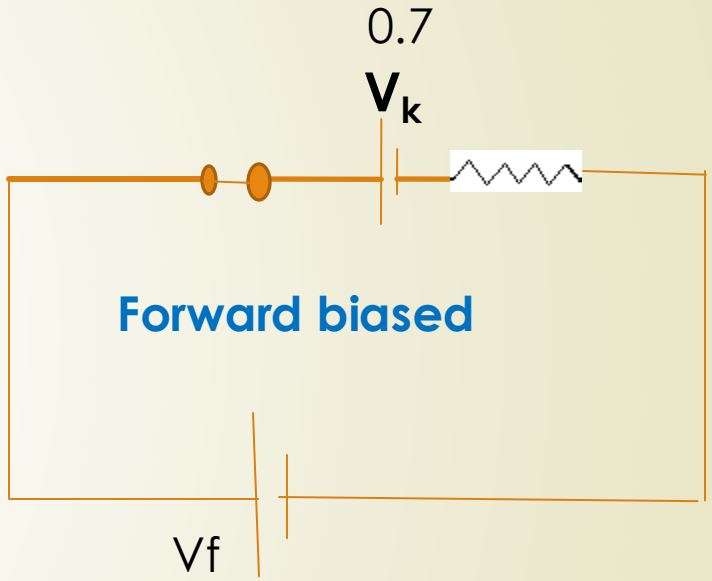
Real diode: 2. Piecewise linear model

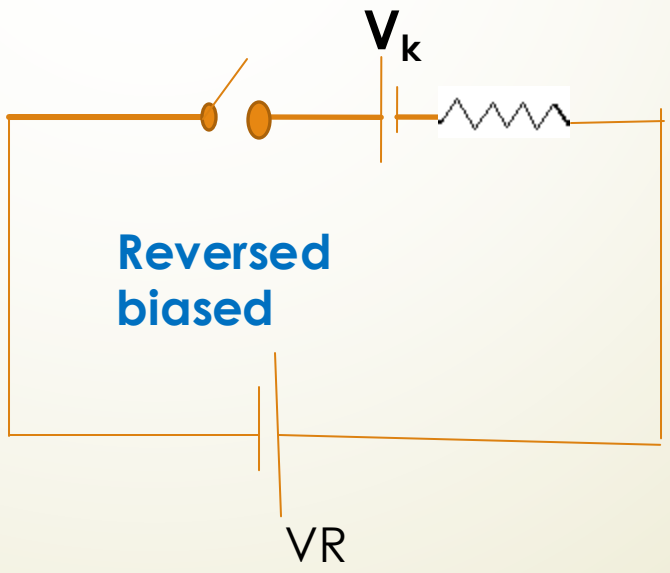
A real diode does not offer zero resistance in forward direction neither it offers infinite resistance in reverse direction

(a) First factor is that forward current does not start flowing until the voltage applied to the diode exceeds the knee voltage V_k

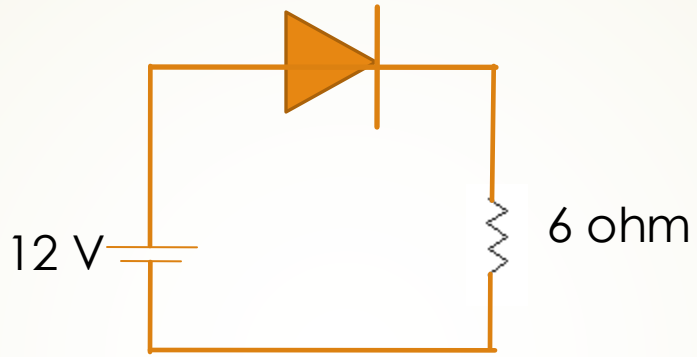




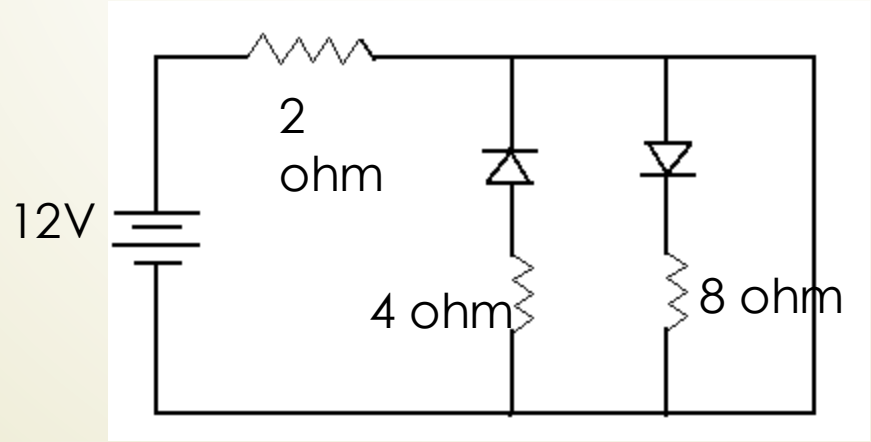




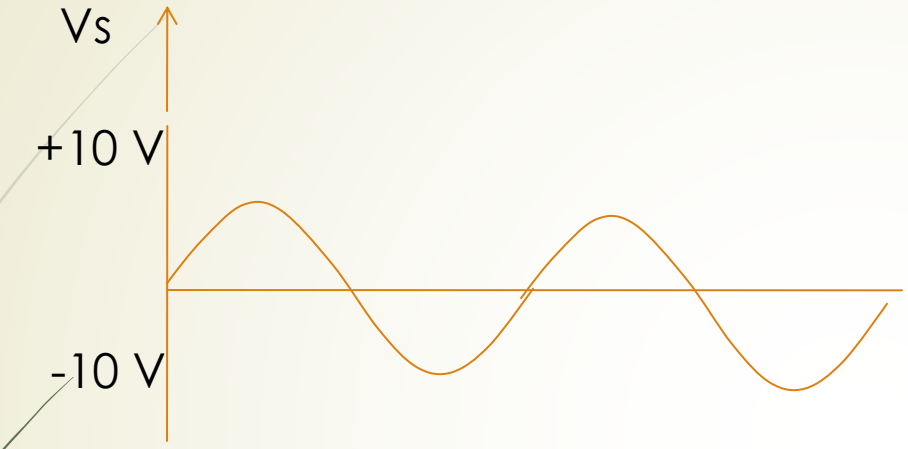
Q. Calculate the circuit current and power dissipated in the (a) ideal diode and (b) 6 ohm resistor of the circuit.

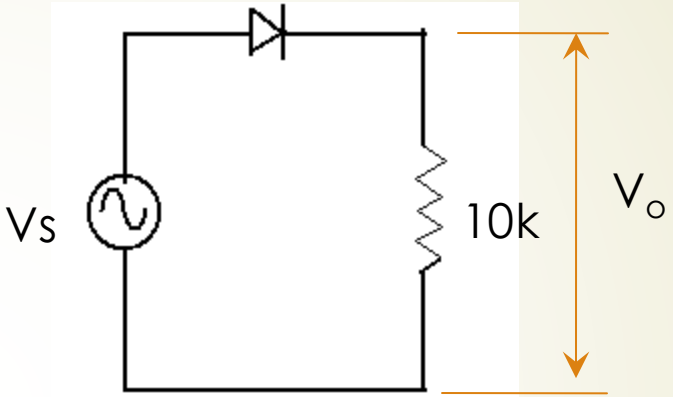


Q. Find the circuit current if any in the following circuit

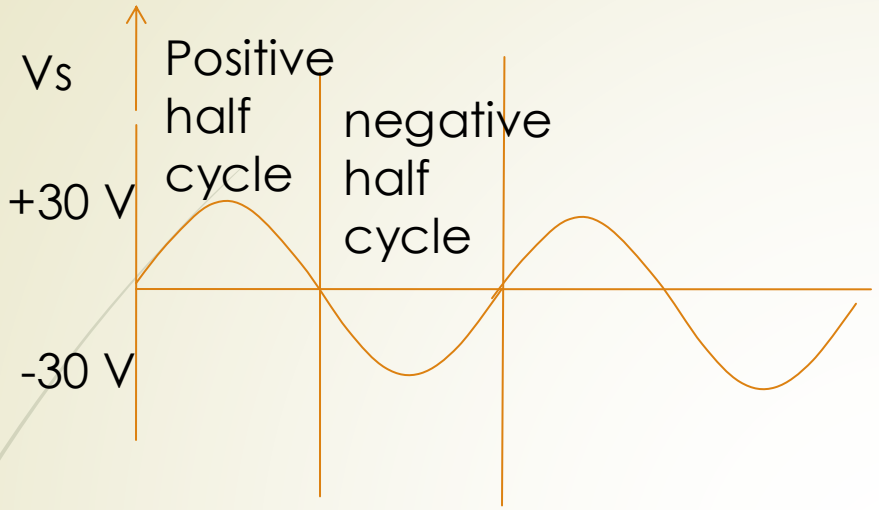


Q. Sketch the waveform of voltage V_o across 10K

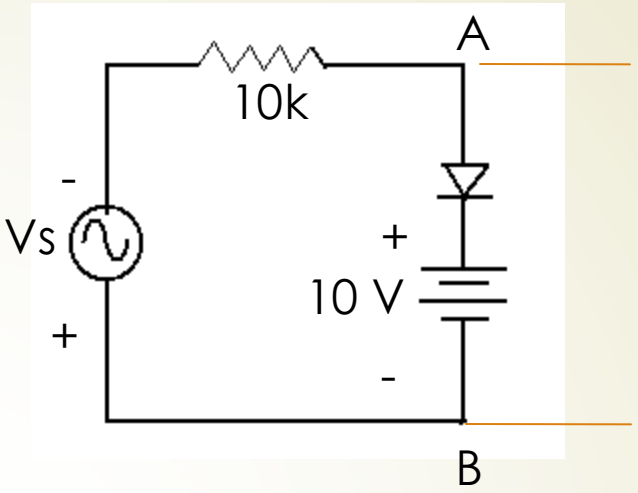




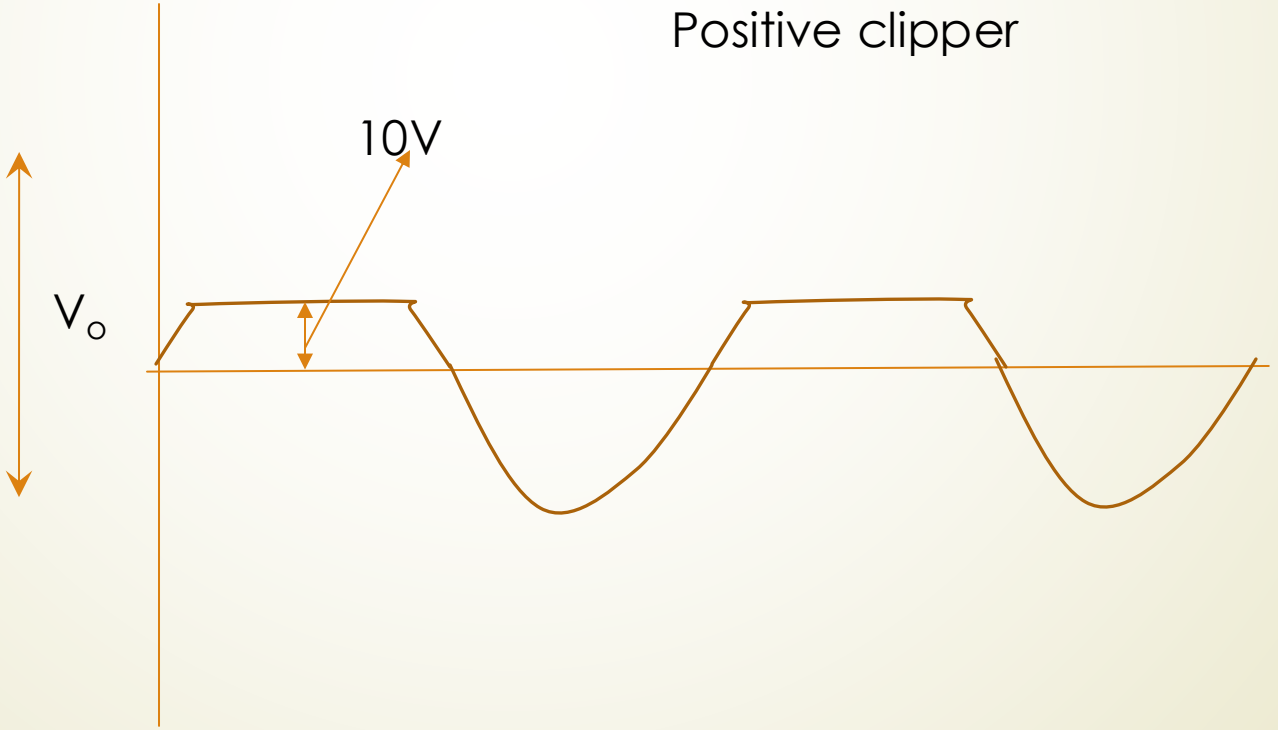
Q. Sketch the waveform of voltage V_o



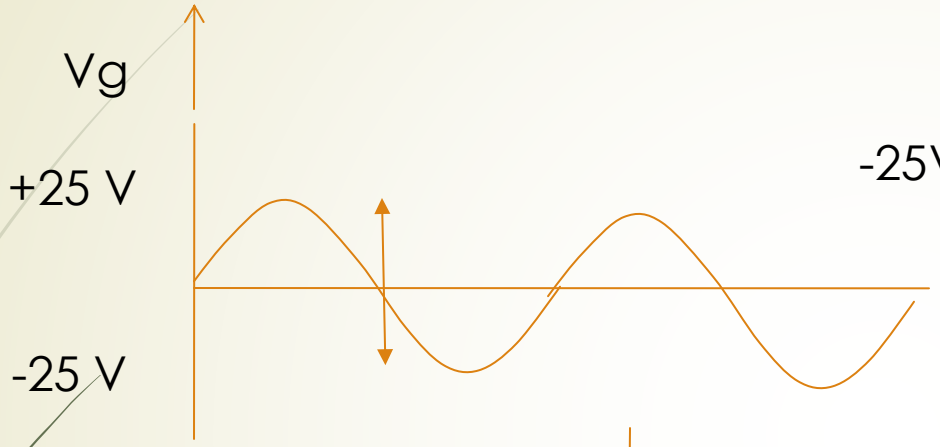
V(p-p)
=60 V

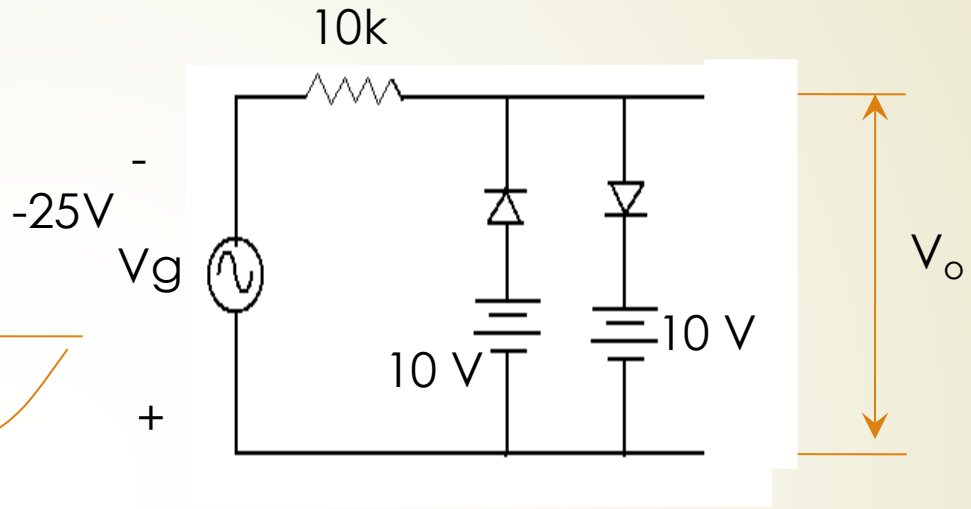


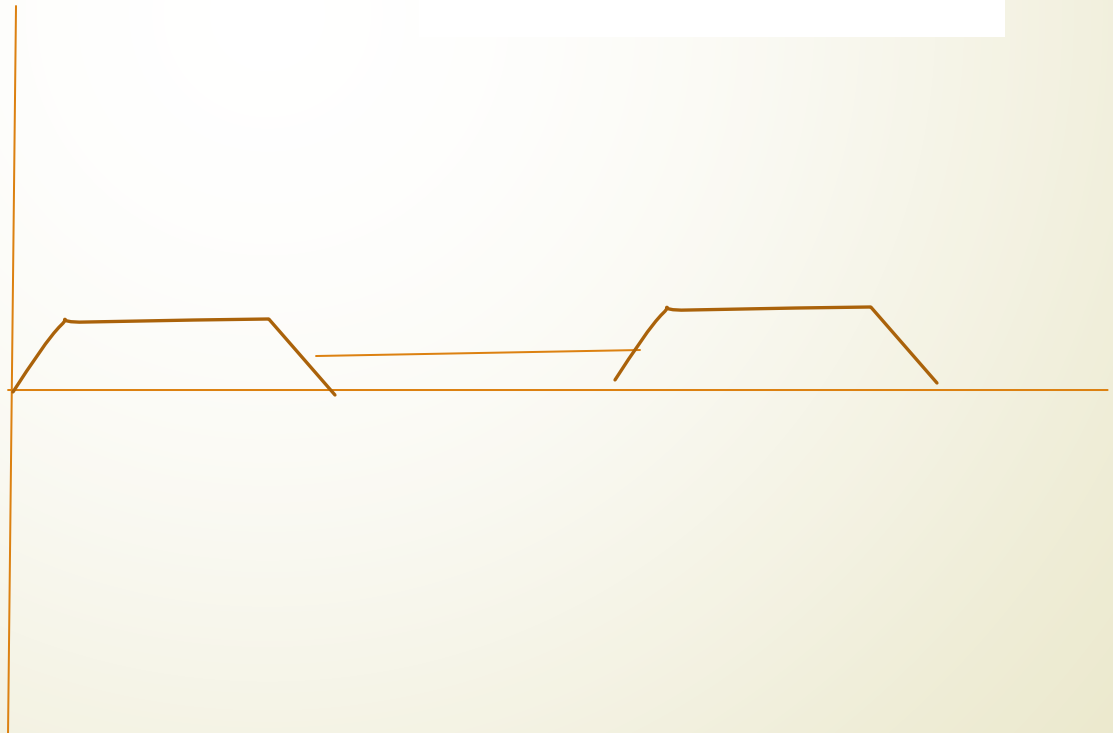
Positive clipper



Q. Sketch the waveform of voltage V_o across 10K







Determine V_o, I_1, I_{D_1}, and I_{D_2} for the parallel diode configuration

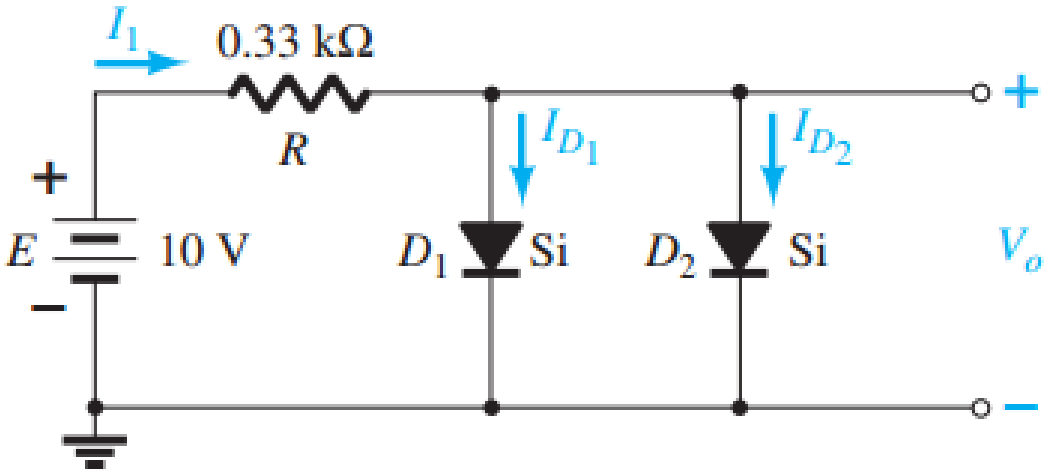


FIG. 2.28

I_1= 10-0.7/0.33k=28 mA
Vo=0.7 V
Id1=Id2=28/2=14 mA

EXAMPLE 2.9 Determine I, V_1, V_2, and V_o for the series dc configuration of Fig. 2.25.

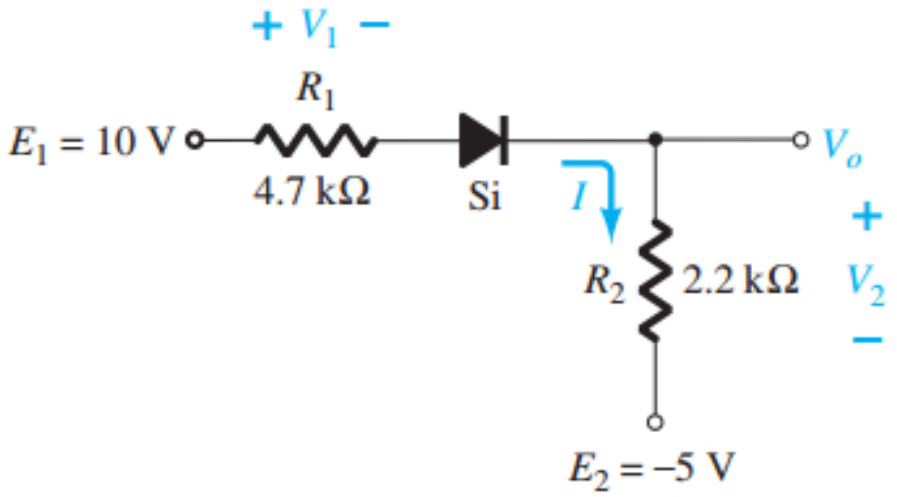


FIG. 2.25

10+5-0.7=14.3 V
Current=14.3/(4.7+2.2)
V2=currentX2.2
Vo=V2-5

***9.** Determine V_{o_1} and V_{o_2} for the networks of Fig. 2.159.

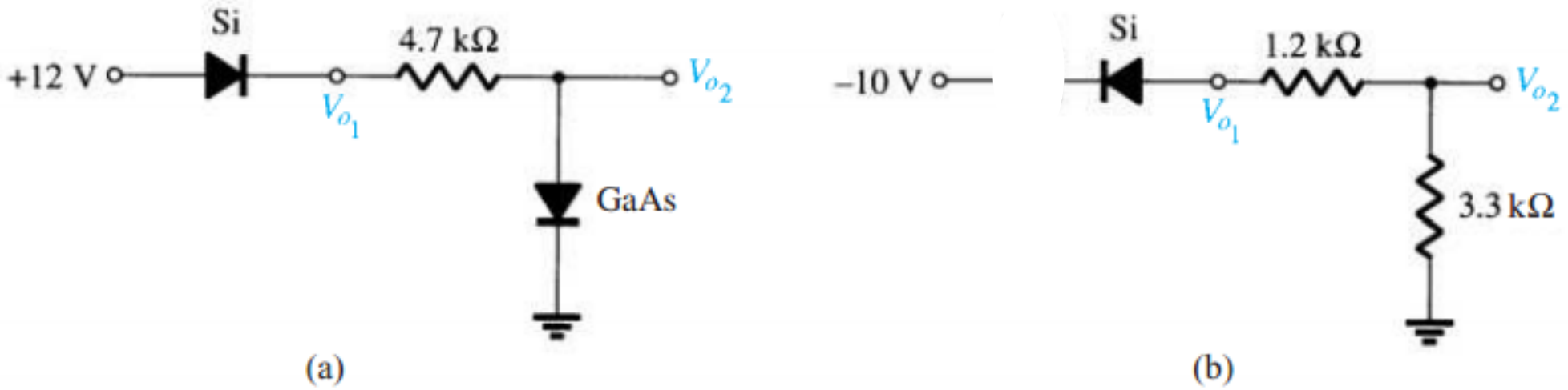


FIG. 2.159

12-(Vk+Vk)=12-(0.7+1.2)=10 V

Vo2=1.2 V

Vo1=1.2 + 10=11.2

Vo1=0

Vo2=0

EXAMPLE 2.9 Determine I, V_1, V_2, and V_o for the series dc configuration of Fig. 2.25.

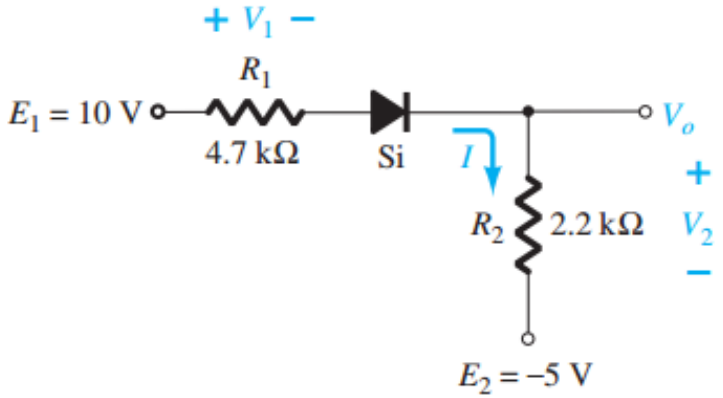


FIG. 2.25

Determine V_o, I_1, I_{D_1}, and I_{D_2} for the parallel diode configuration

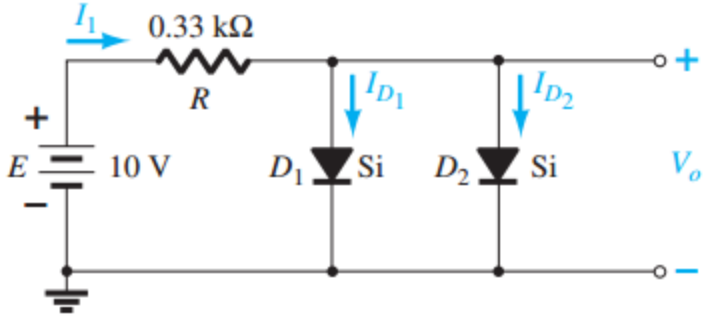


FIG. 2.28

***9.** Determine V_{o_1} and V_{o_2} for the networks of Fig. 2.159.

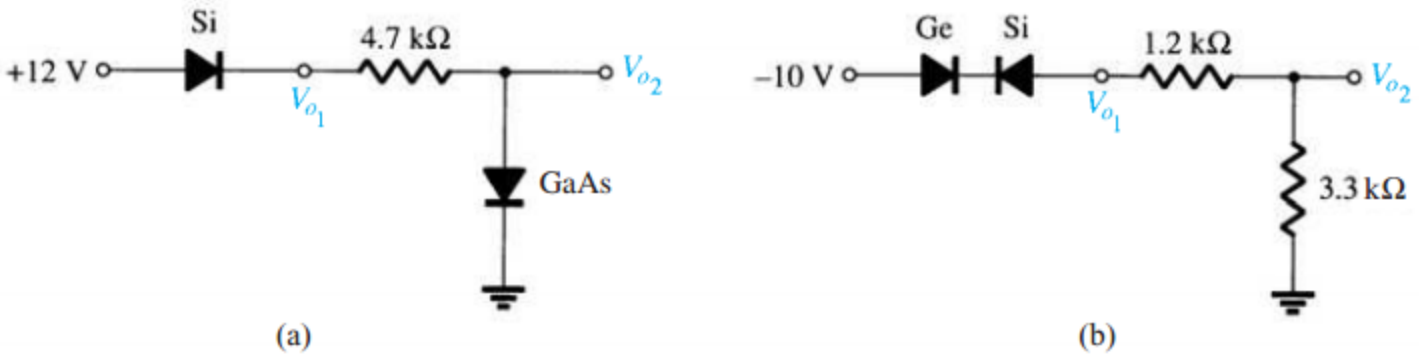


FIG. 2.159

10. Determine V_o and I_D for the networks of Fig. 2.160.

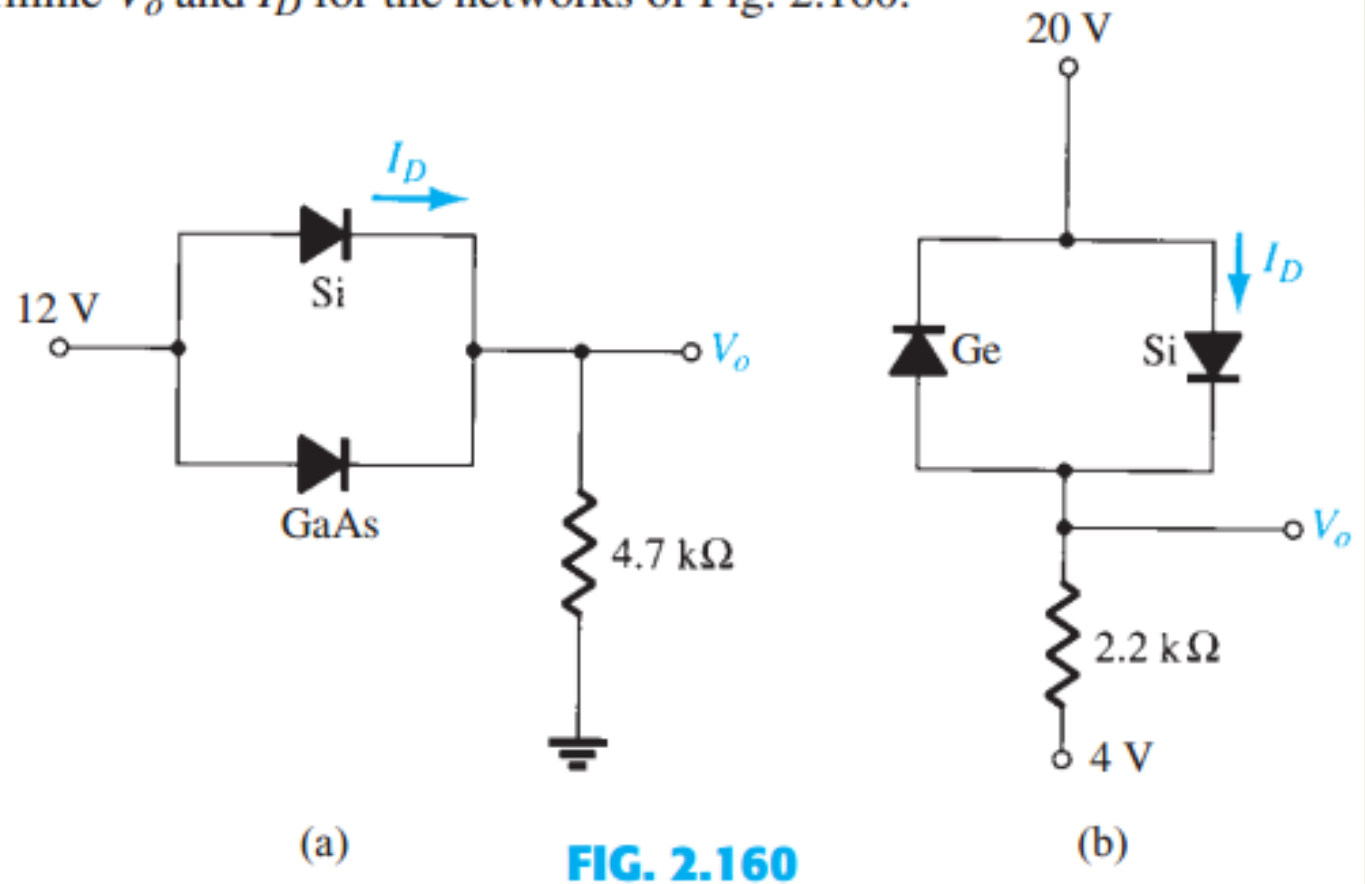


FIG. 2.160

Net effective voltage 16 Volt

Vo=11.3

Current=(16-0.7)/2.2
Vo=6.9x2.2 +4 =

***11.** Determine V_o and I for the networks of Fig. 2.161.

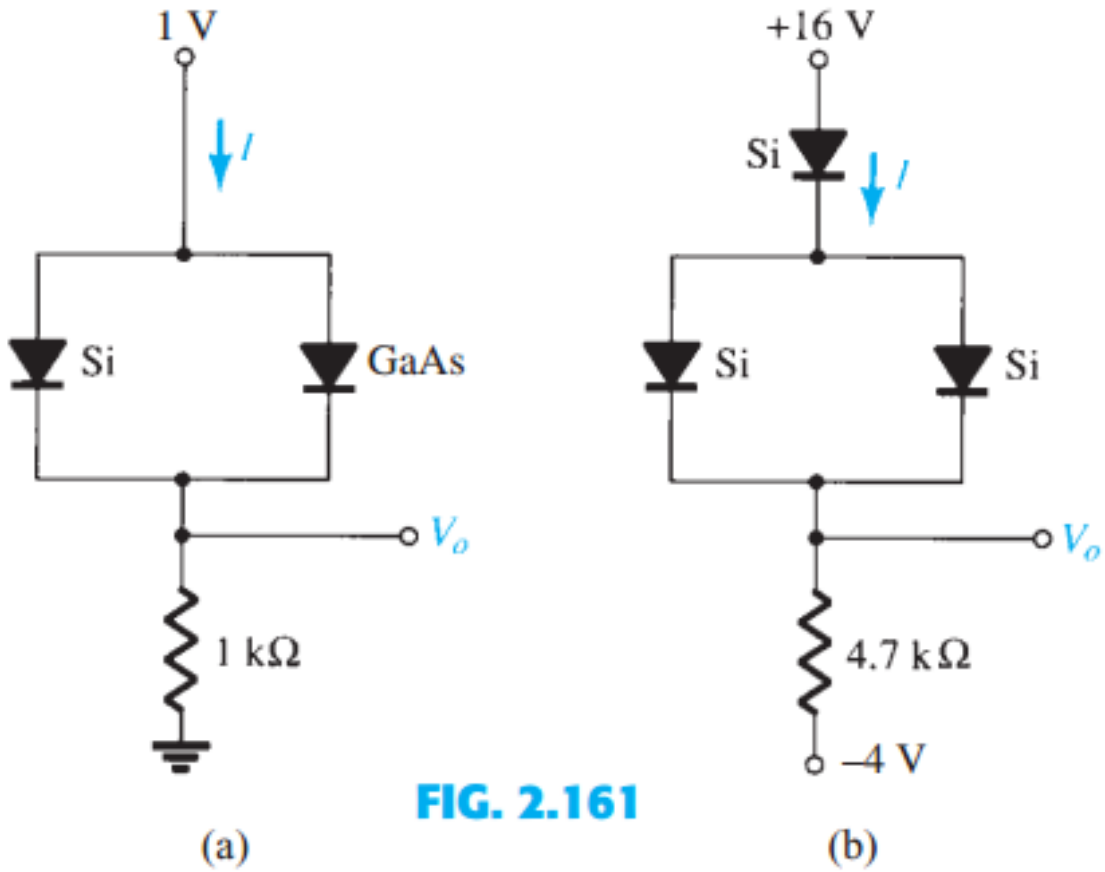


FIG. 2.161

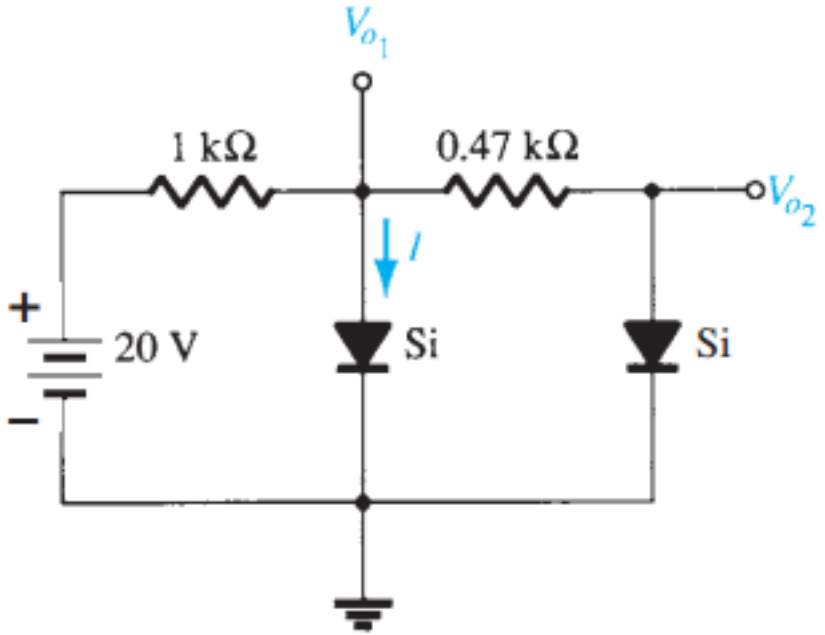


FIG. 2.162

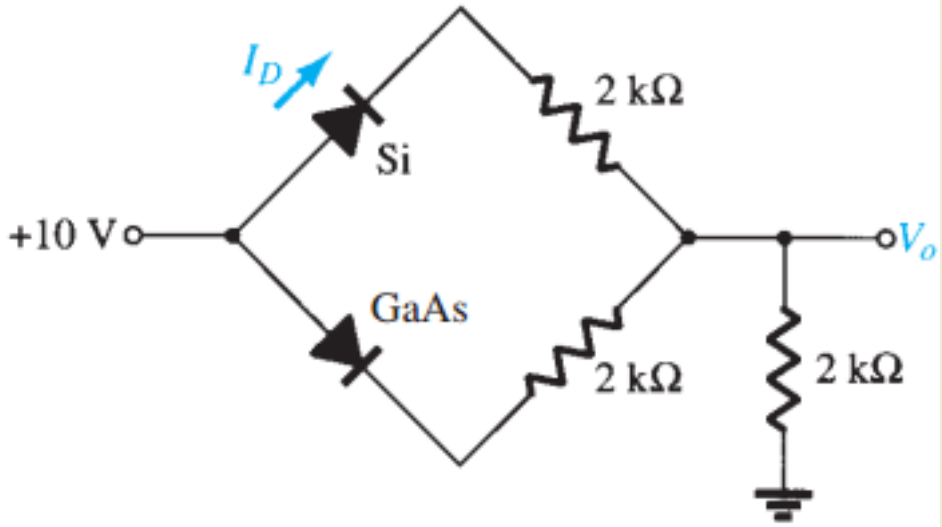


FIG. 2.163

Example 6.9. *Determine the currents I_1, I_2 and I_3 for the network shown in Fig. 6.16(i). Use simplified model for the diodes.*

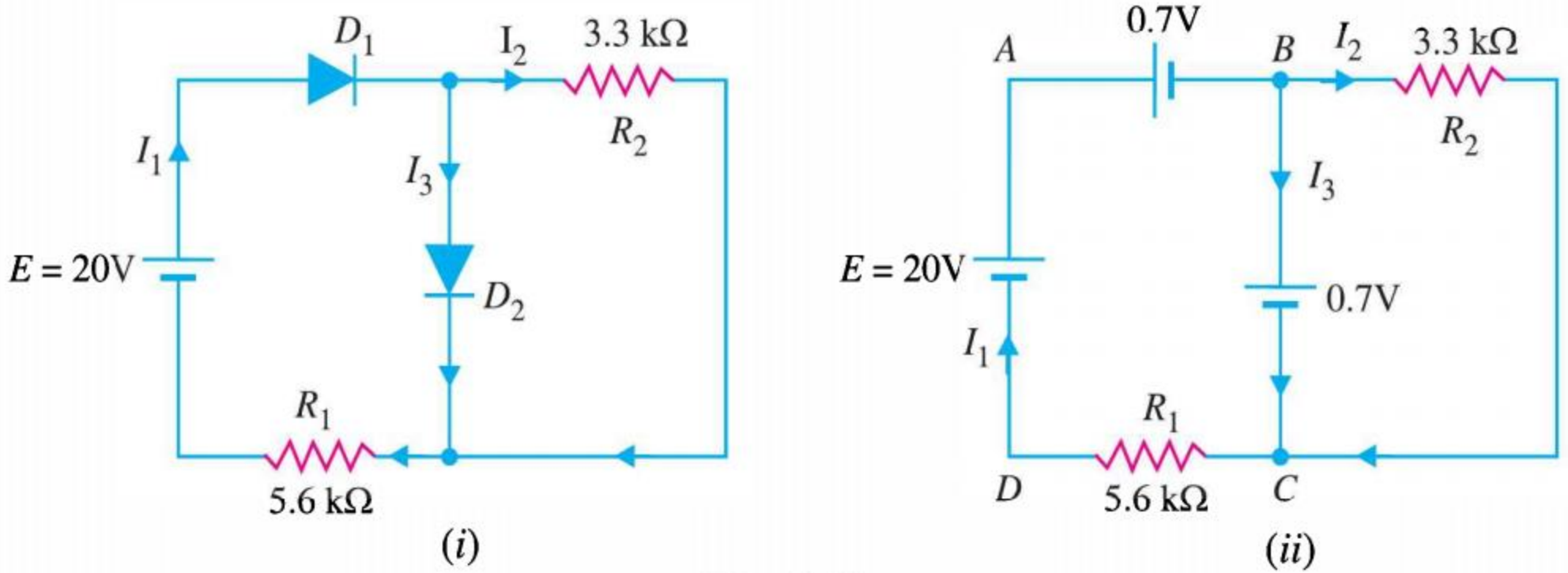
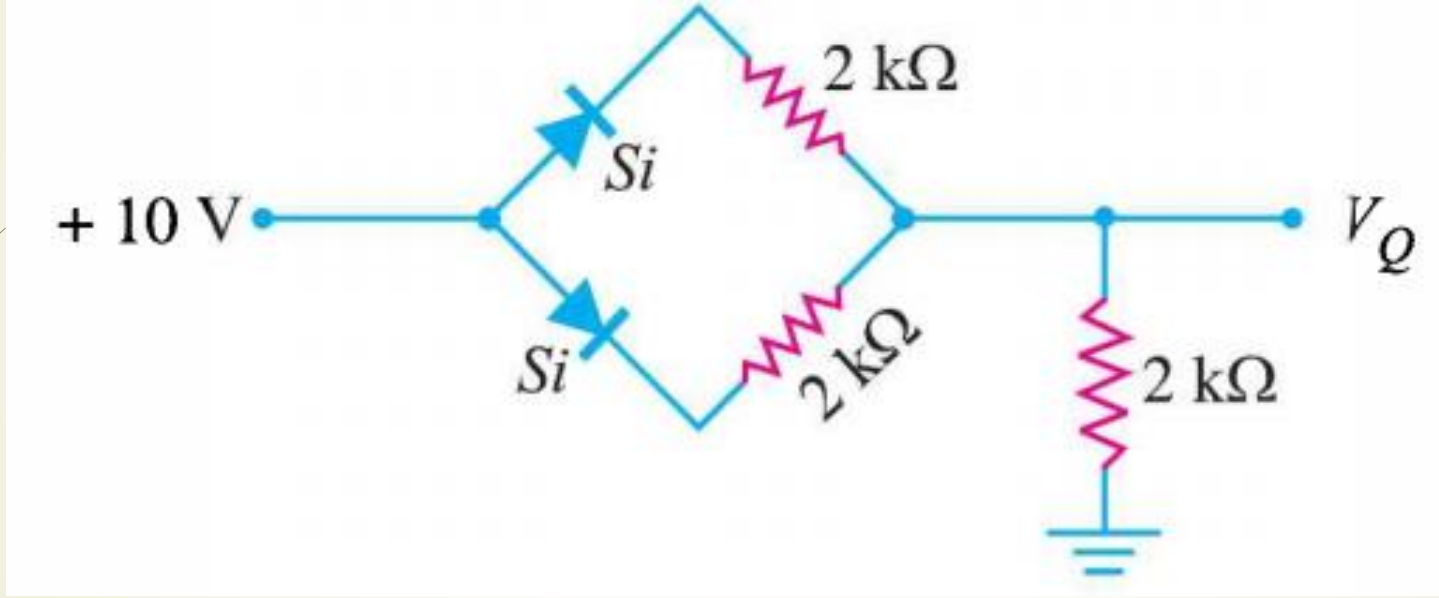
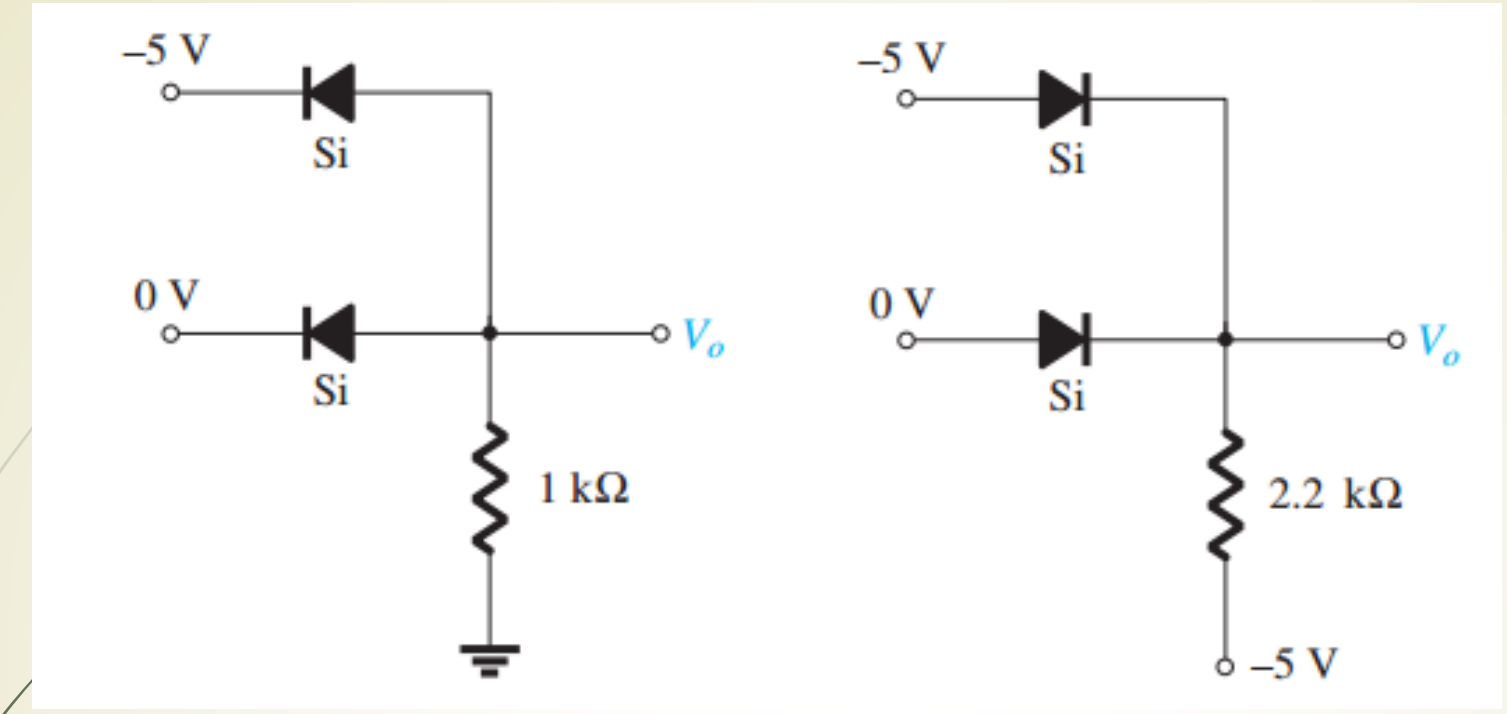


Fig. 6.16


+ 10 V
Si
Si
2 kΩ
2 kΩ
2 kΩ
V_o


–5 V
Si
0 V
Si
V_o
1 kΩ
–5 V
Si
0 V
Si
V_o
2.2 kΩ
–5 V

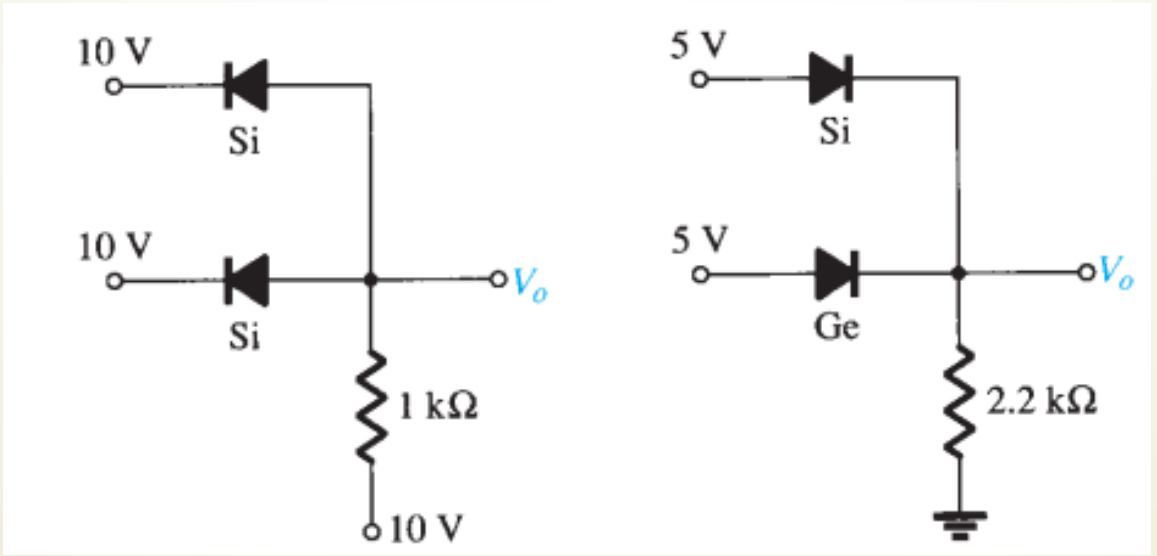
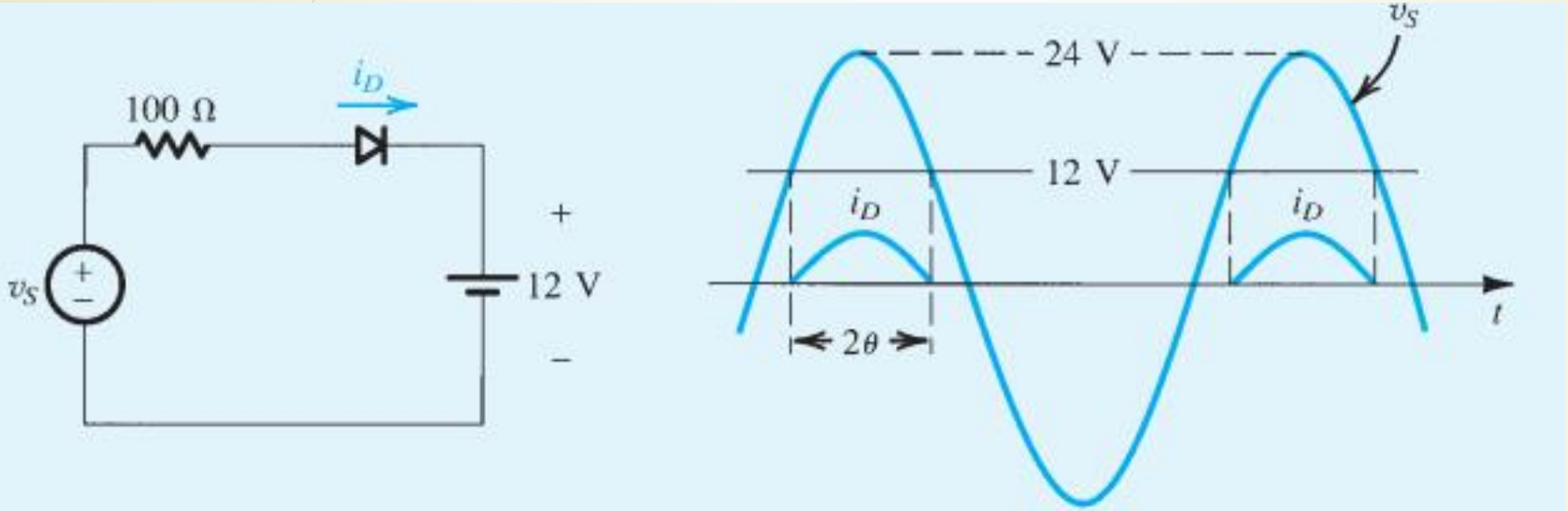

10 V
Si
10 V
Si
V_o
1 kΩ
10 V
5 V
Si
5 V
Ge
V_o
2.2 kΩ

Figure 4.4(a) shows a circuit for charging a 12-V battery. If ***V***s is a sinusoid with 24-V peak amplitude, find the fraction of each cycle during which the diode conducts. Also, find the peak value of
the diode current and the maximum reverse-bias voltage that appears across the diode.



(a)

Figure 4.4 Circuit and waveforms for Example 4.1.

Solution

The diode conducts when v_s exceeds 12 V, as shown in Fig. 4.4(b). The conduction angle is 2θ, where θ is given by

$$24 \cos\theta = 12$$

Thus $\theta = 60°$ and the conduction angle is 120°, or one-third of a cycle.

The peak value of the diode current is given by

$$I_d = \frac{24 - 12}{100} = 0.12 \text{ A}$$

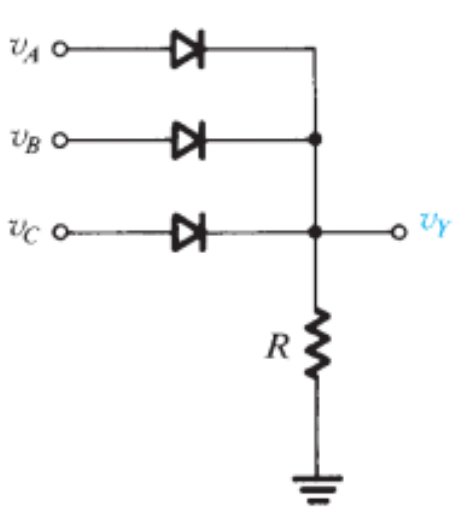
The maximum reverse voltage across the diode occurs when v_s is at its negative peak and is equal to $24 + 12 = 36$ V.

Another Application: Diode Logic Gates

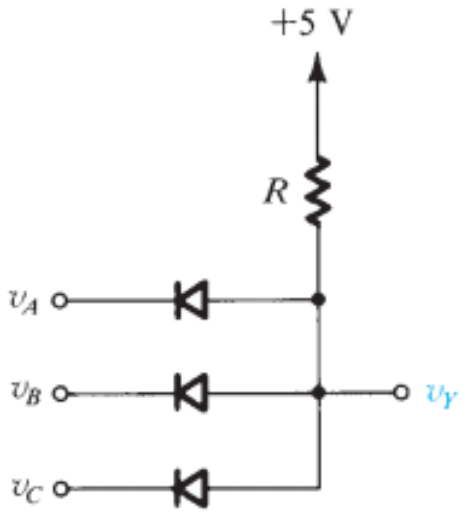
Figure 4.5 shows two diode logic gates. To see how these circuits function, consider a positive-logic system in which voltage values close to 0 V correspond to logic 0 (or low) and voltage values close to +5 V correspond to logic 1 (or high). The circuit in Fig. 4.5(a) has three inputs, V_A, V_B , and V_C. It is easy to see that diodes connected to +5-V inputs will conduct, thus clamping the output V_Y to a value equal to +5 V. This positive voltage at the output will keep the diodes whose inputs are low (around 0 V) cut off. Thus the output will be high if one or more of the inputs are high. The circuit therefore implements the logic OR function, which in Boolean notation is expressed as the circuit of Fig. 4.5(b) implements the logic AND function,

Y (A B C) = A+B+C

Y A B C = A·B·C



(a)



(b)

Figure 4.5 Diode logic gates: **(a)** OR gate; **(b)** AND gate (in a positive-logic system).

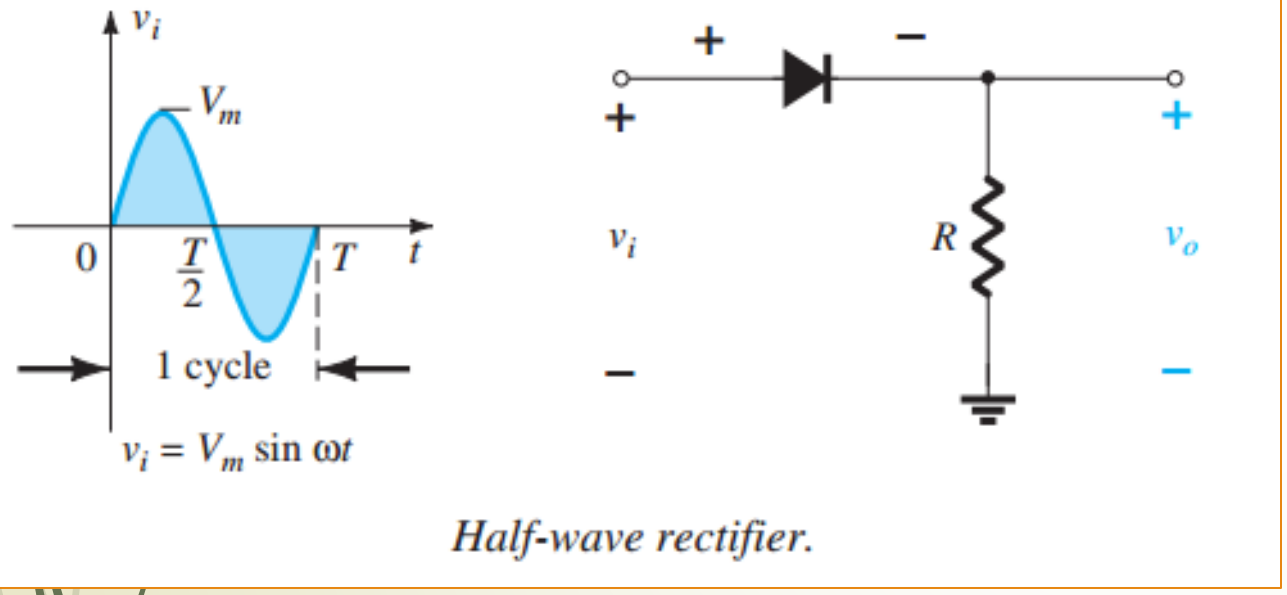
Rectifier:

1. Half wave rectifier

2. Full wave rectifier

1. SINUSOIDAL INPUTS; HALF-WAVE RECTIFICATION:

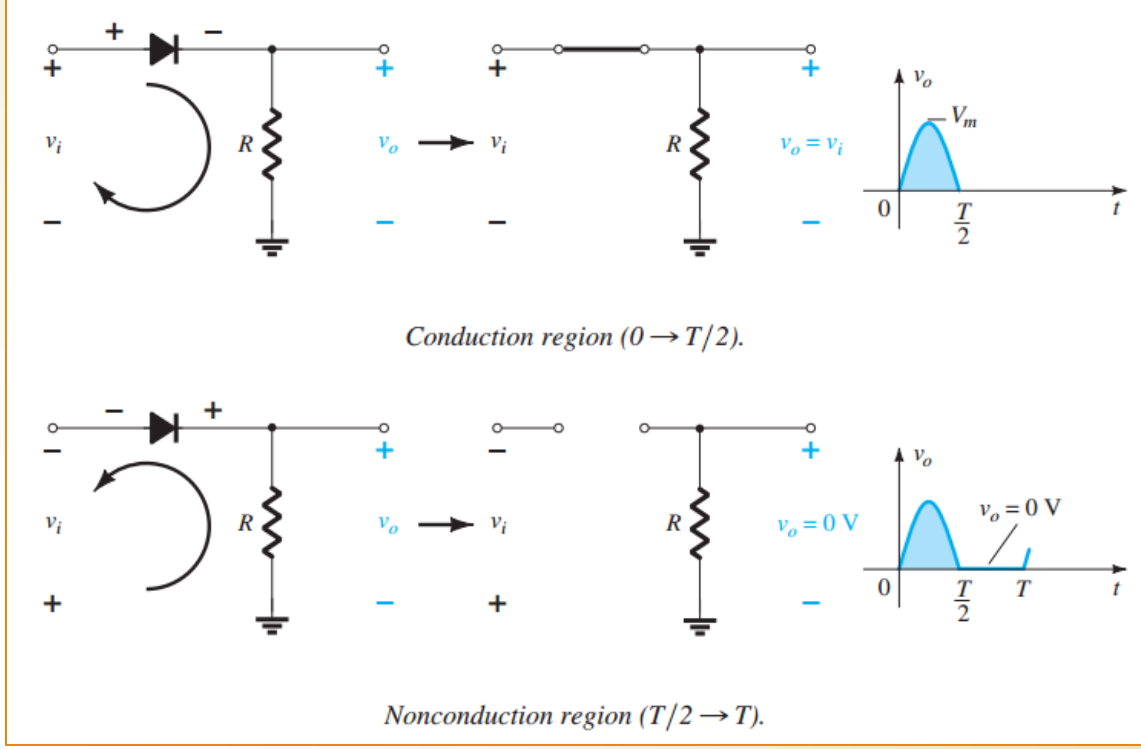
The process of removing one-half the input signal to establish a dc level is called *halfwave rectification*.



Half-wave rectifier.

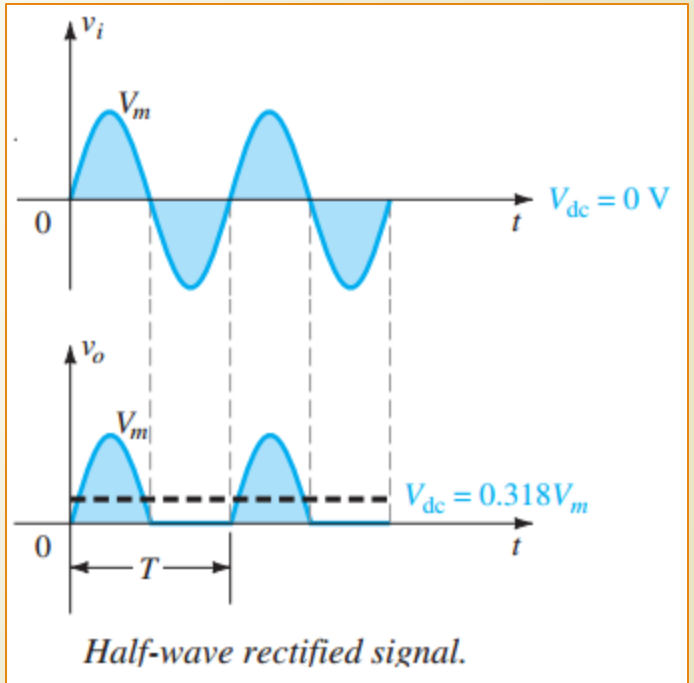
a full period and an average value determined by

$$V_{dc} = 0.318\,V_m$$



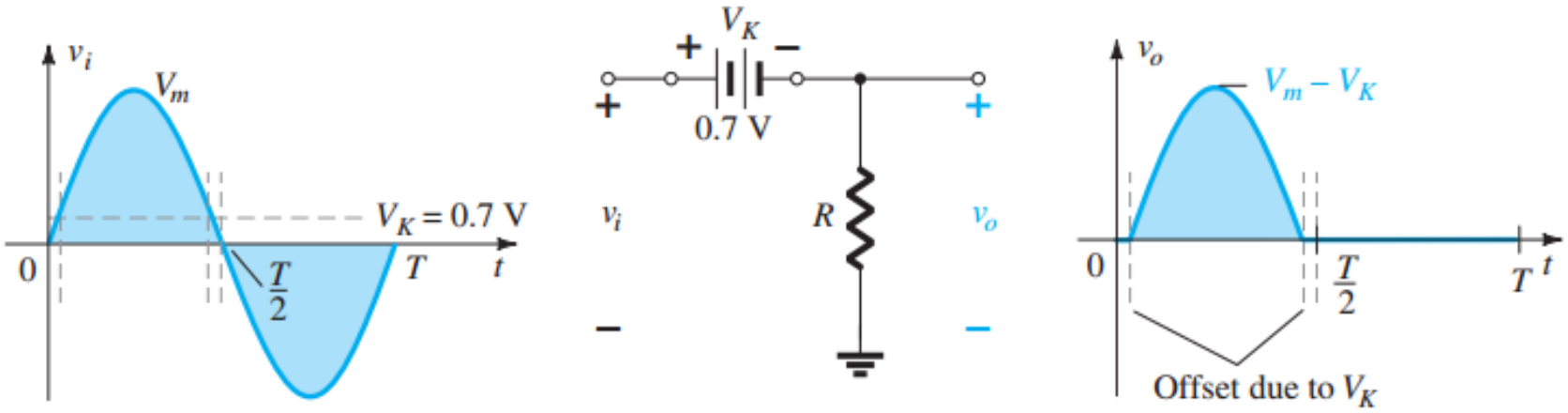
Conduction region ($0 \rightarrow T/2$).

Nonconduction region ($T/2 \rightarrow T$).



Half-wave rectified signal.

The effect of using a silicon diode with $V_K = 0.7$ V is demonstrated in Fig. 2.48 for the forward-bias region. The applied signal must now be at least 0.7 V before the diode can turn "on." For levels of v_i less than 0.7 V, the diode is still in an open-circuit state and $v_o = 0$ V, as shown in the same figure. When conducting, the difference between v_o and v_i is a fixed



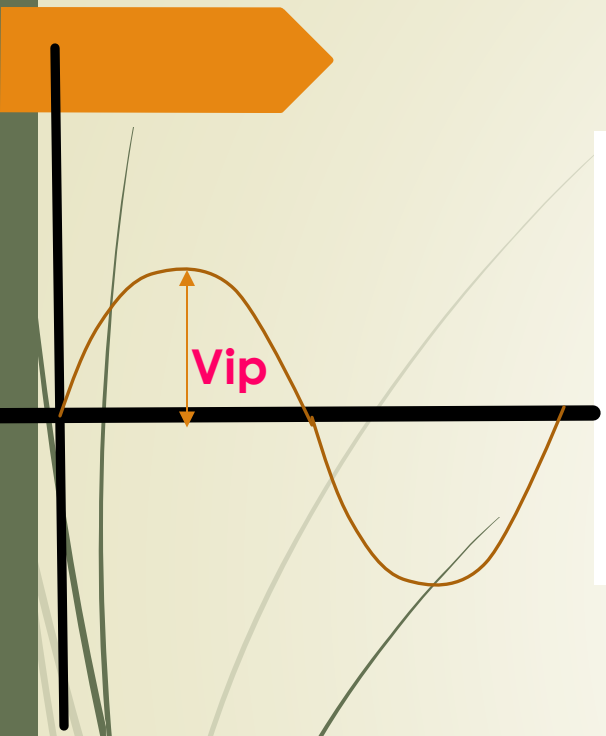
Effect of V_K on half-wave rectified signal.

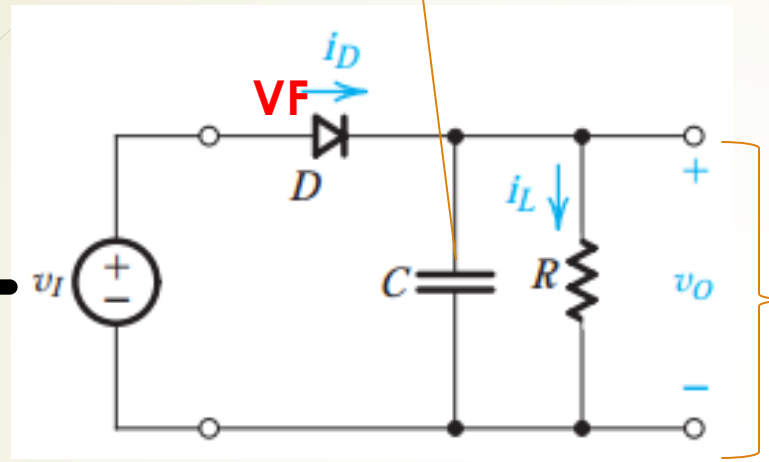
level of $V_K = 0.7$ V and $v_o = v_i - V_K$, as shown in the figure. The net effect is a reduction in area above the axis, which reduces the resulting dc voltage level. For situations where $V_m \gg V_K$, the following equation can be applied to determine the average value with a relatively high level of accuracy.

$$V_{dc} \cong 0.318(V_m - V_K)$$

In fact, if V_m is sufficiently greater than V_K, Eq. (2.7) is often applied as a first approximation for V_{dc}.

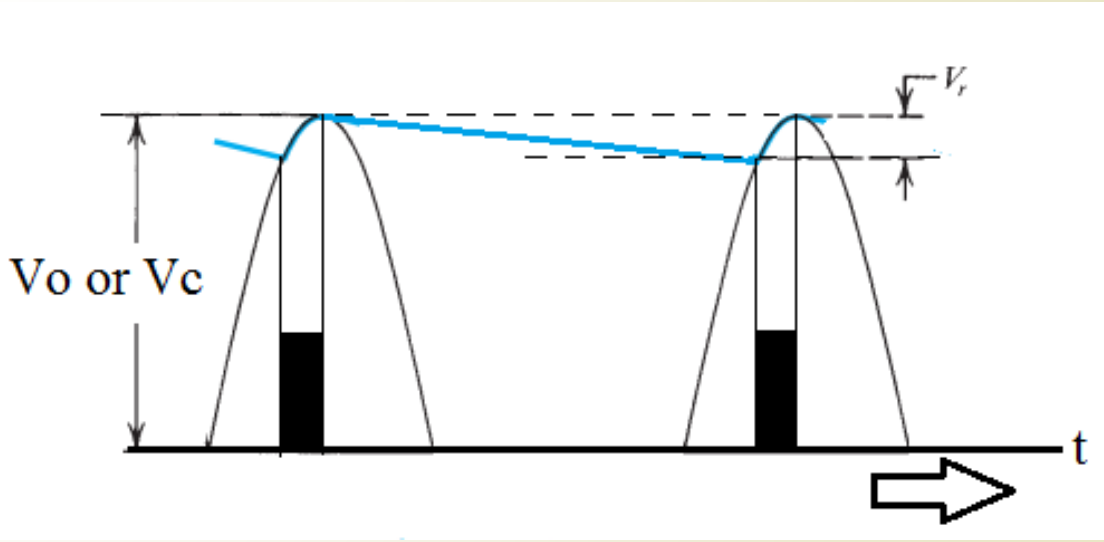
Half wave rectifier circuit: Capacitor reservoir, capacitor filter circuit:



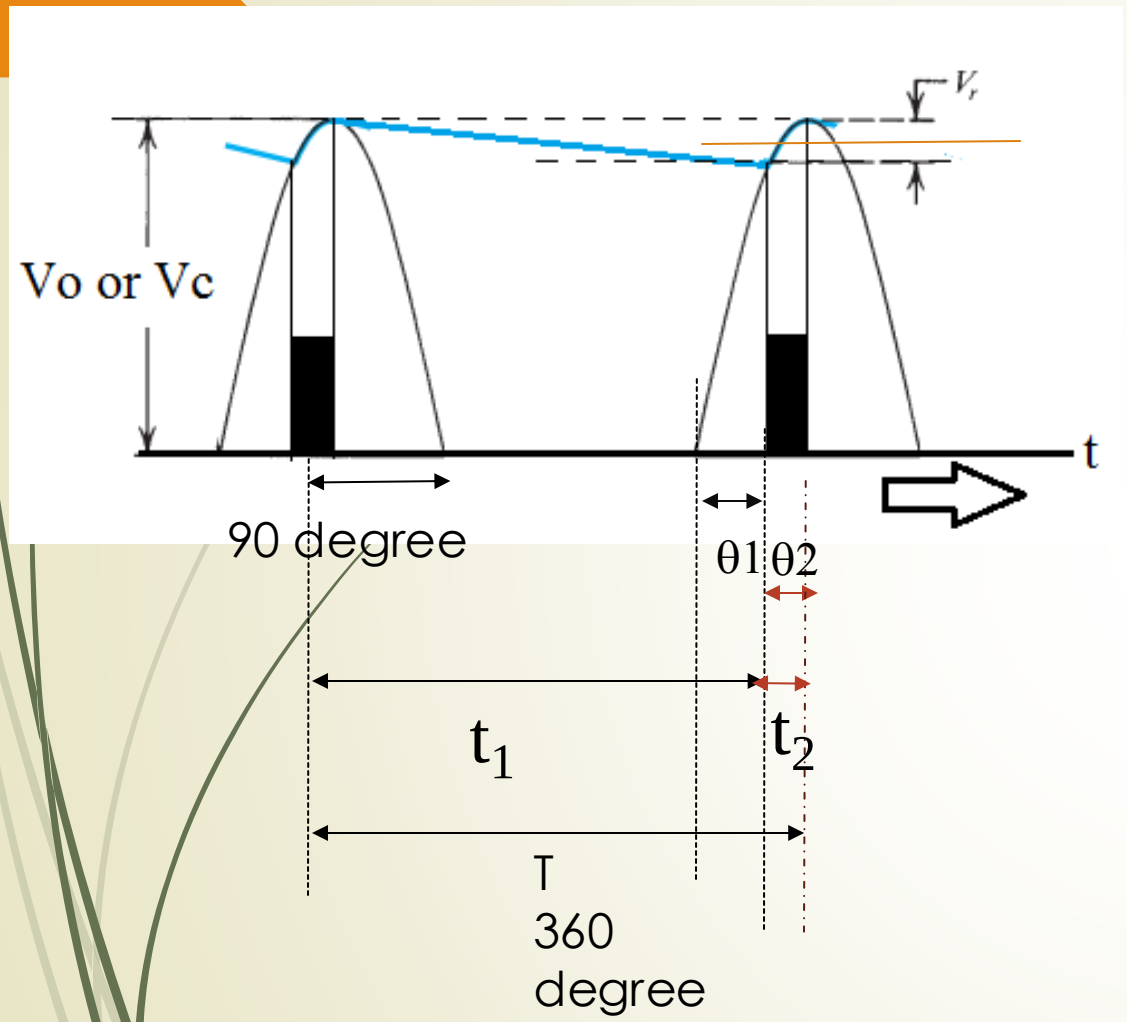


Vc=Vip - VF

When the instantaneous level of input drops below the Vpi, The diode becomes reverse bias. There is no capacitor charging current and the capacitor begins to discharge through the load R.



Ripple amplitude and capacitance:



E_{ave}= Average DC output voltage

$E_{o(max)}$= maximum DC output voltage

$E_{o(min)}$= minimum DC output voltage

V_r= ripple pick to peak Voltage

T= total time period

t_1=discharging time

t_2=charging time

θ_1=phase angle of input wave from 0 to $E_{o(min)}$

θ_2= phase angle of input wave from $E_{o(min)}$ to Eo(max)

$\mathbf{E_{o(min)} = E_{o(max)} Sin\theta_1}$

$\mathbf{\theta_1 = sin^{-1}(E_{o(min)} / E_{o(min)})}$

$\mathbf{\theta_1 = 90^0 - \theta_1}$

$$t_2 = \frac{\theta_2 T}{360}$$

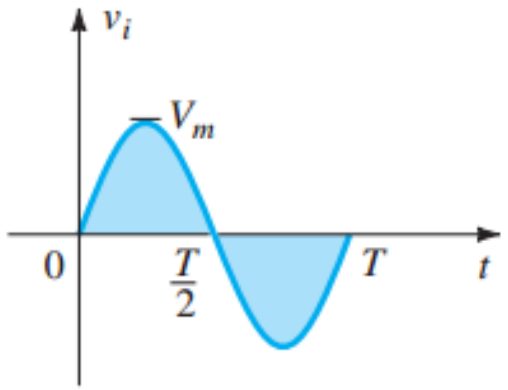
$$t_1 = T - t_2$$

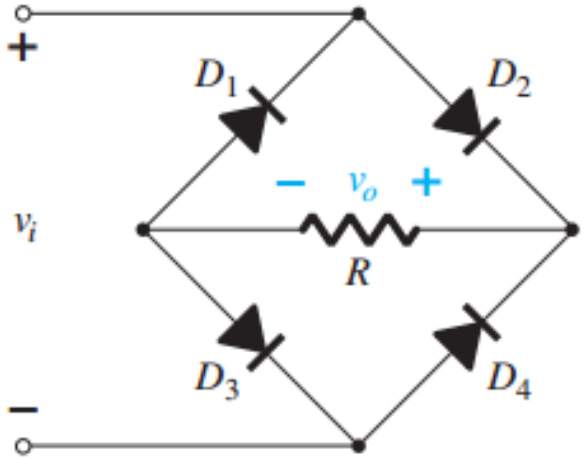
$$C = \frac{I_L t_1}{V_r}$$

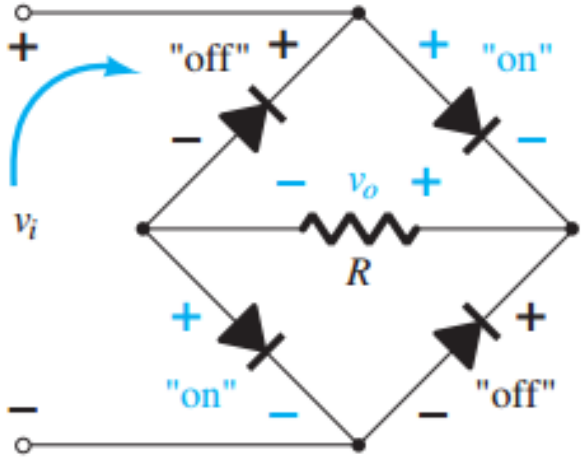
FULL-WAVE RECTIFICATION

Bridge Network

The dc level obtained from a sinusoidal input can be improved 100% using a process called *full-wave rectification*. The most familiar network for performing such a function appears in Fig. 2.53 with its four diodes in a *bridge* configuration. During the period $t = 0$ to $T/2$ the polarity of the input is as shown in Fig. 2.54. The resulting polarities across the ideal diodes are also shown in Fig. 2.54 to reveal that D_2 and D_3 are conducting, whereas D_1 and D_4 are in the "off" state. The net result is the configuration of Fig. 2.55, with its indicated current and polarity across R. Since the diodes are ideal, the load voltage is $v_o = v_i$, as shown in the same figure.







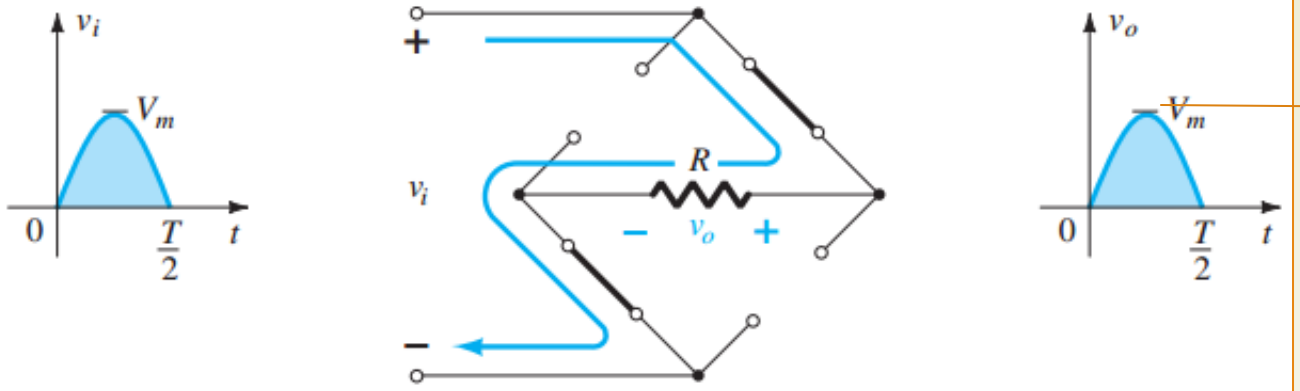


FIG. 2.55

Conduction path for the positive region of v_i.

Vm-(2xVk)

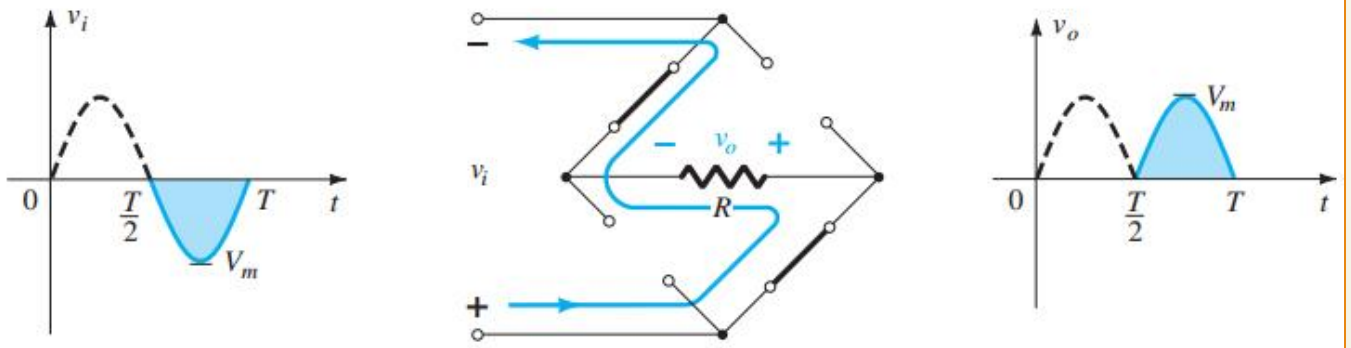
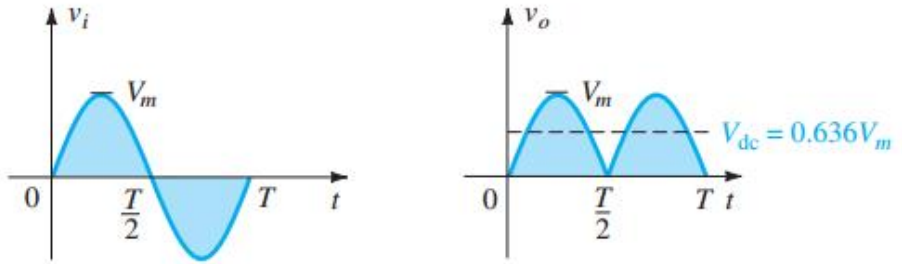
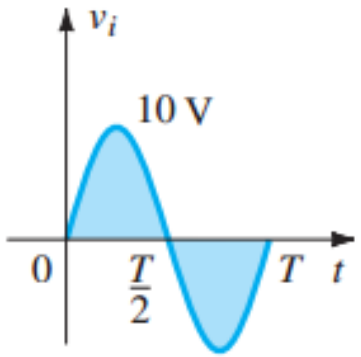


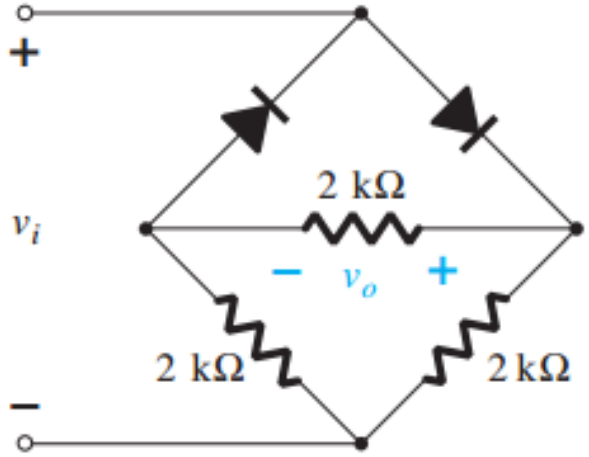
FIG. 2.56

Conduction path for the negative region of v_i.



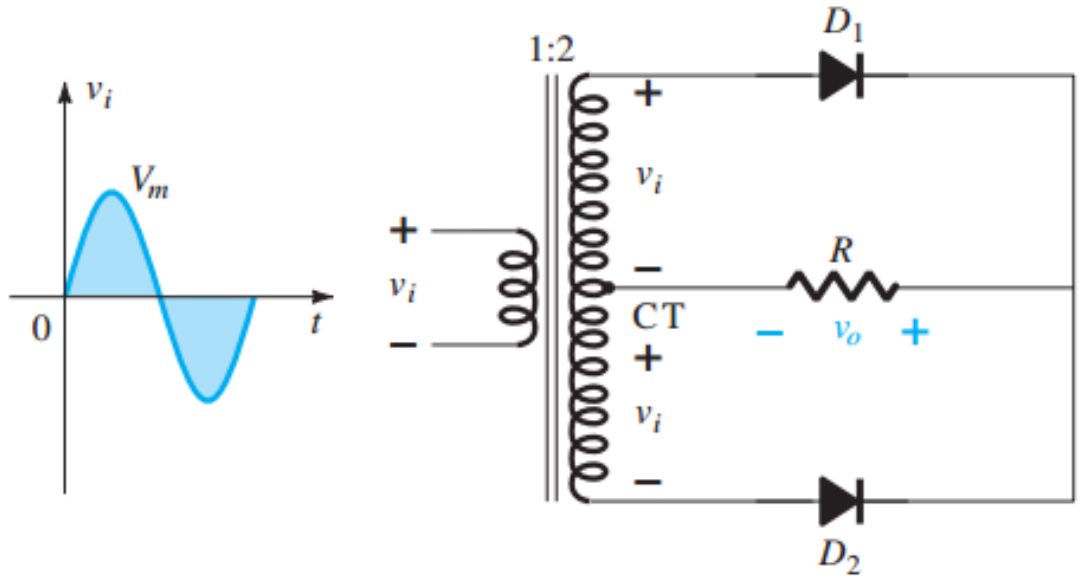
EXAMPLE 2.17 Determine the output waveform for the network of Fig. 2.64 and calculate the output dc level and the required PIV of each diode.

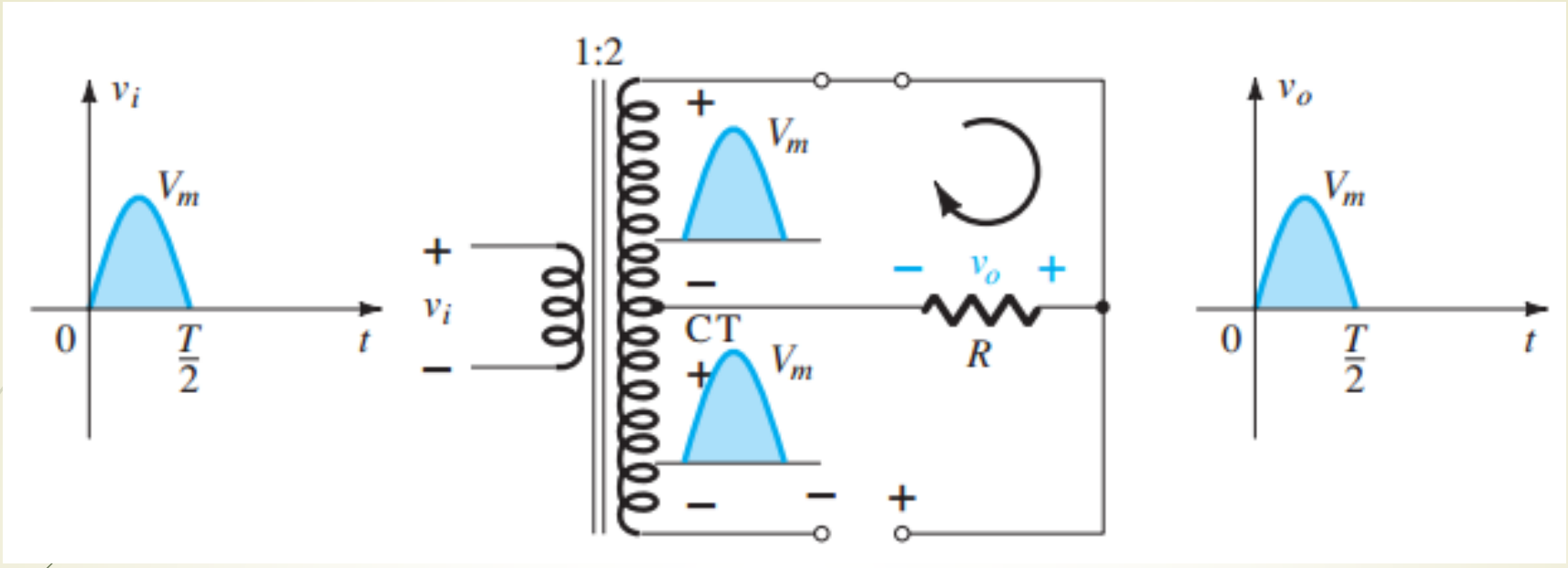


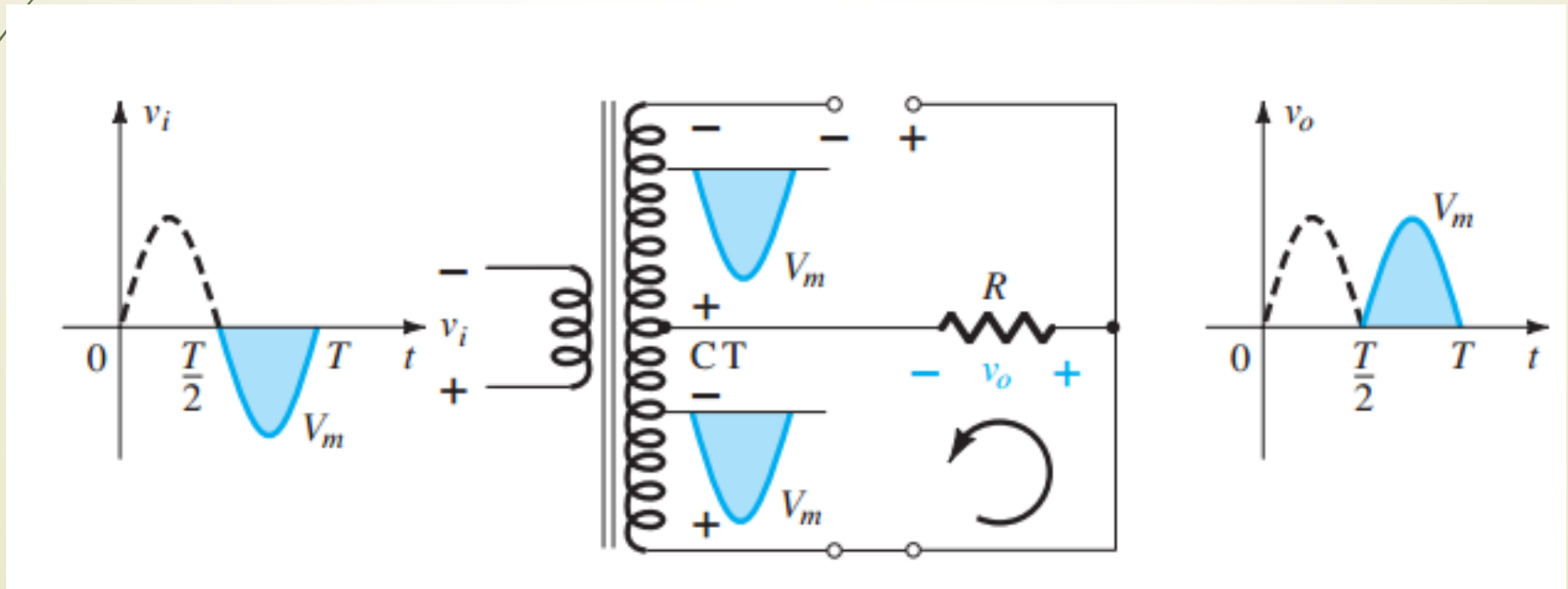


Center-Tapped Transformer

A second popular full-wave rectifier appears in Fig. 2.60 with only two diodes but requiring a center-tapped (CT) transformer to establish the input signal across each section of the secondary of the transformer. During the positive portion of v_i applied to the primary of the transformer, the network will appear as shown in Fig. 2.61 with a positive pulse across each section of the secondary coil. D_1 assumes the short-circuit equivalent and D_2 the open-circuit equivalent, as determined by the secondary voltages and the resulting current directions. The output voltage appears as shown in Fig. 2.61.




1:2
v_i
V_m
0
$\frac{T}{2}$
t
+
v_i
−
CT
V_m
V_m
+
−
v_o
+
R
v_o
V_m
0
$\frac{T}{2}$
t


v_i
0
$\frac{T}{2}$
T
t
V_m
−
v_i
+
CT
V_m
V_m
+
−
R
v_o
+
v_o
V_m
0
$\frac{T}{2}$
T
t

Next class:

1. **diode circuit analysis**
2. **Diode small signal model**
3. **Diode high frequency model**
4. **Depletion layer capacitance**
5. **Diffusion capacitance**
6. **Zener break down, avalanche break down**
7. **Voltage regulation**

SIGNIFICANT EQUATIONS

1 Semiconductor Diodes $W = QV$, $1\text{ eV} = 1.6 \times 10^{-19}\text{ J}$, $I_D = I_s\,(e^{V_D/nV_T} - 1)$, $V_T = kT/q$, $T_\text{K} = T_\text{C} + 273°$, $k = 1.38 \times 10^{-23}\text{ J/K}$, $V_K \cong 0.7\text{ V (Si)}$, $V_K \cong 0.3\text{ V(Ge)}$, $V_K \cong 1.2\text{ V (GaAs)}$, $R_D = V_D/I_D$, $r_d = 26\text{ mV}/I_D$, $r_\text{av} = \Delta V_d/\Delta I_d\big|_\text{pt. to pt.}$, $P_D = V_D\,I_D$, $T_C = (\Delta V_Z/V_Z)/(T_1 - T_0) \times 100\%/°\text{C}$

2 Diode Applications Silicon: $V_K \cong 0.7\text{ V}$, germanium: $V_K \cong 0.3\text{ V}$, GaAs: $V_K \cong 1.2\text{ V}$; half-wave: $V_\text{dc} = 0.318V_m$; full-wave: $V_\text{dc} = 0.636V_m$