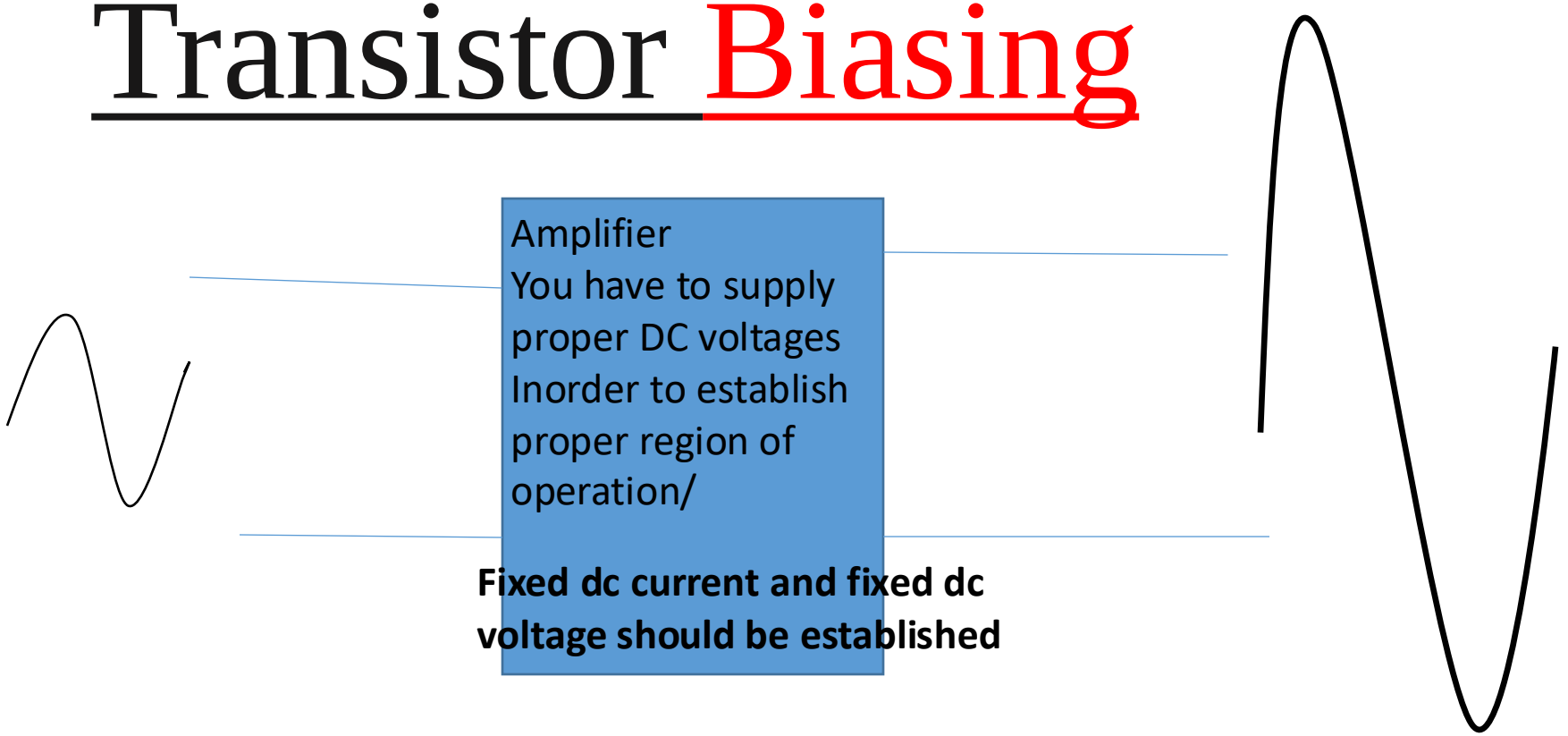
- **Active/linear**
- **Saturation**
- **Cutoff**

Collector current, Emitter current (mA)
Base current micro Ampere.

BE forward biased
CB reverse biased

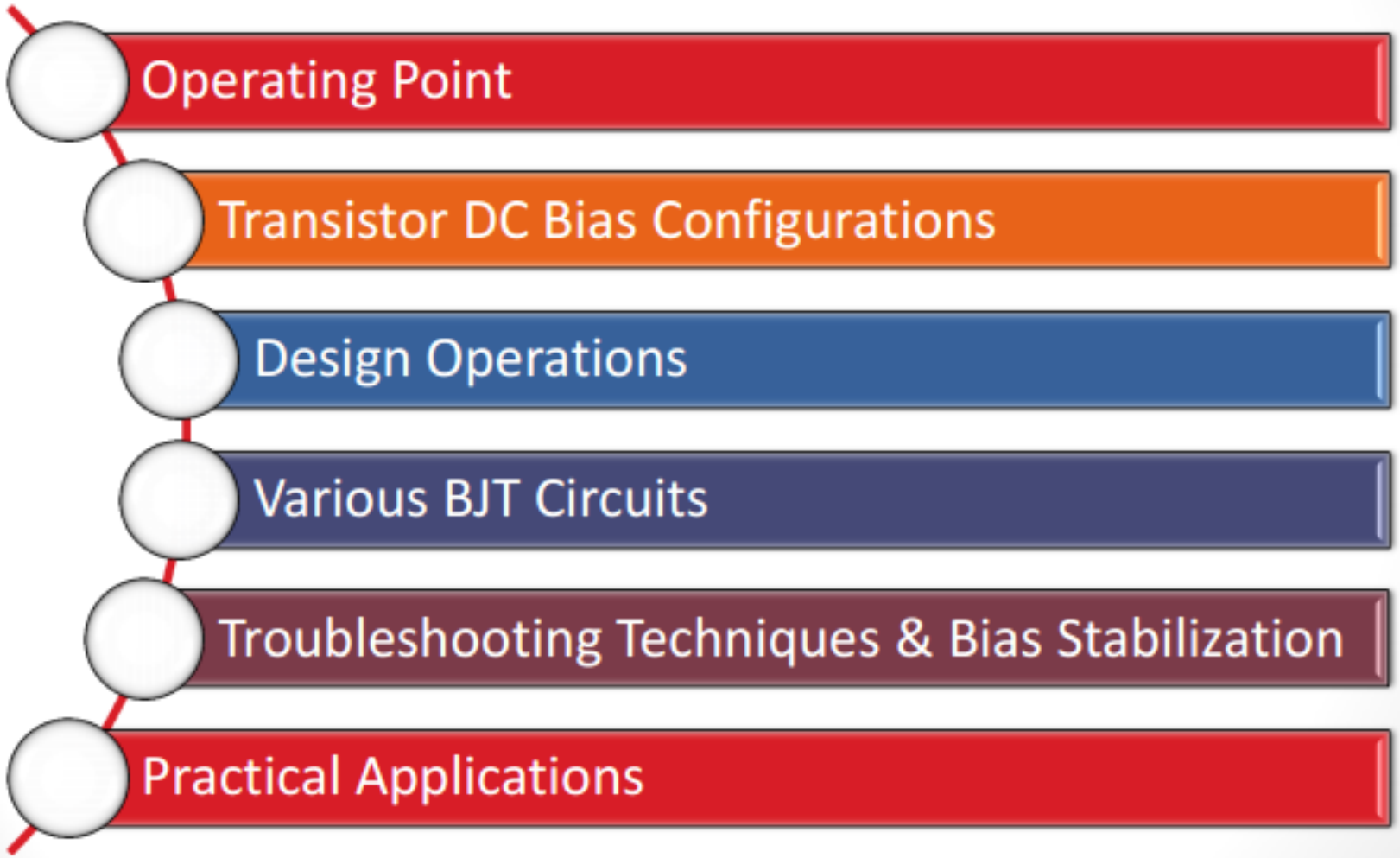
Transistor Biasing



Amplifier
You have to supply proper DC voltages Inorder to establish proper region of operation/

Fixed dc current and fixed dc voltage should be established

Agenda


Operating Point
Transistor DC Bias Configurations
Design Operations
Various BJT Circuits
Troubleshooting Techniques & Bias Stabilization
Practical Applications

Introduction

- Any increase in ac voltage, current, or power is the result of a transfer of energy from the applied dc supplies.
- The analysis or design of any electronic amplifier therefore has two components: a dc and an ac portion.

- Basic Relationships/formulas for a transistor:

$$V_{BE} = 0.7\ \text{V}$$

$$I_E = I_B + I_C = I_B + \beta I_B = I_B(1+\beta)$$

$$I_C = \beta I_B$$

- ***Biasing*** means applying of dc voltages to establish a fixed level of current and voltage. >>> Q-Point

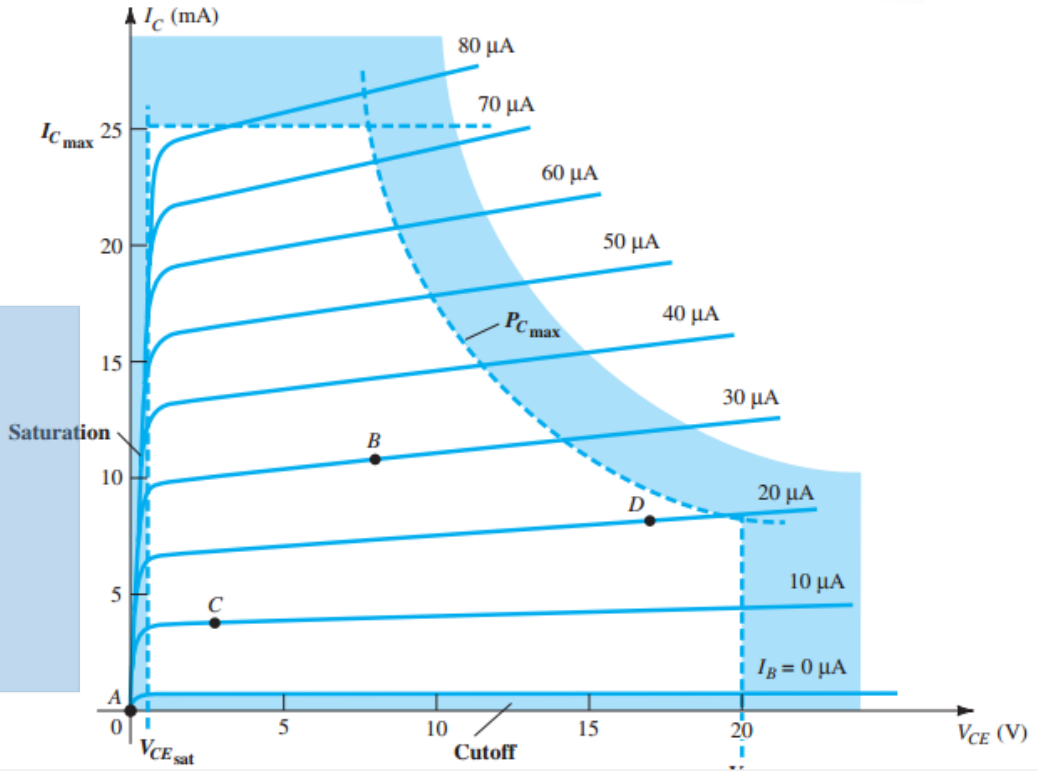
Operating Point

Base current, collector current, emitter current, V_{CE}, V_{BE}

- For transistor amplifiers the resulting dc current and voltage establish an operating point on the characteristics that define the region that will be employed for amplification of the applied signal.
- Because the operating point is a fixed point on the characteristics, it is also called the quiescent point (abbreviated Q-point).

Transistor Regions Operation:

1. Linear-region operation:
   - Base–emitter junction forward-biased
   - Base–collector junction reverse-biased
2. Cutoff-region operation:
   - Base–emitter junction reverse-biased
   - Base–collector junction reverse-biased
3. Saturation-region operation:
   - Base–emitter junction forward-biased
   - Base–collector junction forward-biased



For the BJT to be biased in its linear or active operating region the following must be true:

1. ***The base–emitter junction must be forward-biased (p-region voltage more positive), with a resulting forward-bias voltage of about 0.6 V to 0.7 V.***
2. ***The base–collector junction must be reverse-biased (n-region more positive), with the reverse-bias voltage being any value within the maximum limits of the device.***

TRANSISTOR DC BIAS CONFIGURATIONS

- Fixed-Bias Configuration
- Emitter-Bias Configuration
- Voltage-Divider Bias Configuration
- Collector Feedback Configuration
- Emitter-Follower Configuration
- Common-Base Configuration

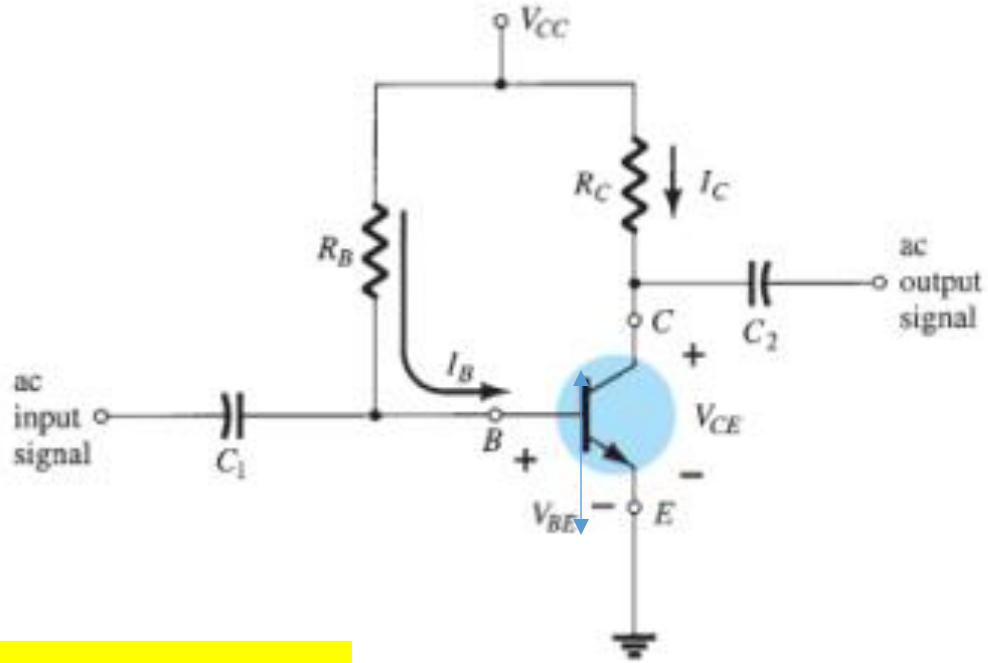
CE (common emitter)
4 types

CC (Common collector), output is taken from emitter

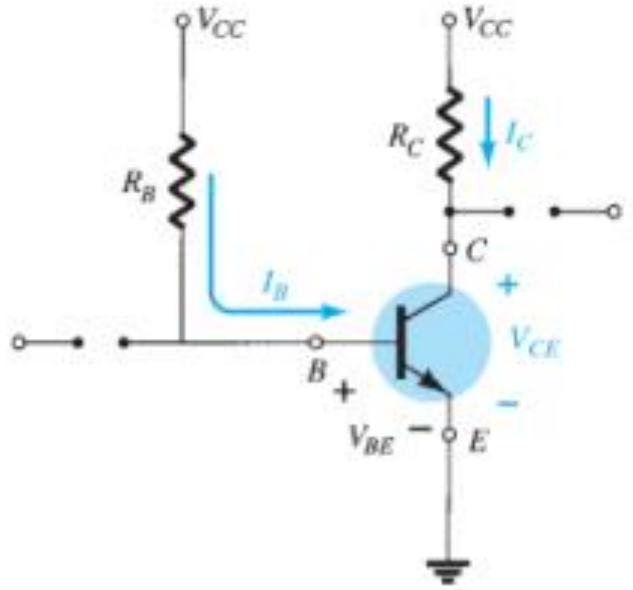
CB, CE, CC

Fixed-Bias Configuration

- Fixed-bias circuit.



- DC equivalent ct.



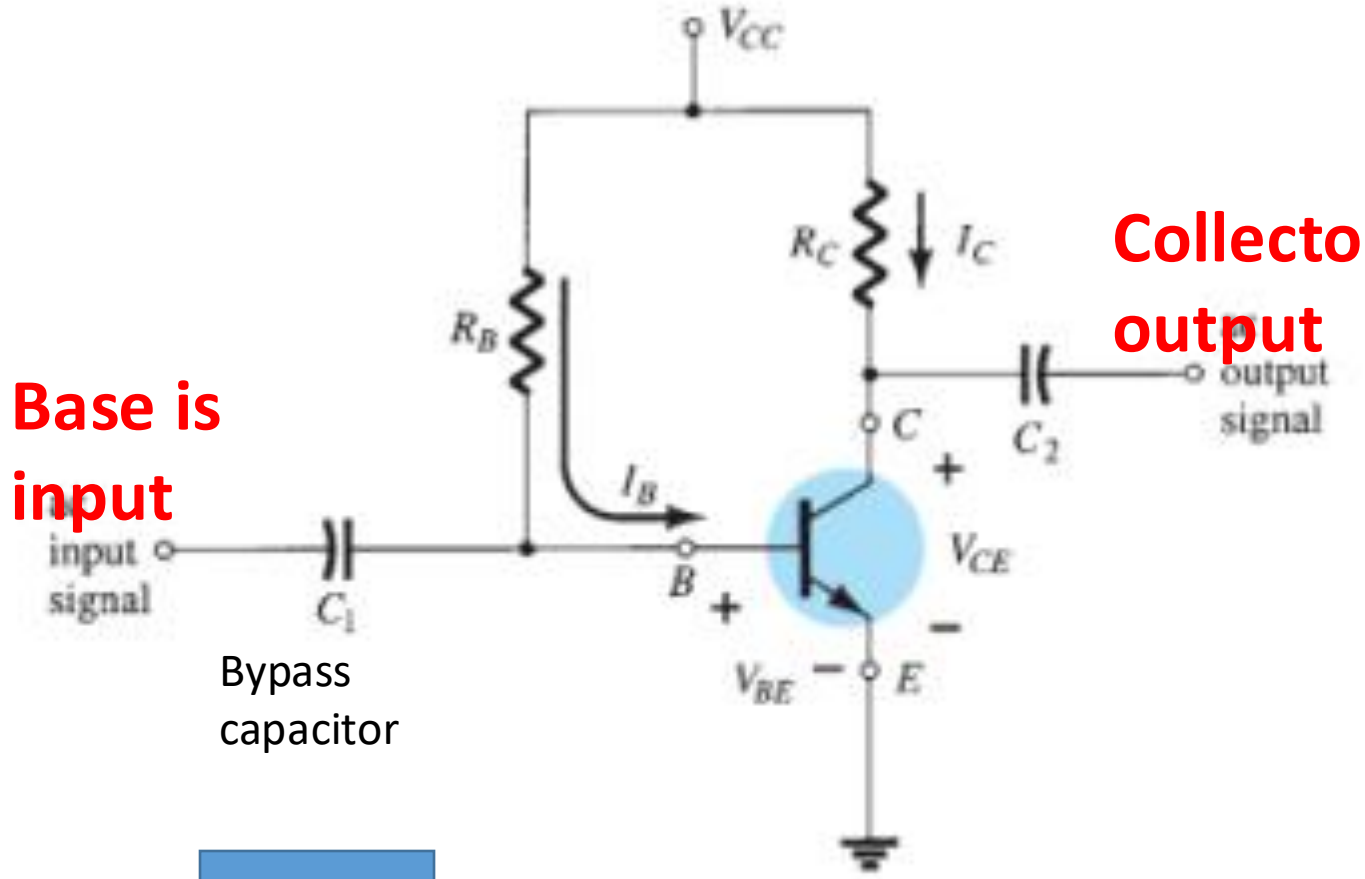
First step is to find I_B
Then determine $I_c = I_E$
Afterwards, we can find the value of V_{CE}

$$V_{BE} = 0.7\ \text{V}$$

$$I_E = I_B + I_C = I_B + \beta I_B = I_B(1+\beta)$$

$$I_C = \beta I_B$$

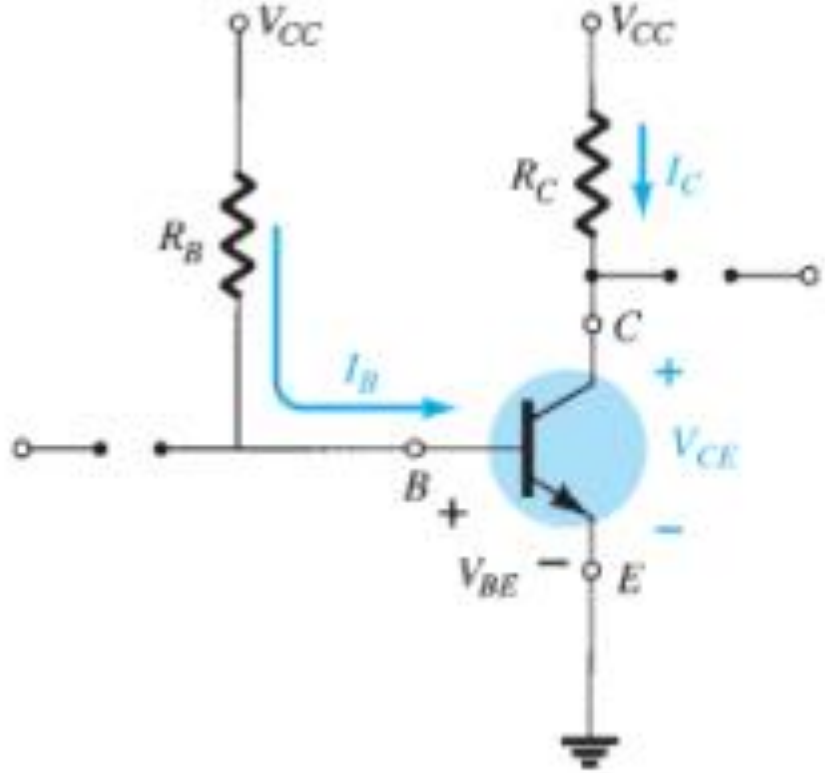
- Fixed-bias circuit.
- DC equivalent ct.



Base is input

Collector is output

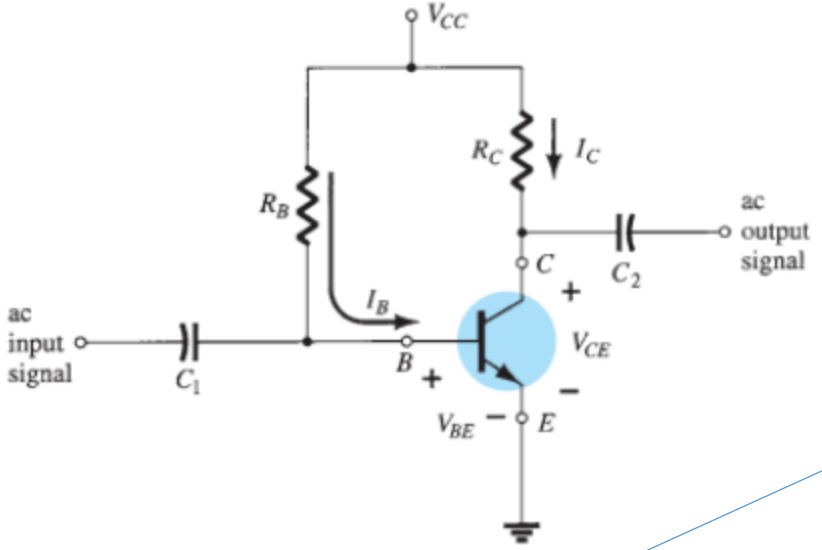
Bypass capacitor



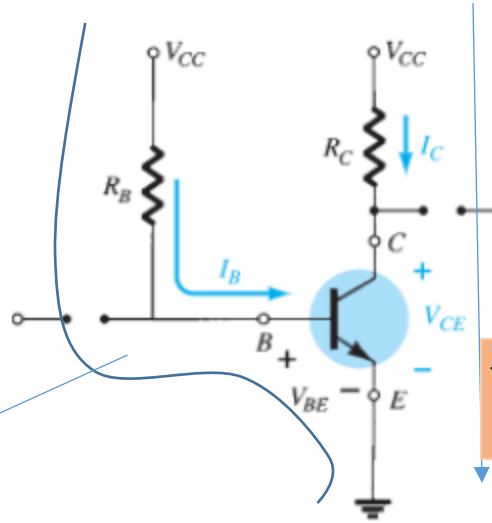
CE

First step is to find I_B
Then determine $I_c=\beta I_B=I_E$
Afterwards, we can find the value of V_{CE}

- Fixed-bias circuit.



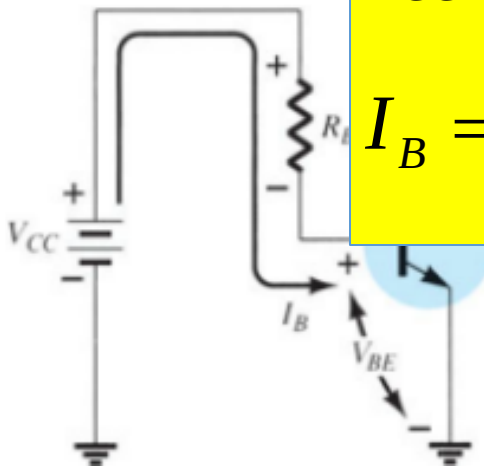
- DC equivalent ct.



$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CE} = V_{CC} - I_C R_C$$

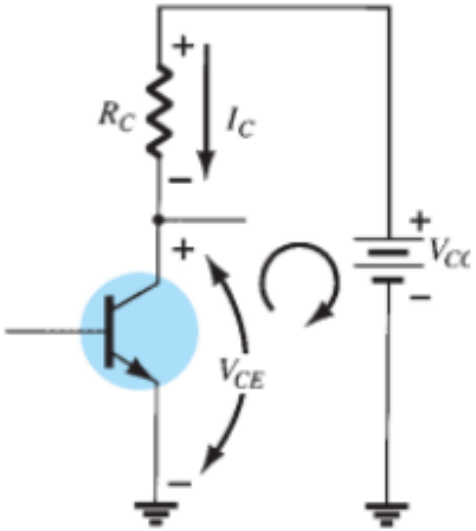
- Base–emitter loop.



$$V_{CC} = I_B R_B + V_{BE}$$

$$I_B = \frac{V_{CC} - 0.7}{R_B}$$

- Collector–emitter loop.



$$I_C = \beta I_B$$

$$V_{CE} + I_C R_C - V_{CC} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = V_C - V_E$$

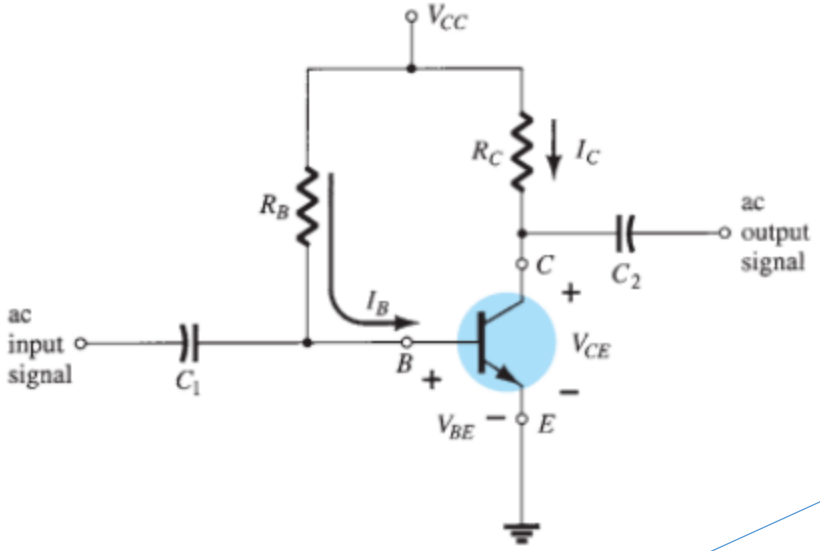
$$V_{CE} = V_C$$

$$V_{BE} = V_B - V_E$$

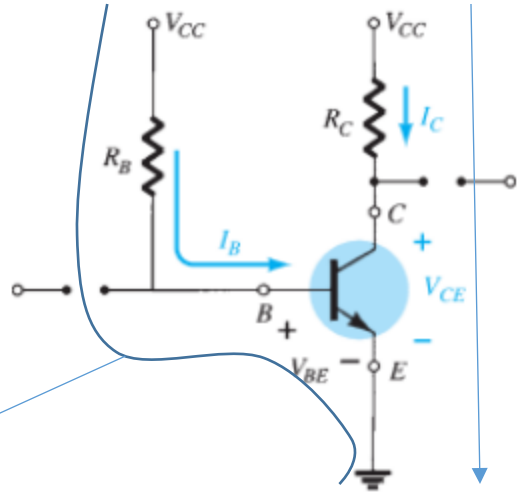
$$V_{BE} = V_B$$

First step is to find I_B
Then determine $I_c=\beta I_B=I_E$
Afterwards, we can find the value of V_{CE}

- Fixed-bias circuit.



- DC equivalent ct.

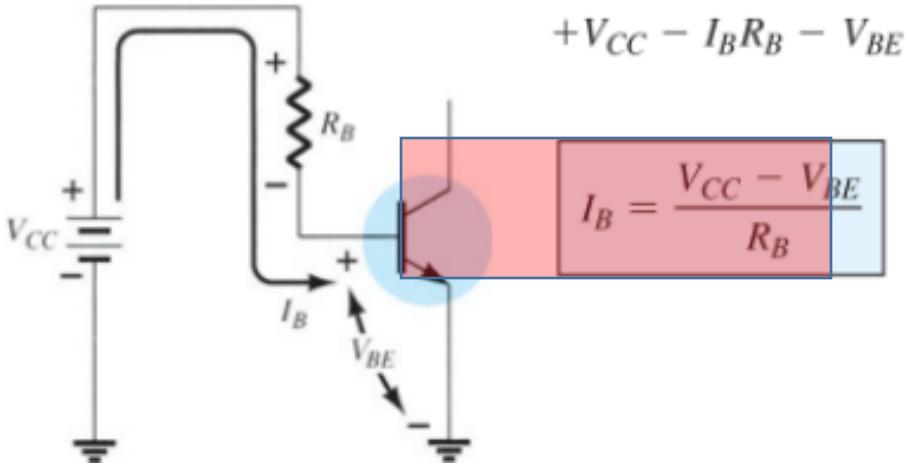


$$V_{CC} = I_C R_C + V_{CE}$$

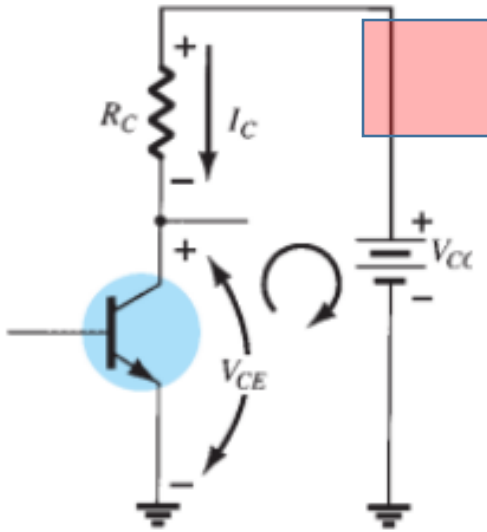
$$V_{CE} = V_{CC} - I_C R_C$$

- Base–emitter loop.

$$V_{CC} = I_B R_B + V_{BE}$$



- Collector–emitter loop.



Fixed-Bias Configuration Example

EXAMPLE 4.1 Determine the following for the fixed-bias configuration of Fig. 4.7.

a. I_{B_Q} and I_{C_Q}.
b. V_{CE_Q}.
c. V_B and V_C.
d. V_{BC}.

Solution

$$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega} = \mathbf{47.08\ \mu A}$$

$$I_{C_Q} = \beta I_{BQ} = (50)(47.08\ \mu\text{A}) = \mathbf{2.35\text{ mA}}$$

$$V_{CE_Q} = V_{CC} - I_C R_C$$
$$= 12\text{ V} - (2.35\text{ mA})(2.2\text{ k}\Omega)$$
$$= \mathbf{6.83\text{ V}}$$

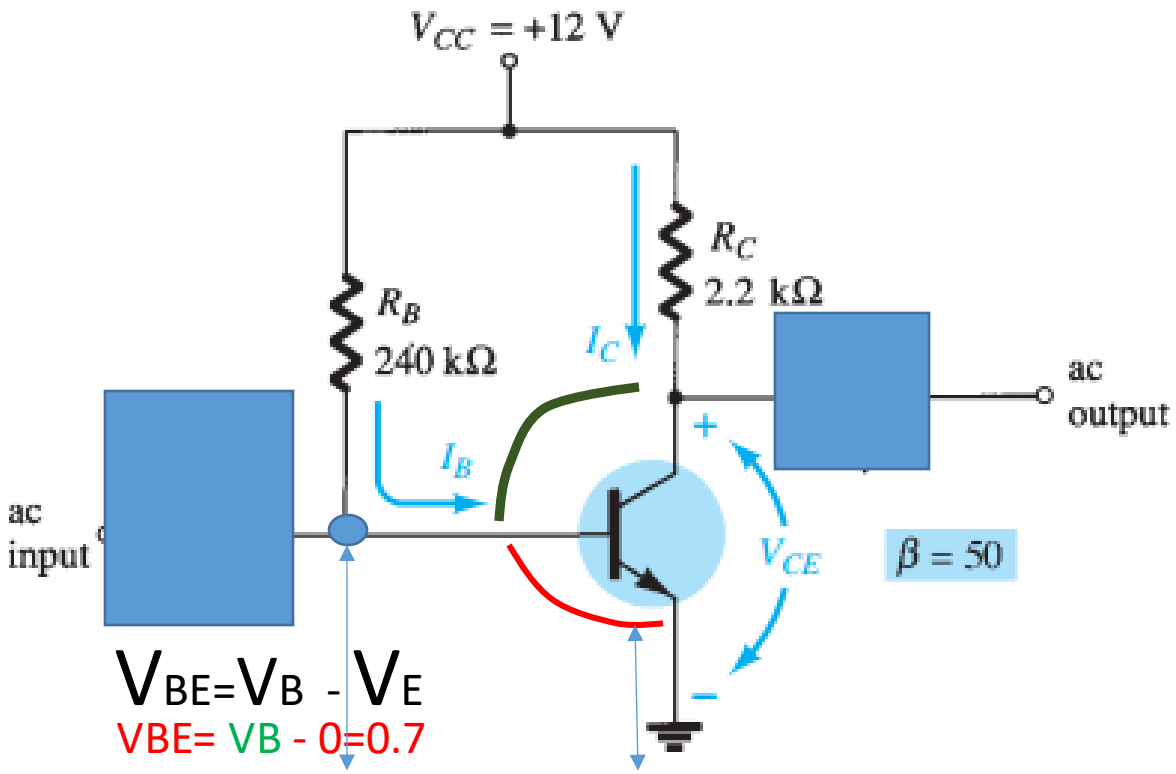
$V_B = V_{BE} = \mathbf{0.7\text{ V}}$
$V_C = V_{CE} = \mathbf{6.83\text{ V}}$

Using double-subscript notation yields

$$V_{BC} = V_B - V_C = 0.7\text{ V} - 6.83\text{ V}$$
$$= \mathbf{-6.13\text{ V}}$$

with the negative sign revealing that the junction is reversed-biased, as it should be for linear amplification.

$V_{BC}=V_B - V_C$

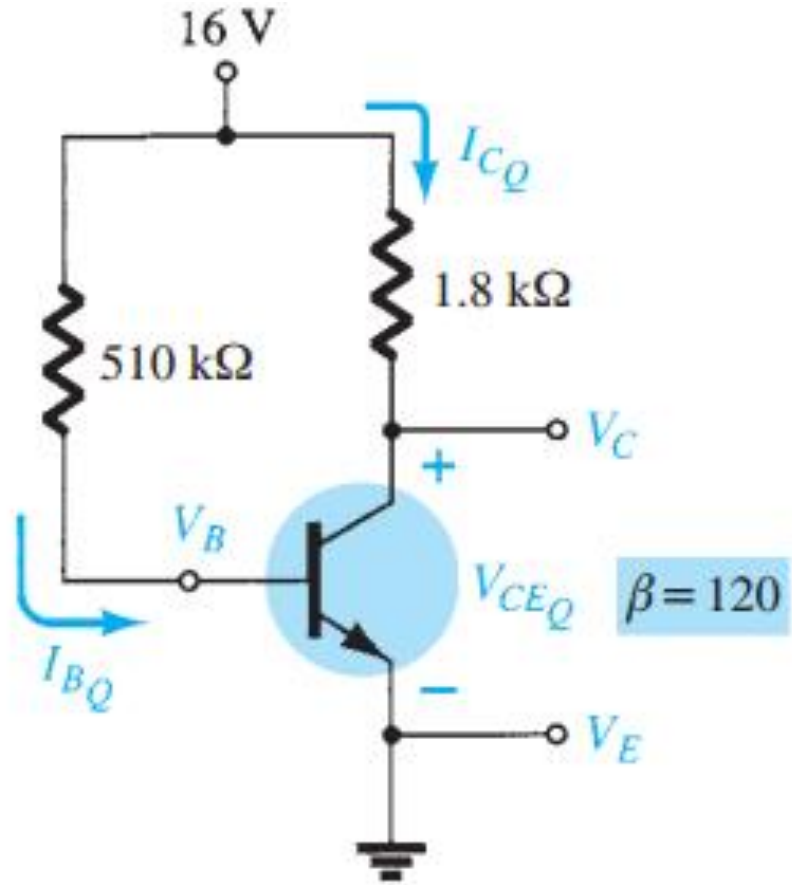


$V_{BE}=V_B - V_E$

VBE= VB - 0=0.7

$V_{CE}=V_C - V_E$

1.



$V_{BE} = 0.7\ \text{V}$

$I_E = I_B + I_C = I_B + \beta I_B = I_B(1+\beta)$

$I_C = \beta I_B$

on appearing in Fig. 4.119, determine:

on appearing in Fig. 4.120, determine:

a. I_C.
b. V_{CC}.
c. β.
d. R_B.

$$I_B = \frac{V_{CC} - 0.7}{R_B}$$

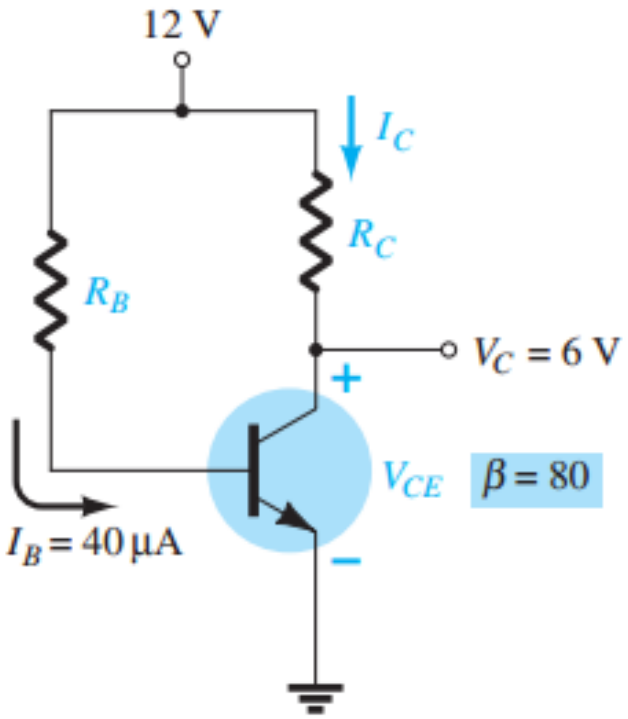
$$I_C = \beta I_B$$

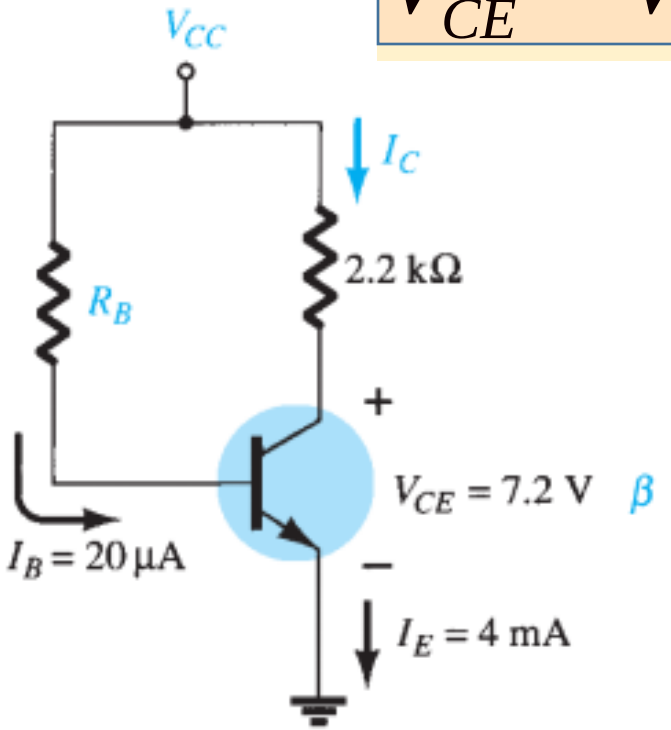
$$V_{CE} = V_{CC} - I_C R_C$$

$V_{BE} = 0.7\ \text{V}$

$I_C = \beta I_B$

$V_C = V_{CE} = 6\ \text{V}$

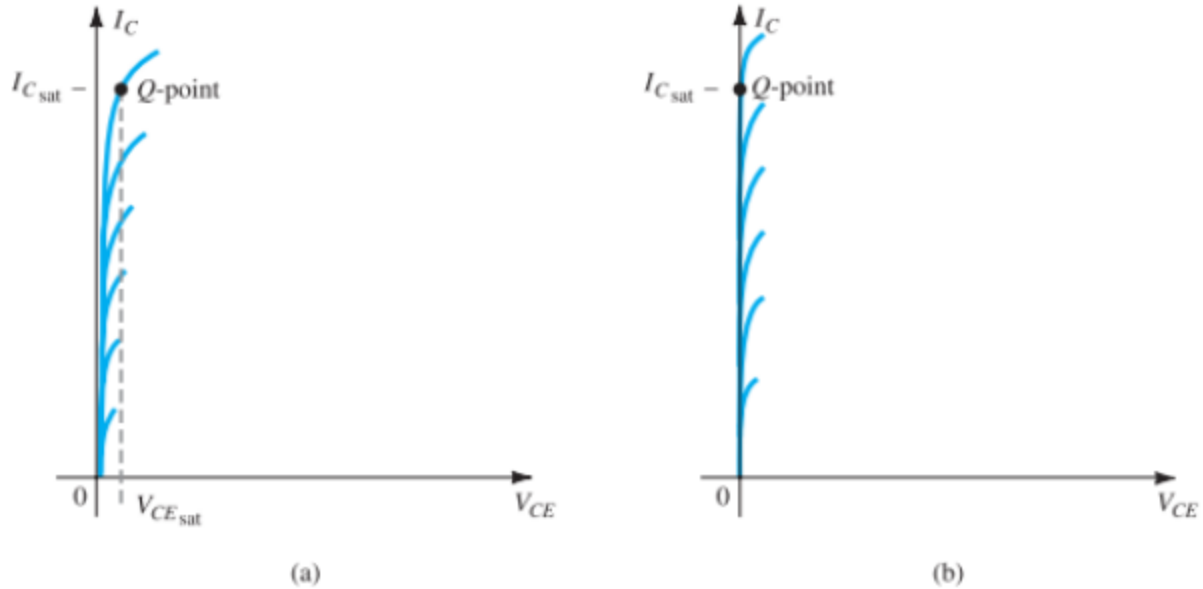




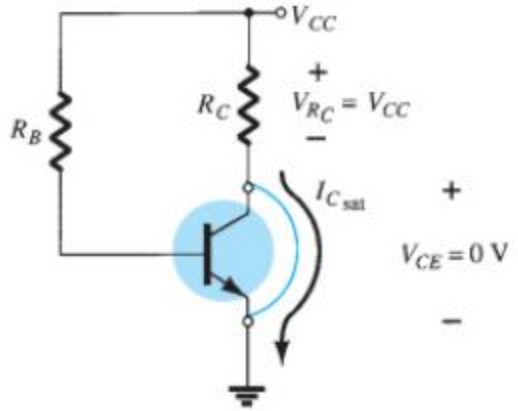
Fixed-Bias Configuration Example

- **Transistor Saturation**

- Saturation regions:
  (a) Actual
  (b) approximate.



- Determining I_{Csat} for the fixed-bias configuration.

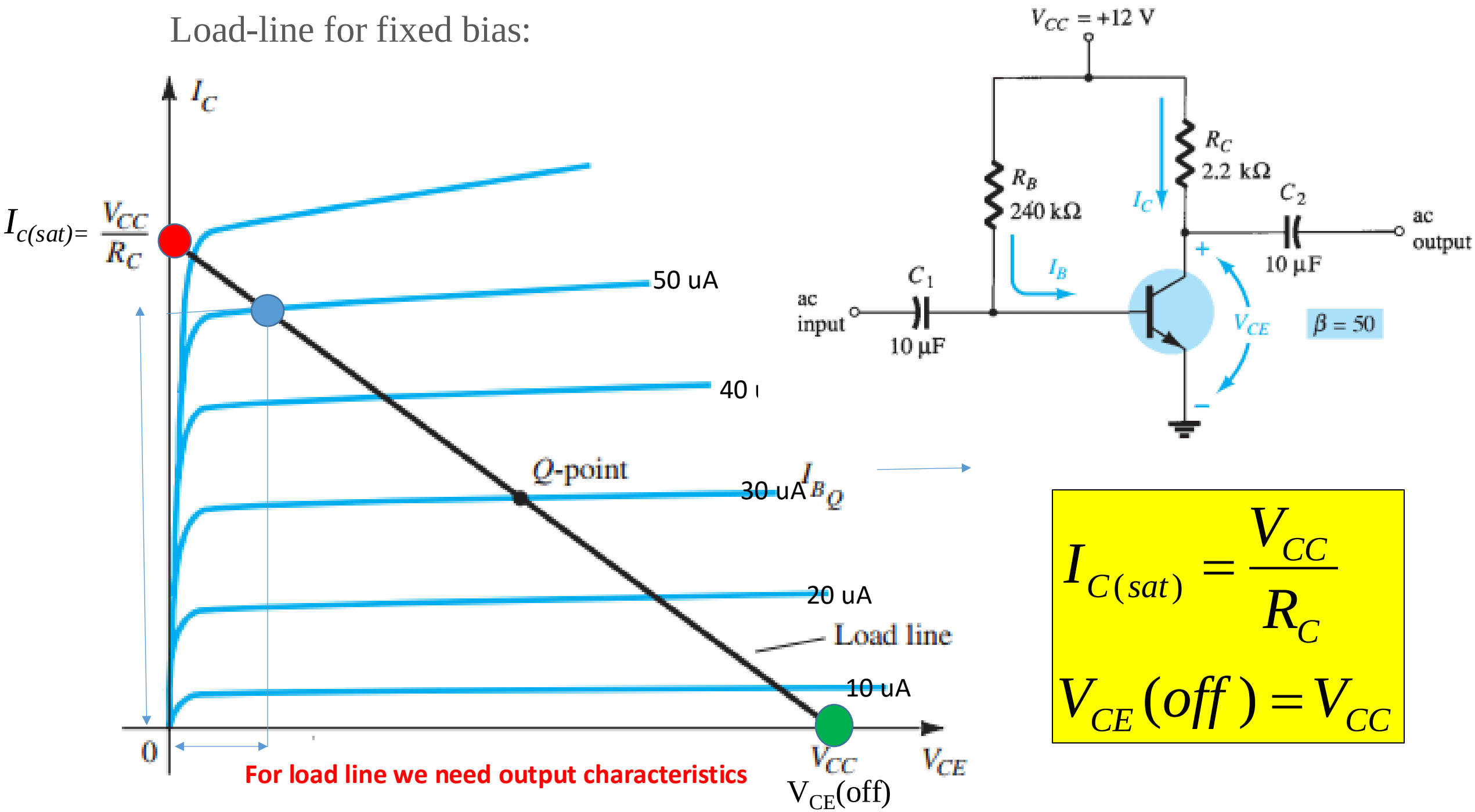


$$I_{C_{sat}} = \frac{V_{CC}}{R_C}$$

$$I_{C(sat)} = \frac{V_{CC}}{R_C}$$

$$V_{CE}(off) = V_{CC}$$

Load-line for fixed bias:



For load line we need output characteristics

V_{CE}(off)

$$I_{C(sat)} = \frac{V_{CC}}{R_C}$$

$$V_{CE}(off) = V_{CC}$$

• Load Line Analysis
For Fixed Biased

$$V_{CE} = V_{CC} - I_C R_C$$

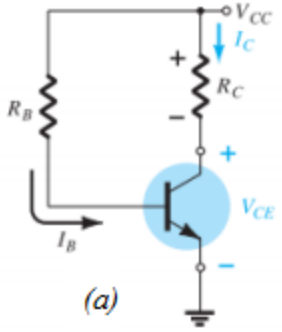
$$V_{CE} = V_{CC} - (0)R_C$$

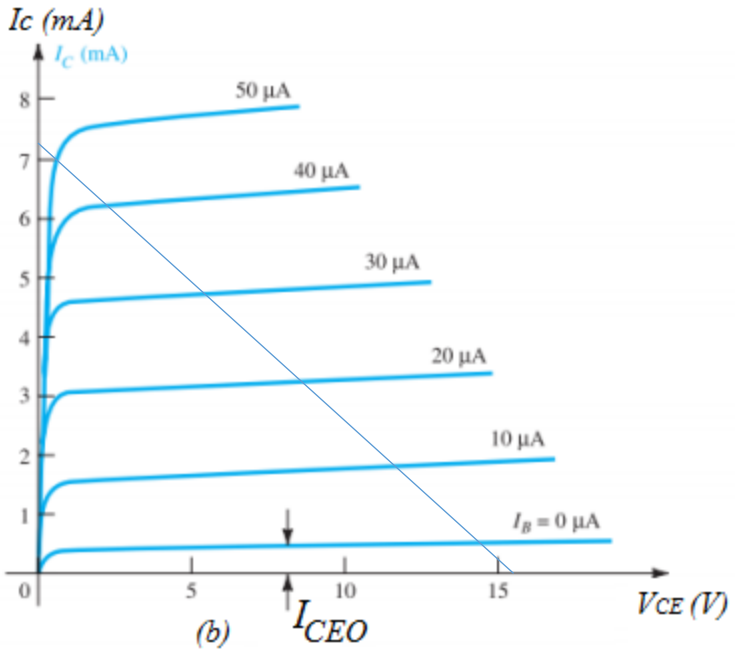
$$V_{CE} = V_{CC}|_{I_C=0\,\text{mA}}$$

0

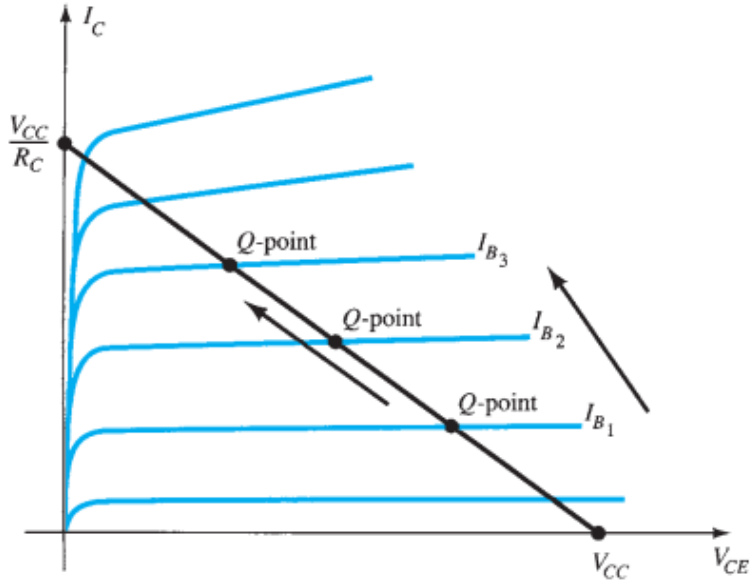
I_C

$$I_{C(sat)} = \frac{V_{CC}}{R_C}$$

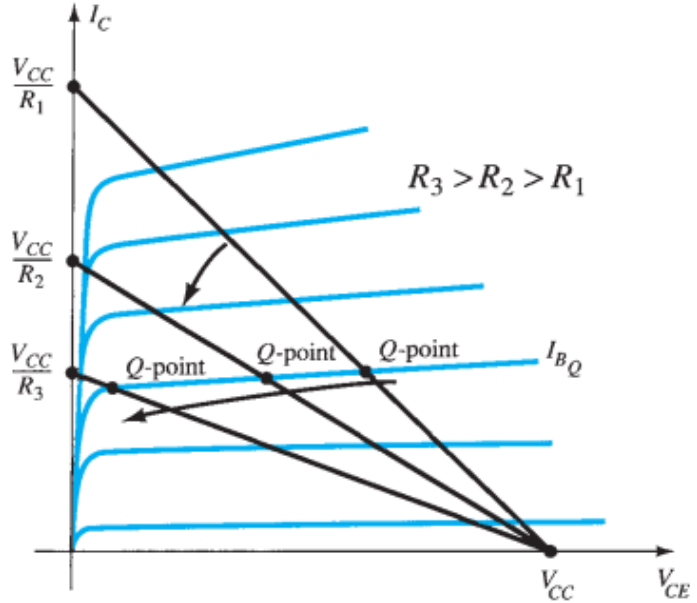




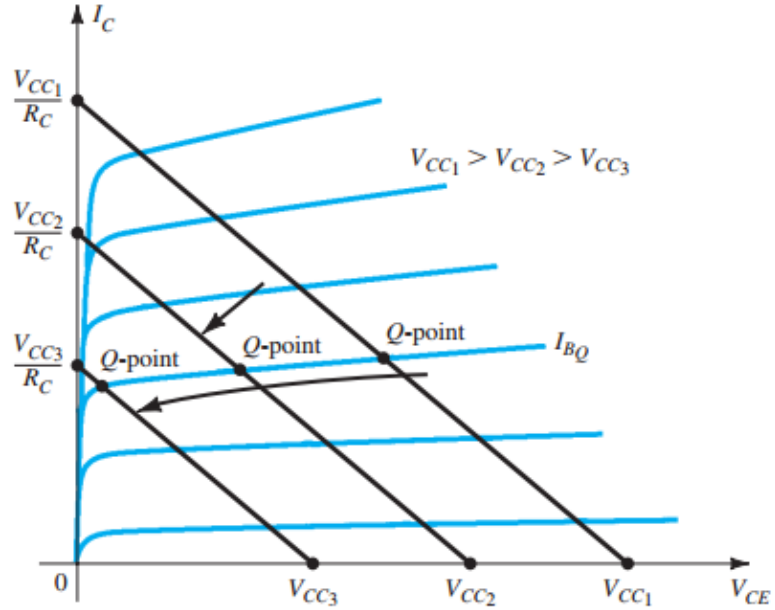
Load line analysis (a) network (b) device caharcteristics



Movement of the Q-point with increasing level of I_B.

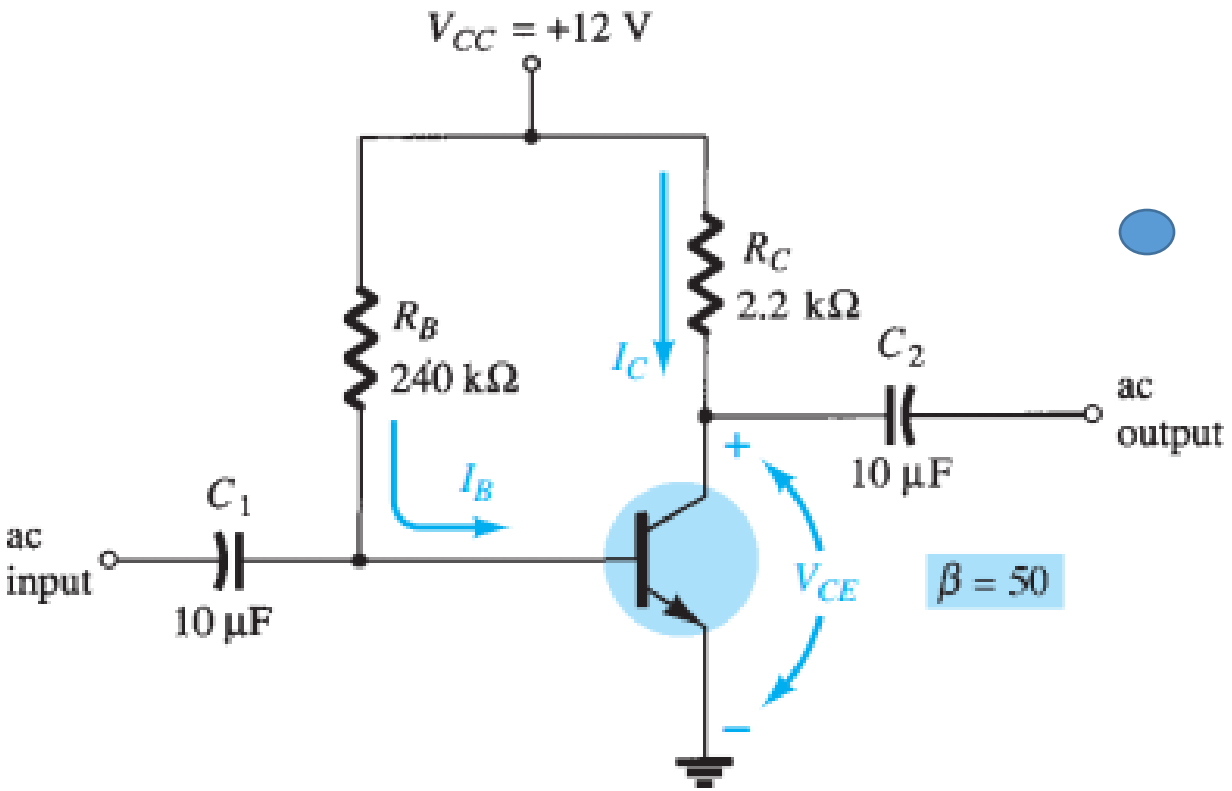


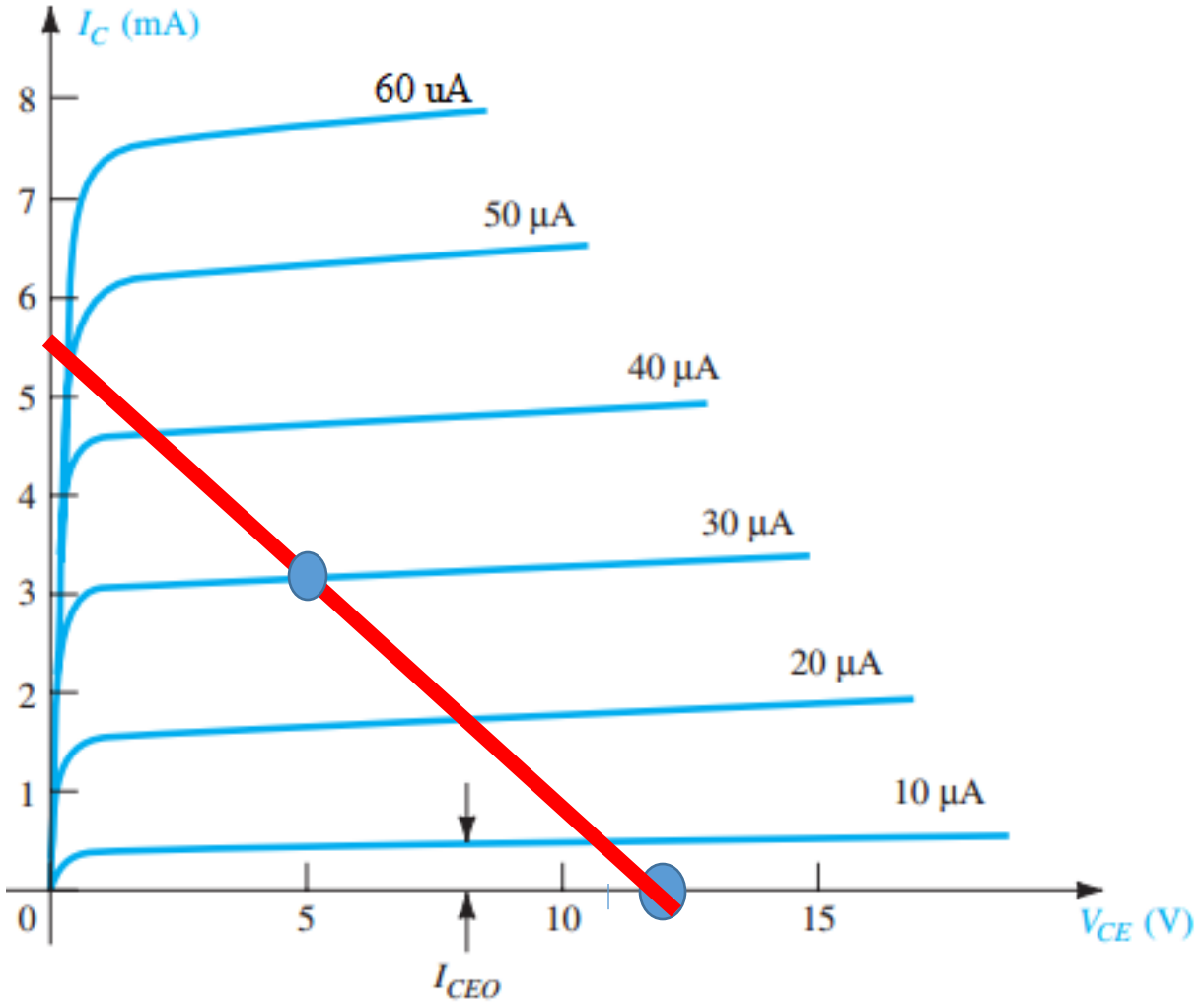
Effect of an increasing level of R_C on the load line and the Q-point.



Effect of lower values of V_{CC} on the load line and the Q-point.

Draw the load-line for the above network



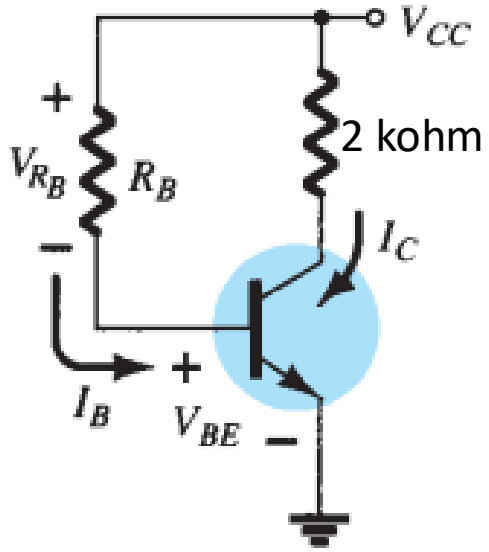


$$I_{C(sat)} = \frac{V_{CC}}{R_C}$$

Load line for Fixed Biased

$$I_{C(sat)} = \frac{V_{CC}}{R_C}$$

$$V_{CE}(off) = V_{CC}$$



EXAMPLE 4.3 Given the load line of Fig. 4.16 and the defined Q-point, determine the required values of V_{CC}, R_C, and R_B for a fixed-bias configuration.

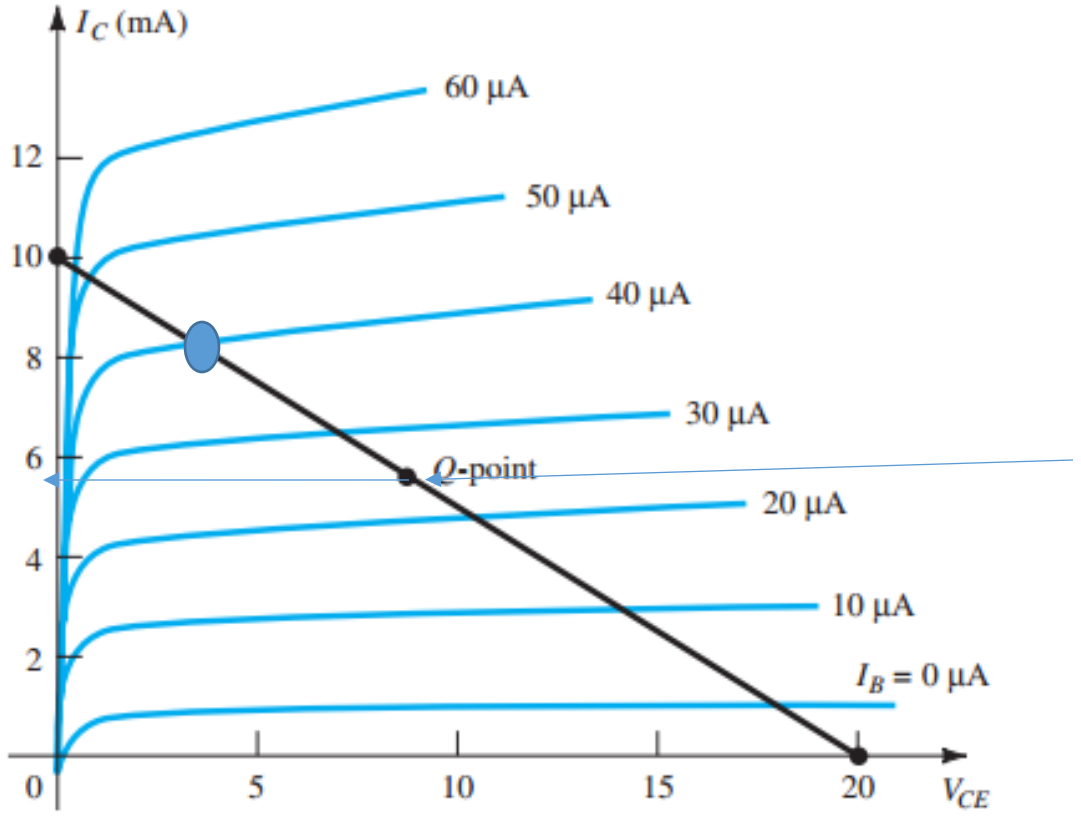


FIG. 4.16

Solution: From Fig. 4.16,

$$V_{CE} = V_{CC} = \mathbf{20\ V} \text{ at } I_C = 0\ \text{mA}$$

$$I_C = \frac{V_{CC}}{R_C} \text{ at } V_{CE} = 0\ \text{V}$$

and

$$R_C = \frac{V_{CC}}{I_C} = \frac{20\ \text{V}}{10\ \text{mA}} = \mathbf{2\ k\Omega}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

and

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20\ \text{V} - 0.7\ \text{V}}{25\ \mu\text{A}} = \mathbf{772\ k\Omega}$$

10=20/Rc

Formula's for Fixed Bias:

$$I_B = \frac{V_{CC} - 0.7}{R_B}$$

$$I_C = \beta I_B$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$I_{C(Sat)} = \frac{V_{CC}}{R_C}$$

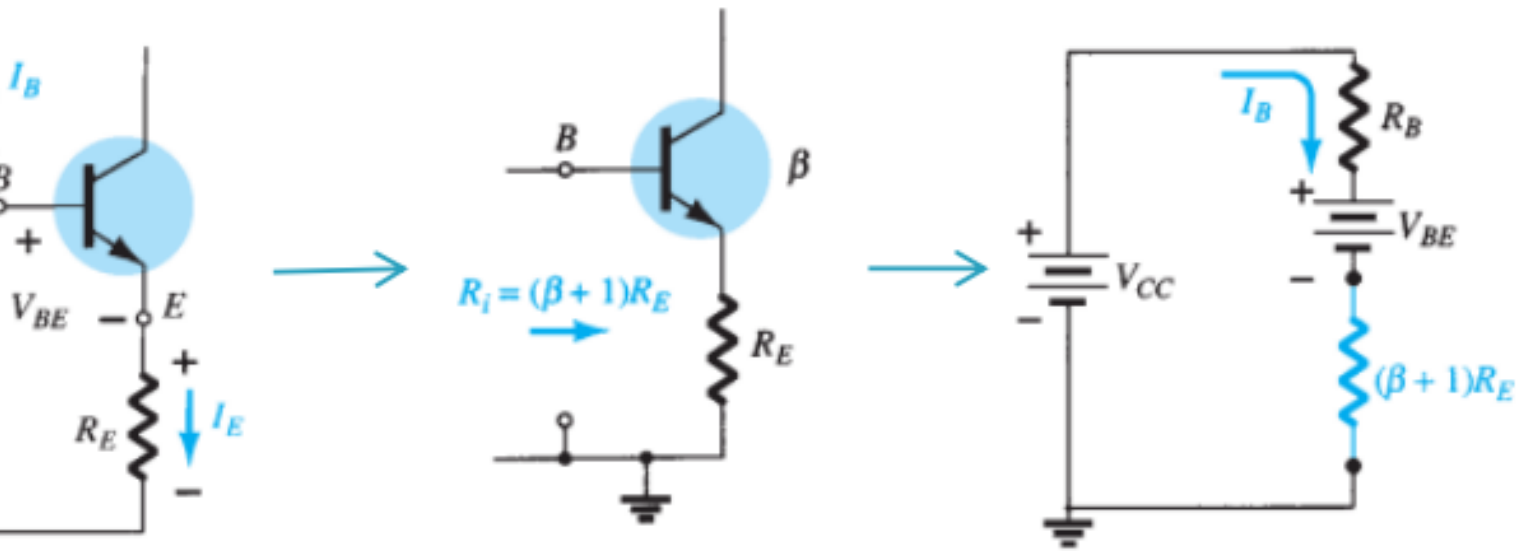
Cutoff voltage

$V_{CE(off)} = V_{cc}$

Emitter-Bias Configuration

- BJT bias circuit with emitter resistor.
- DC equivalent ct

e-Emitter Loop



$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$I_E = (\beta + 1)I_B$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$$R_i = (\beta + 1)R_E$$

Emitter-Bias Configuration

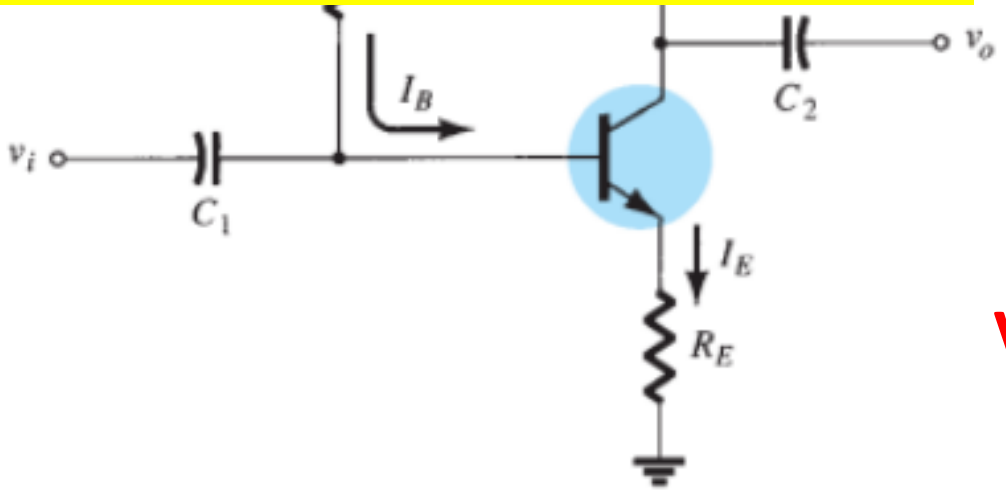
$V_{BE} = 0.7\ \text{V}$

$I_E = I_B + I_C = I_B + \beta I_B = I_B(1+\beta)$

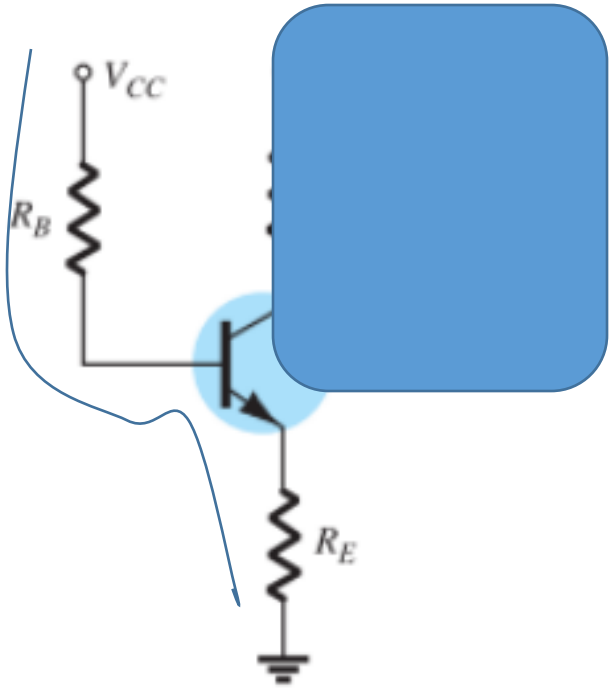
$I_C = \beta I_B$

resistor.

- DC equivalent ct

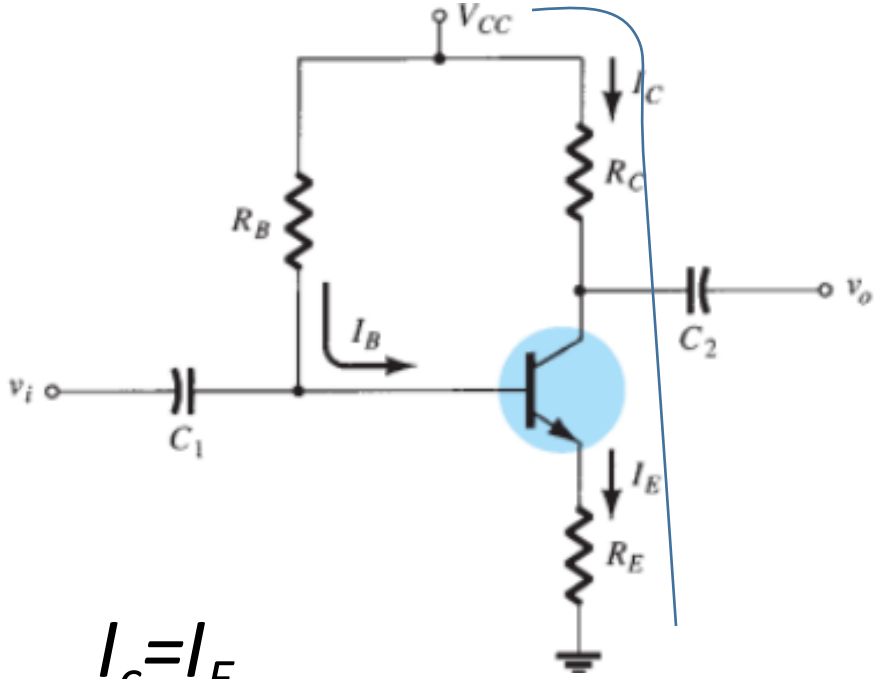


Base-emitter loop:

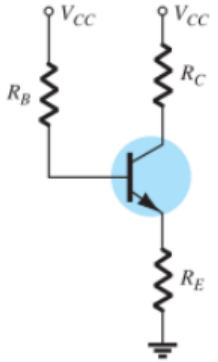


$V_{CC} = I_B R_B + V_{BE} + I_E R_E$

Emitter-Bias Configuration

- 

- DC equivalent ct



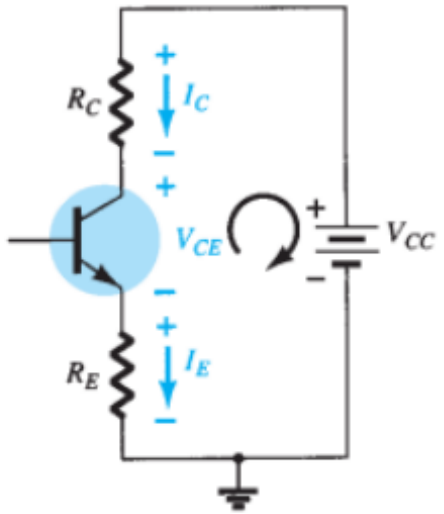
$I_c = I_E$

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Collector-Emitter Loop



$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$

$I_E \cong I_C$

$V_{CE} = V_{CC} - I_C(R_C + R_E)$

$V_E = I_E R_E$

$V_{CE} = V_C - V_E$

$V_C = V_{CE} + V_E$

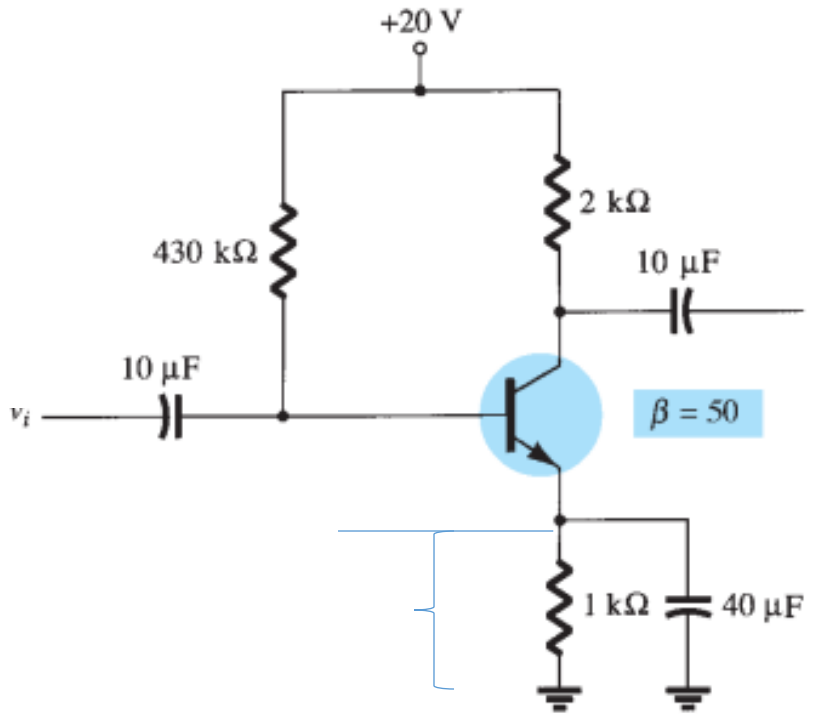
$V_B = V_{CC} - I_B R_B$

$V_C = V_{CC} - I_C R_C$

$V_B = V_{BE} + V_E$

EXAMPLE 4.4 For the emitter-bias network of Fig. 4.23, determine:

a. I_B.
b. I_C.
c. V_{CE}.
d. V_C.
e. V_E.
f. V_B.
g. V_{BC}.



Solution:

a. Eq. (4.17): $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{430\text{ k}\Omega + (51)(1\text{ k}\Omega)}$$
$$= \frac{19.3\text{ V}}{481\text{ k}\Omega} = \mathbf{40.1\ \mu A}$$

b. $I_C = \beta I_B$
$= (50)(40.1\ \mu\text{A})$
$\cong$ **2.01 mA**

13.97 V= Vc - 2
0.7= VB - 2 =
VBC= VB - VC

c. Eq. (4.19): $V_{CE} = V_{CC} - I_C(R_C + R_E)$
$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega + 1\text{ k}\Omega) = 20\text{ V} - 6.03\text{ V}$
$=$ **13.97 V**

d. $V_C = V_{CC} - I_C R_C$
$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega) = 20\text{ V} - 4.02\text{ V}$
$=$ **15.98 V**

e. $V_E = V_C - V_{CE}$
$= 15.98\text{ V} - 13.97\text{ V}$
$=$ **2.01 V**

or $V_E = I_E R_E \cong I_C R_E = (2.01\text{ mA})(1\text{ k}\Omega) =$ **2.01 V**

f. $V_B = V_{BE} + V_E$
$= 0.7\text{ V} + 2.01\text{ V}$
$=$ **2.71 V**

g. $V_{BC} = V_B - V_C$
$= 2.71\text{ V} - 15.98\text{ V}$
$=$ **−13.27 V** (reverse-biased as required)

Load line for

Emitter-Bias Configuration

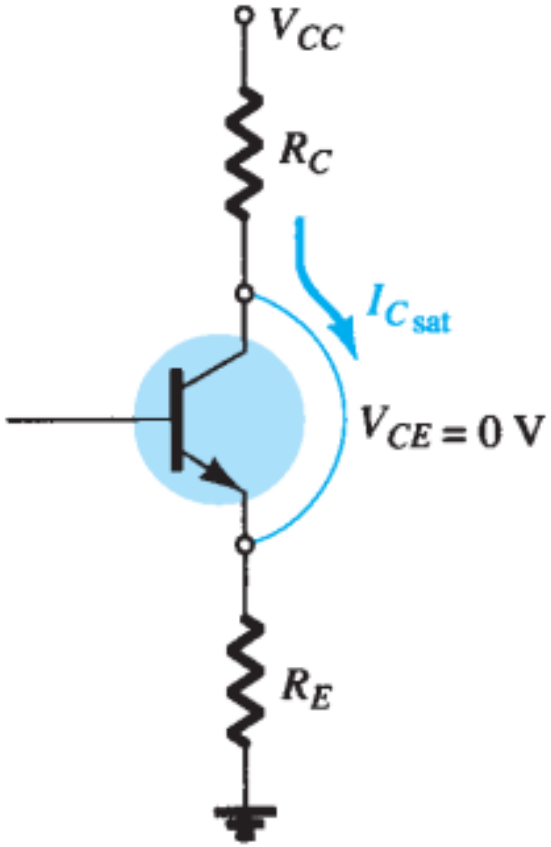
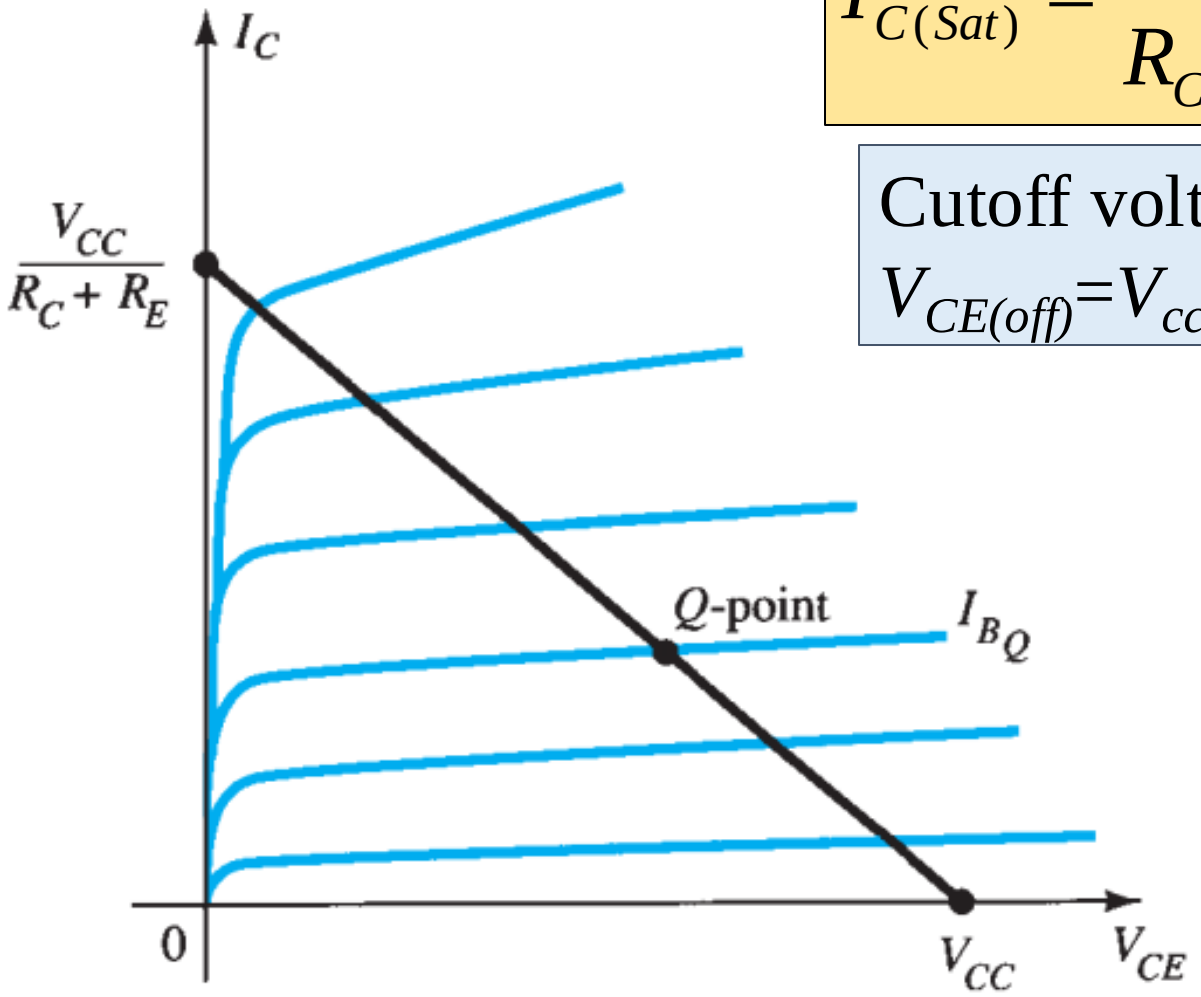


FIG. 4.24
Determining $I_{C_{sat}}$ for the emitter-stabilized bias circuit.



$$I_{C(Sat)} = \frac{V_{CC}}{R_C + R_E}$$

Cutoff voltage
$V_{CE(off)} = V_{cc}$

Formula's for emitter Bias:

$$I_B = \frac{V_{CC} - 0.7}{R_B + (\beta + 1)R_E}$$

$$I_C = \beta I_B$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$I_{C(Sat)} = \frac{V_{CC}}{R_C + R_E}$$

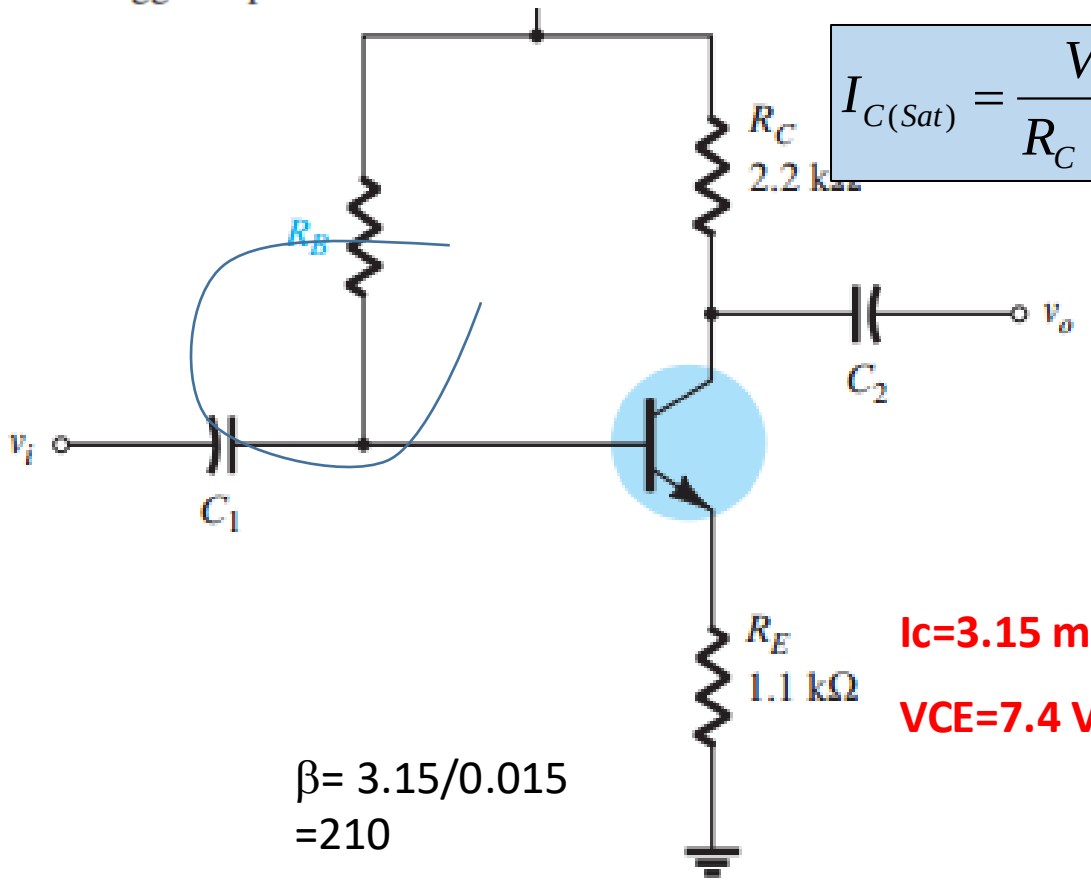
Cutoff voltage

$V_{CE(off)} = V_{cc}$

a. Draw the load line for the network of Fig. 4.26a on the characteristics for the transistor appearing in Fig. 4.26b.
b. For a Q-point at the intersection of the load line with a base current of 15 μA, find the values of I_{C_Q} and V_{CE_Q}.
c. Determine the dc beta at the Q-point.
d. Using the beta for the network determined in part c, calculate the required value of R_B and suggest a possible standard value.

Q-point ?

$$I_{C(Sat)} = \frac{V_{CC}}{R_C + R_E}$$



Ic=3.15 mA

VCE=7.4 V

β= 3.15/0.015
=210

FIG. 4.26a

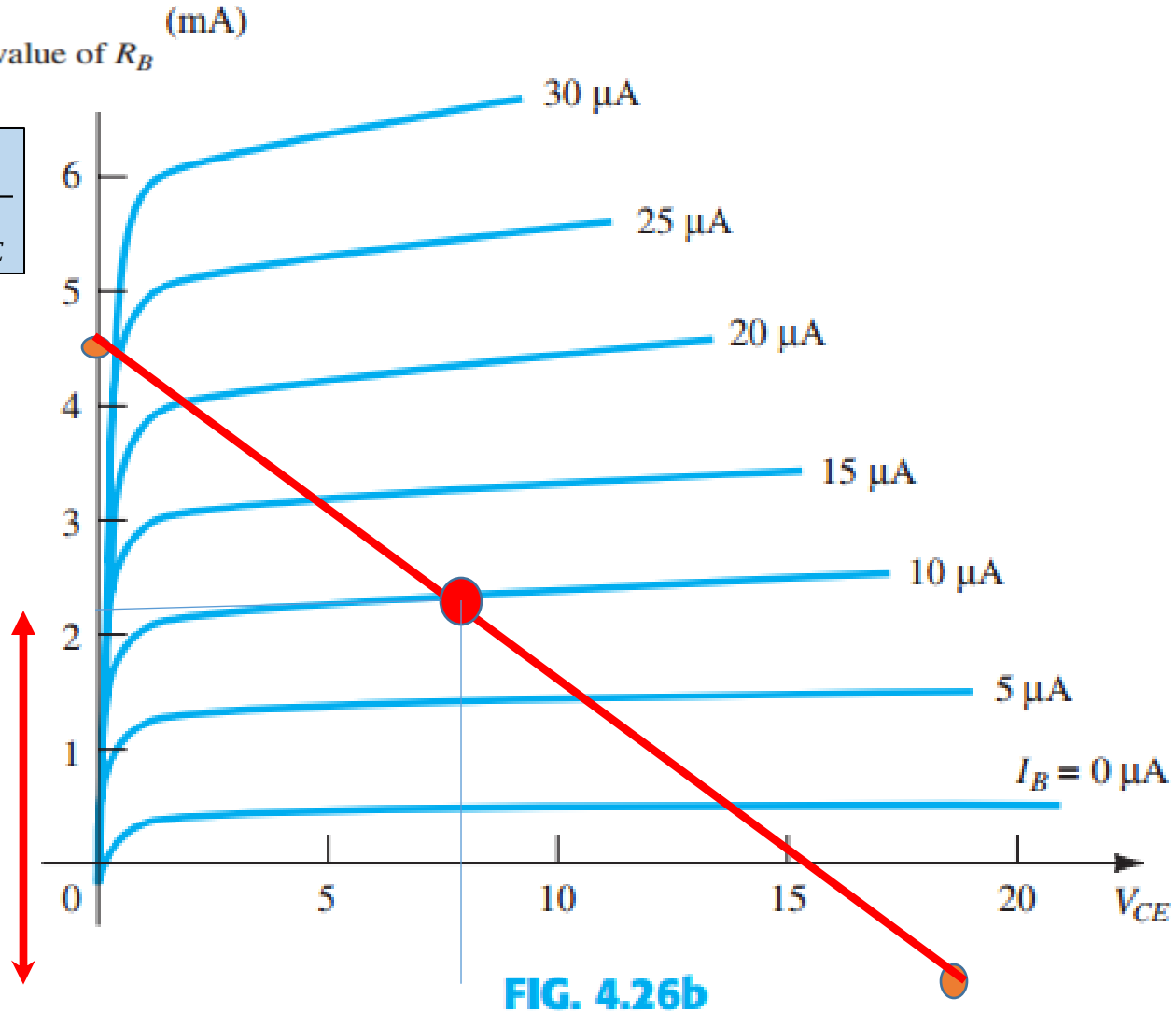
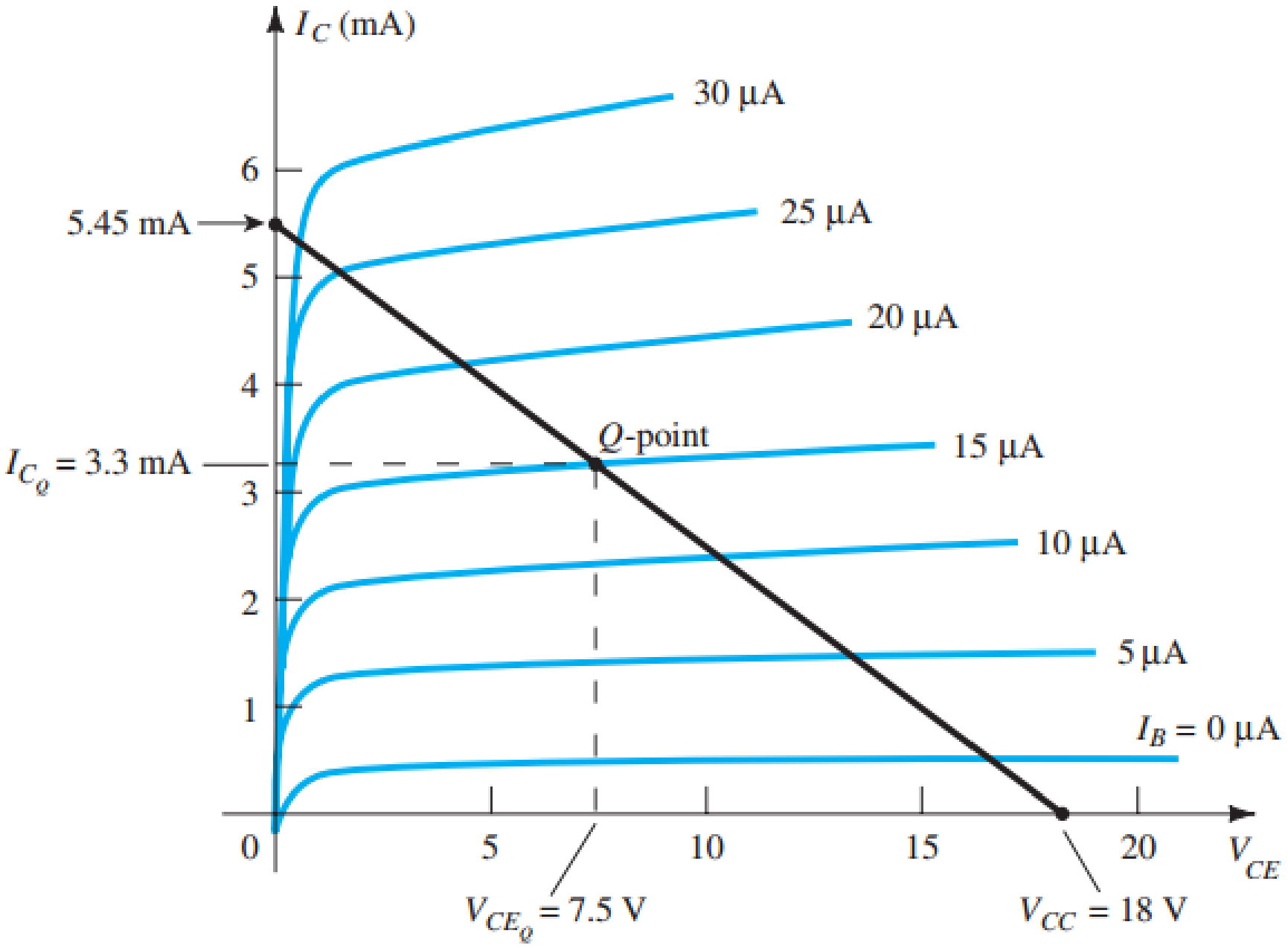
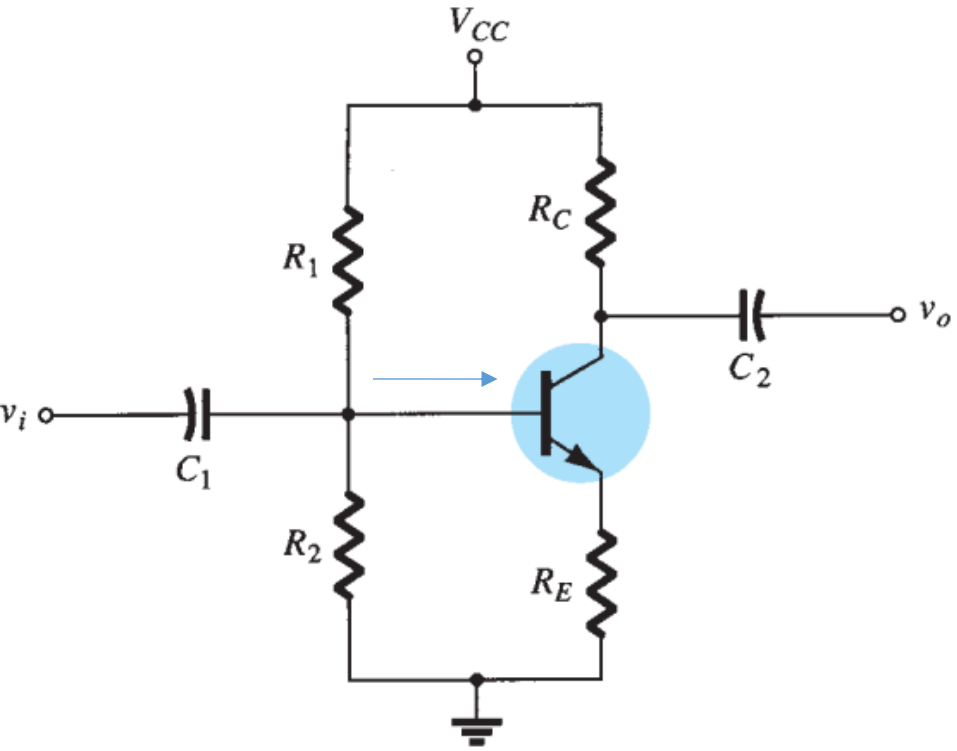


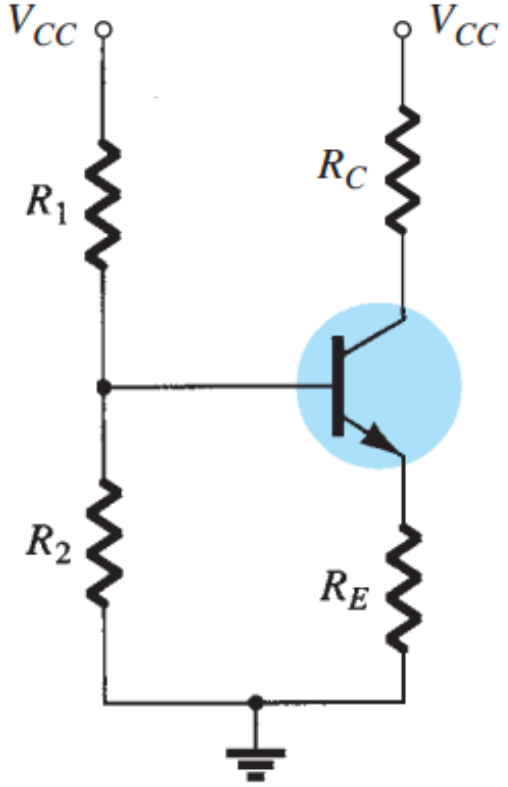
FIG. 4.26b


I_C (mA)
30 µA
25 µA
20 µA
15 µA
10 µA
5 µA
I_B = 0 µA
6
5
4
3
2
1
0
5.45 mA
I_{C_Q} = 3.3 mA
Q-point
5
10
15
20
V_{CE}
V_{CE_Q} = 7.5 V
V_{CC} = 18 V

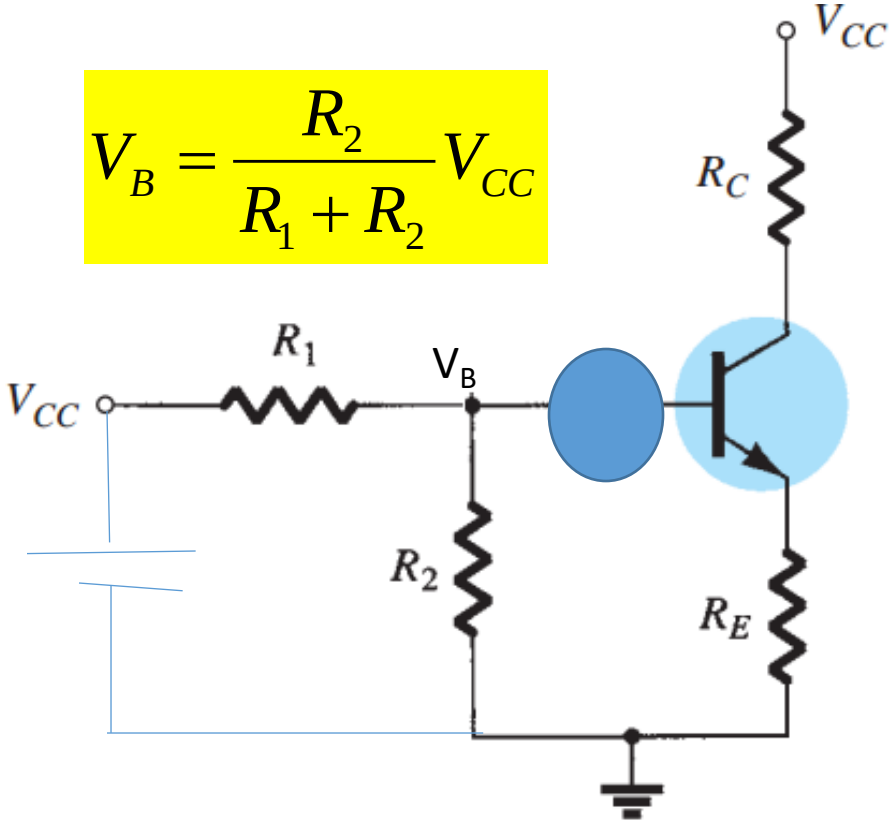
Voltage-Divider Configuration

1. Exact analysis
2. Approximation analysis (design)



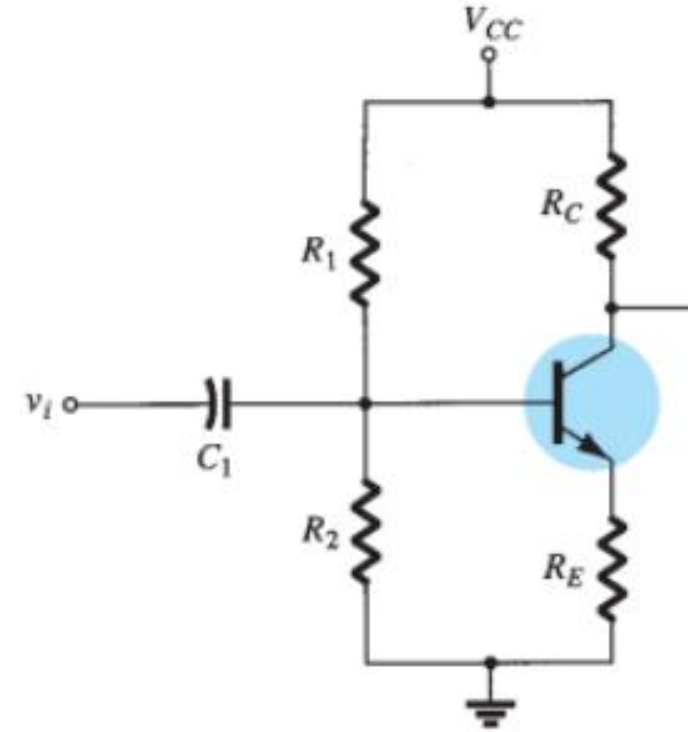


$$V_B = \frac{R_2}{R_1 + R_2} V_{CC}$$

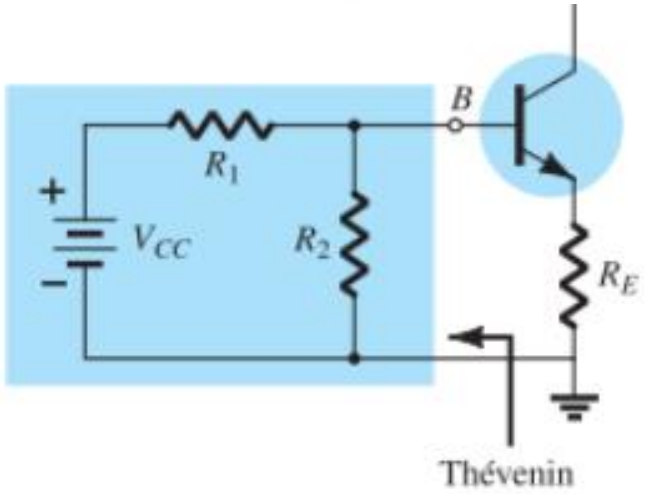


Voltage-Divider Configuration

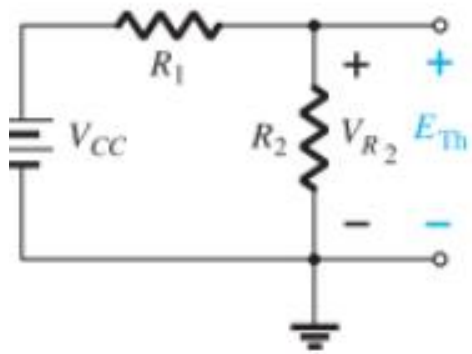
- Voltage-divider bias configuration.



- Exact Analysis



$$R_{\text{Th}} = R_1 \| R_2$$



Applying the voltage-divider rule gives

$$E_{\text{Th}} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

Voltage-Divider Configuration

$$R_{Th} = R_1 \| R_2$$

The Thévenin network is then redrawn

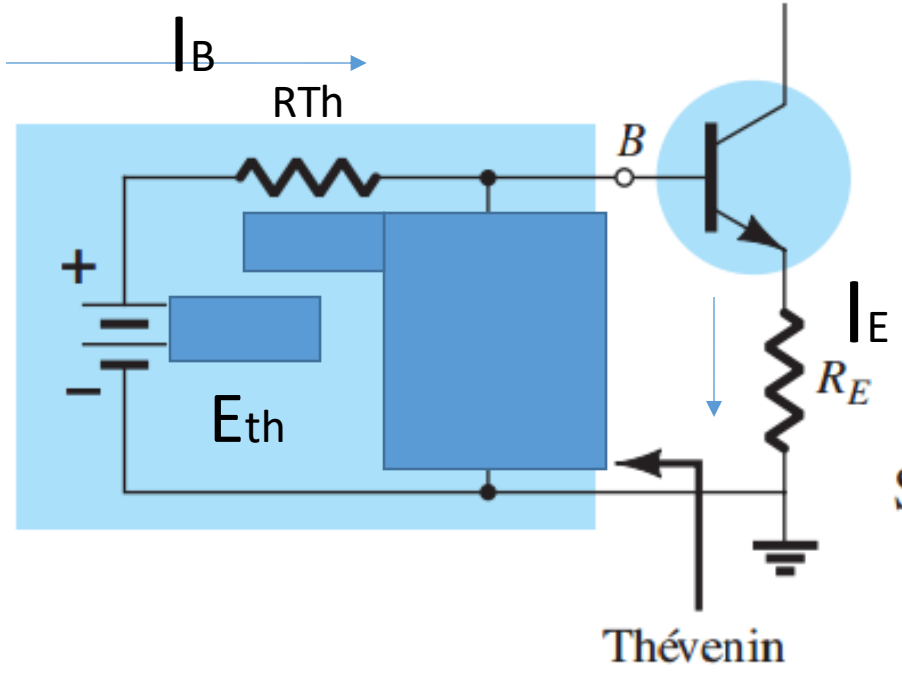


FIG. 4.31

$$E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

by first applying Kirchhoff's voltage law

$$E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

Substituting $I_E = (\beta + 1) I_B$ and solving for I_B yields

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1) R_E}$$

Formula's for Voltage Divider Bias:

For Exact Method

$$I_B = \frac{V_{th} - 0.7}{R_{th} + (\beta + 1)R_E}$$

$$I_C = \beta I_B$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$R_{Th} = R_1 \| R_2$$

$$V_{th} = R_2 \frac{V_{CC}}{R_1 + R_2}$$

$$I_{C(Sat)} = \frac{V_{CC}}{R_C + R_E}$$

Cutoff voltage

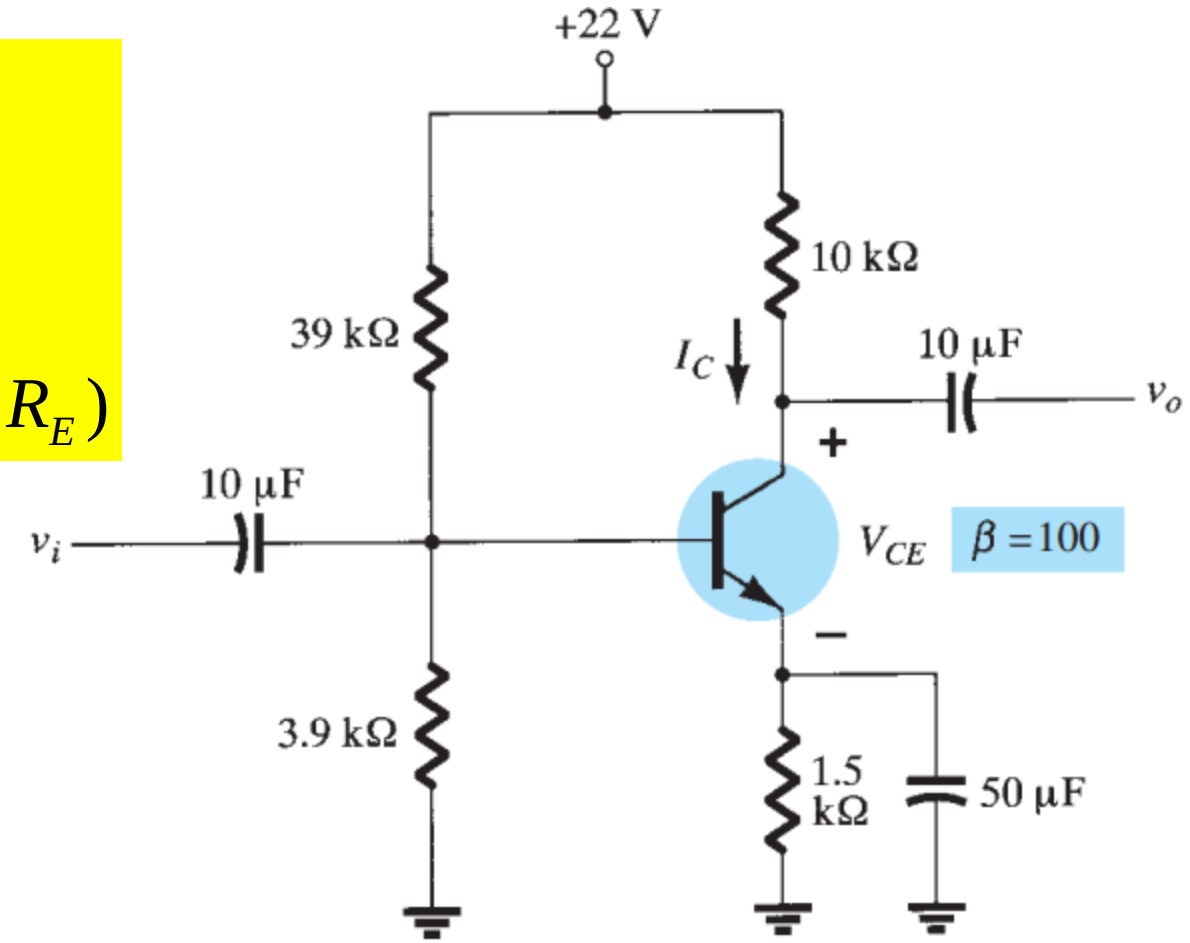
$V_{CE(off)} = V_{cc}$

Find I_c and V_{CE} in the following circuit.

$$I_B = \frac{V_{th} - 0.7}{R_{th} + (\beta + 1)R_E}$$

$$I_C = \beta I_B$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$



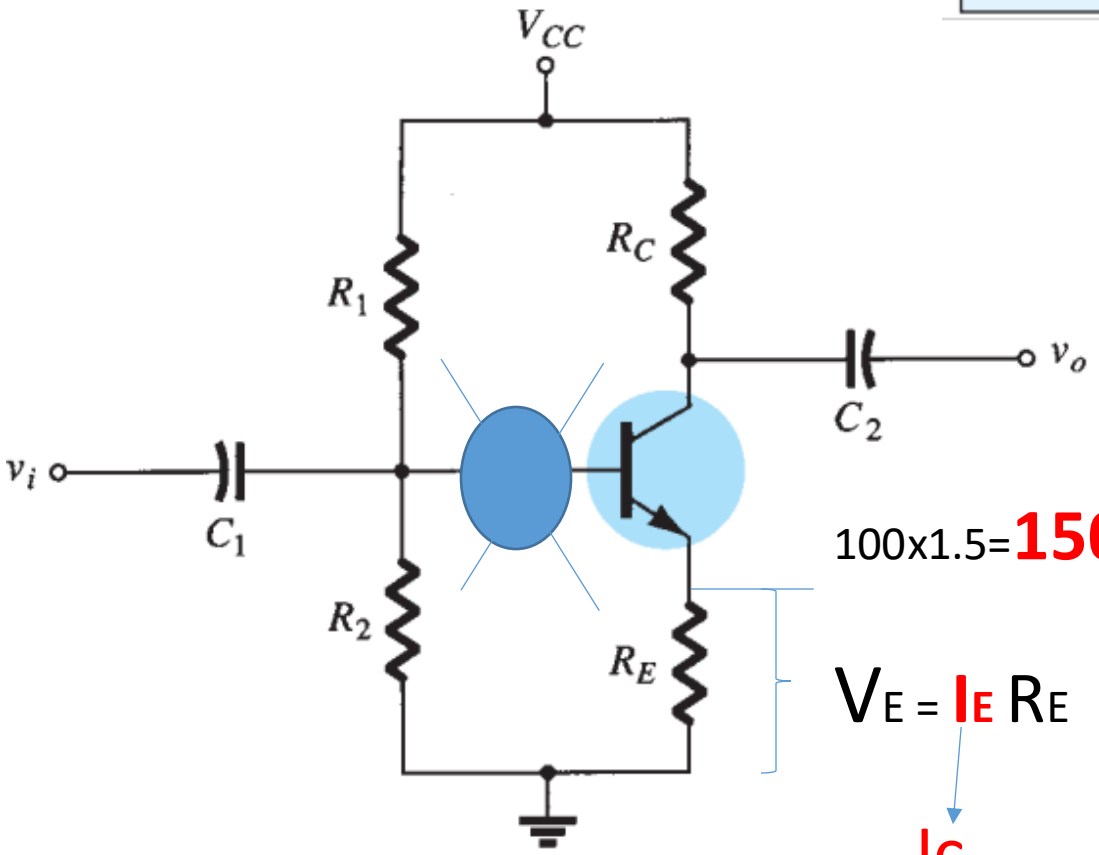
Voltage-Divider Configuration

Approximate Analysis

We assume that the base current I_B is zero

$$\beta R_E \geq 10R_2$$

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC}$$



100x1.5=**150>39**

$V_E = I_E R_E$

I_C

$V_{BE} = V_B - V_E$

$$V_E = V_B - V_{BE}$$

and the emitter current can be determined from

$$I_E = \frac{V_E}{R_E}$$

and

$$I_{C_Q} \cong I_E$$

The collector-to-emitter voltage is determined by

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

but because $I_E \cong I_C$,

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Formula's for Voltage Divider Bias:

Approximate Analysis

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$V_{BE} = V_B - V_E$$

$$V_E = V_B - V_{BE} = V_B - 0.7$$

$$V_E = I_E R_E$$

$$I_E = \frac{V_E}{R_E}, \text{and } I_E \cong I_C$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Determine the voltage and current levels in the following circuit.

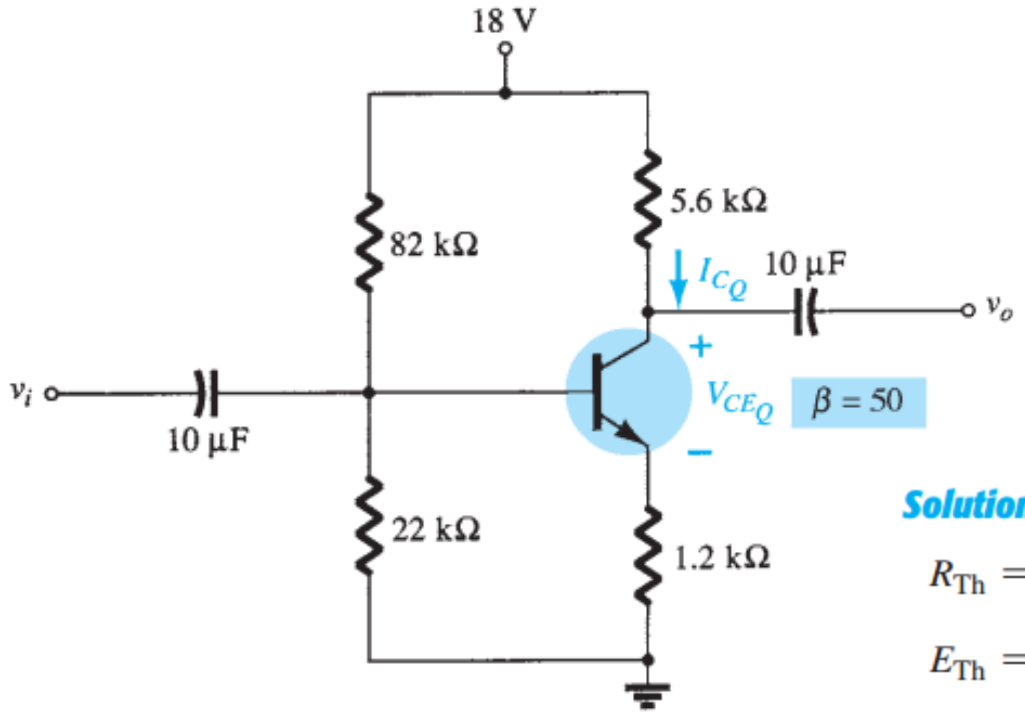
I_B

I_c

V_{CE}

V_C

V_B



Solution: Exact analysis:

$$R_{Th} = R_1 \| R_2 = 82\,k\Omega \| 22\,k\Omega = 17.35\,k\Omega$$

$$E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{22\,k\Omega(18\,V)}{82\,k\Omega + 22\,k\Omega} = 3.81\,V$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E} = \frac{3.81\,V - 0.7\,V}{17.35\,k\Omega + (51)(1.2\,k\Omega)} = \frac{3.11\,V}{78.55\,k\Omega} = 39.6\,\mu A$$

$$I_{C_Q} = \beta I_B = (50)(39.6\,\mu A) = \mathbf{1.98\,mA}$$

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$

$$= 18\,V - (1.98\,mA)(5.6\,k\Omega + 1.2\,k\Omega)$$

$$= \mathbf{4.54\,V}$$

Determine the voltage and current levels in the following circuit.

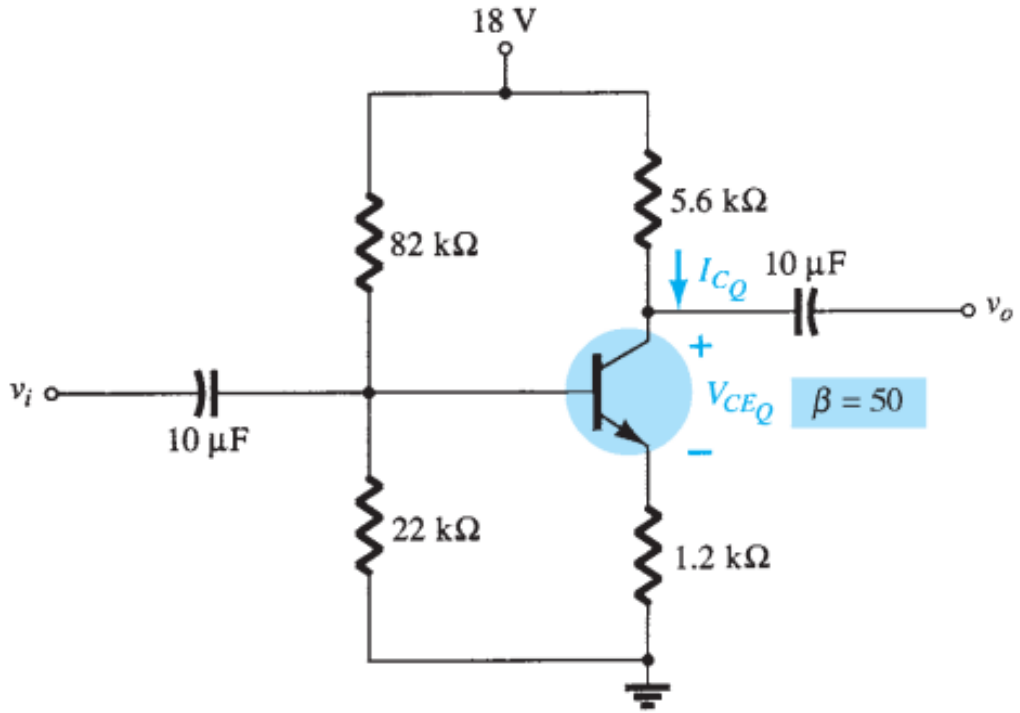
I_B

I_c

V_{CE}

V_C

V_B



$$\beta R_E \geq 10R_2$$

$$(50)(1.2\,\text{k}\Omega) \geq 10(22\,\text{k}\Omega)$$

$$60\,\text{k}\Omega \not\geq 220\,\text{k}\Omega \ (\textit{not satisfied})$$

EXAMPLE 4.31 Determine V_{CE} for the voltage-divider bias configuration of Fig. 4.86.

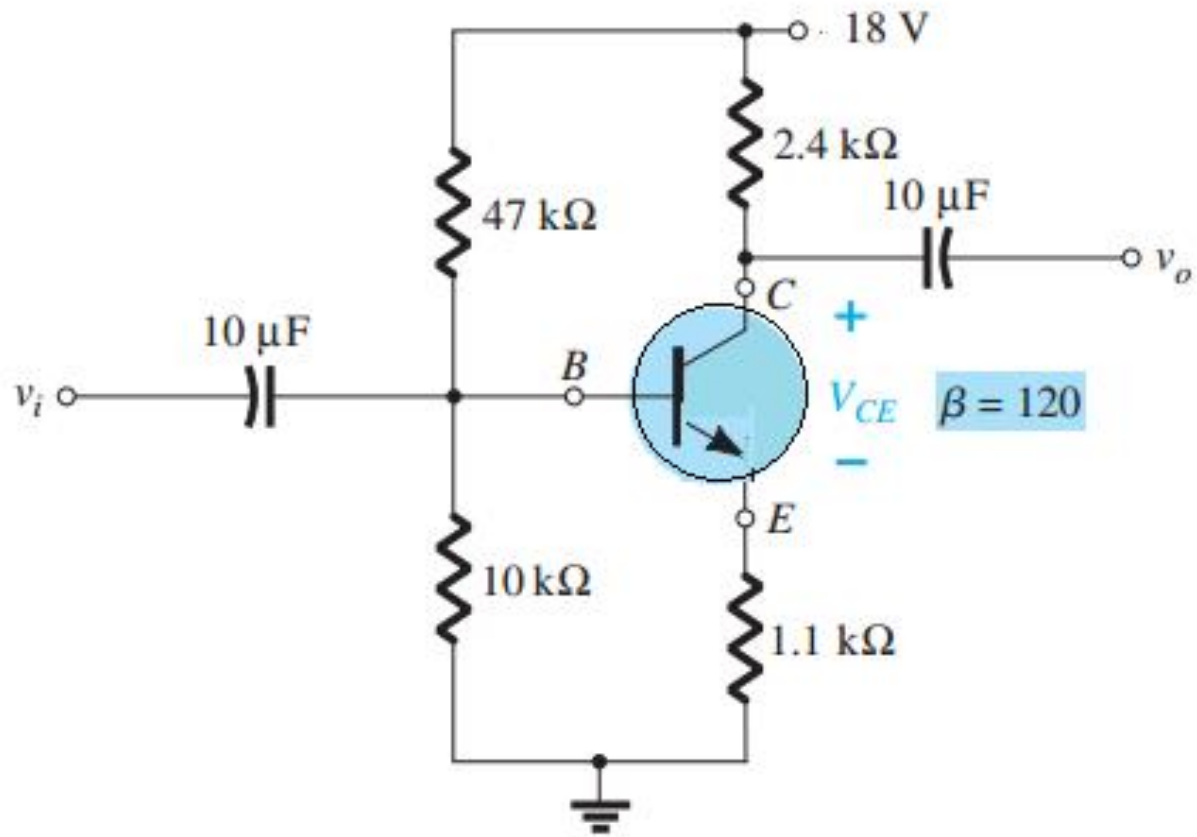


FIG. 4.86

Load line for

Voltage-Divider Configuration

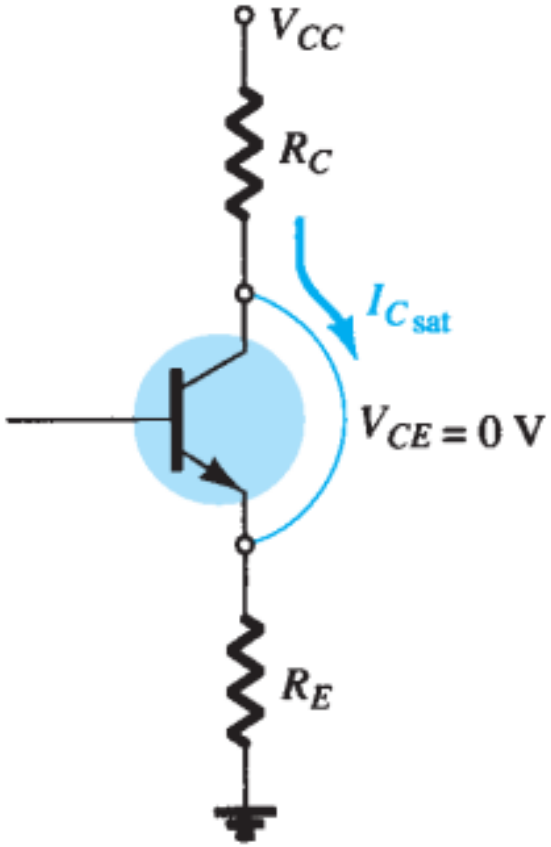
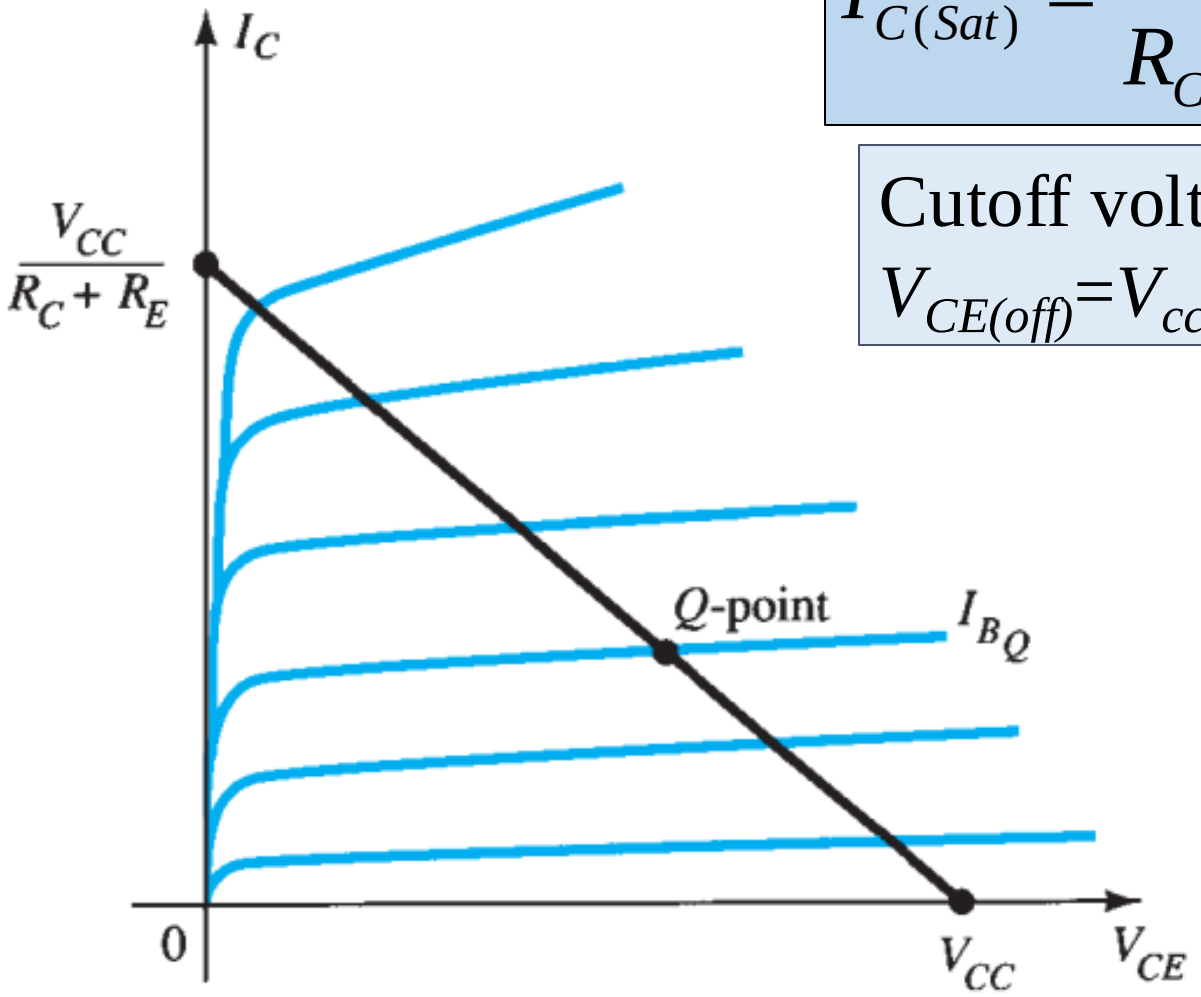
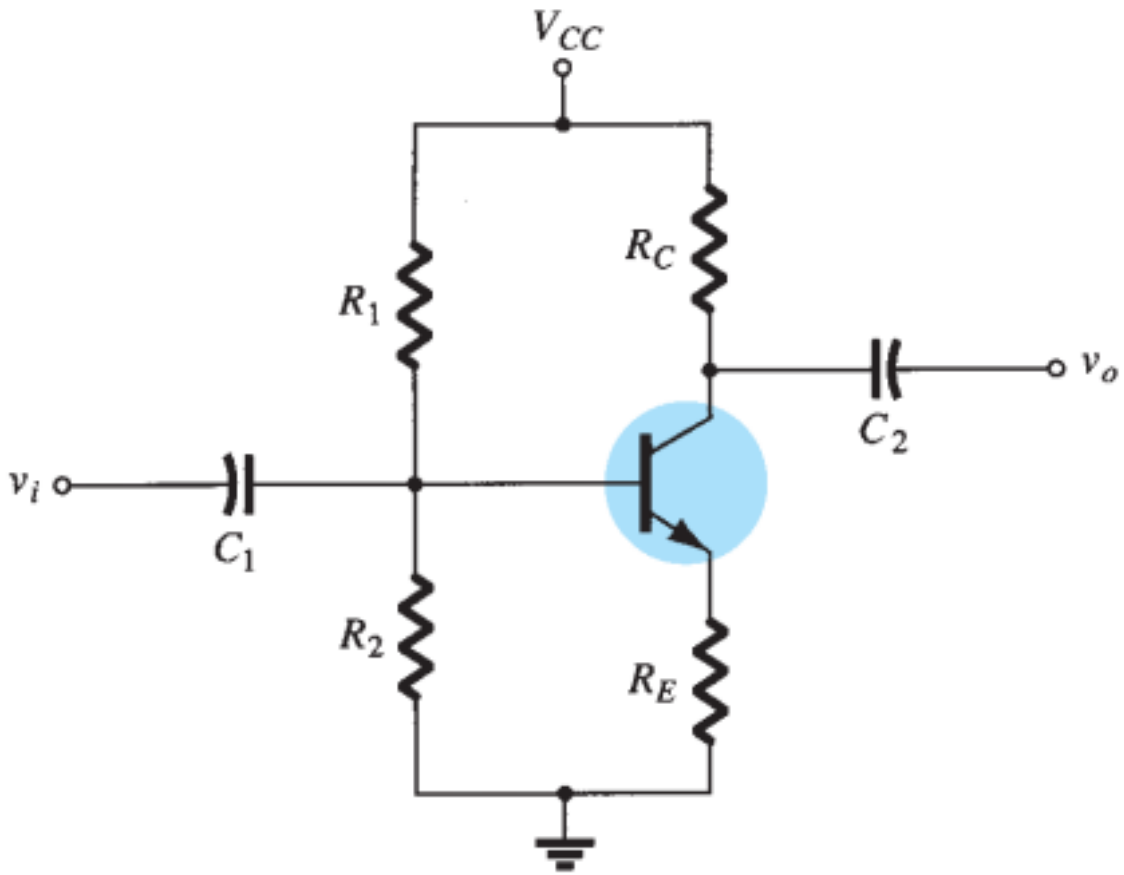


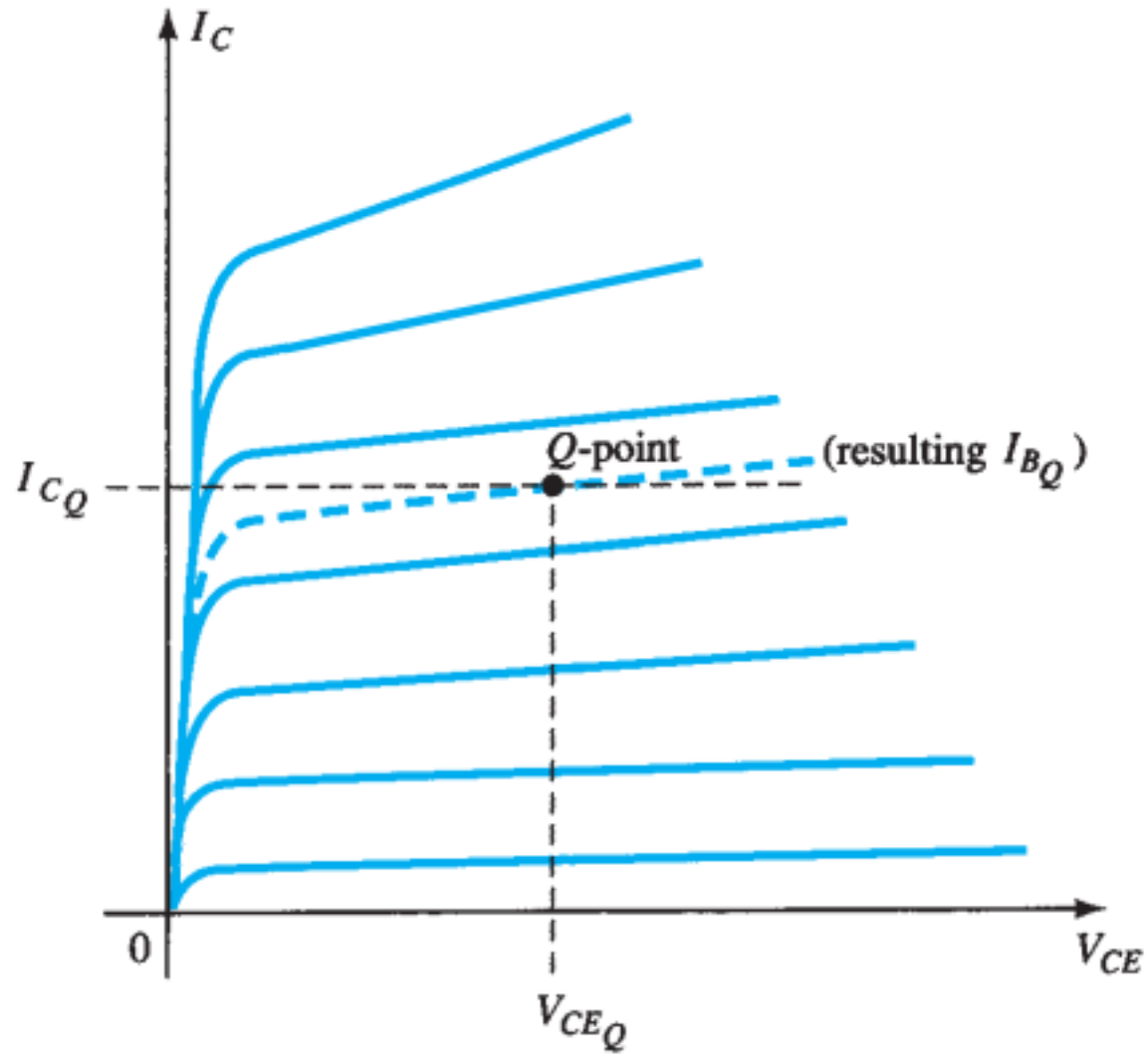
FIG. 4.24
Determining $I_{C_{sat}}$ for the emitter-stabilized bias circuit.



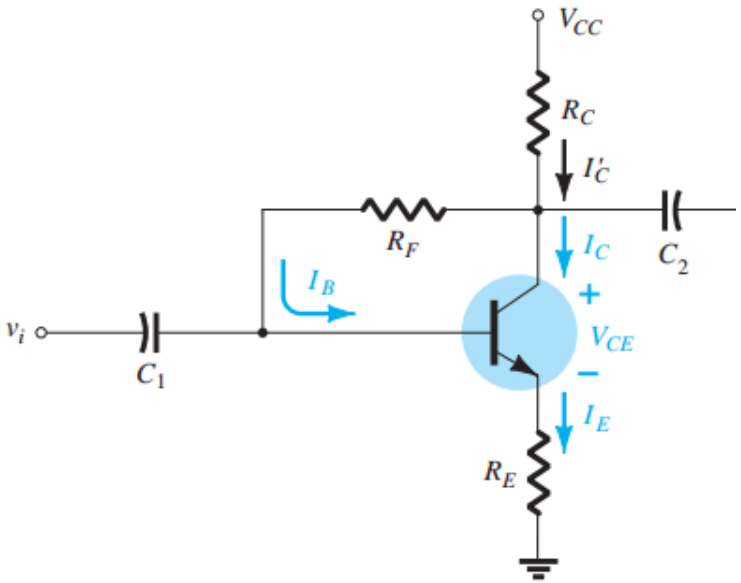
$$I_{C(Sat)} = \frac{V_{CC}}{R_C + R_E}$$

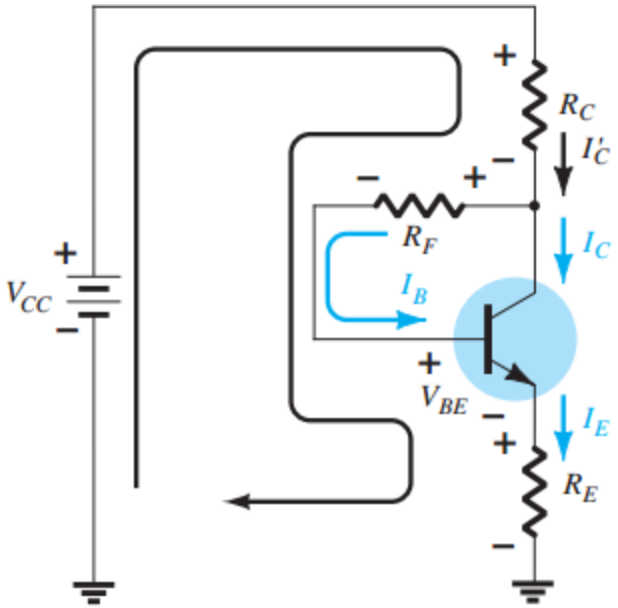
Cutoff voltage
$V_{CE(off)} = V_{cc}$


V_{CC}
R_C
R_1
v_o
C_2
v_i
C_1
R_2
R_E


I_C
I_{C_Q}
Q-point
(resulting I_{B_Q})
0
V_{CE}
V_{CE_Q}

COLLECTOR FEEDBACK CONFIGURATION





Base–Emitter Loop

$$V_{CC} - I'_C R_C - I_B R_F - V_{BE} - I_E R_E = 0$$

but I'_C (where $I'_C = I_C + I_B$).

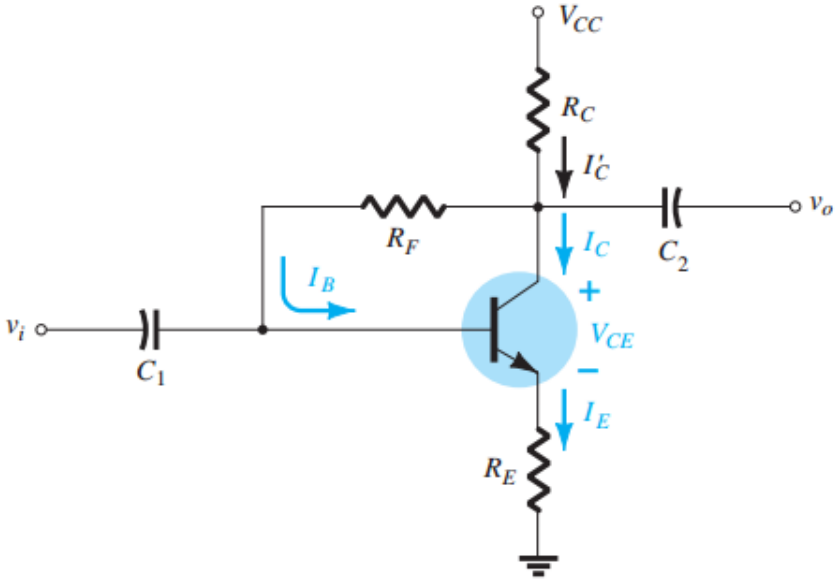
However, $I'_C \cong I_C$ Substituting $I'_C \cong I_C = \beta I_B$ and $I_E \cong I_C$ results in

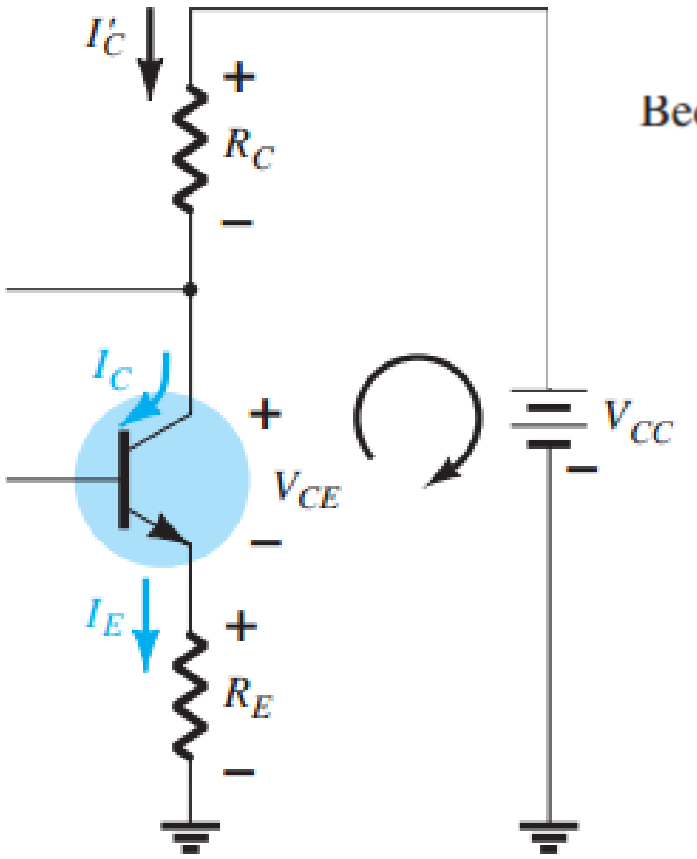
$$V_{CC} - \beta I_B R_C - I_B R_F - V_{BE} - \beta I_B R_E = 0$$

$$V_{CC} - V_{BE} - \beta I_B (R_C + R_E) - I_B R_F = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)}$$

COLLECTOR FEEDBACK CONFIGURATION





$$V_{CC} = I_E R_E + V_{CE} + I'_C R_C$$

Because $I'_C \cong I_C$ and $I_E \cong I_C$, we have

$$I_C(R_C + R_E) + V_{CE} - V_{CC} = 0$$

$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)}$$