Course title: **Electronic circuit I**

Course code: **EEE 215**

**Lecture 4**

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Semester: Summer 2020

# Classification of Semiconductor

in terms of adding impurity or doping

1. Minority
2. Majority

**Intrinsic Semiconductor (pure form/no dopant)**

Temperature/photon source (minority)

Si, Ge (4)

**Extrinsic Semiconductor (impurity are added)**

Majority

**N-type semiconductor**

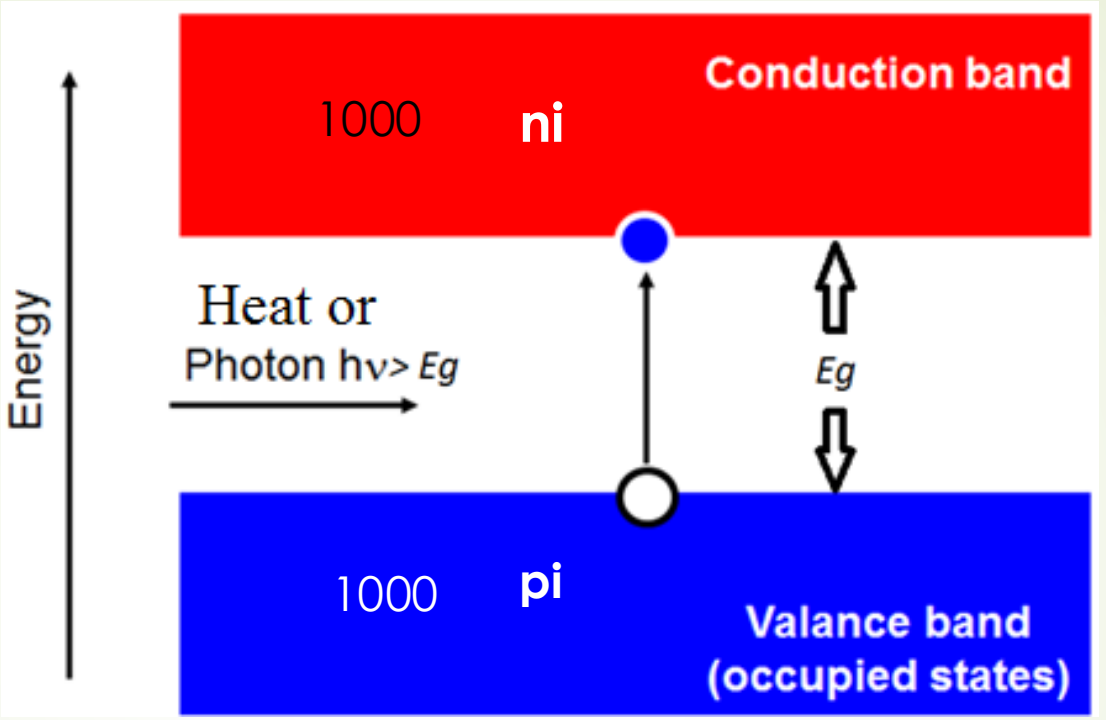
**Majority are electrons**

**p-type semiconductor**

**Majority are holes**

Energy is equivalent to temperature

E= KT
E=hv




empty

Filled by electrons

Holes mean absence of electron

**When T is 0 kelvin**

**When T is increased to 300 Kelvin**

**EHP= electron-hole pair, ni=pi**

**Minority**

1. **Thermalization process.**
2. **Laser/light absortion**

# Extrinsic Semiconductors: 1. n-type & 2. p-type

Extrinsic semiconductors are made from intrinsic semiconductors by a process called doping, and the impurity atoms are called dopants

The impurity atom can be penta-valent (n-type doping, donor) or tri-valent (p-type doping, acceptor)

Atoms on the right column are donors and on the left column are acceptors

**Example: For Si, P, As are donors while B, Ga are acceptors**

**Table 1.2** Abbreviated Periodic Chart of the Elements.

| II | III | IV | V | VI |
|---|---|---|---|---|
| 4 Be | 5 B | 6 C | 7 N | 8 O |
| 12 Mg | 13 Al | 14 Si | 15 P | 16 S |
| 30 Zn | 31 Ga | 32 Ge | 33 As | 34 Se |
| 48 Cd | 49 In | 50 Sn | 51 Sb | 52 Te |
| 80 Hg | 81 Tl | 82 Pb | 83 Bi | 84 Po |

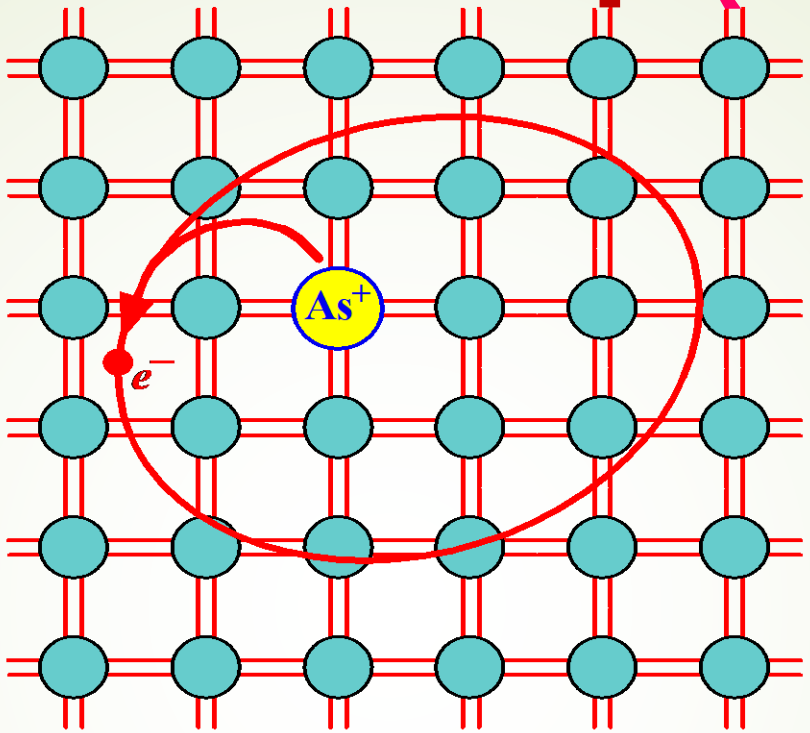
# Extrinsic Semiconductors [n (electron)-type]

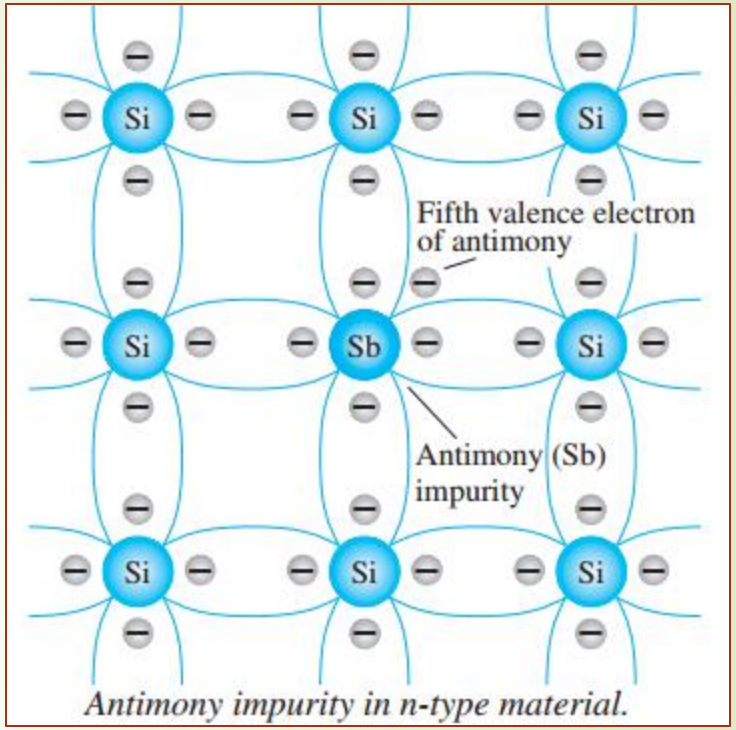
1 electron
1 As

10000 As/Sb/P
10000 electron
As/Sb/P= Donor impurity

**Donor impurity=$N_D^+$= $n_n$**

$n_n$= majority carrier



Antimony impurity in n-type material.

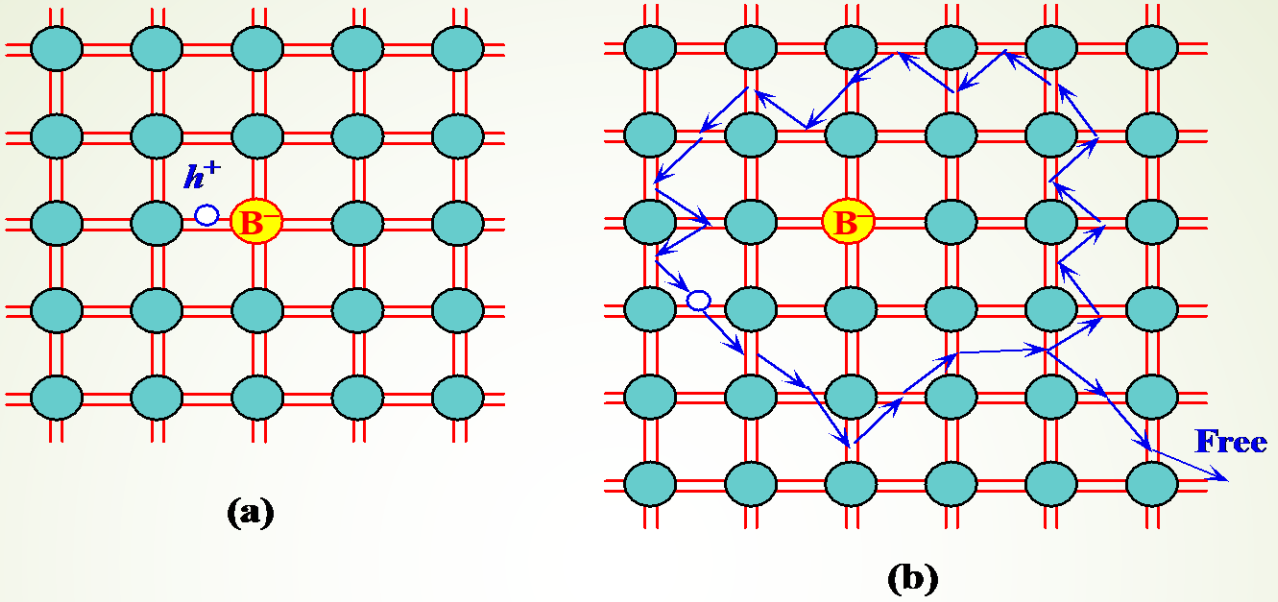
**Si (4)+ pentavalent-As or Sb-impurity (4+1) = n-type**

Fig. 5.9: Arsenic doped Si crystal. The four valence electrons of As allow it to bond just like Si but the fifth electron is left orbiting the As site. The energy required to release to free fifth-electron into the CB is very small.

From *Principles of Electronic Materials and Devices, Second Edition*, S.O. Kasap (© McGraw-Hill, 2002)
http://Materials.Usask.Ca

# Extrinsic Semiconductors (p(holes)-type)

1 B
1 hole




For complete bond we need 8 electrons;
But we have one missing

**Hole is absence or shortage of electron**

1000000 B
1000000 Holes

**Na=Acceptor impurity**

**Si (4) + trivalent-B-impurity (3) = p-type**

**$Na^- = p_p$**

$Holes = p_p$

$1x10^{16}$

Fig. 5.11: Boron doped Si crystal. B has only three valence electrons. When it substitutes for a Si atom one of its bonds has an electron missing and therefore a hole as shown in (a). The hole orbits around the B– site by the tunneling of electrons from neighboring bonds as shown in (b). Eventually, thermally vibrating Si atoms provides enough energy to free the hole from the B– site into the VB as shown.

From *Principles of Electronic Materials and Devices, Second Edition*, S.O. Kasap (© McGraw-Hill, 2002)
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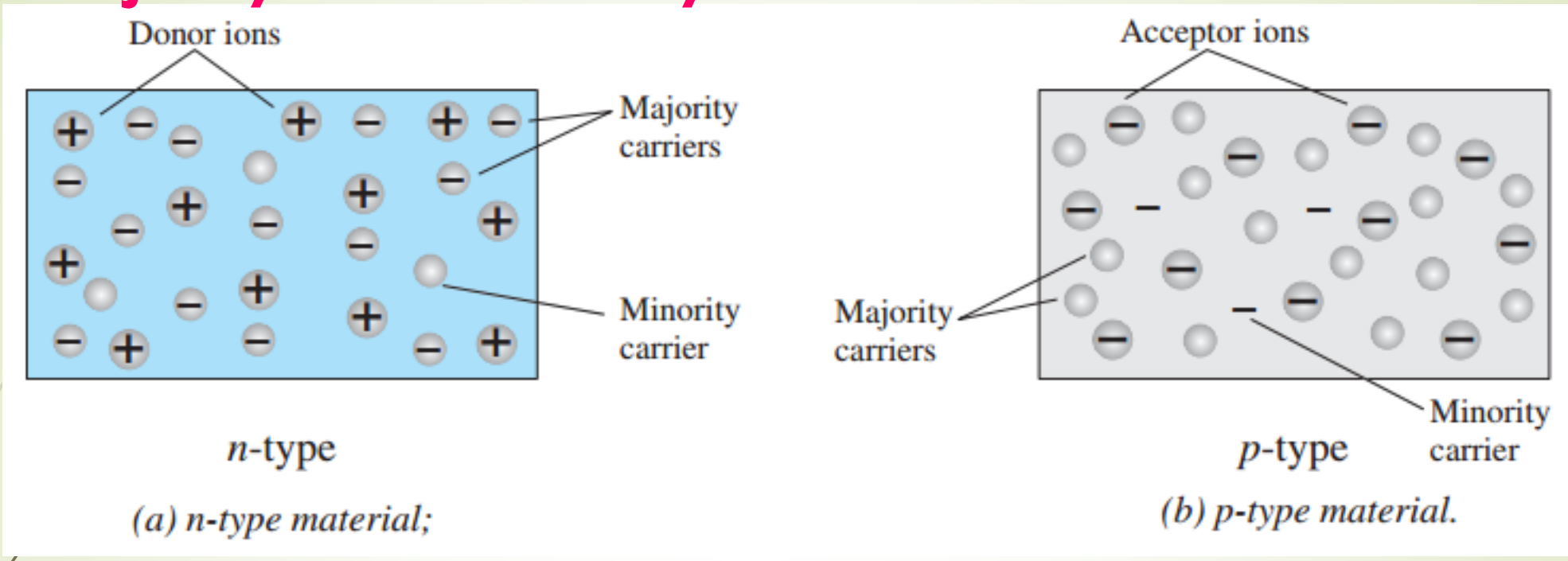
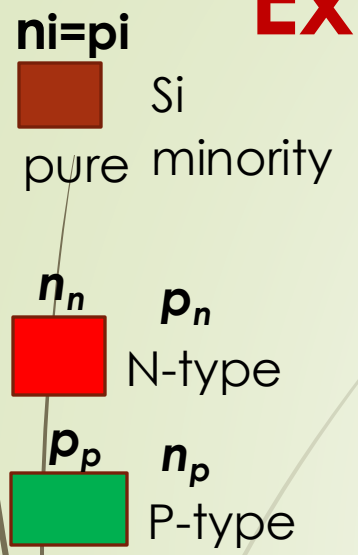
# Majority and minority carriers:




- ***In an n-type material the electron is called the majority carrier and the hole the minority carrier. ($N_D^+$=donor, $n_n$=majority electron in 'n', $p_n$=minority holes in 'n')***
- ***In a p-type material the hole is the majority carrier and the electron is the minority carrier. ($N_a^-$=Acceptor, $p_p$=majority holes in 'p', $n_p$=minority electrons in 'p')***

# Extrinsic Semiconductors (Carrier Density)




**At equilibrium:** $p_p n_p = n_n p_n = n_i^2$

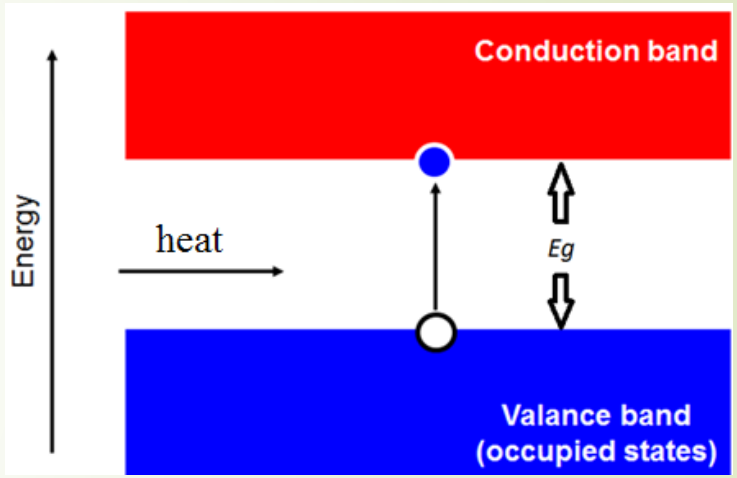
n-type $n_n p_n = n_i^2$ p-type $p_p n_p = n_i^2$

**For n-type doped materials:**

$$n_n = N_D \qquad p_n = \frac{n_i^2}{N_D}$$

**For p-type doped materials:**

$$p_p = N_A \qquad n_p = \frac{n_i^2}{N_A}$$




**EHP**

**ni=pi it depends on Temperarure**

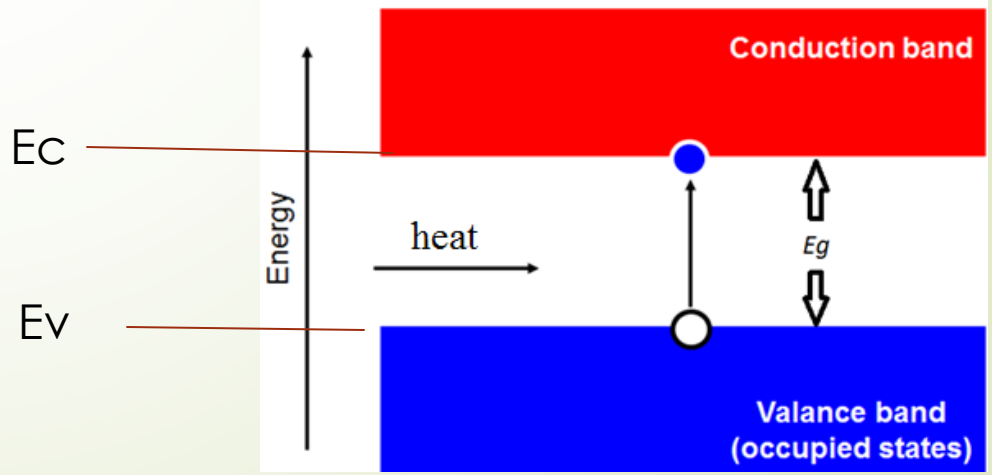
**T=300 and Si**

**ni=1.5x10$^{15}$ /cm3**

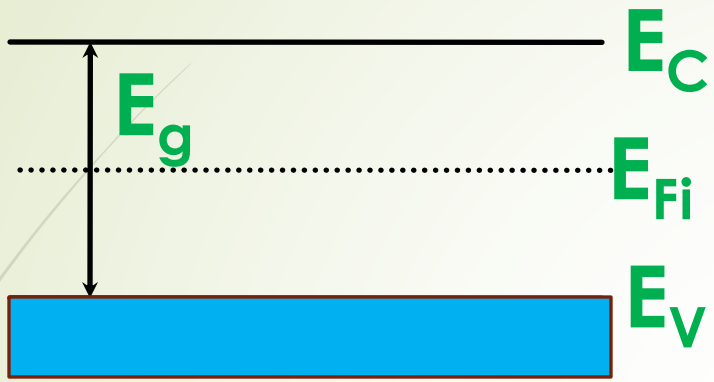
- Thermalization process creates pair of electrons-holes that are called Minority charge carriers (**Thermally induced minority carriers, ni, pi, ni=pi**).

**Table 4.2** | Commonly accepted values of $n_i$ at $T = 300$ K

| | |
|---|---|
| Silicon | $n_i = 1.5 \times 10^{10}\ \text{cm}^{-3}$ |
| Gallium arsenide | $n_i = 1.8 \times 10^{6}\ \text{cm}^{-3}$ |
| Germanium | $n_i = 2.4 \times 10^{13}\ \text{cm}^{-3}$ |



# Intrinsic/pure Semiconductors




CB : Free electrons reside

VB : Bound electrons & free holes reside

$E_C$ : Conduction band edge

$E_V$ : valence band edge

$E_g$ : band gap

$E_F$ : Fermi energy (probability of finding electrons)

We are interested in free electrons in CB and free holes in VB for electronic properties & desired conductivity

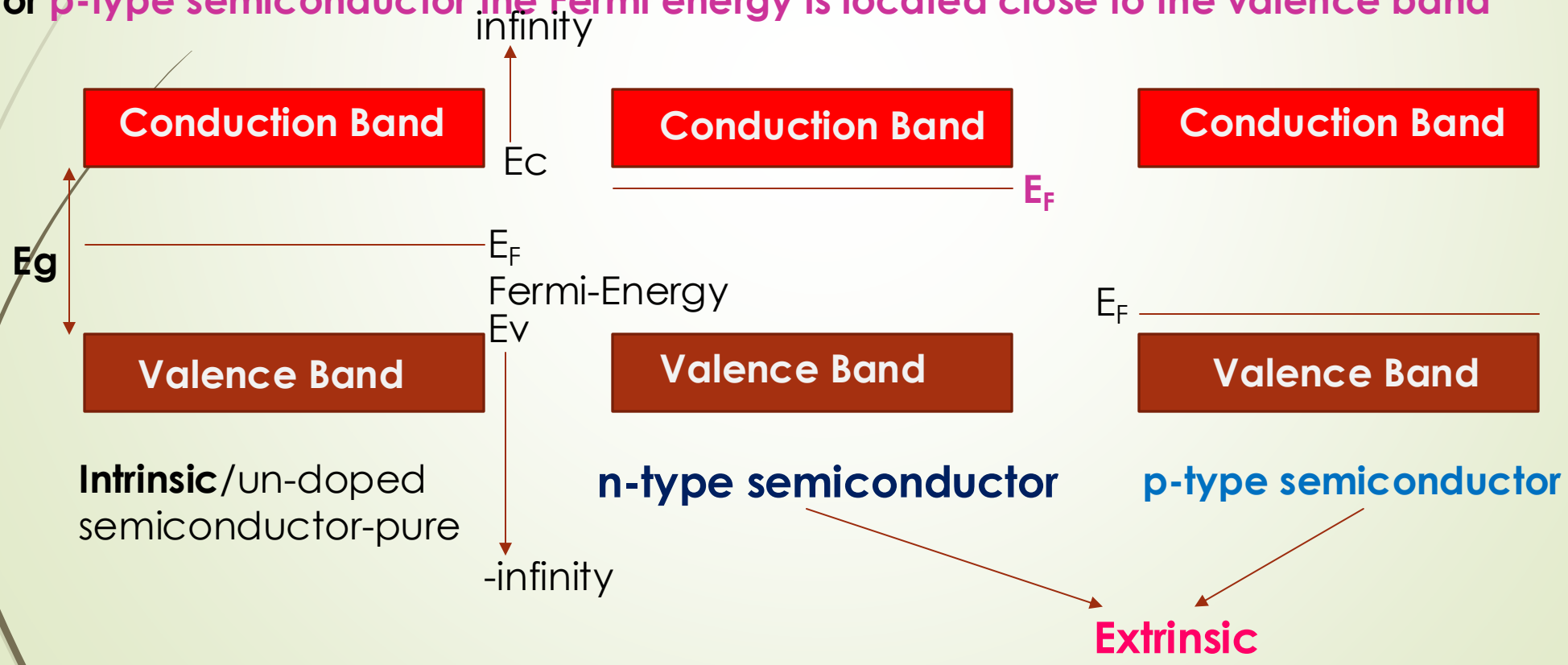
- ***For intrinsic/un-doped semiconductor the Fermi energy lies at the middle of the conduction band***
- **Fermi Energy** (it is the energy **below** which all states are filled by electrons)

# Extrinsic Semiconductors

## 1. n-type

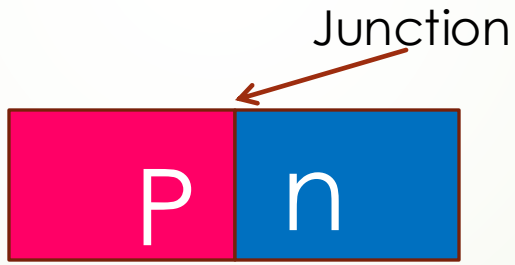
## 2. p-type

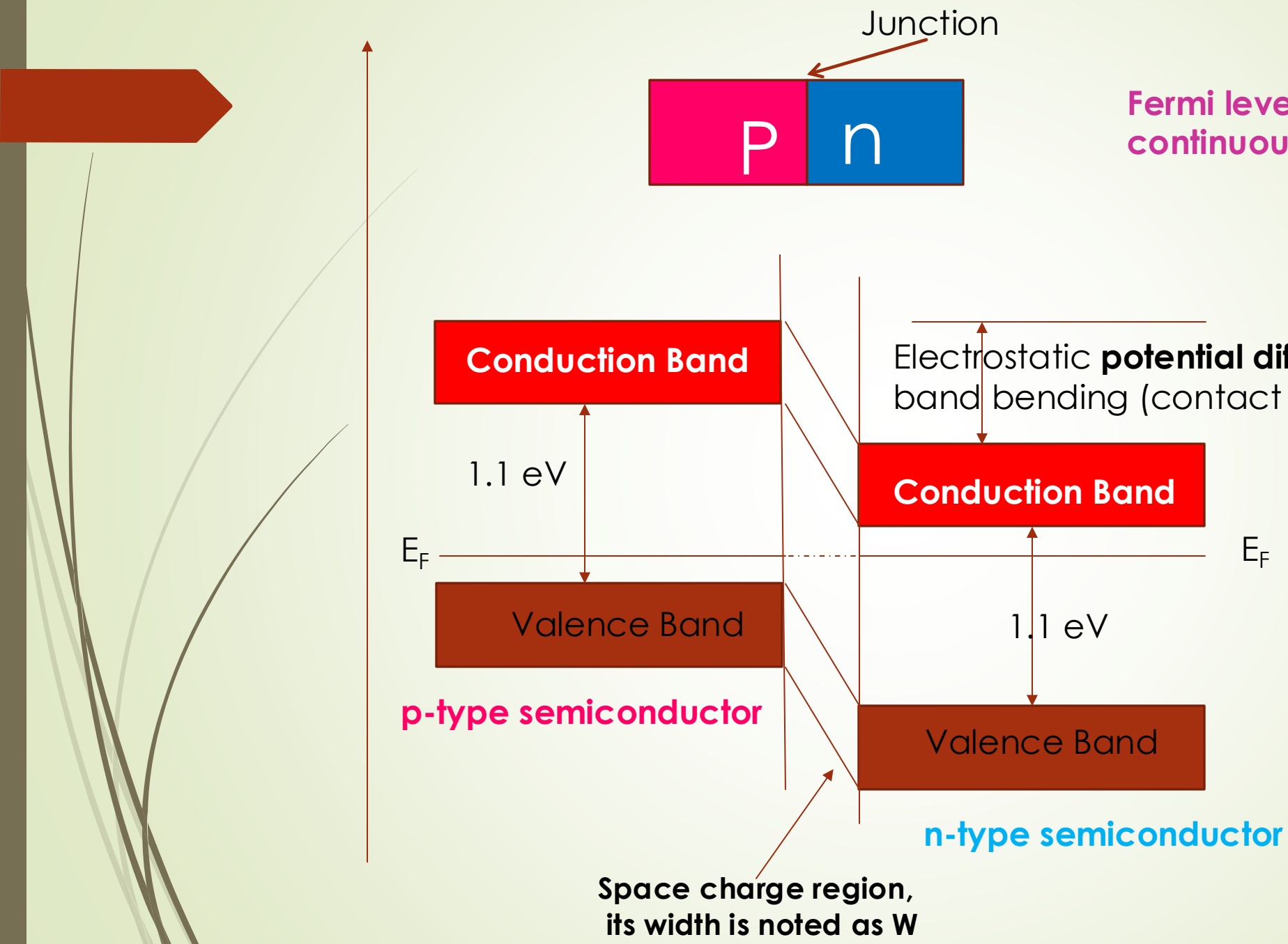
- For intrinsic/un-doped/pure semiconductor the Fermi energy lies at the middle of the conduction band
- For n-type semiconductor the Fermi energy, $E_F$ is located close to the conduction band
- For p-type semiconductor the Fermi energy is located close to the valence band



# p-n Junction is the most fundamental device building block

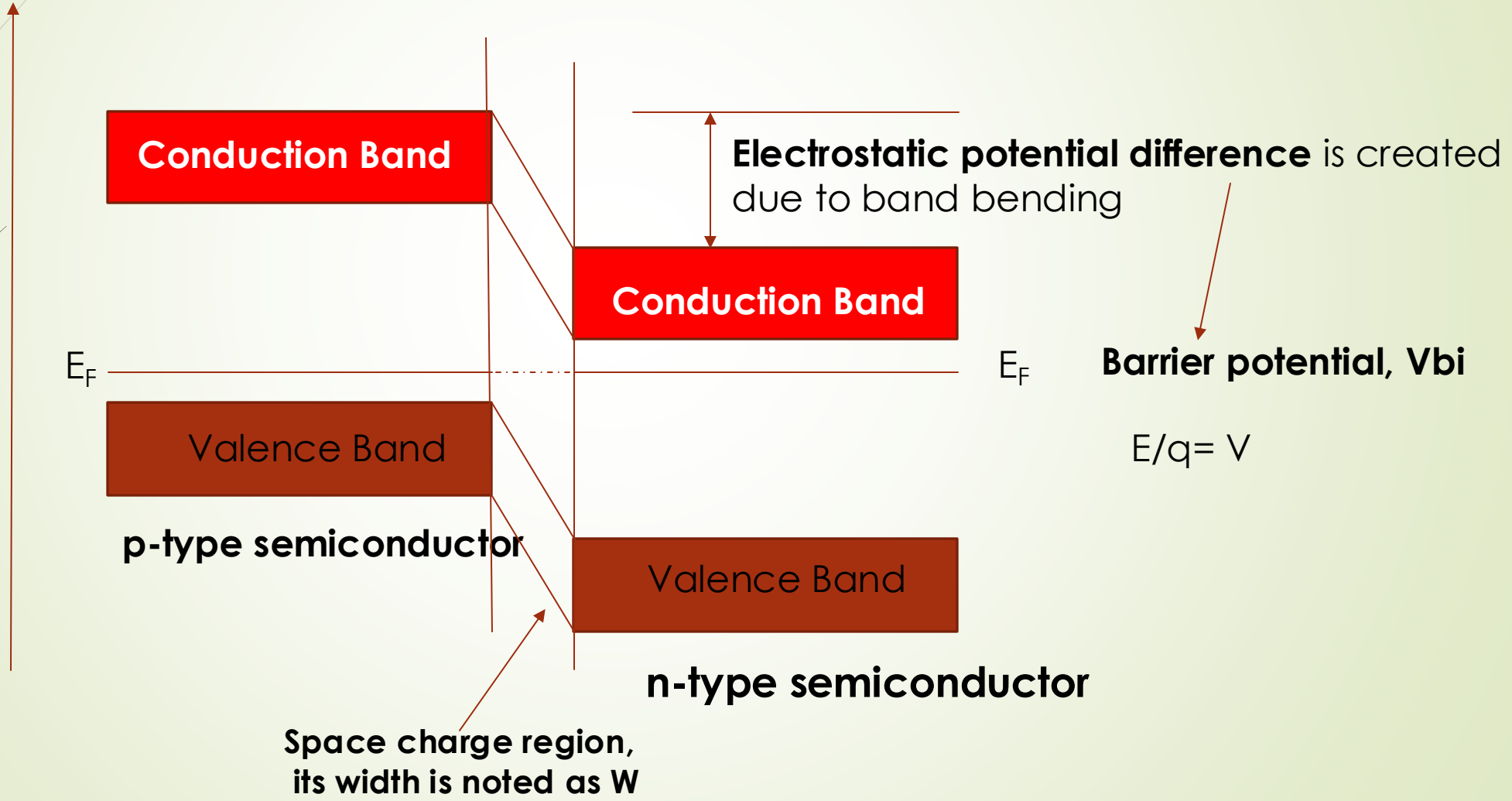
- When p-type Semiconductor is suitably in contact with n-type semiconductor, the p-n junction is formed.




Junction
P
n
Fermi level will be continuous
Conduction Band
1.1 eV
$E_F$
Valence Band
p-type semiconductor
Electrostatic potential difference is created due to band bending (contact or barrier potential) Vb
Conduction Band
$E_F$
1.1 eV
Valence Band
n-type semiconductor
E/q=V
Vq=E
Space charge region,
its width is noted as W

# p-n junction: when p type is suitably in contact with n type how does the energy diagram look?

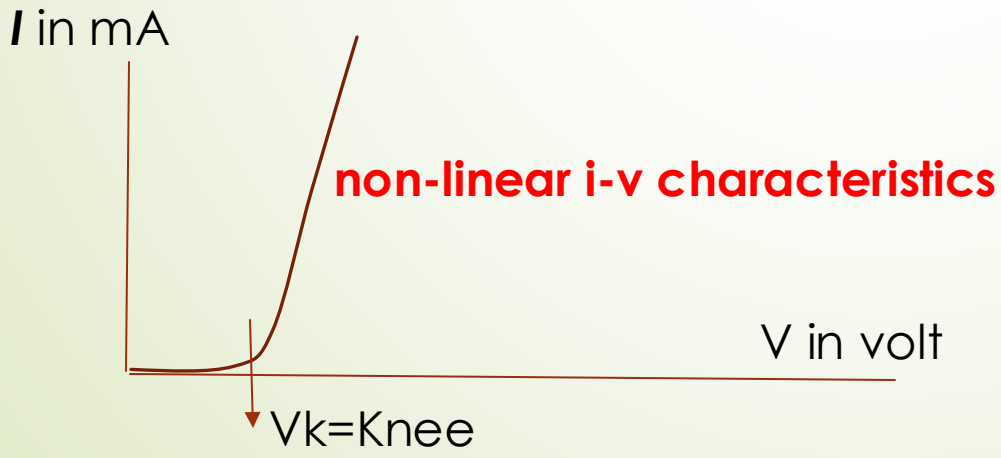
1. **Fermi level should be continuous throughout the junction**
2. **and therefore there will be band bending at the junction**

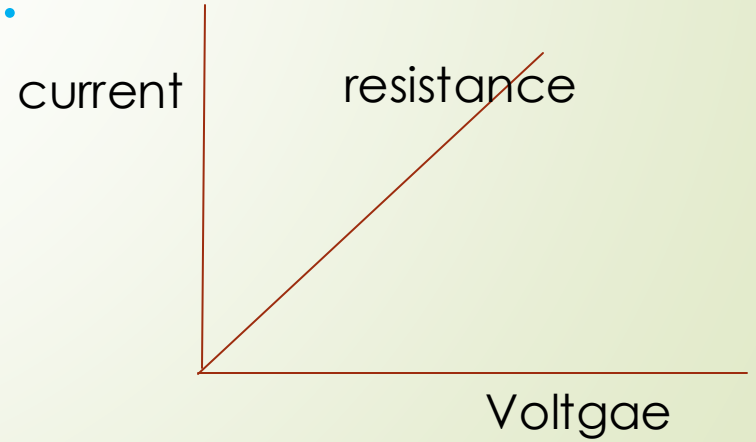


# Semiconductor diode:

**Diodes are the most simplest and fundamental non-linear circuit elements.**

- A **diode** is a **two-terminal electronic component**, Just like resistors, but unlike the resistor which has linear relationship between the current flowing through it and the voltage appearing across it, **the diode has non-linear i-v characteristics.**

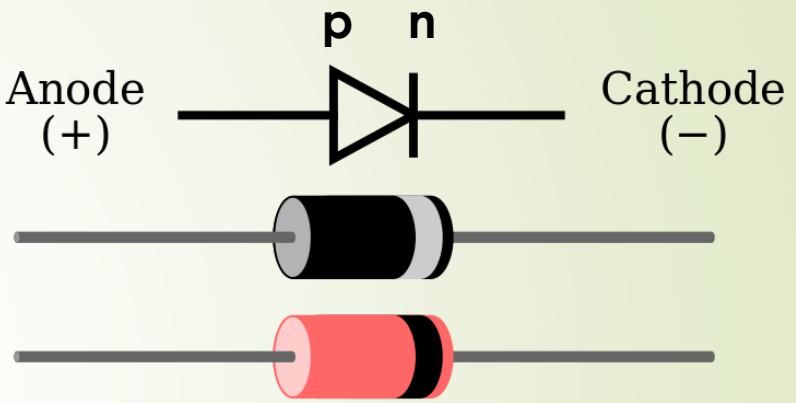


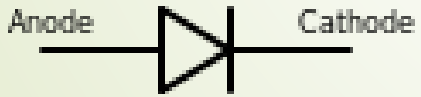



# Semiconductor diode:

A **diode** shows

- low (ideally zero) resistance to current flow in forward direction,
- and high (ideally infinite) resistance in the reverse.
- The discovery of crystals' rectifying abilities was made by German physicist Ferdinand Braun in 1874. Today most diodes are made of silicon (Si), but other semiconductors such as selenium or germanium (Ge) are sometimes used.
- **A semiconductor diode, the most common type today, is a crystalline piece of semiconductor material with a p–n junction connected to two electrical terminals.**



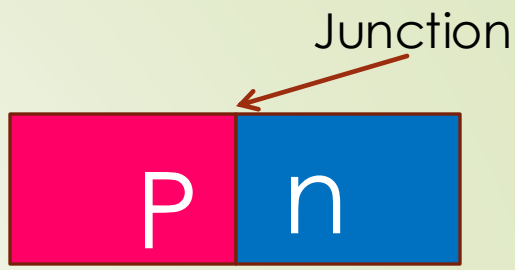




Conventional Diode


Photo diode symbol


Zener diode symbol

# A diode is formed by the formation of p-n junction:




**When a p-type semiconductor is suitably in contact with a n-type semiconductor, the contact surface is called p-n junction.**

It is important to note that simply butting an n-type semiconductor against a p-type semiconductor does not form a junction. The irregular surface atomic forces at such a physical discontinuity at the interface simply prevent junction formation. It is essential that the crystalline background forces are uniform across the junction, i.e., the basic internal crystal regularity is maintained across the junction.

***A semiconductor junction is commonly formed by doping a semiconductor so that the impurity concentration varies from n-type to p-type. The electrical junction forms about the 'metallurgical' junction where the transition from one doping type to the other occurs.***

***The p-n junction may be produced by any one of the following***

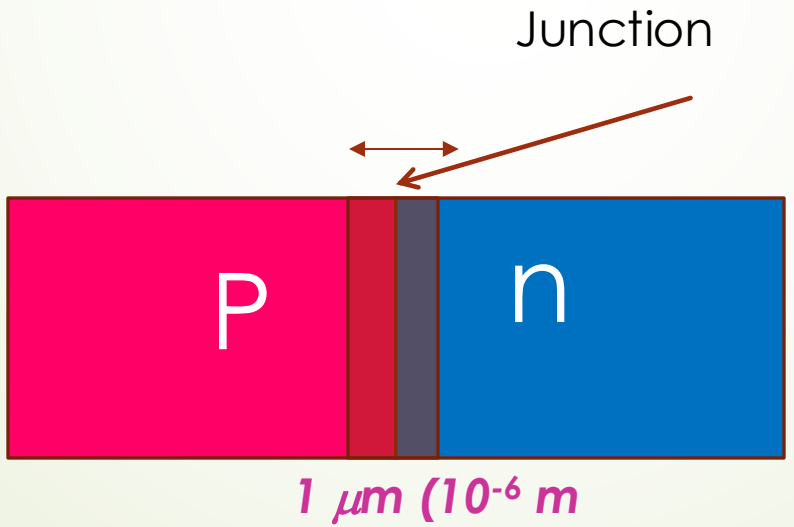
***i. Grown junction***
***ii. Alloy junction***
***iii. Diffused junction***
***iv. Epitaxial growth, v. point contact junction***

# Physical properties of p-n junction:

During the formation of p-n junction, following two phenomena take place:

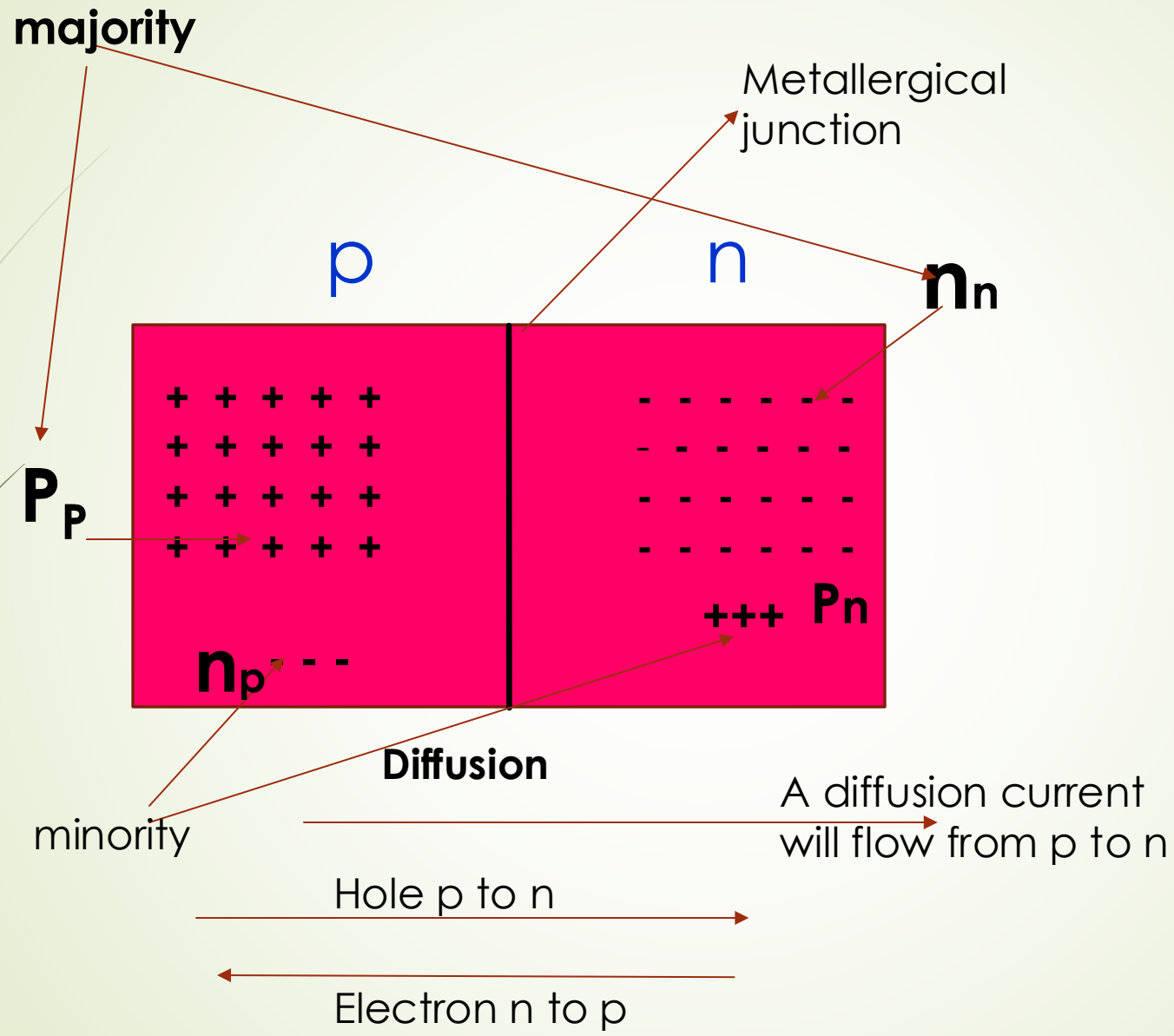
i. *A thin depletion layer (or region) is set up on both sides of the junction and is so called because it is depleted or devoid of free charge carriers. Its typical width is about 1 $\mu$m ($10^{-6}$ m).*

ii. *A junction or barrier potential $V_B$ is developed across the junction whose value is about 0.3 V for Ge and 0.7 V for Si.*



**High** concentration to **low** concentration

# diffusion



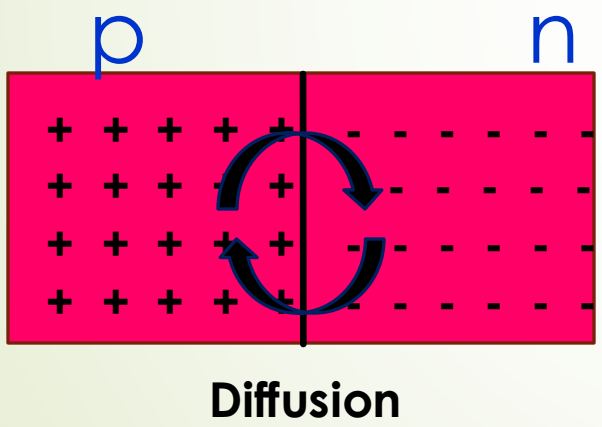
**Two current**

1. Diffusion current (high to low concentration)
2. Drift current ( it depends on electric field)

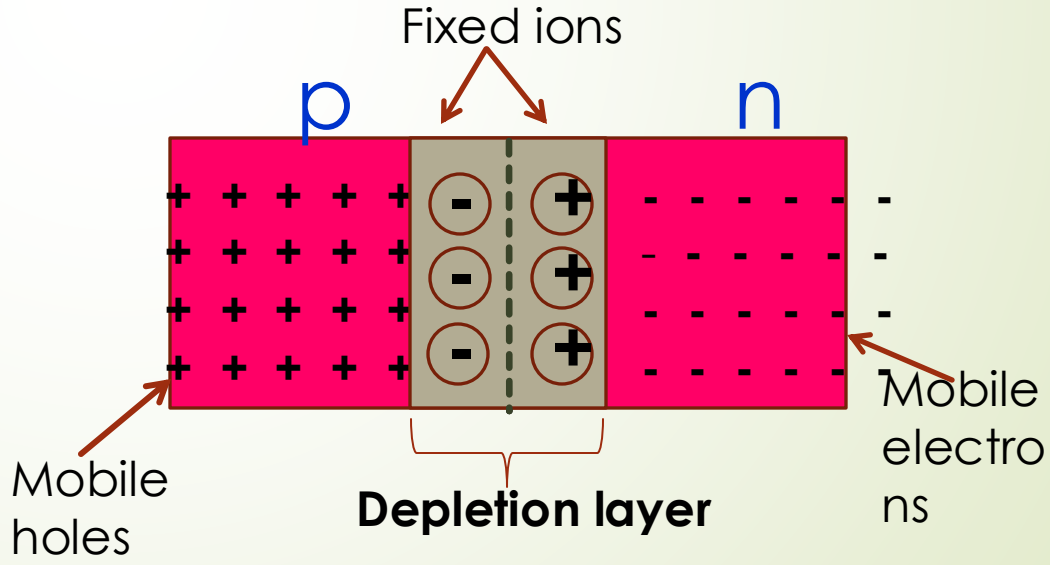
# Formation of depletion region:

After a p-n junction is formed, a difference in concentration of carriers creates a density gradient of carriers across junction which will result is majority carrier diffusion .

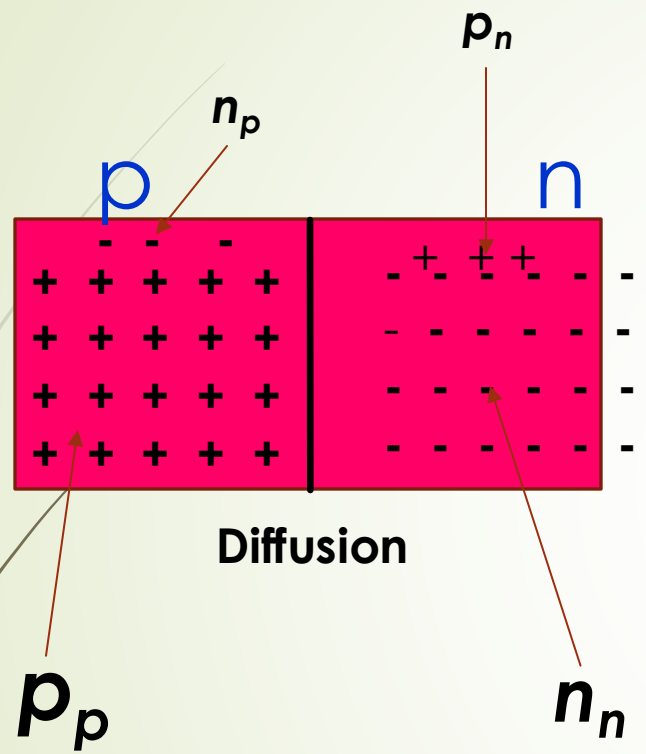
i. ***The holes diffuse from p to n region while electrons from n to p. This recombination of carrier will cause a lack of free carrier at the junction leaving behind the fixed/immobile ions .***
ii. ***This region of uncovered positive and negative ion is called depletion region/layer.***
iii. ***Since this layer contain no free charge it behaves like insulator.***



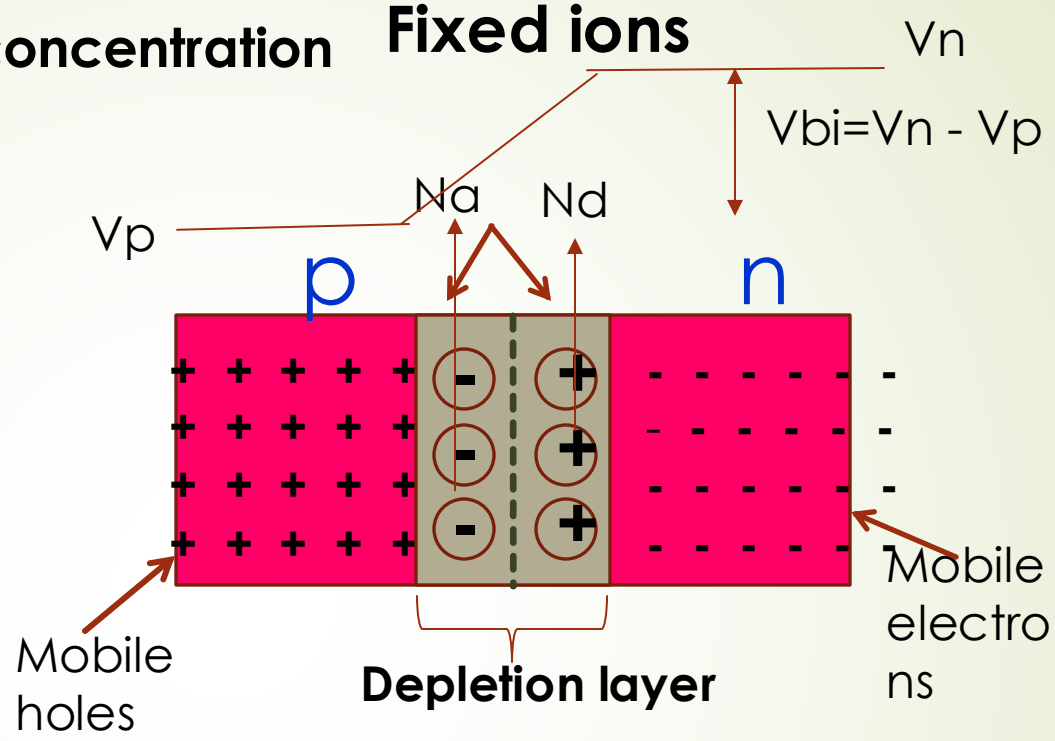

**Diffusion**



**High concentration to low concentration**




**Fixed ions**




ni=pi

Pure-Si

N-type

P-type

**Hole will diffuse from p to n**

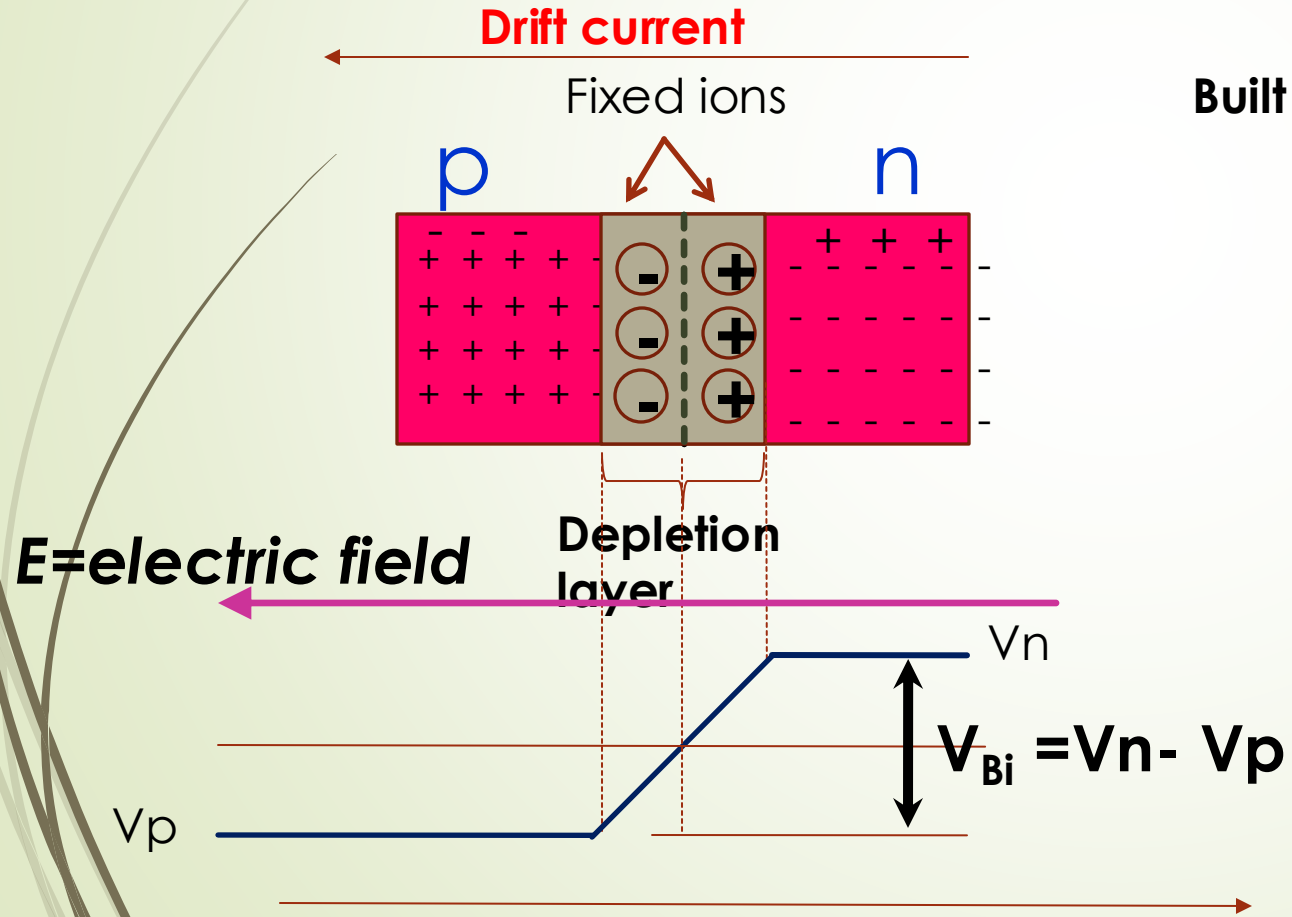
**Electron will diffuse from n to p**

**There is diffusion current from p to n**

# Formation of junction or barrier voltage:

Since the depletion layer contain only fixed rows of oppositely charged carriers,

i. ***due to this charge separation an electric potential $V_B$ is established across the junction***
ii. ***This potential difference further opposes the diffusion of majority carriers across the junction***
iii. ***The width of depletion region/layer depends on doping level. For heavy doping, depletion layer is physically thin.***




**Built in Electric Field** $= \frac{change - in - potential}{change - in - distance}$

$$E = -\frac{dV}{dx}$$

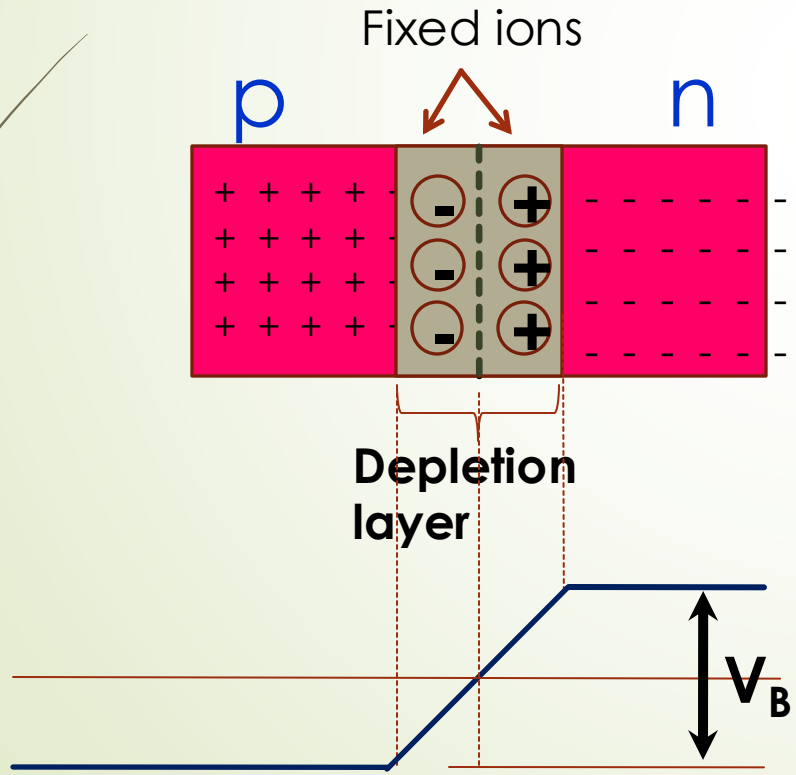
Velocity= mobility X electric field

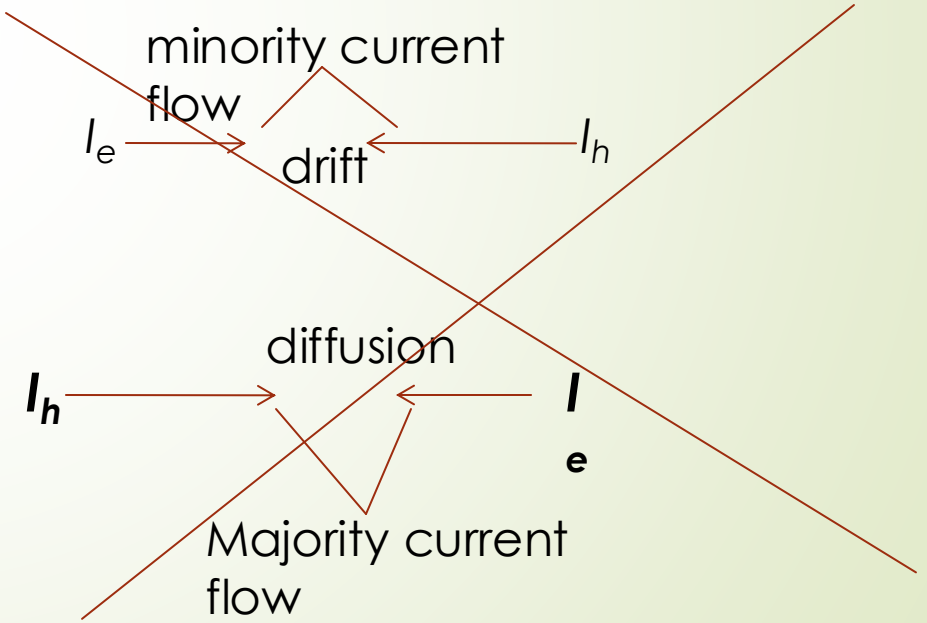
# Formation of junction or barrier voltage:

Since the depletion layer contain only fixed rows of oppositely charged carriers,

i. ***due to this charge separation an electric potential $V_B$ is established across the junction***
ii. ***This potential difference further opposes the diffusion of majority carriers across the junction***
iii. ***The width of depletion region/layer depends on doping level. For heavy doping, depletion layer is physically thin.***

***Under no bias net current flow across the junction = zero***



***J= I/A*** current density

# Drift and diffusion:

There are two mechanisms by which holes and electrons move through the silicon crystal-**drift** and **diffusion**.

**Diffusion**: is associated with random motion due to thermal agitation. Carriers diffuse from the higher region of concentration to lower concentration. This diffusion process gives rise to a net flow of charge, or diffusion current.

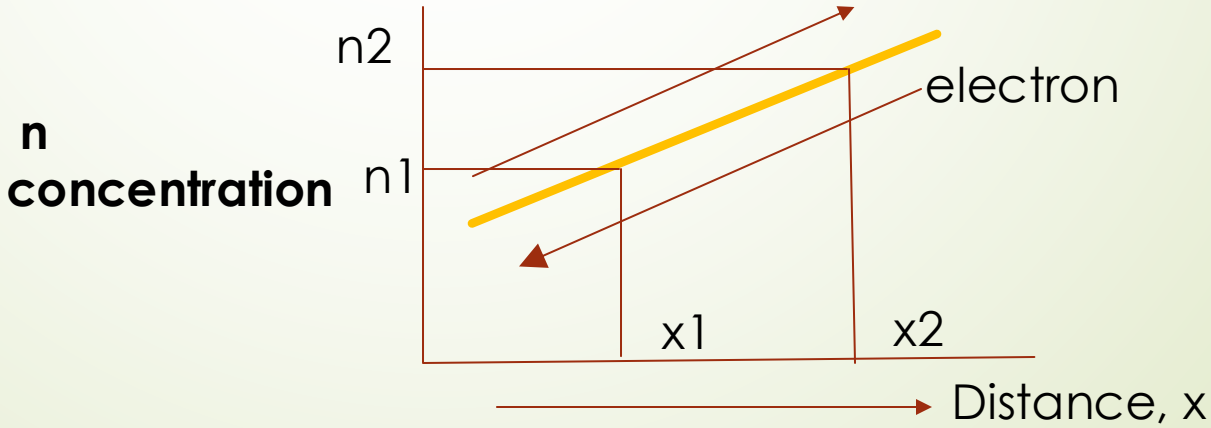
Diffusion current density

$$J_n = qD_n \frac{dn}{dx}$$

Eeeeeee
eeeeee

Where $D_p$ = 12 cm$^2$/s, is **the hole diffusion coefficient**, $D_n$ = 34 cm$^2$/s, is the **electron diffusion coefficient**.

$$J_p = -qD_p \frac{dp}{dx}$$



## Drift:

The other mechanism in semiconductors is drift. Carrier drift when an electric field is applied across a piece of semiconductor. Free electrons and holes are accelerated by the applied electric field and acquire velocity component called drift velocity,

$v_{drift} = \mu_{p,n} E$, where $\mu_{p,n}$ is the mobility of holes/electrons

The hole-drift current density is $J_{p\text{-}drift} = qp\mu_p E$

The electron-drift current density is $J_{n\text{-}drift} = qn\mu_n E$

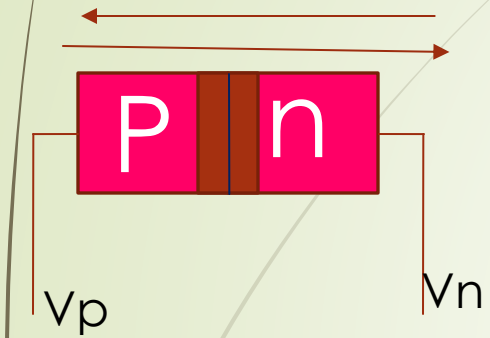
The total drift current density is $J_{drift} = q(p\mu_p + n\mu_n)E$

## The Einstien relation

$$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = V_T = \frac{KT}{q} = thermal\ voltage = 25mV, at 300K$$

# Quantitative relation between barrier potential and doping concentration on each side of the junction:

We know the drift and diffusion component **of hole** current just **cancel out each other at equilibrium**




$$q[\mu_p pE - D_p \frac{dp}{dx}] = 0 \qquad (1)$$

$$\frac{\mu_p}{D_p} E = \frac{1}{p}\frac{dp}{dx}$$

We know,

$$E = -\frac{dV}{dx}$$

$$V_B = \frac{kT}{q} \ln \frac{n_n}{n_p}$$

ing Einstein relation,

$$-\frac{q}{KT}\frac{dV}{dx} = \frac{1}{p}\frac{dp}{dx} \qquad (4)$$

$$\frac{n_n}{n_p} = e^{qV_B/kT}$$

After integrating,

$$-\frac{q}{KT}\int_{V_p}^{V_n} dV = \int_{P_p}^{P_n} \frac{1}{p}\,dp \qquad \text{or, } -\frac{q}{KT}(V_n - V_p) = \ln\frac{P_n}{P_p} \qquad (5)$$

$V_n$-$V_p$=$V_B$= contact potential,

$$V_B = \frac{kT}{q}\ln\frac{P_p}{P_n}, \quad \text{or, } \frac{P_p}{P_n} = e^{qV_B/kT} \qquad (6)$$

We know, $p_p n_p = n_i^2 = p_n n_n$ We can extend equation 6 for also electron concentration

$$\frac{P_p}{P_n} = \frac{n_n}{n_p} = e^{qV_0/kT}$$

$$V_B = \frac{kT}{q}\ln\frac{N_a}{n_i^2/N_d} = \frac{kT}{q}\ln\frac{N_a N_d}{n_i^2}$$

**Hole** diffusion and hole drift

P n

$$q[\mu_p pE - D_p \frac{dp}{dx}] = 0 \qquad (1)$$

$$\frac{\mu_p}{D_p} E = \frac{1}{p}\frac{dp}{dx} \qquad (2)$$

$$E = -\frac{\mathrm{dV}}{\mathrm{dx}} \qquad (3)$$

$$-\frac{q}{KT}\frac{dV}{dx} = \frac{1}{p}\frac{dp}{dx} \qquad (4)$$

$$-\frac{q}{KT}\int_{V_p}^{V_n} dV = \int_{P_p}^{P_n} \frac{1}{p}\,dp \qquad \text{or,} -\frac{q}{KT}(V_n - V_p) = \ln\frac{P_n}{P_p} \qquad (5)$$

$$\mathrm{V_B} = \frac{kT}{q}\ln\frac{P_p}{P_n}, \qquad \text{or,} \frac{P_p}{P_n} = e^{qV_B/kT} \qquad (6)$$

$$V_B = \frac{kT}{q} \ln \frac{n_n}{n_p}$$

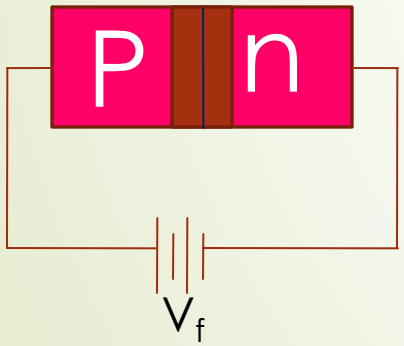
$$\frac{n_n}{n_p} = e^{qV_B / kT}$$

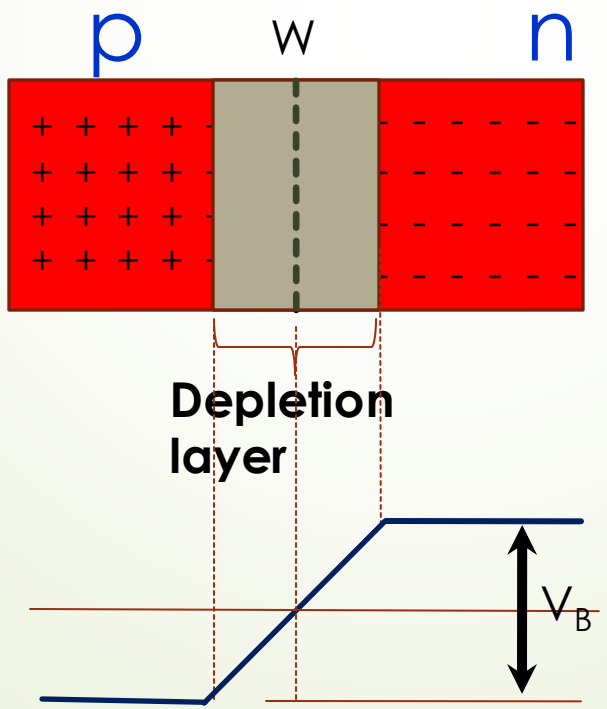
$$V_B = \frac{kT}{q} \ln \frac{N_a}{n_i^2 / N_d} = \frac{kT}{q} \ln \frac{N_a N_d}{n_i^2}$$

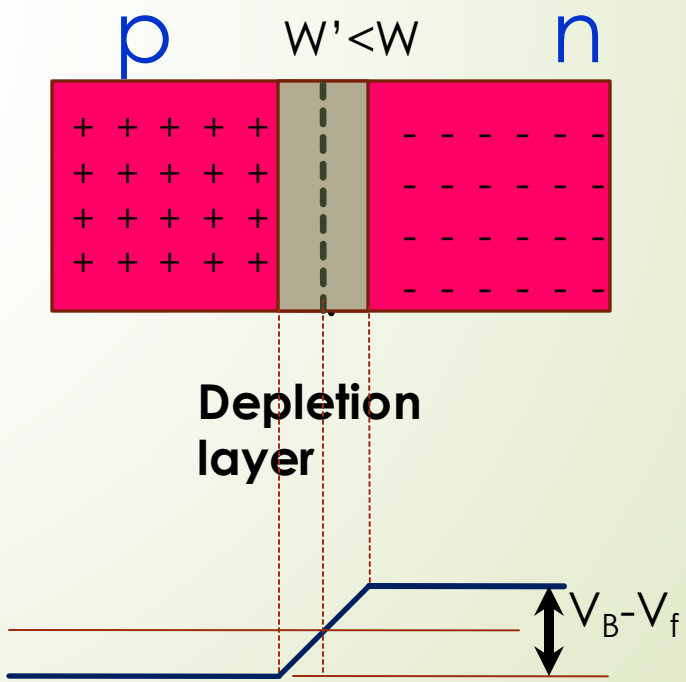
## Forward biased condition of p-n junction semiconductor diode:

i. *A forward biased 'on' condition is obtained by applying a positive potential to the p-side of the junction and negative potential to the n-side.*

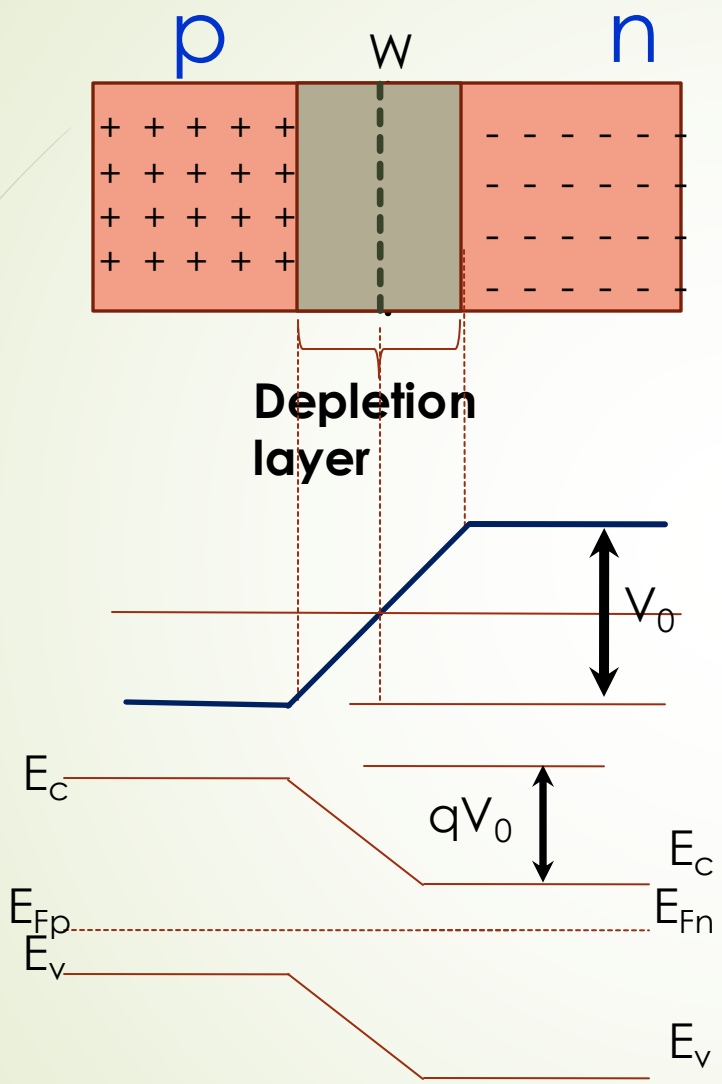
ii. *The application forward bias will cause the electrons and holes driven towards the junction where they recombine and will reduce the width of the depletion region . The resulting minority carrier flow of electrons from p to n will not change, but the reduction of depletion layer will create large amount of current flow across junction.*

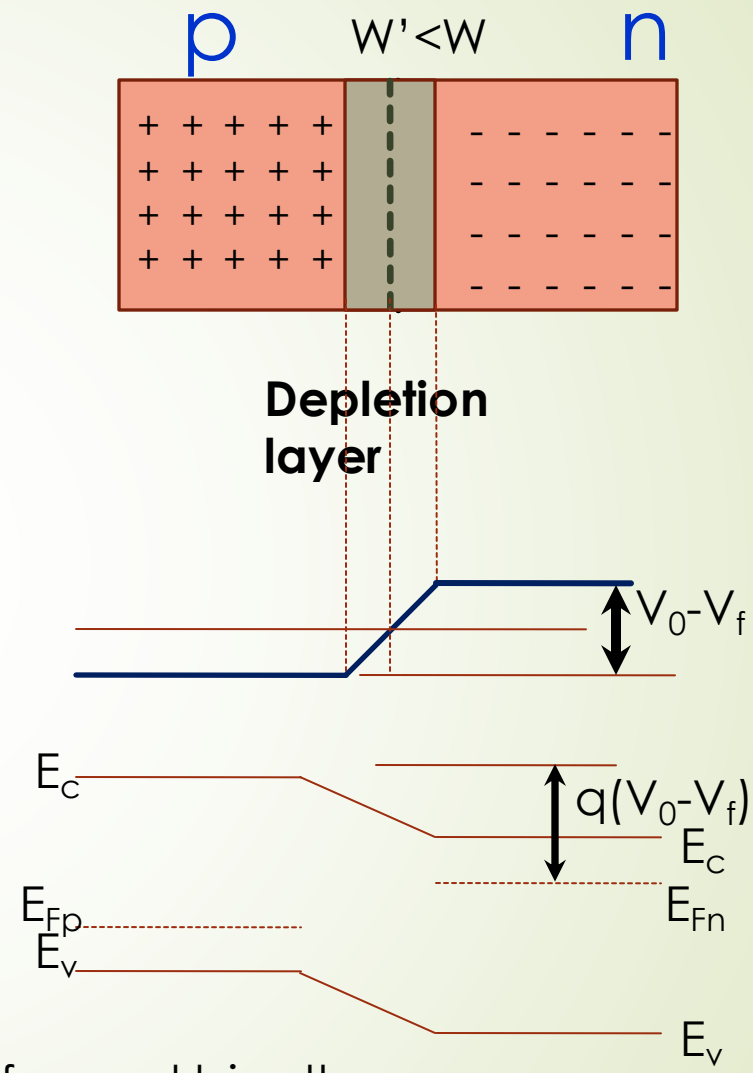


# Effect of forward biased on the energy band diagram of p-n junction semiconductor diode:

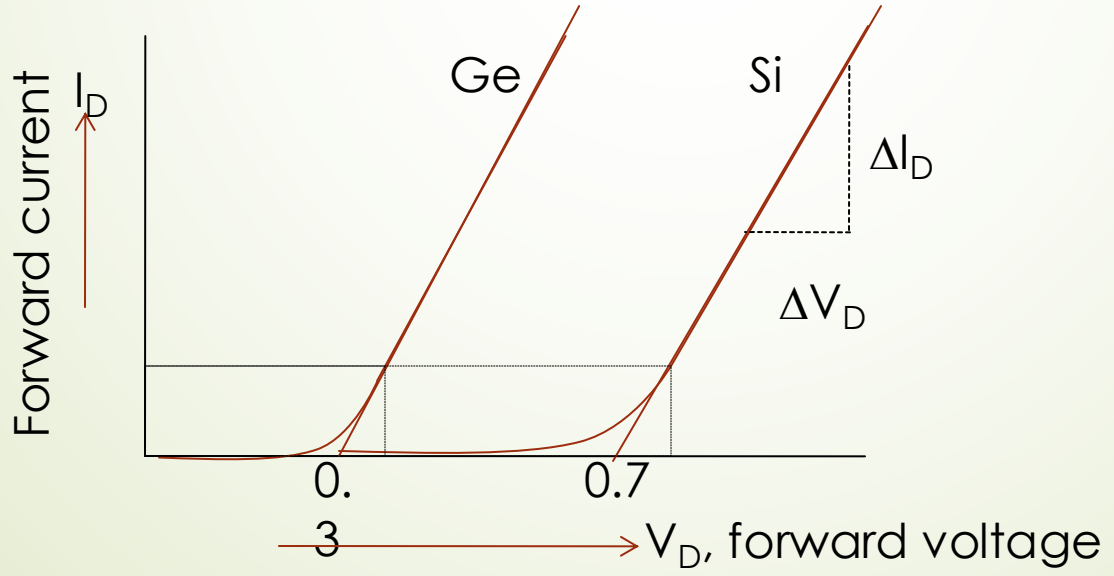


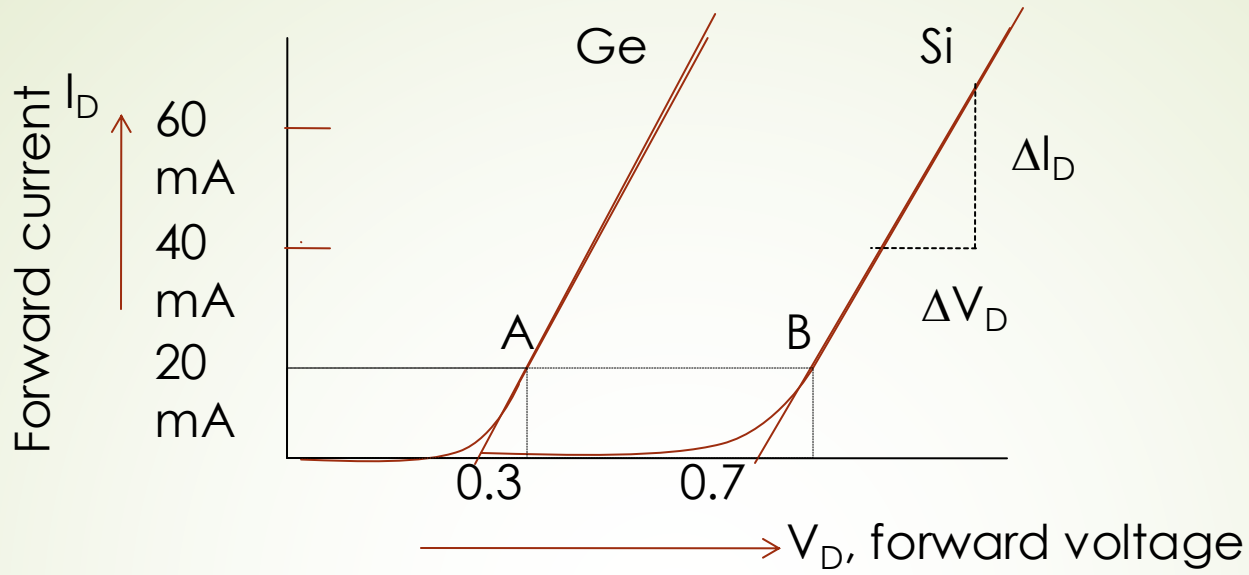

With forward bias the electrostatic potential is lowered from the equilibrium contact potential to $V_0$-$V_f$.

# Forward V/I characteristics of p-n junction semiconductor diode:

i. *When diode is forward bias and the applied voltage is increased from zero, hardly any current flow the device in the beginning.*
ii. *It is so because the external voltage is opposed by the internal barrier voltage $V_B$ which is 0.7 for Si and 0.3 for Ge.*
iii. *As soon as $V_B$ is neutralized It is seen that the forward current rises exponentially with the applied forward voltage.*
iv. *This voltage is known as threshold voltage $V_{th}$, cut-in voltage or knee voltage.*
v. *When $V<V_{th}$, negligible current flow*
vi. *When $V>V_{th}$, current rise exponentially*



# Forward biased junction resistance:



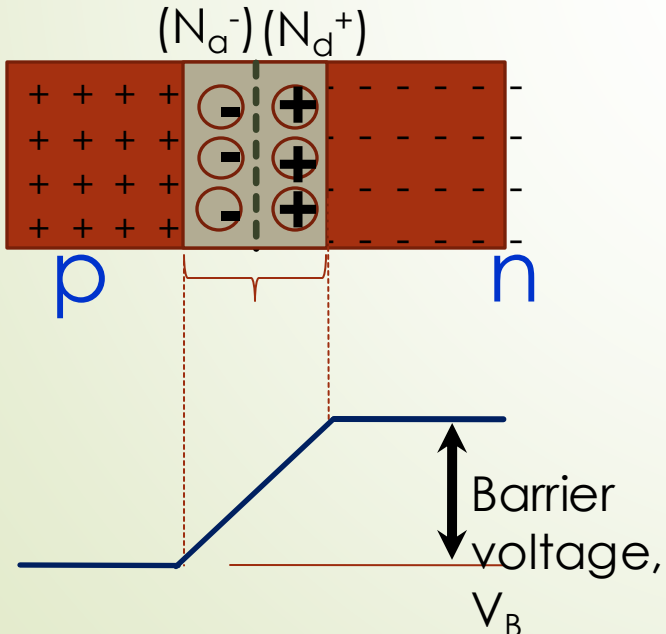

Obviously the forward-biased junction has very low resistance,
For point B in Si,
Static forward resistance is $R_F = \frac{0.76V}{20mA}$

In practice static resistance is not used instead ***dynamic resistance*** or ***ac resistance*** is used. It is given by the reciprocal of the slop of the forward characteristics.

$$\frac{1}{R_{ac}} = \frac{\Delta I_D}{\Delta V_D}$$

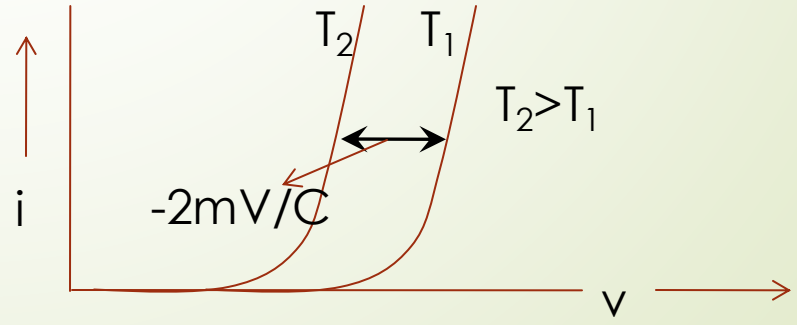
# Effect of temperature on barrier voltage:

i. *Barrier voltage depends on doping density, electronic charge and temperature.*
ii. *For a given junction the first two factors are fixed, therefore $V_B$ (barrier voltage) is mainly dependent on temperature.*
iii. *With increase in temperature results in increase of minority carriers leading to their increased drift across the junction.*
iv. *As a result equilibrium occurs at slightly reduced barrier potential.*
v. *It is found that for both Ge and Si VB is decreased about 2mV/°C*




$$\Delta V_B = -0.002.\Delta T$$

$$\Delta T = Change \text{ in } Temperature \text{ in } {}^{o}\text{C}$$



# Problem:

Q. Calculate the barrier potential of Si junction at (a) 100 °C and (b) at 0 °C if its value at 25 °C is 0.7 V.

# Problem:

**Q. Calculate the barrier potential of Si junction at (a)100 °C and (b) at 0 °C if its value at 25 °C is 0.7 V.**

$$\Delta T = Change \text{ in } Temperature \text{ in } ^{\circ}\text{C}$$

$$= -25$$

$$\Delta V_B = -0.002 \times \Delta T$$

$$V_{B1} - V_{B2} = -0.002 \times 75 = -0.15$$

$$V_{B2} = 0.55$$

$$\Delta V_B = -0.002 \times \Delta T$$

$$V_{B1} - V_{B2} = -0.002 \times -25 = 0.05$$

$$V_{B2} = 0.75$$

## Reverse biased p-n junction:

i. ***A reversed biased 'off' condition is obtained by applying a negative potential to the p-side of the junction and positive potential to the n-side.***

ii. *The application forward bias will cause the electrons and holes driven towards the junction where they recombine and will reduce the width of the depletion region . The resulting minority carrier flow of electrons from p to n will not change, but the reduction of depletion layer will create large amount of current flow across junction.*

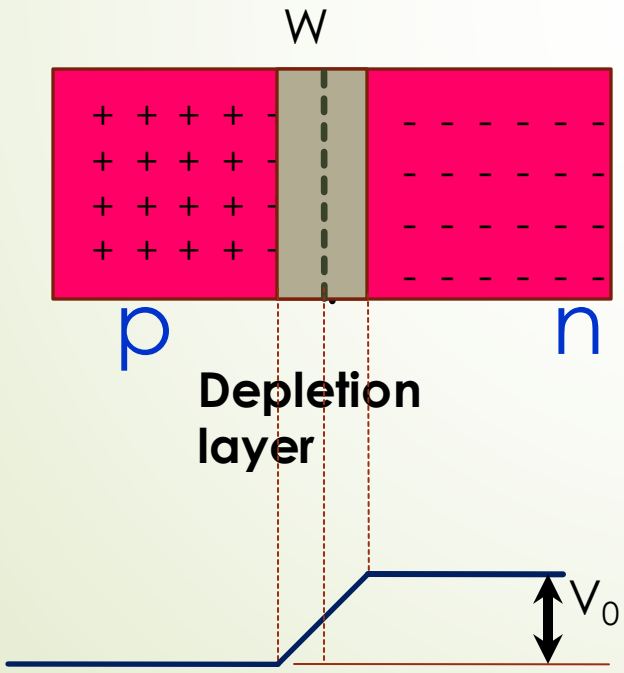
# Reverse biased p-n junction:

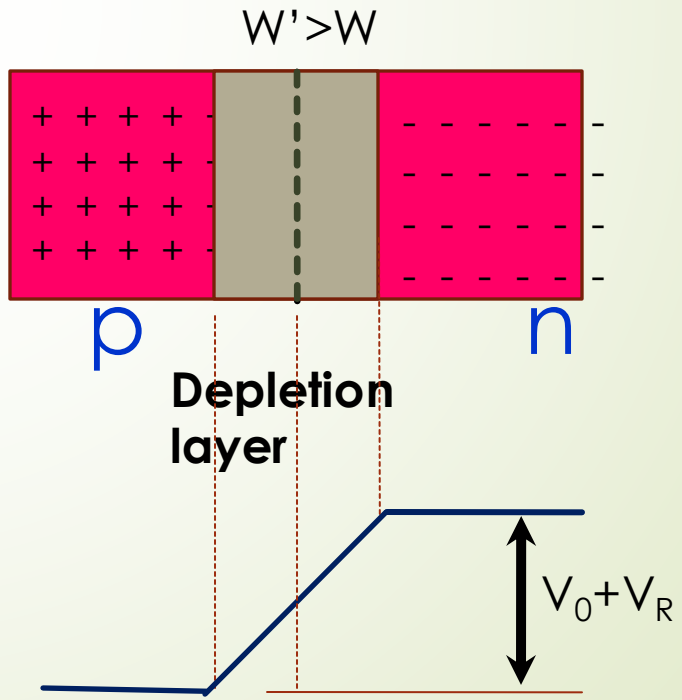
i. ***A reversed biased 'off' condition is obtained*** *by applying a negative potential to the p-side of the junction and positive potential to the n-side.*

ii. *The application forward bias will cause the electrons and holes attracted by the positive and negative battery terminals. Both electrons and holes move away from junction and away from each other*

iii. *No current flows and junction offers high resistance*

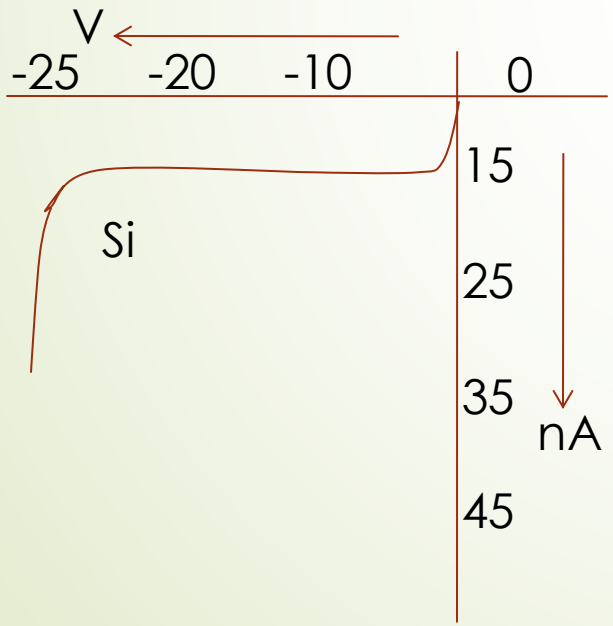
iv. *Under this condition depletion width increases and also barrier potential increases.*

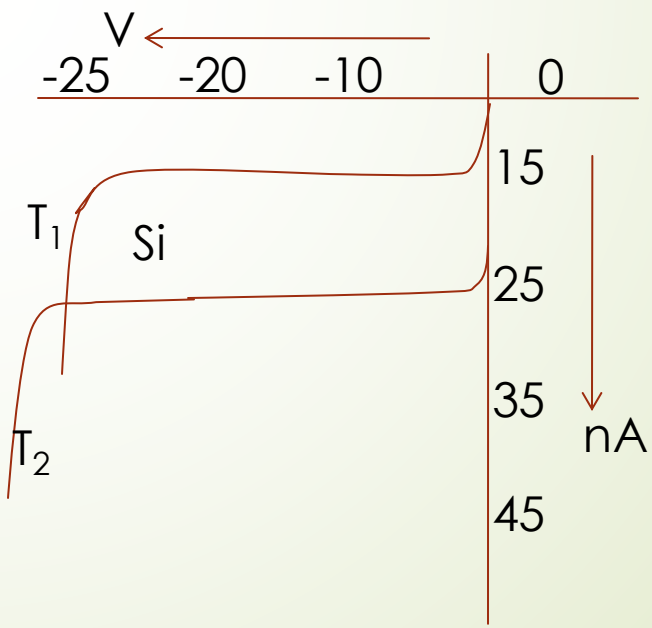


# Reverse saturation current:

i. Although under reverse bias no current flows due to majority of carriers
ii. There is small amount of current (a few Pico-amp—micro-amp) flows due minority charge carriers generated by thermal agitation.
iii. This current is called reverse saturation current, $I_s$.
iv. Since minority carriers are thermally generated, the reverse current is extremely temperature dependent.
v. $I_s$ is found doubled for every 10 degree C rise in temperature in Ge and for every 6 degree C rise in temperature for Si.



# Equation of diode/ diode Shockley's equation:

The general characteristics of a semiconductor diode can be defined by the following equations for the forward and reverse biased region

$$I_D = I_S (e^{V_D / nV_T} - 1)$$

$I_D$= diode current
$I_s$= Reverse saturation current
$V_D$= applied forward bias across junction
n= ideality factor; function of operating condition or physical construction, its value is generally considered 1.
$V_T$= thermal voltage

$$V_T = \frac{kT}{q}$$

K= is the bothzmann constant $1.38 \times 10^{-23}$ J/K
q= magnitude of electronic charge $1.6 \times 10^{-19}$ C
T= absolute temperature in Kelvin

# Equation of diode/ diode Shockley's equation:

The general characteristics of a semiconductor diode can be defined by the following equations for the forward and reverse biased region

$$I_D = I_S (e^{V_D / nV_T} - 1) \qquad (1.1)$$

For forward bias or positive value of $V_D$, equation 1.1 will become

$$I_D \cong I_S e^{V_D / nV_T} \qquad (1.2)$$

For negative value of $V_D$, equation 1.1 will become

$$I_D \cong -I_S \qquad (1.3)$$

At zero voltage $I_D = I_S (e^0 - 1) = 0 \qquad (1.4)$

We know for forward bias or positive value of $V_{D1}$, diode current will become

$$I_{D1} \cong I_S e^{V_{D1}/nV_T}$$

If forward bias value is $V_{D1}$, diode current will become

$$I_{D1} \cong I_S e^{V_{D1}/nV_T}$$

The combination of the two equation will become

$$\frac{I_{D2}}{I_{D1}} = e^{\frac{V_{D2}-V_{D1}}{nV_T}}$$

$$V_{D2} - V_{D1} = nV_T \ln \frac{I_{D2}}{I_{D1}}$$

$$V_{D2} - V_{D1} = 2.3nV_T \log \frac{I_{D2}}{I_{D1}}$$

For a decade change in current diode voltage drop changes by $2.3nV_T$

# Junction resistance/dynamic resistance:

We have found the dynamic resistance graphically. However, there is a basic definition:

***The derivative of a function at a point is equal to the slop of the tangent line drawn at that point***

Lets take the derivative of equation 1.1

$$\frac{d}{dV_D} I_D = \frac{d}{dV_D} I_S (e^{V_D / nV_T} - 1) \qquad (1.1)$$

$$\frac{d}{dV_D} I_D = \frac{1}{nV_T} (I_D + I_S), \qquad \text{in general } I_D >> I_S$$

$$\frac{d}{dV_D} I_D = \frac{1}{nV_T} I_D$$

$$\frac{dV_D}{dI_D} = r_d = \frac{nV_T}{I_D}$$

Substituting n=1 and $V_T$=26 mV $\quad r_d = r_j = \frac{26mV}{I_D}$

Dynamic rsistance $\quad r_{ac} = \frac{26mV}{I_D} + r_B$

Where $r_B$ is the body resistance

$$\frac{d}{dV_D} I_D = \frac{d}{dV_D}[I_S(e^{V_D/nV_T} - 1)]$$

$$= \frac{d}{dV_D}[I_S e^{V_D/nV_T} - I_s] = \frac{I_s}{nV_T} e^{V_D/nV_T} = \frac{1}{nV_T}[I_s e^{V_D/nV_T}]$$

$$= \frac{1}{nV_T}[I_s e^{V_D/nV_T} - I_s + I_s]$$

$$== \frac{1}{nV_T}[I_s(e^{V_D/nV_T} - 1) + I_s]$$

$$\frac{d}{dV_D} I_D = \frac{1}{nV_T}(I_D + I_S), \qquad \text{in general } I_D >> I_S$$

$$\frac{d}{dV_D} I_D = \frac{1}{nV_T} I_D$$

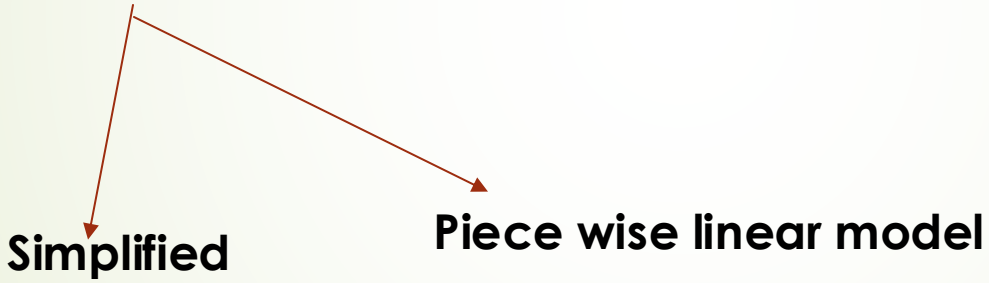
nA

mA

**In order to solve the diode circuits: We need to replace the diodes by its equivalent models:**

1. **Ideal Model**

2. **Real Model**

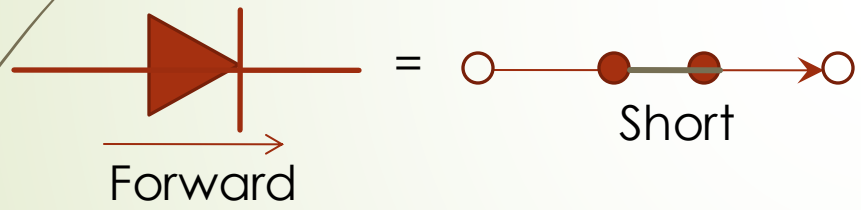


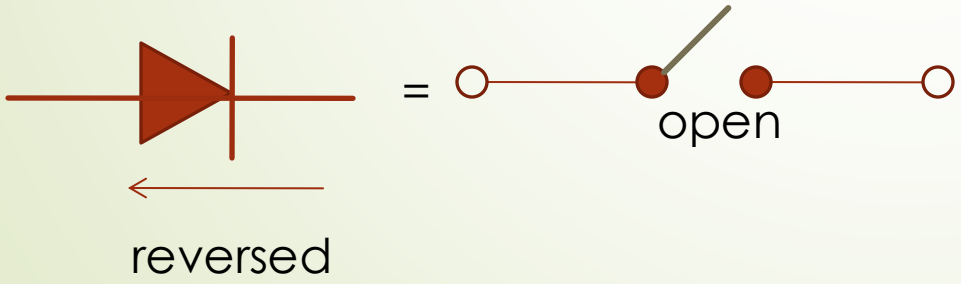
# Ideal diode:

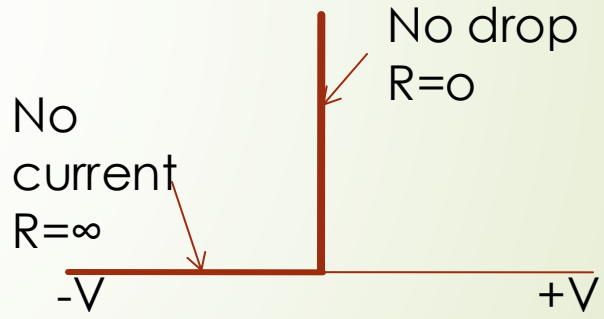
The terminal characteristics of an ideal diode can be interpreted as follows:

i. If a negative voltage is applied to diode, no current flows, the diode behaves as an open circuit. Diode in this mode is said to be reversed bias. It has zero current in the reverse direction and said to be **Cut-off.**

ii. If positive voltage is applied, zero voltage drop appear across diode and the diode behaves as short circuit. A forward/positive bias diode is said to be **Turned on**.



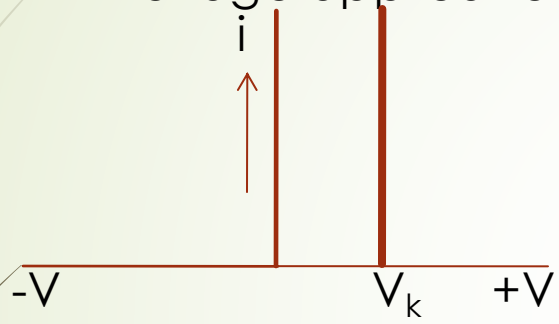



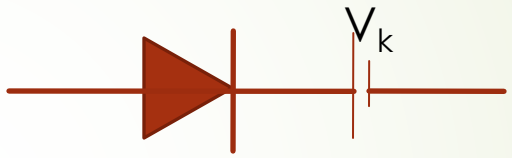



# Real diode:

A real diode does not offer zero resistance in forward direction neither it offers infinite resistance in reverse direction

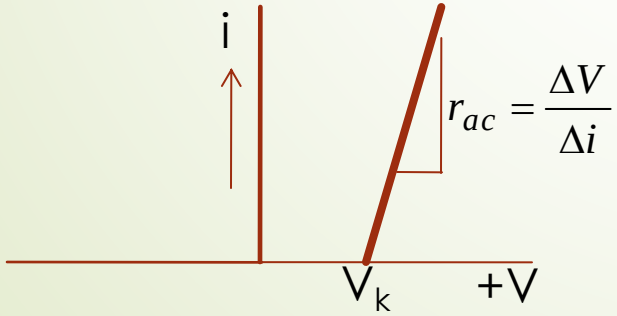
(a) First factor is that forward current does not start flowing until the voltage applied to the diode exceeds the knee voltage $V_k$




**Simplified model**

(b) Second factor is that forward dynamic or ac resistance ($r_{ac}$) offered by the circuit. If we take $r_{ac}$ into account, the forward characteristics becomes



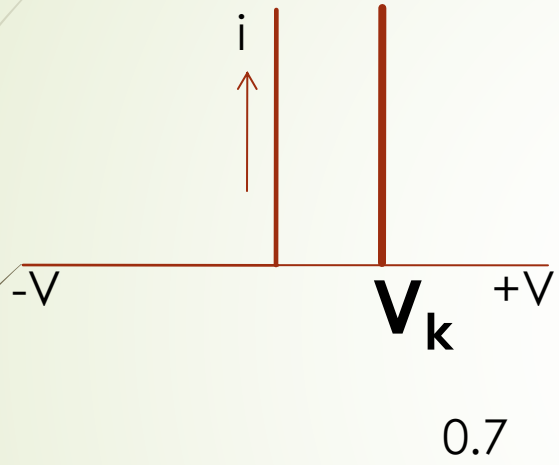


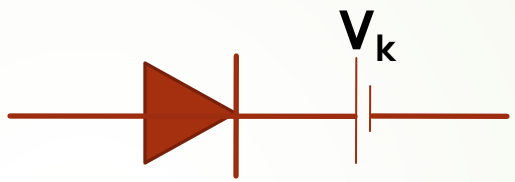
**Piecewise linear model**

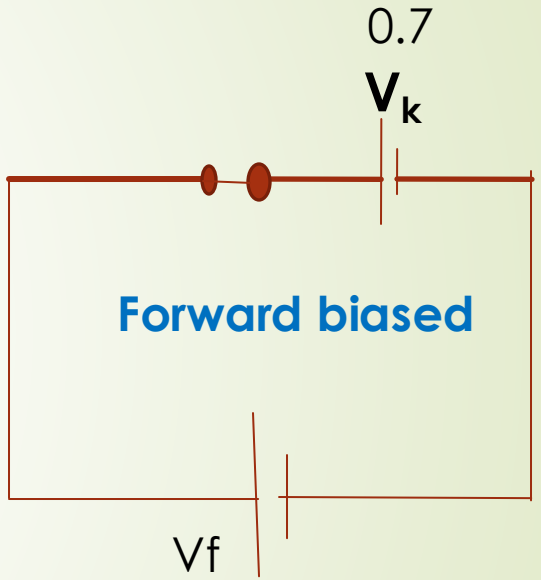
# Real diode: 1. Simplified model

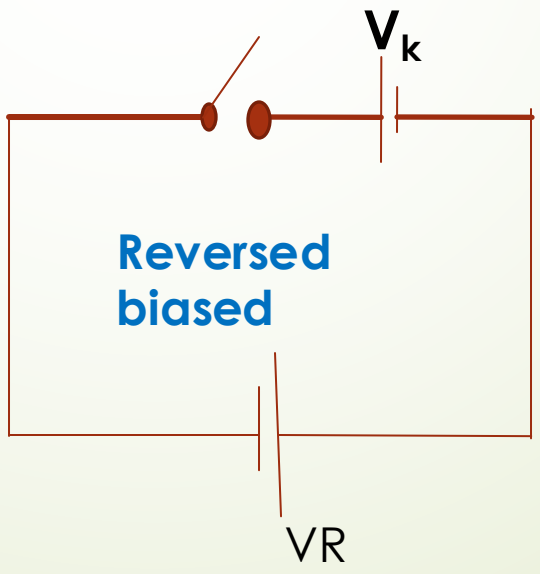
A real diode does not offer zero resistance in forward direction neither it offers infinite resistance in reverse direction

(a) First factor is that forward current does not start flowing until the voltage applied to the diode exceeds the knee voltage $V_k$



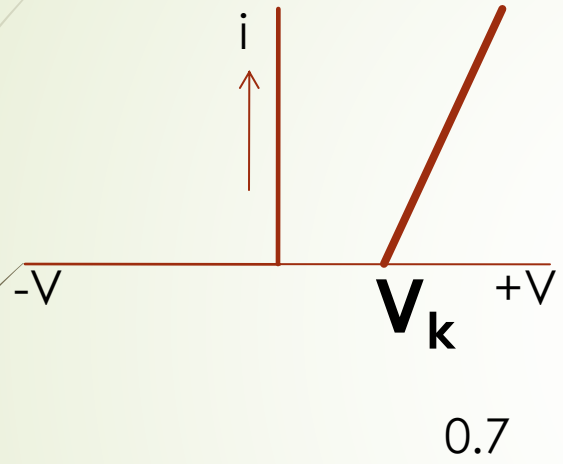



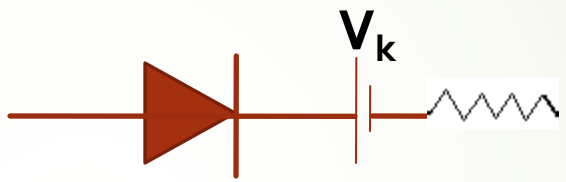



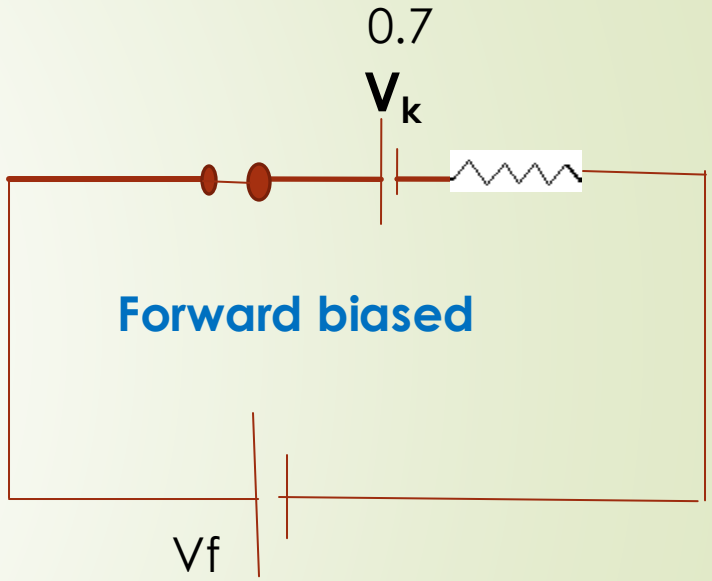
# Real diode: 2. Piecewise linear model

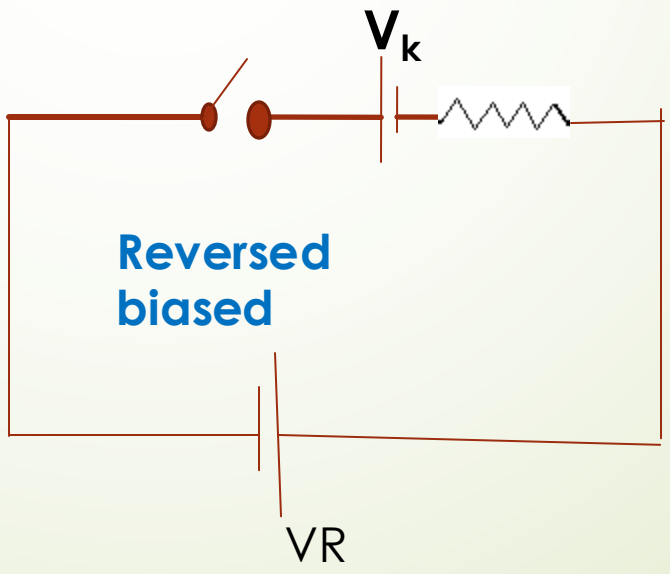
A real diode does not offer zero resistance in forward direction neither it offers infinite resistance in reverse direction

(a) First factor is that forward current does not start flowing until the voltage applied to the diode exceeds the knee voltage $V_k$

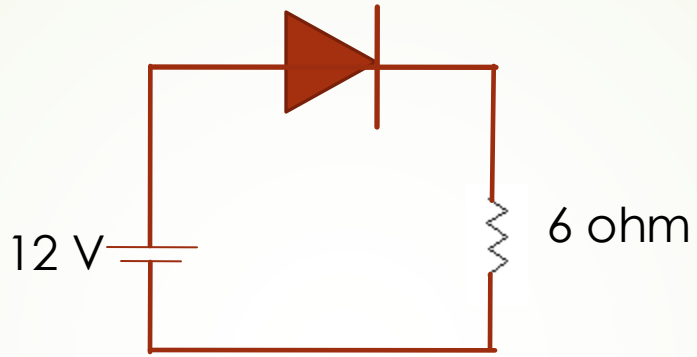


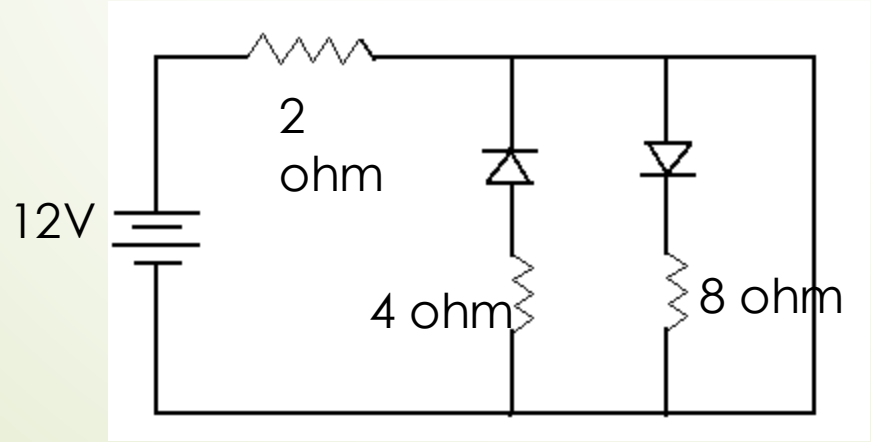



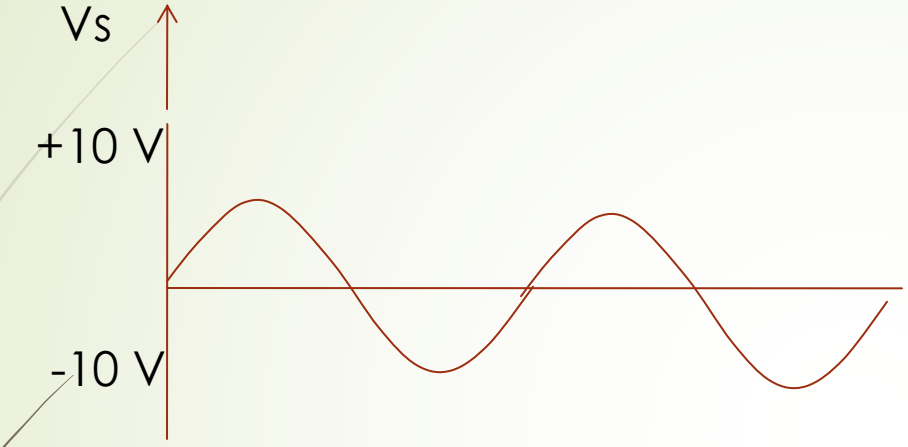
Q. Calculate the circuit current and power dissipated in the (a) ideal diode and (b) 6 ohm resistor of the circuit.

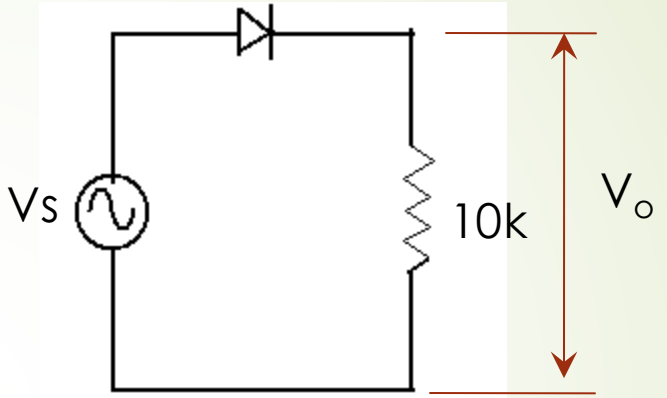



Q. Find the circuit current if any in the following circuit

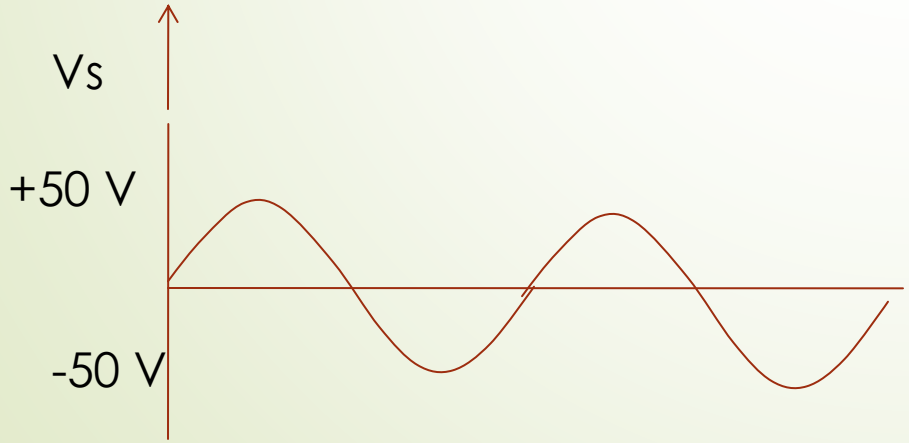


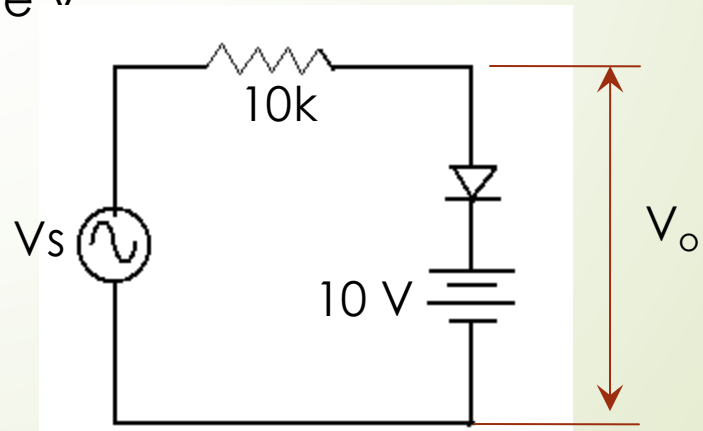
Q. Sketch the waveform of voltage $V_o$ across 10K



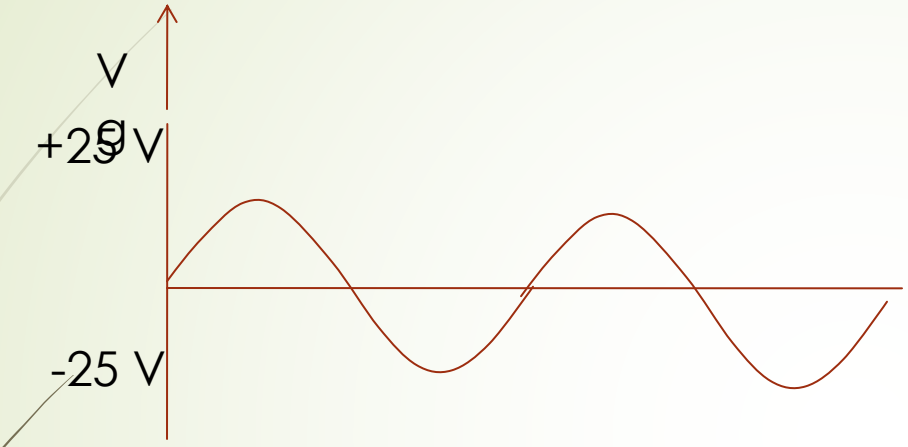



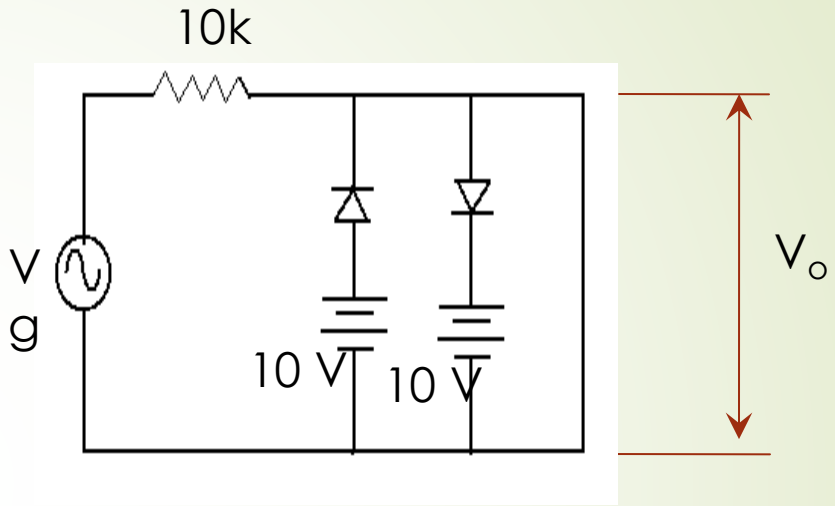

Q. Sketch the waveform of voltage V



Q. Sketch the waveform of voltage $V_o$ across 10K



**EXAMPLE 2.9** Determine $I$, $V_1$, $V_2$, and $V_o$ for the series dc configuration of Fig. 2.25.

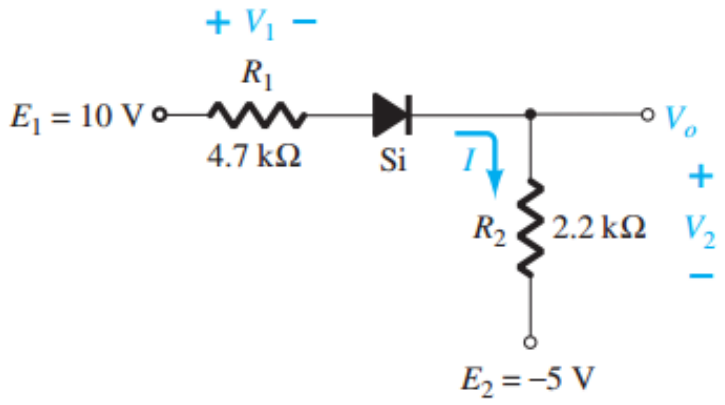



**FIG. 2.25**

***9.** Determine $V_{o_1}$ and $V_{o_2}$ for the networks of Fig. 2.159.

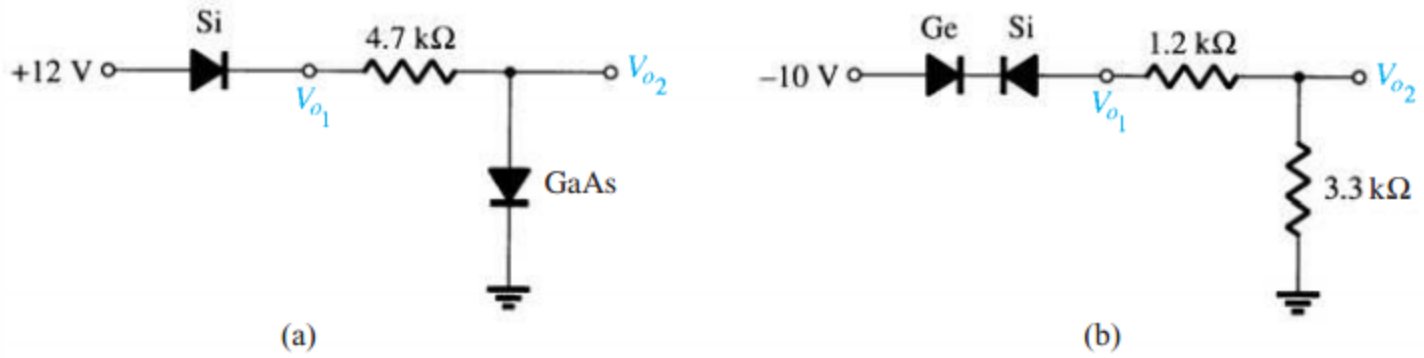
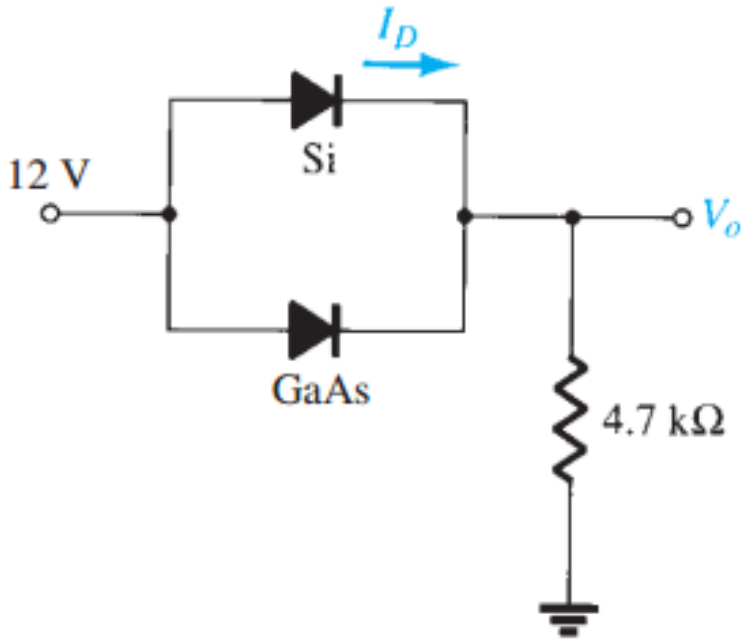
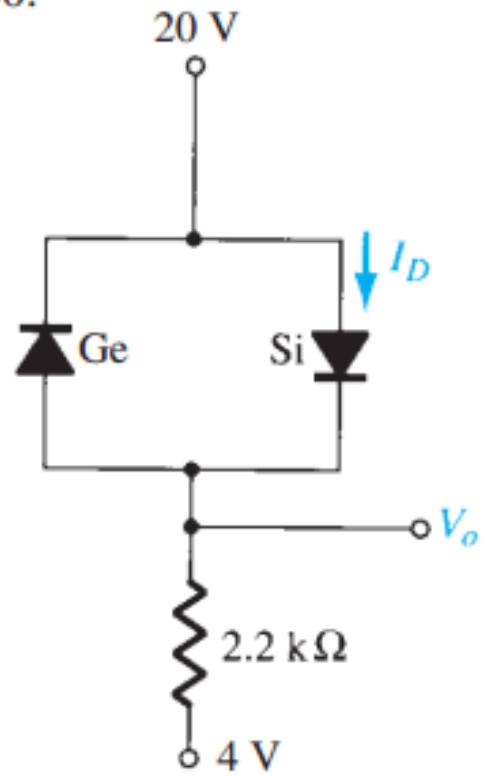



**FIG. 2.159**

**10.** Determine $V_o$ and $I_D$ for the networks of Fig. 2.160.




(a)




(b)

**FIG. 2.160**

***11.** Determine $V_o$ and $I$ for the networks of Fig. 2.161.

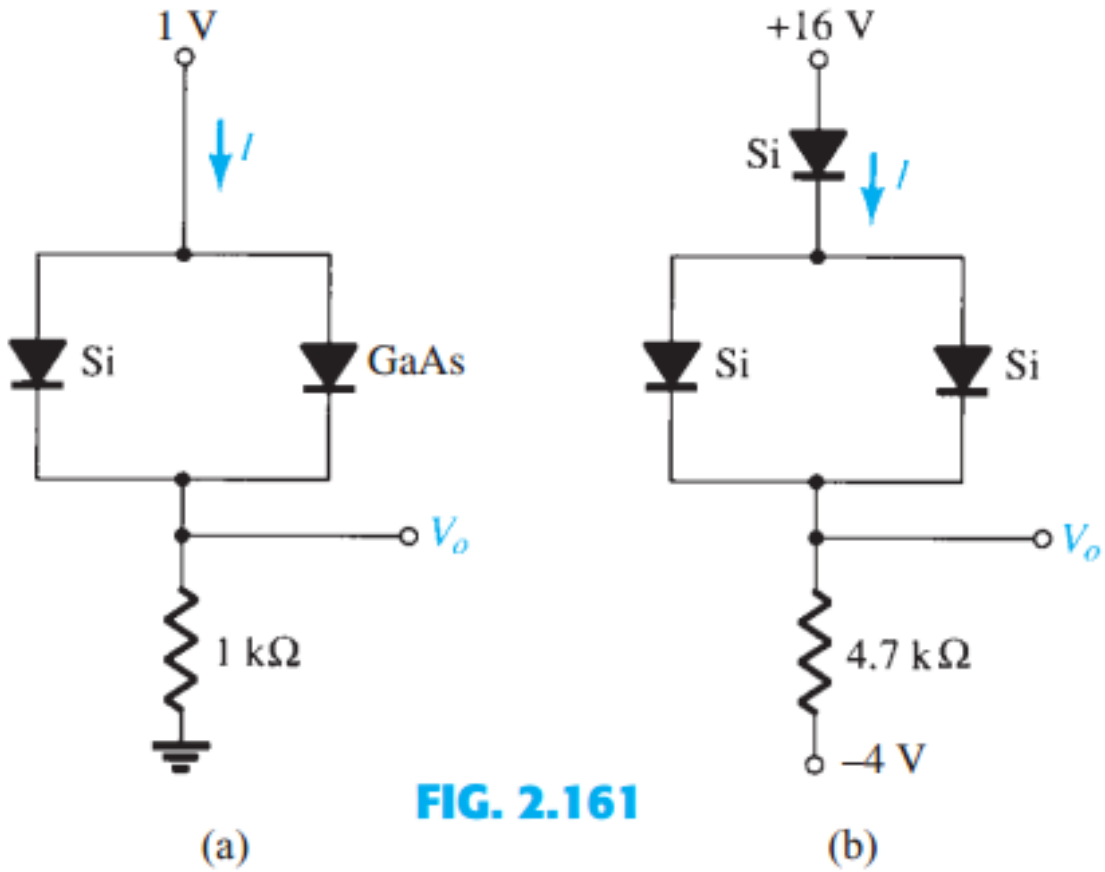



**FIG. 2.161**

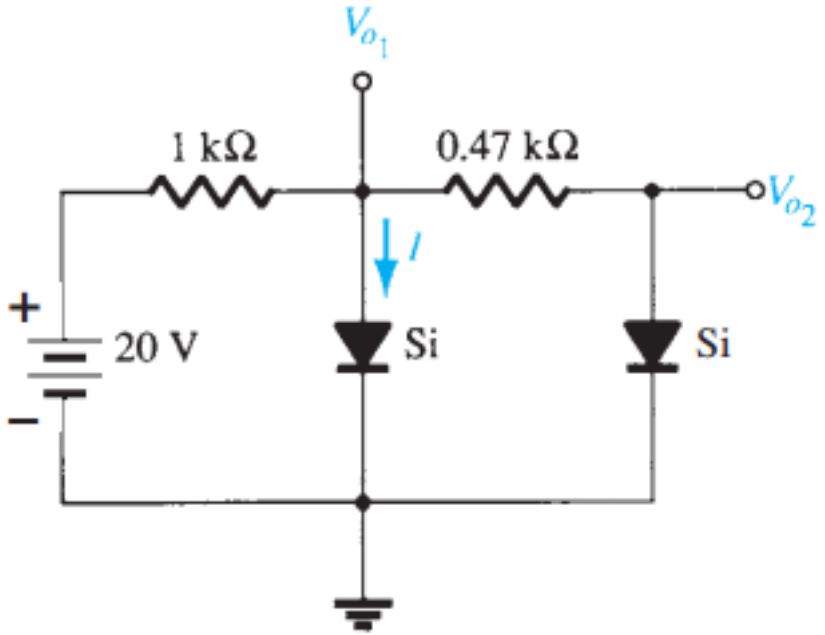



FIG. 2.162

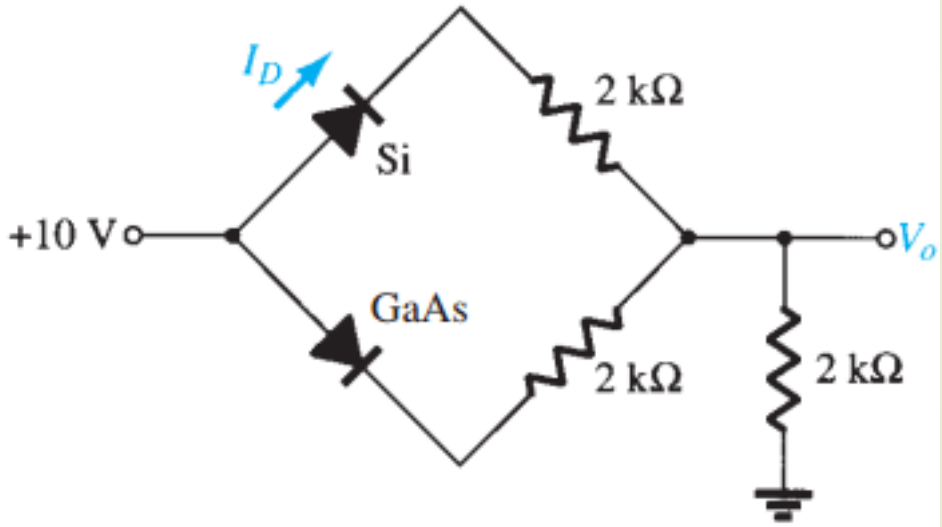



FIG. 2.163

Next class:

1. **diode circuit analysis**
2. **Diode small signal model**
3. **Diode high frequency model**
4. **Depletion layer capacitance**
5. **Diffusion capacitance**
6. **Zener break down, avalanche break down**
7. **Voltage regulation**

# SIGNIFICANT EQUATIONS

**1 Semiconductor Diodes** $W = QV$, $1\text{ eV} = 1.6 \times 10^{-19}\text{ J}$, $I_D = I_s\,(e^{V_D/nV_T} - 1)$, $V_T = kT/q$, $T_\text{K} = T_\text{C} + 273°$, $k = 1.38 \times 10^{-23}\text{ J/K}$, $V_K \cong 0.7\text{ V (Si)}$, $V_K \cong 0.3\text{ V(Ge)}$, $V_K \cong 1.2\text{ V (GaAs)}$, $R_D = V_D/I_D$, $r_d = 26\text{ mV}/I_D$, $r_\text{av} = \Delta V_d/\Delta I_d\big|_\text{pt. to pt.}$, $P_D = V_D\,I_D$, $T_C = (\Delta V_Z/V_Z)/(T_1 - T_0) \times 100\%/°\text{C}$

**2 Diode Applications** Silicon: $V_K \cong 0.7\text{ V}$, germanium: $V_K \cong 0.3\text{ V}$, GaAs: $V_K \cong 1.2\text{ V}$; half-wave: $V_\text{dc} = 0.318V_m$; full-wave: $V_\text{dc} = 0.636V_m$