DNJ

Southeast University

School of Science and Engineering

Department of Electrical and Electronic Engineering

Program: B.Sc. Engr. in EEE

Midterm Assignment, Summer 2024

EEE 215 Electronic Circuits I

Section: 1

Full Marks: 50 **Time: 60 hours including submission**

*Answer **all** questions from the following assignments. Answers should be written in the word file or white page and should be submitted on time in corresponding classroom.*

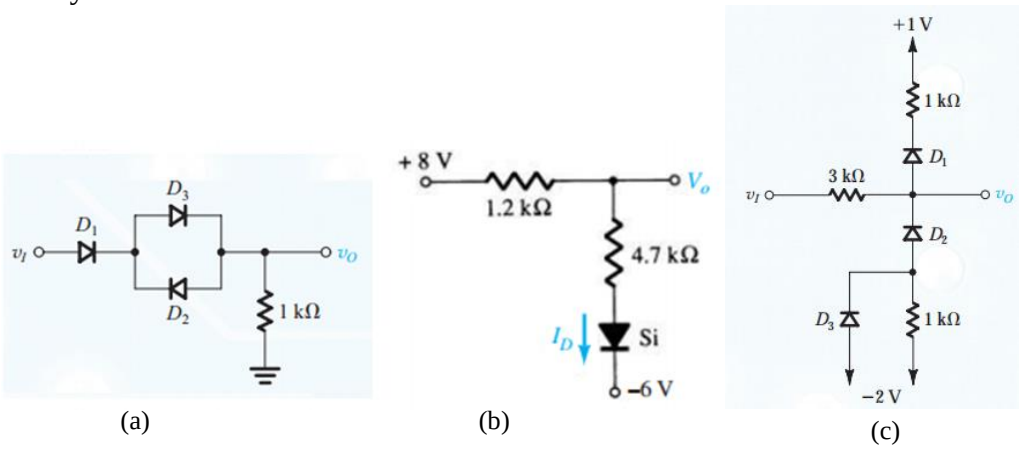
[The marks on the right hand side in square brackets indicate marks allocated for that question only]

1. (a) What is meant by majority charge carrier and minority carrier?
Draw a diagram to illustrate diffusion current in semiconductor.
The drift current velocity in a germanium sample is estimated as 12.9 cm/s, and the terminal voltage is 14.5 V, calculate the length of the sample. 5

(b) Prove that for barrier Potential of V_B, the ratio of majority to minority carriers is, $\frac{n_n}{n_p} = e^{qV_B/kT}$. Also draw the energy band diagram of p-n junction under forward and reverse biased. 6

(c) A silicon p-n junction has a reverse saturation current of 30 nA at 35°C and 90 nA at 45°C, Calculate the current at both temperature when the forward bias voltage is 0.79 V. 4

2. (a) Sketch and clearly label the output of the circuits in Fig 1 for a sinusoidal signal v_i that has a positive half cycle +14 V and negative half cycle -14 V peak. Assume that the diodes can be represented by ideal diode model. 6



(a) (b) (c)

Figure 1

(b) Sketch the output for the following circuits of Fig 2: 4

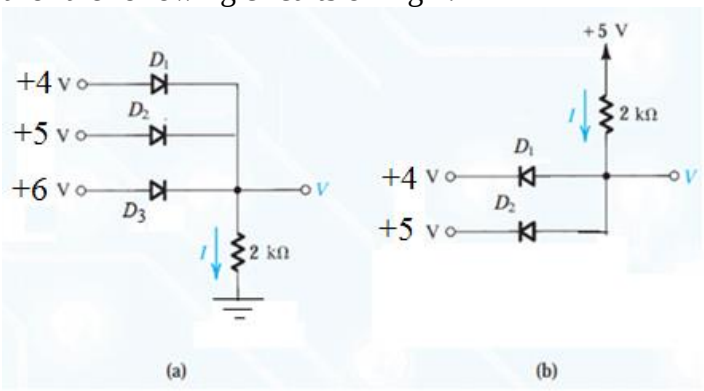


Figure 2

(c) Sketch and label the voltage characteristic v_O versus v_i of the circuit shown in Fig 3 over a ±12-V range of input signals. All diodes are Silicon made (i.e., each exhibits a 0.7-V drop at a current of 1 mA). 6

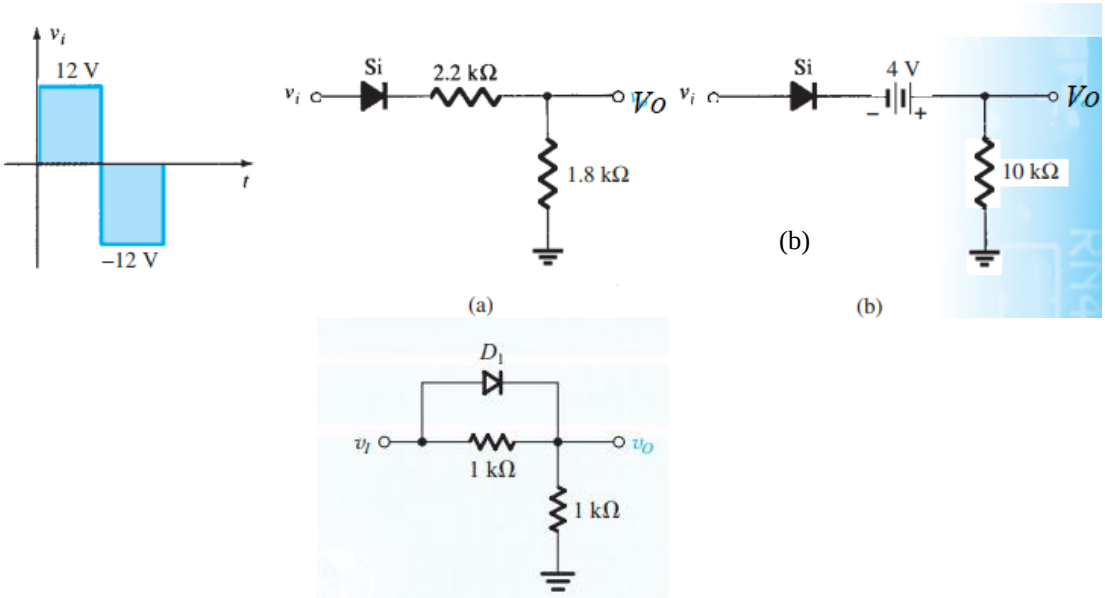


Figure 3

3. (a) Design a clamper to perform the following function indicated in Fig 4. 4

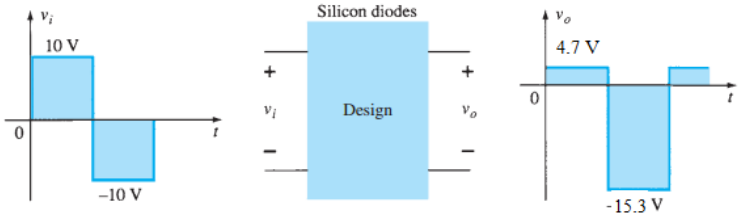


Figure 4

(b) Design and draw a full-wave rectifier with average voltage across the load is 24 volt to a load of 200 ohm. The peak to peak cannot exceed more than 8% of the average output. Calculate the charging and discharging time and calculate the value of reservoir capacitor. 5

(c) Determine VL, IL, IZ, and IR for the network of Fig 5,

i. if R_L = 180 Ω.

ii. Repeat part (i) if R_L = 470 Ω.

iii. Determine the value of R_L that will establish maximum power conditions for the Zener diode.

iv. Determine the minimum value of R_L to ensure that the Zener diode is in the "on" state. 5

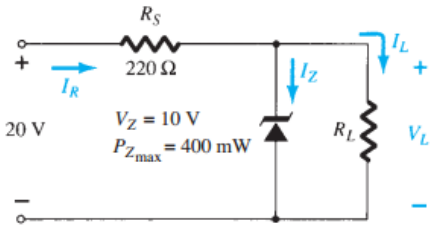


Figure 5

4. (a) Draw the output of the following networks of Fig 6. 5

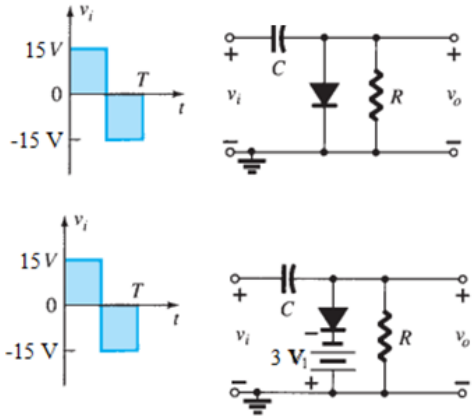


Figure 6