100-Day SystemVerilog Challenge Schedule

Week 1: Basics of SystemVerilog

- Day 1: Introduction to SystemVerilog and its significance in Verification
- Day 2: Data Types (2-state and 4-state, logic vs reg)
- Day 3: Operators in SystemVerilog
- Day 4: Procedural Blocks (initial, always)
- Day 5: SystemVerilog vs Verilog Differences
- Day 6: Modules and Ports
- Day 7: Testbench Structure and First Simulation

Week 2: Control Flow and Arrays

- Day 8: Conditional Statements (if-else, case)
- Day 9: Loops (for, while, repeat, forever)
- Day 10: Tasks and Functions
- Day 11: Introduction to Arrays (Packed vs Unpacked)
- Day 12: Static and Dynamic Arrays
- Day 13: Queues and Associative Arrays
- Day 14: Array Methods

Week 3: RTL Design and FSMs

- Day 15: RTL Design Guidelines
- Day 16: Combinational Logic Design
- Day 17: Sequential Logic Design
- Day 18: Finite State Machines - Moore
- Day 19: Finite State Machines - Mealy
- Day 20: FSM Coding Techniques
- Day 21: FSM Case Study

Week 4: Interfaces and Packages

- Day 22: Interfaces - Basics
- Day 23: Modport and Clocking Blocks
- Day 24: Interfaces in TB and DUT
- Day 25: Packages and Importing
- Day 26: Constants and Parameters

- Day 27: Type Definitions
- Day 28: Using Packages in Simulation

Week 5: Object-Oriented Programming (OOP) Basics

- Day 29: Class and Object
- Day 30: Class Properties and Methods
- Day 31: Inheritance
- Day 32: Polymorphism
- Day 33: Encapsulation
- Day 34: Constructors and Destructors
- Day 35: Shallow and Deep Copy

Week 6: Randomization and Constraints

- Day 36: Introduction to Randomization
- Day 37: Constraint Basics
- Day 38: Inline Constraints
- Day 39: Distribution Constraints
- Day 40: Constraint Inheritance
- Day 41: Solving Constraint Conflicts
- Day 42: Randomization Case Studies

Week 7: Assertions - Immediate and Concurrent

- Day 43: Immediate Assertions
- Day 44: Concurrent Assertions
- Day 45: Sequence and Property
- Day 46: Temporal Operators
- Day 47: SVA Examples
- Day 48: Using Assertions in TB
- Day 49: Assertion-Based Verification

Week 8: Covergroups and Functional Coverage

- Day 50: Introduction to Coverage
- Day 51: Coverpoints and Bins
- Day 52: Cross Coverage
- Day 53: Covergroup Options
- Day 54: Sampling and Triggers
- Day 55: Functional Coverage Planning
- Day 56: Coverage Report and Analysis

Week 9: UVM Foundations

- Day 57: UVM Introduction
- Day 58: UVM Environment Structure
- Day 59: UVM Component Hierarchy
- Day 60: UVM Factory and Build Phase
- Day 61: UVM Configuration Database
- Day 62: UVM TLM Ports and Exports
- Day 63: UVM Macros

Week 10: UVM Testbench Development

- Day 64: UVM Driver and Sequencer
- Day 65: UVM Sequence and Sequence Items
- Day 66: UVM Monitor and Scoreboard
- Day 67: UVM Agent and Environment
- Day 68: UVM Phase Execution
- Day 69: UVM Reporting and Messaging
- Day 70: UVM Case Study: Simple Protocol

Week 11: Advanced UVM Concepts

- Day 71: Objections and Phase Control
- Day 72: UVM Callbacks
- Day 73: Virtual Sequences
- Day 74: Register Layer (UVM RAL)
- Day 75: RAL Model Creation
- Day 76: Integration with DUT
- Day 77: Factory Overrides and Overrides with Config DB

Week 12: Scoreboarding and Checkers

- Day 78: Introduction to Scoreboards
- Day 79: Functional vs Formal Checkers
- Day 80: Predictors in UVM
- Day 81: Reference Models
- Day 82: Self-Checking Testbenches
- Day 83: Advanced Scoreboarding Techniques
- Day 84: Debugging Strategies

Week 13: SystemVerilog Projects and Integration

- Day 85: Mini Project 1 - FIFO Verification

- Day 86: Mini Project 2 - UART Verification
- Day 87: Mini Project 3 - SPI Verification
- Day 88: Mini Project 4 - I2C Verification
- Day 89: Project Setup and Documentation
- Day 90: Reusability Techniques in SV/UVM
- Day 91: Tips for Real-Time Debugging

Week 14: Industry Preparation and Final Week

- Day 92: Interview Preparation - SV/UVM
- Day 93: Resume Building for Verification
- Day 94: Coding Best Practices
- Day 95: Testbench Optimization
- Day 96: Coverage Closure Techniques
- Day 97: Real-World Case Studies
- Day 98: Final Project Review
- Day 99: Final Q&A / AMA Session
- Day 100: Certificate of Completion + Next Steps