Princess Sumaya University for Technology

The King Abdullah II School for Electrical Engineering
Electronics Engineering Department

Digital Electronics Lab

In Lab Report

Experiment 10:

Introduction to VERILOG (2)

Names of Group: 1. ..... ID#:.....
2. ..... ID#:.....
3. ..... ID#:.....

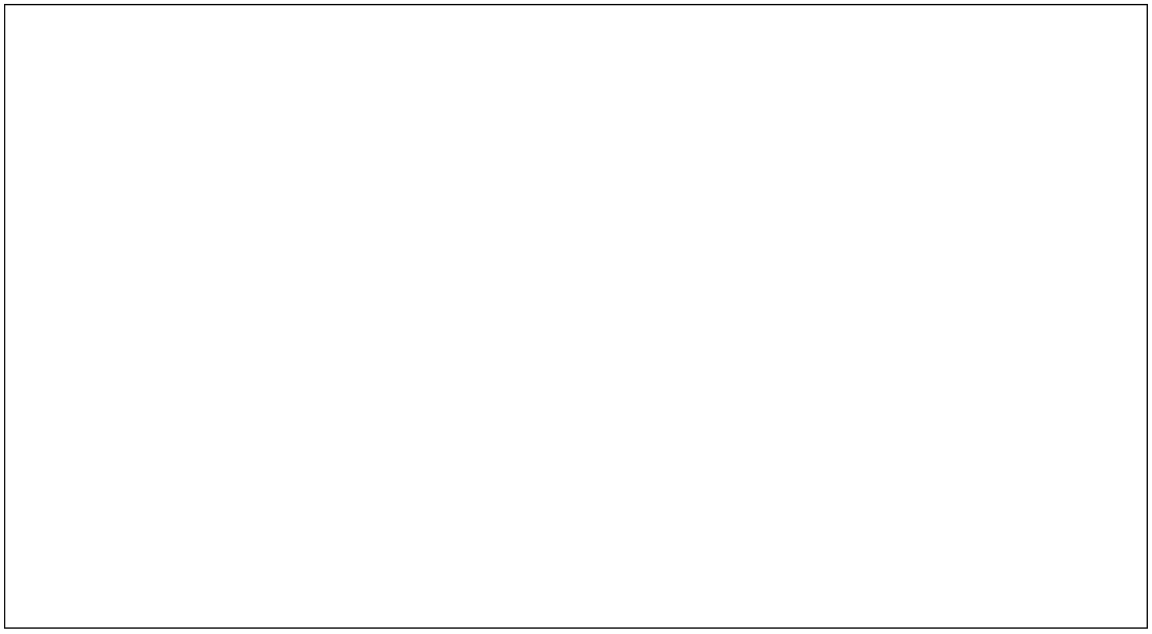
Group No.:
Section:
Date: / /

Objectives

1. ……..
2. ……

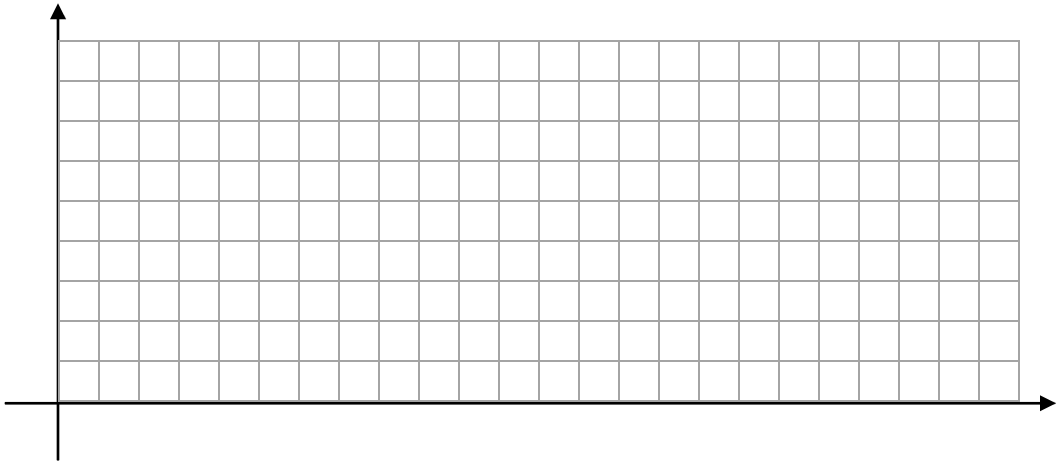
A) Basic Logic Gates

1. Draw a Moore FSM that describes an odd parity checker (assert when number of 1s is odd)



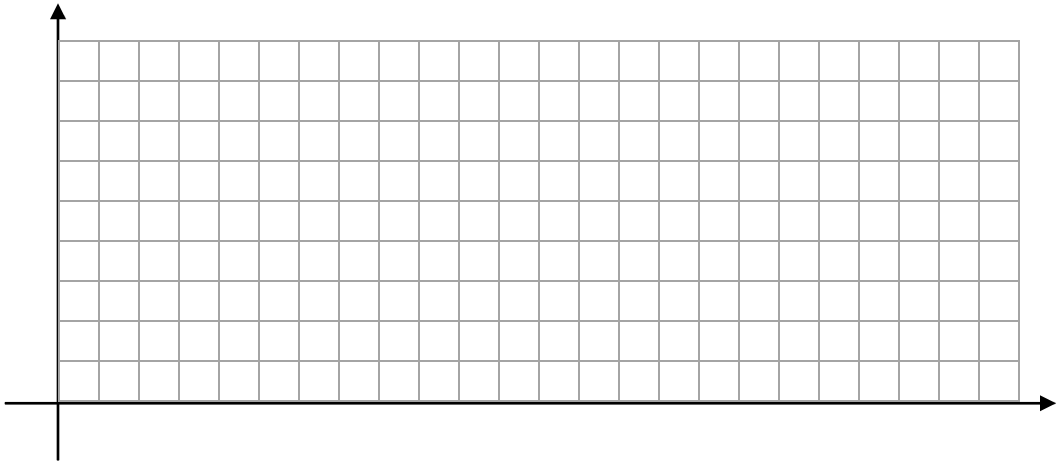
2. Write down the VERILOG code for a tri-state buffer and the testbench code to test it.

2. Draw the resulting waveform



2. Write down the VERILOG code for a 4-input multiplexer and the testbench code to test it.

2. Draw the resulting waveform



2. Write down the VERILOG code for a 2-to-4 decoder and the testbench code to test it.

2. Draw the resulting waveform