

Princess Sumaya University for Technology

The King Abdullah II School for Electrical Engineering
Electronics Engineering Department

Digital Electronics Lab

In Lab Report

Experiment 9:

Introduction to VERILOG

Names of Group: 1. ID#:.....
2. ID#:.....
3. ID#:.....

Group No.:

Section:

Date: / /

Objectives

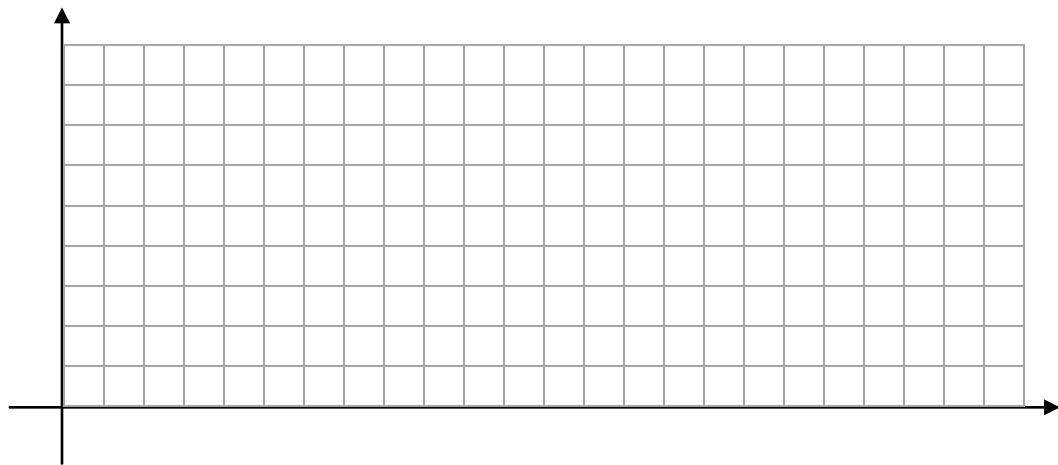
1.
2.
3.
4.

A) Basic Logic Gates

1. Write down the VERILOG code for an inverter and the testbench code to test it.

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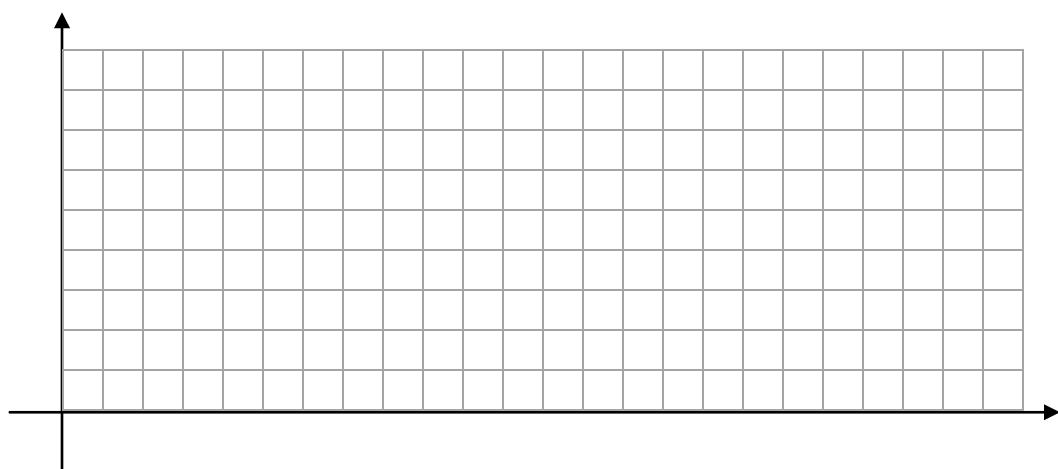
2. Draw the resulting waveform



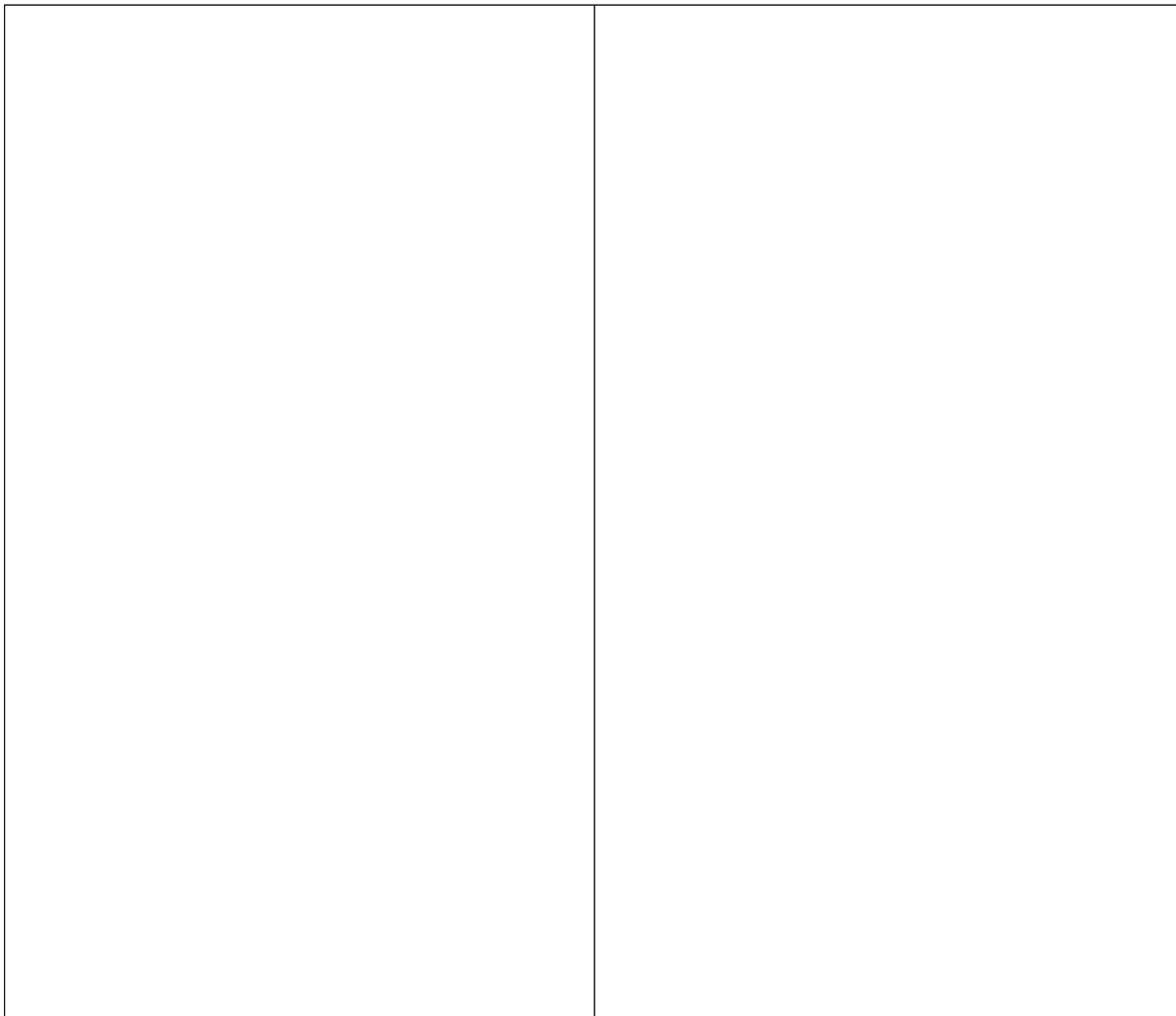
2. Write down the VERILOG code for an AND gate and the testbench code to test it.

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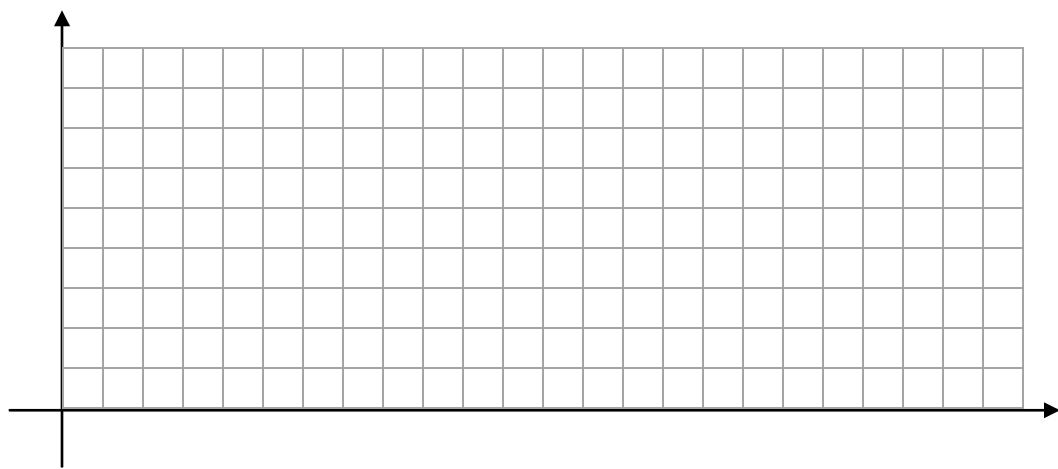
2. Draw the resulting waveform



2. Write down the VERILOG code for an XOR gate and the testbench code to test it.



2. Draw the resulting waveform



2. Write down the VERILOG code for $F=XY+Z'$ function and the testbench code to test it.

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2. Draw the resulting waveform

