Digital Electronics Laboratory Project

Using Verilog, **design the following:**

1. A module for 2-input AND
2. A module for 2-input OR
3. A module for a 2-input XOR

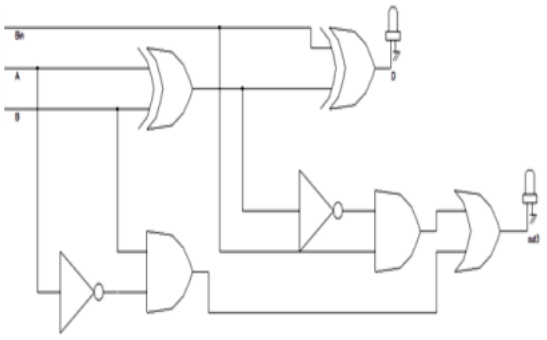
Using the above modules, Design a 2-bit full subtractor as seen below:

Provide your verilog code+ testbench file + simulations for each part.

- Submit your work using the **full-report template**.
- **Deadline for Online Submission**: 2 Jan. 2026 (4:00 p.m.)

- **For simplicity:**
  Inputs and Outputs:
  - **Inputs**:
    - A: Minuend (1-bit)
    - B: Subtrahend (1-bit)
    - Bin: Borrow-in (1-bit)
  - **Outputs**:
    - Diff: Difference (1-bit)
    - Bout: Borrow-out (1-bit)
  - **Truth Table:**

Input			Output	
A	**B**	**B_{in}**	**D**	**B_{out}**
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



Full Subtractor using XOR, NOT, AND, OR logic gates