

Course Code: 0714 02 CSE 2203	Year: Second	Term: Second
Course Title: Computer Architecture		
Course Status: Core		
Credit: 3.00		
Prerequisite(s): 0714 02 CSE 2105		
Rationale	This course aims to provide a strong foundation to understand modern computer system architecture and to apply these insights and principles to future computer designs. The course is structured around the three primary building blocks of general-purpose computing systems: processors, memories, and parallel processing.	

Course Contents		CLOs
Section A		
1	Introduction: Information representation, performance measurements, instruction and data access method, operation and operand of computer hardware, representing instruction, addressing styles.	1, 2
2	Basic Processing Unit: Arithmetic logic unit (ALU) operations, floating point operations, designing ALU, Single Bus Architecture, 3-Bus Architecture, Fetching a word from memory, Control Sequence of an instruction, Implementation of Control Sequence in Hardware, Branch Instructions, Hardwired Control, Micro programmed Control, Microinstructions, Micro routine, Control word.	2
3	Control Unit: Hardwired and Micro-programmed, Hazards, exceptions.	1, 2
4	Memory: Memory Hierarchy, Register, cache memory, primary memory, secondary memory, Multiple Level Cache Memory, performance measure for first, second and third level cache memory, virtual memory, page fault, translation look a side buffer.	1, 3, 4
Section B		CLOs
5	Input Output Devices: Types of i/o devices, how they connected to computer, interrupt, use of interrupt to control the i/o devices, daisy chain connection, interrupt priority. Direct Memory Access (DMA), Standard i/o, Memory Mapped I/O.	1, 2
6	Pipelining: Parallel processing using pipelining, improved performance for pipelining, classification of pipeline processors, interleaved memory organization, design of pipeline instruction unit, design of pipeline arithmetic unit, job sequencing and collision prevention, Various types of Hazards, Data Hazard, Instruction Hazard, Control Hazard, Avoiding data hazard, avoiding instruction hazard, avoiding structural hazard. Instruction queue, branch folding, static and dynamic branch prediction, superscalar operation, precise and imprecise exception, out of order execution.	2, 3, 4
7	Structure Algorithms for Array Processors: SIMD computer organization, SIMD interconnection networks, exploiting concurrency	2, 3, 4

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CSE 22 BATCH

Course Teacher: Atanu Shome Sir

CT: Missing

Term Final

Date: December 22, 2024
Khulna University, Khulna
Computer Science and Engineering Discipline
Second Year, Term-2 Examination, Session: 2022-2023
Course No.: 0714 02 CSE 2203
Title of the Course: Computer Architecture

Time: 3.0 Hours Full Marks: 60

* The figures in the margin denote the full marks allocated to each part of a question, with all questions having equal total marks.
* Use a separate sheet for each section.

Section A

There are **FOUR** questions in this section. Answer any **THREE** questions.

1. (a) "Increasing one aspect of a computer system can't assure overall increase in the system performance" – explain this statement. [L2; CLO1] 3
(b) Differentiate between fetch cycle and execute cycle that occur during instruction execution phase. Briefly explain their functionalities. [L2; CLO1] 4
(c) What is meant by multiplexed BUS architecture? What are the advantages and disadvantages. [L1; CLO1] 3

2. (a) State the Amdahl's law. Consider the following scenario:
Suppose, a program runs in 100 seconds on a computer, with multiply operations responsible for 80 seconds of this time. How much do I have to improve the speed of multiplication if I want my program to run five times faster? Can you analyze the law in this case using Amdahl's law equation. [L4; CLO2] 4

$$\text{Execution time after improvement} = \frac{\text{Execution time affected by improvement}}{\text{Amount of improvement}} + \text{Execution Time Unaffected}$$

(b) Imagine, we are trying to reduce the time for a program by 30% but this leads to an increase of 20% in the CPI for the following configuration. What clock rate should we have to get this time reduction? [L3; CLO2] 4

Processor	Clock Rate	No. of Instructions	Execution Time
P1	3 GHz	2000000000	7sec

(c) Do you think "CPI" is an accurate measurement? Why or why not – justify. [L5; CLO2] 2

3. (a) A hypothetical machine has three instructions:
1001=Load AC from memory
0110=Store AC to memory
0111=Multiply AC with memory
Each instruction and data are 16 bit long, where first 4-bit represent opcode and last 12-bit represents the address of memory location. Show the program execution diagrams (including PC, AC, IR contents) step by step for the following instruction set:
"Multiply the contents of memory location 111 & 112 and store the result in 115".
Assume that the program location starts from 015. [L3; CLO3] 4

(b) Analyze how the program flow of control differs when interrupts are absent compared to when they are utilized (both Long I/O wait and short I/O wait). Provide proper explanation with appropriate figures. [L4; CLO4] 5

(c) Why BUS width is a key determinant of performance? [L2; CLO2] 1

4. (a) A digital computer has a memory unit with a capacity of 16,384 words, 40 bits per word. The instruction code format consists of six bits for the operation part and 14 bits for the address part (no indirect mode bit). Two instructions are packed in one memory word and a 40-bit instruction register IR is available in the control unit. Formulate a procedure for fetching and executing instructions for this computer. [L3; CLO3] 5
- (b) The following program is stored in the memory unit of the basic computer. Show the contents of the AC, PC, and IR (in hexadecimal) at the end, after each instruction is executed. All numbers listed below are in hexadecimal. [L6; CLO2] 5

Location	Instruction
010	CLA
011	ADD 016
012	BUN 014
013	HLT
014	ADD 017
015	BUN 013
016	C1A5
017	93C6

Section B

There are **FOUR** questions in this section. Answer any **THREE** questions.

5. (a) What is the difference between a microprocessor and a microprogram? Is it possible to design a microprocessor without a microprogram? Are all the microprogrammed computers also microprocessors? [L4; CLO3] 3
- (b) Explain the difference between hardwired control and microprogrammed control. Is it possible to have a hardwired control associated with a control memory? [L4; CLO3] 3
- (c) Define the following: (a) microoperation; (b) microinstruction; (c) microprogram; (d) microcode. [L1; CLO2] 4
6. (a) Discuss locality of reference and its two types. [L2; CLO1] 2
- (b) What is meant by memory hierarchy? [L1; CLO1] 2
- (c) Explain Direct cache mapping by imagining a main memory of size 64 bytes and a cache size of 4 lines. Each cache line can hold 4 words. Show the CPU-generated address format to access a single word from both main memory and cache for the above-mentioned scenario. [L4; CLO4] 6
7. (a) Stating the purpose of Translation Lookaside Buffer (TLB), explain how TLB works. [L2; CLO4] 1+3
- (b) Analyze the techniques of Polled Interrupt I/O and Daisy Chain Interrupt I/O. Provide figures. [L4; CLO4] 4
- (c) Why DMA chip is better than other I/O modules? [L4; CLO3] 2
8. (a) Discuss how virtual memory provides security? [L2; CLO3] 4
- (b) Consider a computer with four floating-point pipeline processors. Suppose that each processor uses a cycle time of 40 ns. How long will it take to perform 400 floating point operations? Is there a difference if the same 400 operations are carried out using a single pipeline processor with a cycle time of 10 ns? [L6; CLO4] 4
- (c) Define control word and micro-routine. [L1; CLO1] 2

CSE 21 BATCH

Course Teacher: Atanu Shome

CT: Missing

Term Final

Date: 19.11.2023

Khulna University

Computer Science and Engineering Discipline

2nd Year Term II Examination 2023

Session: 2021-2022

Course No: CSE 2203

Full Title of Course: Computer Architecture

Full Marks: 60

Time: 03

Hours

- The figure in the margin indicates full marks. The questions are of equal value.
- Use separate sheet for each section.

SECTION A

There are FOUR questions in this section. Answer any THREE questions.

1.a List four reasons for learning computer architecture. 04

1.b Describe data movement, data storage, data processing from/to storage and data processing from storage to I/O function with suitable diagram and example. 06

✓ 2.a A compiler designer is trying to decide between two code sequences for a particular computer. The hardware designers have supplied the following facts: 05

CPI for each instruction class			
	A	B	C
CPI	1	2	3

For a particular high-level language statement, the compiler writer is considering two code sequences that require the following instruction counts:

Code Sequence	Instruction counts for each instruction class		
	A	B	C
1	2	1	2
2	4	1	1

- Which code sequence executes the most instructions?
- Which will be faster?
- What is the CPI for each sequence?

2.b Consider the following performance measurements for a program: 05

Measurement	Computer A	Computer B
Instruction count	10 billion	8 billion
Clock rate	4 GHz	4 GHz
CPI	1.0	1.1

- Which computer has the higher MIPS rating?
- Which computer is faster?

$$\begin{aligned} \text{Execution Time} &= \frac{I \times \text{CPI}}{\text{Clock Rate}} \\ &= \frac{I \times \text{CPI}}{10 \times \text{cycle time}} \end{aligned}$$

$$\frac{P_1}{P_2} = \frac{9}{10} \times \frac{r_1}{r_2}$$

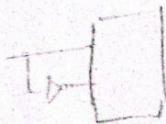
$$\Rightarrow 1000 \times 10^3 = 10^6$$

$$\frac{r_1}{r_2} = \frac{10}{9}$$

$$1000 M = \frac{10}{9} B$$

$$10^6 = \frac{10}{9} \times 10^6$$

- 3.a Briefly explain Nested interrupt handling. How does it differ from Sequential interrupt handling? 03
- 3.b How High-Performance BUS architecture is better than Traditional BUS architecture? 03
- 3.c What are the functionalities of Control BUS? 02
- 3.d What is the difference between asynchronous and synchronous timing architectures in case of memory read/write operations? 02
- 4.a Using parallel adder and gates, demonstrate the design of a 4-bit arithmetic operations for the following specifications: 06



Select lines s1 s0		Output
0	0	(X)
0	1	X+Y ✓
1	0	X+Y' ✓
1	1	X-Y

Use 2×1 MUX or 4×1 MUX if needed.

- 4.b How signed binary multiplication can be designed with only adder circuit? 04
Explain.

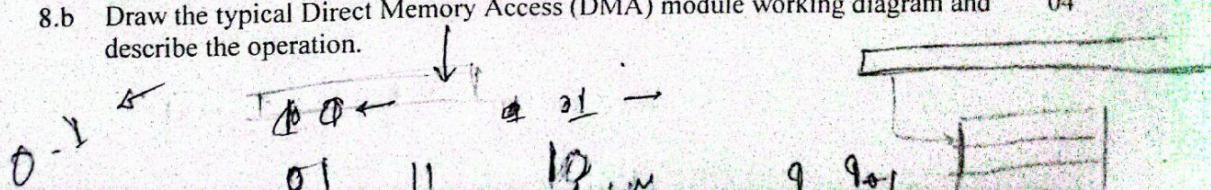
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Section B

There are **FOUR** questions in this section. Answer any **THREE** questions

24
L
34

- 5.a Define control hazard in case of instruction pipelining. Explain "multiple stems", "taken/not taken switch" techniques for handling control hazard. 06
- 5.b What are the three types of data hazard that can occur during instruction pipelining? Briefly explain. 04
- 6.a What are the dilemmas that can occur while choosing memory configuration for a computer system? What is the solution for these dilemmas? 04
- 6.b Write down advantages and disadvantages of all three types of cache mapping. 04
- 6.c In the principle of "locality of reference", what are meant by temporal locality and spatial locality? 02
- 7.a Show the block diagram of a microprogrammed control unit. 02
- 7.b Differentiate between Standard I/O and Memory-mapped I/O. Provide their block diagrams. 04
- 7.c Show the step-by-step multiplication of -5 and -7 using Booth's algorithm. 04
- 8.a What is virtual memory? Show how page fault is dealt with by explaining the address translation via page table with suitable diagram. 06
- 8.b Draw the typical Direct Memory Access (DMA) module working diagram and describe the operation. 04



CSE 20 BATCH

Course Teacher: Atanu Shome

CT: Missing

Term Final

Khulna University, Khulna Bangladesh
Computer Science and Engineering Discipline
2nd Year, 2nd Term, Examination: 2022, Session: 2020 -2021
Course No: CSE-2203, Course Title: Computer Architecture
Full Marks: 60, Time: 03 hours, Credit: 03 Date: 04/12/2022

- Answer 3 questions from each of the Sections A and B.

Section A

- 1 (a) How computer architecture and computer organization differ from each-other? Use real-life example to explain. 03
(b) Is it beneficial to connect high-speed BUS with the system BUS? Why or why not? 02
(c) Illustrate and explain the program flow control for "short I/O wait" based interrupt and "long I/O wait" based interrupt. 05
- 2 (a) A hypothetical machine has three instructions:
1001 = Load AC from memory
0110 = Store AC to memory
0111 = Multiply AC with memory
Each instruction and data are 16 bit long, where first 4-bit represents opcode and last 12-bit represents the address of the memory location. Show the program execution diagrams (including PC, AC, IR contents) step by step for the following instruction set: "Multiply the contents of memory location 111 & 112 and store the result in 115". Assume that the program location starts from 015.
(b) Consider two different processors P1, P2 executing the same instruction set with the clock rates and CPIs given in the following table. 03+03
- | Processor | Clock Rate | CPI |
|-----------|------------|-----|
| P1 | 1.5 GHz | 1 |
| P2 | 2.0 GHz | 2 |
- i. Which processor has the highest performance?
ii. For processor P1, we are trying to reduce the time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?
- 3 (a) Using the flowchart of the unsigned binary multiplication with adder circuit, show the steps of multiplying 5x3. 04
(b) Describe the Set-associative cache mapping with a suitable example and proper figure. Explain the breakdown of microprocessor generated address for identifying a particular word's location in cache lines and primary memory blocks. 06
- 4 (a) Discuss Register direct and Register indirect addressing modes with an appropriate diagram. 04
(b) A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part.
i) How many bits are there in the operation code, the register code part and the address part?
ii) Draw the instruction word format and indicate the number of bits in each part.
iii) How many bits are there in the data and address inputs of the memory? 03
(c) Discuss how CPU registers are connected to ALU through common buses. 03

Section B

- 5 (a) "Instruction execution cycle can be broken down into six separate steps" – what are the steps? [Write down the full names]. 02

- (b) What is the purpose of instruction level pipelining when we can simply apply program level parallel-processing architecture to speedup executions? 02
- (c) Explain in detail both static and dynamic methods of branch prediction for controlling branch hazards. 06
- 6 (a) Using the basic structure of General-Purpose Register (GPR) cell, design a 4-bit GPR for the following: 04
- | S1 | S0 | Operation |
|----|----|---------------|
| 0 | 0 | Parallel load |
| 0 | 1 | Shift left |
| 1 | 0 | Shift right |
| 1 | 1 | No operation |
- (b) Design a 5 bit Carry Look-Ahead (CLA) circuit. Show the steps. 06
- 7 (a) How data is transferred through the Direct Memory Access (DMA) technique? Explain. 05
- (b) Discuss about L1, L2, and L3 cache. 05
- 8 (a) Imagine, you are asked to create an embedded system with a large number of functionalities. Which type of control unit will you choose from hardwired and microprogrammed control unit? State the reason and briefly explain the structure of your chosen type. 04
- (b) Which one of the methods is better between polled interrupt and daisy chain interrupt? Why? 02
- (c) Briefly explain the functions of I/O modules. 04

CSE 19 BATCH

Course Teacher: Atanu Shome

CT: Missing

Term Final

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Khulna University
Computer Science and Engineering Discipline
2nd Year Term II Examination 2021
Session: 2019-2020
Course No: CSE 2203
Full Title of Course: Computer Architecture

Full Marks: 60

Date: 12.12.2021

Time: 03 Hours

- The figure in the margin indicates full marks. The questions are of equal value.
- Use separate sheet for each section.

SECTION A

There are **FOUR** questions in this section. Answer any **THREE** questions.

- | | |
|---|-------|
| 1.(a) Write down the names and purpose of - | 04 |
| PC, MAR, MBR, IR | |
| 1.(b) Draw and explain the instruction lifecycle (assume interrupt may occur). | 04 |
| 1.(c) What are the advantages and disadvantages of multiplexed BUS architecture? | 02 |
| 2.(a) Suppose we have two implementations of the same instruction set architecture. Computer
A has a clock cycle time of 250 ps and a CPI of 2.0 for some program, and computer B has a clock cycle time of 500 ps and a CPI of 1.2 for the same program. Which computer is faster for this program and by how much? | 04 |
| 2.(b) What is Amdahl's law? Explain Amdahl's law after solving the following problem. Suppose a program runs in 100 seconds on a computer, with multiply operations responsible for 80 seconds of this time. How much do you have to improve the speed of multiplication if you want my program to run five times faster? | 04 |
| 2.(c) Define clock rate and clock cycle. | 02 |
| 3.(a) Explain Fully-Associative cache mapping by imagining a main memory of size 64 bytes and a cache size of 4 lines. Each cache line can hold 4 words. Show the CPU-generated address format to access a single word from both main memory and cache for the above-mentioned scenario. | 04+02 |
| 3.(b) How effective address is calculated in register indirect addressing mode and displacement addressing mode? | 02 |
| 3.(c) What are the factors that affect instruction length? | 02 |
| 4.(a) State the differences between RISC and CISC. | 03 |

- 4.(b) Consider three different processors P1, P2, and P3 executing the same instruction set with the clock rates and CPIs given in the following table 03+04

Processor	Clock rate	CPI
P1	2 GHz	1.5
P2	3 GHz	2.5
P3	4 GHz	2.0

- i) Which processor has the highest performance?
- ii) For processor P1, we are trying to reduce the time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

SECTION B

There are **FOUR** questions in this section. Answer any **THREE** questions.

- 5.(a) "Instruction pipeline brought a radical improvement in the family of microprocessors"- justify this statement with explanation. 02
- 5.(b) What is meant by data hazard and control hazard? Explain with figure. 03
- 5.(c) How to handle control hazard? Provide explanation. 05
- 6.(a) Show the technique of address translation via page table in case of virtual memory. 03
- 6.(b) What are the purposes of virtual memory? Do you think virtual memory provides security? Why or why not? 02+02
- 6.(c) What is meant by cache coherence and locality of reference? 03
- 7.(a) What are the differences between standard I/O and memory mapped I/O? 02
- 7.(b) If you are asked to design a system which mode will you choose in case of I/O data transfer? Why? Explain the I/O data transfer mode design with proper figure that you will choose for your system. 02+04
- 7.(c) What is meant by maskable interrupt and non-maskable interrupt? Briefly explain with example. 02
- 8.(a) State the benefits of carry look-ahead adder over ripple carry adder. 02
- 8.(b) Design and implement an ALU circuit that will work as follows: 05

S0	S1	F
0	0	X+1
0	1	X-Y
1	0	X OR Y
1	1	Y'

Here X and Y both are 4 bits.

- 8.(c) Show the steps of multiplying -4 and -6 using Booth's algorithm. 03

CSE 18 BATCH

Course Teacher: Atanu Shome

CT: Missing

Term Final

Khulna University, Khulna
Computer Science and Engineering Discipline
2nd Year Term II Examination 2019
Session: 2018-2019
Course No.: CSE-2203
Full Title of the Course: Computer Architecture

Date: 04/12/2019

Full Marks: 60

Time: 03 Hours

- Figures in the margin indicate full marks. Questions are of equal Value.
- Use separate sheet for each section.

Section A

There are **FOUR** questions in this section. Answer any **THREE** questions

Marks

- 1.a) Our favorite program runs in 10 seconds on computer A, which has a 2 GHz clock. We are trying to help a computer designer build a computer, B, which will run this program in 6 seconds. The designer has determined that a substantial increase in the clock rate is possible, but this increase will affect the rest of the CPU design, causing computer B to require 1.2 times as many clock cycles as computer A for this program. What clock rate should we tell the designer to target? A GHz 04

- 1.b) Draw the instruction cycle state diagram (with interrupts). 04
1.c) Exemplify Register indirect addressing mode and Direct addressing mode with appropriate diagram. 02

- 2.a) Using 4-bit Carry Look-Ahead Adder as a building block, design a combinational circuit that will satisfy the following specification: 06

S ₀	S ₁	F
0	0	A+B
0	1	A-B
1	0	A+1
1	1	A-1

You can use 4x1 MUX.

- 2.b) Using the flowchart for unsigned binary multiplication with adder circuit, show the steps of multiplying 1011 and 1101. 04
- 3.a) What are the differences between Hardwired and Micro-programmed control units? 03
- 3.b) What are the differences between RISC and CISC? 03
- 3.c) Draw the top-level structure of a control unit. F1DLC0 F1W0 02
- 3.d) State the functionalities of MAR and MBR registers. 02
- 4.a) Design a 5-bit Carry Look-Ahead Adder circuit. Show the steps. 06
- 4.b) Draw the diagram of a High-performance Bus configuration architecture. 04

Section B

Marks

There are **FOUR** questions in this section. Answer any **THREE** questions

- | | | |
|------|---|----------|
| 5.a) | What are the three types of hazards that can occur during instruction pipelining?
Explain them briefly. | 05 |
| 5.b) | How to deal with Control hazards? Explain briefly. | 05 |
| 6.a) | Explain the Set Associative Cache mapping with proper diagrams. | 05 |
| 6.b) | Explain how will you find the CPU generated address "1101101" within Fully-
associative cache mapping. Imagine the RAM size is 128 words with 32 frames
and cache size is 4 lines, which can hold 4 words per line. How much bits are
required to represent the address for cache line and tags? | 02+01 |
| 6.c) | What are the advantages of set-associative cache mapping over other types of
cache mapping? | |
| 7.a) | What is page fault? | |
| 7.b) | Show how page fault is dealt with by explaining the address translation via page
table with proper diagram. Explain. | 02
05 |
| 7.c) | How can you speed up address translation using Translation Lookaside Buffer?
Explain. | 03 |
| 8.a) | Explain both ways of serving multiple interrupts (Polled interrupts and Daisy
Chain interrupts). | 02 |
| 8.b) | State the purpose of DMA chip. Discuss the three types of DMA. | 02+06 |

CSE 17 BATCH

Course Teacher: Atanu Shome

CT: Missing

Term Final

Khulna University, Khulna

Computer Science and Engineering Discipline

Session: 2017-2018

2nd Year, Term II, Examination 2018

Course No: CSE 2203

Full Marks: 60

Full Title of Course: Computer Architecture

Time: 03 Hours

- The Figures in the margin indicate full marks. The questions are of equal value.
- Use separate sheet for each section.

SECTION A

There are FOUR questions in this section. Answer any THREE questions.

- (1) a) What, in general terms, is the distinction between computer organization and computer architecture? 02
b) Show the diagram of computer components (top level view) and briefly define them. 03
c) List and briefly define the possible states that define an instruction cycle. 05
- (2) a) Briefly describe the types of computer bus and bus arbitration. 04
b) Describe the approaches to dealing with multiple interrupts. 03
c) Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder contains the immediate operand or an operand address. 03
 a. What is the maximum directly addressable memory capacity (in bytes)? 2
 b. Discuss the impact on the system speed if the microprocessor bus has a 32-bit local address bus and a 16-bit local data bus. 03
- (3) a) Draw the block diagram of Three-bus organization of the datapath inside a processor 03
b) Draw the block diagram of Single-bus organization of the datapath inside a processor 03
c) With the help of a synchronous timing diagram explain the occurrence of events on a bus. 04
- (4) a) Suppose a stack is to be used by the processor to manage procedure calls and returns. Can the program counter be eliminated by using the top of the stack as a program counter? Explain. 02
b) What are the approaches to dealing with branches in pipeline? With appropriate diagram explain the "Branch History Table" strategy for branch prediction. 05
c) Assume a stack-oriented processor that includes the stack operations PUSH and POP. 03
Arithmetic operations automatically involve the top one or two stack elements. Begin with an empty stack. What stack elements remain after the following instructions are executed?

PUSH 4
PUSH 7
PUSH 8
ADD
PUSH 10
SUB
MUL

SECTION B

There are **FOUR** questions in this section. Answer any **THREE** questions.

5. a) List the key characteristics of computer memory systems. 02
b) "One of the sharpest distinctions among memory types is the method of accessing units of data" - What are the methods? Describe them. 04
c) A two-way set-associative cache has lines of 16 bytes and a total size of 8 kbytes. The 64-Mbyte main memory is byte addressable. Calculate the addresses and show the format of main memory. 14-3-4 04
6. a) Describe Direct, Set Associative and fully associative cache Mapping with example 03
b) Why replacement algorithm is necessary in implementing cache memory? Describe the most common replacement algorithms. 04
c) A set-associative cache consists of 64 lines, or slots, divided into four-line sets. Main memory 03

Page 1 of 2

contains 4K blocks of 128 words each. Calculate the addresses and show the format of main memory.

7. a) With a neat diagram show the functional blocks of an I/O module. 02
b) In case of interrupt driven I/O, graphically show and explain how changes are made in memory and registers for an interrupt. 04
c) Consider a system employing interrupt-driven I/O for a particular device that transfers data at an average of 8 KB/s on a continuous basis. 04
- a. Assume that interrupt processing takes about 100 μ s (i.e., the time to jump to the interrupt service routine (ISR), execute it, and return to the main program). Determine what fraction of processor time is consumed by this I/O device if it interrupts for every byte.
- b. Now assume that the device has two 16-byte buffers and interrupts the processor when one of the buffers is full. Naturally, interrupt processing takes longer, because the ISR must transfer 16 bytes. While executing the ISR, the processor takes about 8 μ s for the transfer of each byte. Determine what fraction of processor time is consumed by this I/O device in this case.
8. a) Draw the typical DMA module diagram and describe the operation. 03
b) The DMA mechanism can be configured in a variety of ways. Show the possible DMA configuration and briefly explain. 03
c) Two women are on either side of a high fence. One of the women, named Apple-server, has a beautiful apple tree loaded with delicious apples growing on her side of the fence; she is happy to supply apples to the other woman whenever needed. The other woman, named Apple-eater, loves to eat apples but has none. In fact, she must eat her apples at a fixed rate (an apple a day keeps the doctor away). If she eats them faster than that rate, she will get sick. If she eats them slower, she will suffer malnutrition. Neither woman can talk, and so the problem is to get apples from Appleserver to Apple-eater at the correct rate. 04

Assume that there is an alarm clock sitting on top of the fence and that the clock can have multiple alarm settings. How can the clock be used to solve the problem? Draw a timing diagram to illustrate the solution. (Hint: This problem is based on illustration of I/O mechanisms)