CO-2 Home Assignment :

1. Discuss about the Register Transfer & Arithmatic micro operations.

Register Transfer :

Information transferred from one register to another is designated in symbolic from by means of replacement operator.

$$R_2 \rightarrow R_1$$

It denoted the transfer of the data from register R_1 into R_2. Normally we want the transfer to occur only in the predetermined control condition. This can be shown by following if-then statements - if(P=1) then ($P_2 \leftarrow R_1$)

2. ## Arithmatic micro operations :

Some of the basic micro operations are addition Subtraction, increment and decrement.

Add microoperation :

It is defined by the following statement -

$$R_3 \leftarrow R_1 + R_2$$

The above statement instructs the data or contents of Register R_1 to be added to data or content of Register R_2 and the sum should be transfered to Register R_3.

Subtract micro-Operation

In subtract micro-operation, instead of using minus operator we take 1's Compliment and add 1 to the Register which gets Subtracted

i.e $R_1 - R_2$ is equivalent to $R_3 \rightarrow R_1 + R_2' + 1$

Increment or Decrement micro-operation

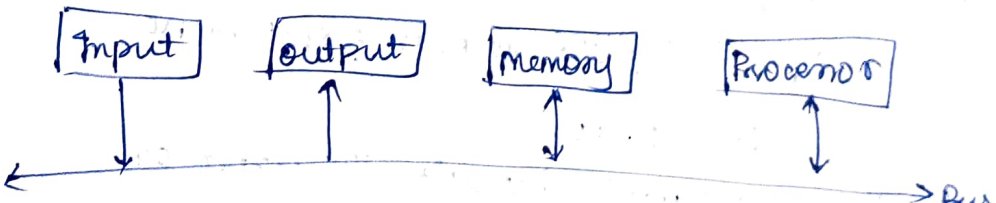
Increment and Decrement micro-operations are generally performed by adding and subtracting 1 to and from the Register Respectively.

$R_1 \rightarrow R_1 + 1$

$R_1 \rightarrow R_1 - 1$.

2. Explain the operations of Single Bus architecture of CPU?

In Single Bus architecture, all components including the central processing unit, memory and Peripherals share a common bus. When many devices need the bus at the same time this creates a status of conflict called bus contention. Some wait for the Bus while another has control of it.



Single Bus Structure

One Common Bus is used for communication between peripherals and processors. Instructions and data both are transferred in Same Bus.

Its performance is low.

Cost of single Bus structure is low.

Numbers of cycles for execution is more.

Execution of process is low.

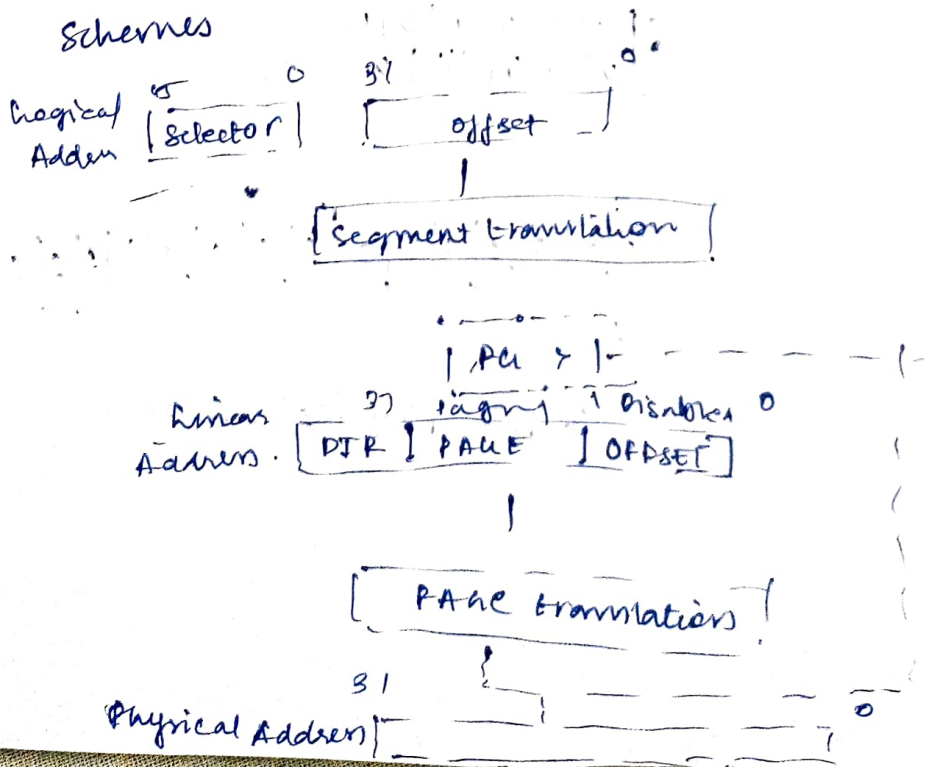
Numbers of Registers associated are less.

At a time single operand can be read from Bus.

3. Demonstrate the process of converting logical address into low physical address.

conversion of logical address to physical address.

* The concept of a logical address space that is bound to a seperate physical space is central to proper memory management.
* logical address - generated by the CPU, also referred to as virtual address.
* physical address - address seen by the memory unit.
* Logical and physical address are the same in compile time & load time address binding schemes

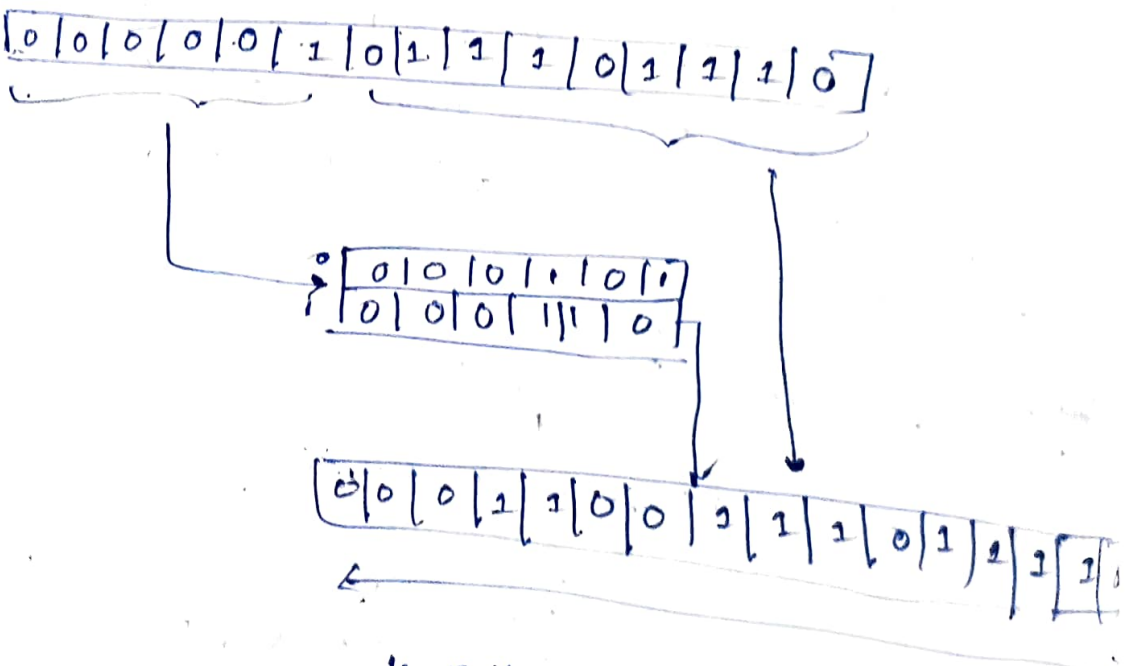


There are steps to translate logical address to physical address.

Step 1: Find the Index field from the Segment Selector and use the Index field to locate the segment descriptor for the segment in global descriptor table (GDT)

Step 2: Test the access and limit the field of Descriptor to make sure that the segment is accessible and the offset is within the limit of the segment.

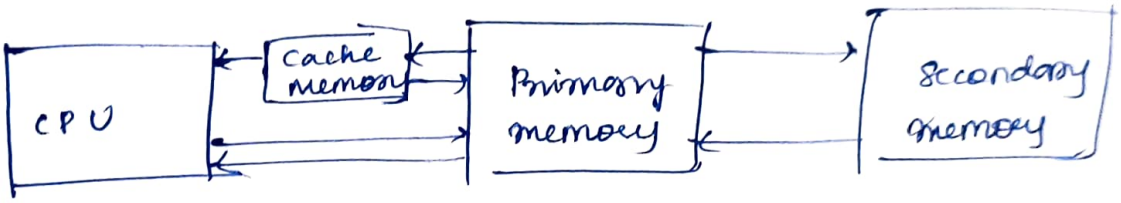
Step 3: The base address of the segment will be obtained from the segment descripter. Then the base address of the segment will be added to the offset to determine a linear address.



4. Infer the Operation of cache memory based on their storage functioning and mapping techniques.

Cache memory:

Cache memory is a special high-speed memory. It is used to speed up and synchronizing with high speed CPU. cache memory is costlier than main memory or disk memory but economical than CPU registors.



Cachemaping:

There are three different types of mapping used for the purpose of cache memory. which are as follows:

1) Direct mapping.
2) Associate mapping.
3) Set Associate mapping.

* Direct mapping:

The simple technique, known as direct mapping, maps each block of main memory into only one possible Cache line.

$$i = j \text{ modulo } m$$

where i: cache line number
j: main memory block number.
m: numbers of lies in the Cache.