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EEE 525 Spring 2024 Lab #1

Given effective width for all types of device models(SLVT, LVT, SRAM, RVT) is 1000 nm which is 1 micron. Let's say we have Nfin, which is the number of fins in each transistor. Then effective width of the transistor = Nfin*(2*hfin + wfin), where hfin and wfin are the width and height of fin respectively. The values of hfin and wfin for all device models are obtained from their HSPICE models from the 7nm_TT.pm file.

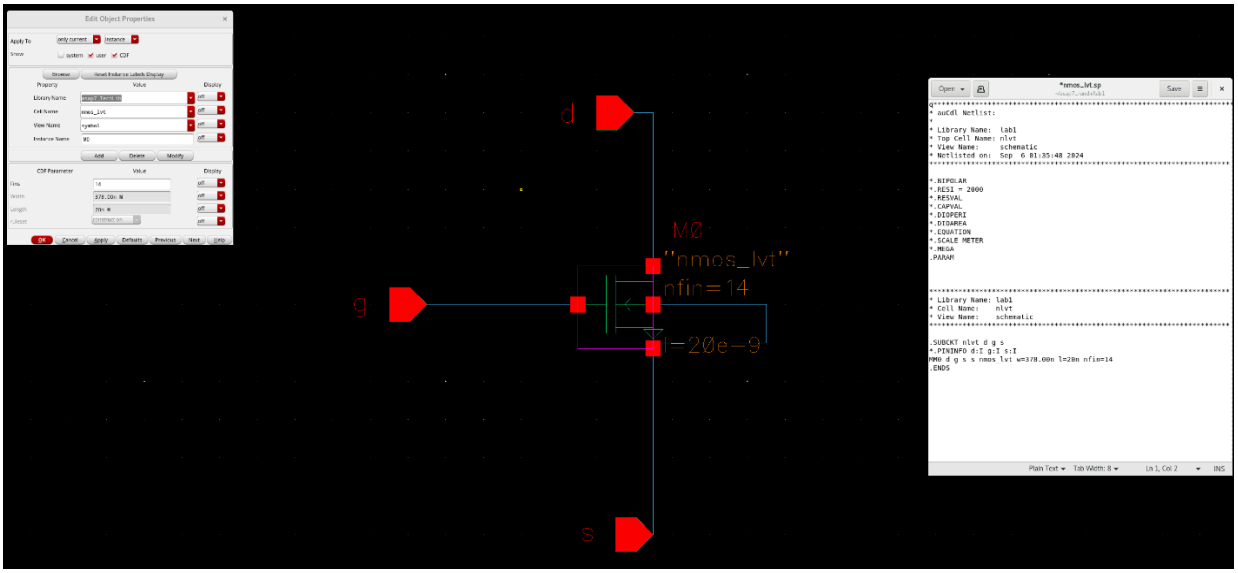
```
** ASAP TT models v1.0 8/3/16

** Hspice modelcard
.model nmos_lvt nmos level = 72
************************************************************
*                          general                         *
************************************************************
+version = 107            bulkmod = 1            igcmod  = 1            igbmod  = 0
+gidlmod = 1              iimod   = 0            geomod  = 1            rdsmod  = 0
+rgatemod= 0              rgeomod = 0            shmod   = 0            nqsmod  = 0
+coremod = 0              cgeomod = 0            capmod  = 0            tnom    = 25
+eot     = 1e-009         eotbox  = 1.4e-007     eotacc  = 1e-010       tfin    = 6.5e-009
+toxp    = 2.1e-009       nbody   = 1e+022       phig    = 4.307        epsrox  = 3.9
+epsrsub = 11.9           easub   = 4.05         ni0sub  = 1.1e+016     bg0sub  = 1.17
+nc0sub  = 2.86e+025      nsd     = 2e+026       ngate   = 0            nseg    = 5
+l       = 2.1e-008       xl      = 1e-009       lint    = -2e-009      dlc     = 0
+dlbin   = 0              hfin    = 3.2e-008     deltaw  = 0            deltawcv= 0
+sdterm  = 0              epsrsp  = 3.9
+toxg    = 1.80e-009
```

Device Models	LVT	RVT	SLVT	SRAM
NMOS	hfin = 3.2e-008 wfin = 6.5e-009 Nfin = 14	hfin = 3.2e-008 wfin = 6.5e-009 Nfin = 14	hfin = 3.2e-008 wfin = 6.5e-009 Nfin = 14	hfin = 3.2e-008 wfin = 6.5e-009 Nfin = 14
PMOS	hfin = 3.2e-008 wfin = 6.5e-009 Nfin = 14	hfin = 3.2e-008 wfin = 6.5e-009 Nfin = 14	hfin = 3.2e-008 wfin = 6.5e-009 Nfin = 14	hfin = 3.2e-008 wfin = 6.5e-009 Nfin = 14

1000e-009 = Nfin*(2*3.2e-008 + 6.5*e-009) => Nfin = 1000/70.5 = 14 (rounded off to integer)

Now, through the virtuoso schematic editor, I generated the netlists for all my device models. Below is an example schematic and netlist generated for the NMOS LVT device.



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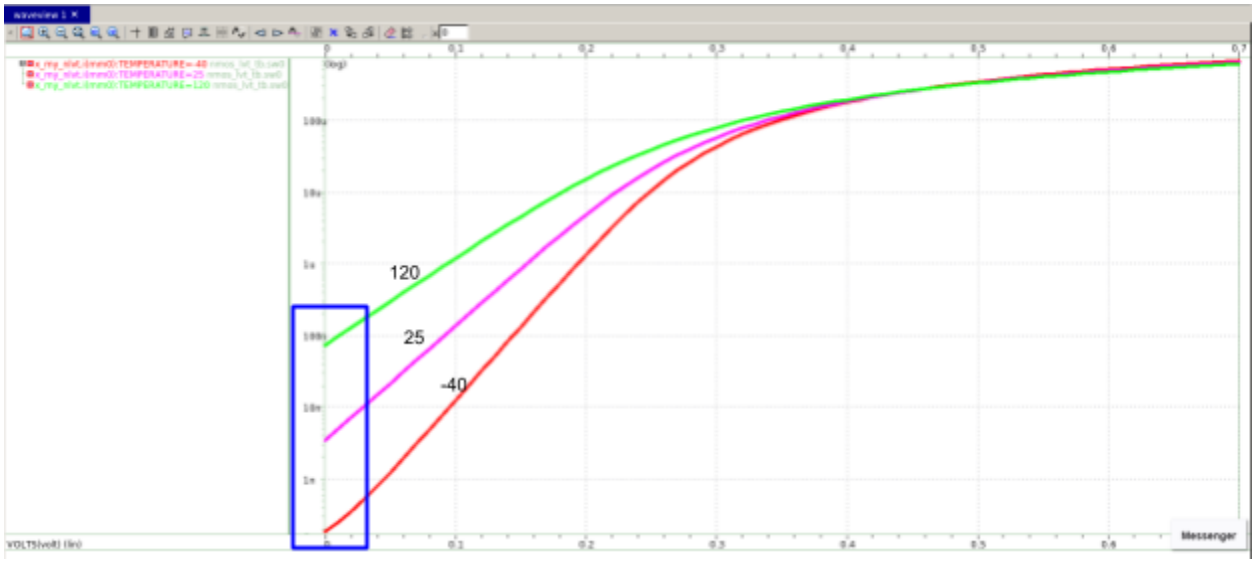
For plotting logIds vs Vgs at different temperatures, below are the testbenches I have written for PMOS and NMOS LVT devices in HSPICE for simulation and generated the below waveforms.

```
.option ACCURATE
.option measdgt=5
.OPTIONS GMINDC= 1e-18
.option probe post=2
.option INGOLD=1
.OPTIONS RELTOL=0.01

.inc "/usr/local2/ASAP7/afs/asu.edu/class/e/e/e/eee525b/asap7/asap7PDK/
models/hspice/7nm_TT.pm"

.include "./pmos_lvt.sp"
.TEMP 25


.param Vgnd=0
.param Vvdd= 0.7

X_my_plvt d g s plvt

vS s 0 dc=Vvdd
vD d 0 dc=Vgnd
Vgs g s dc=0

.DC Vgs -0.7 0 0.01 TEMP POI 3 -40 25 120

.PROBE i(X_my_plvt)
.PROBE i(*)
.PROBE v(*)
.option post
.end
```

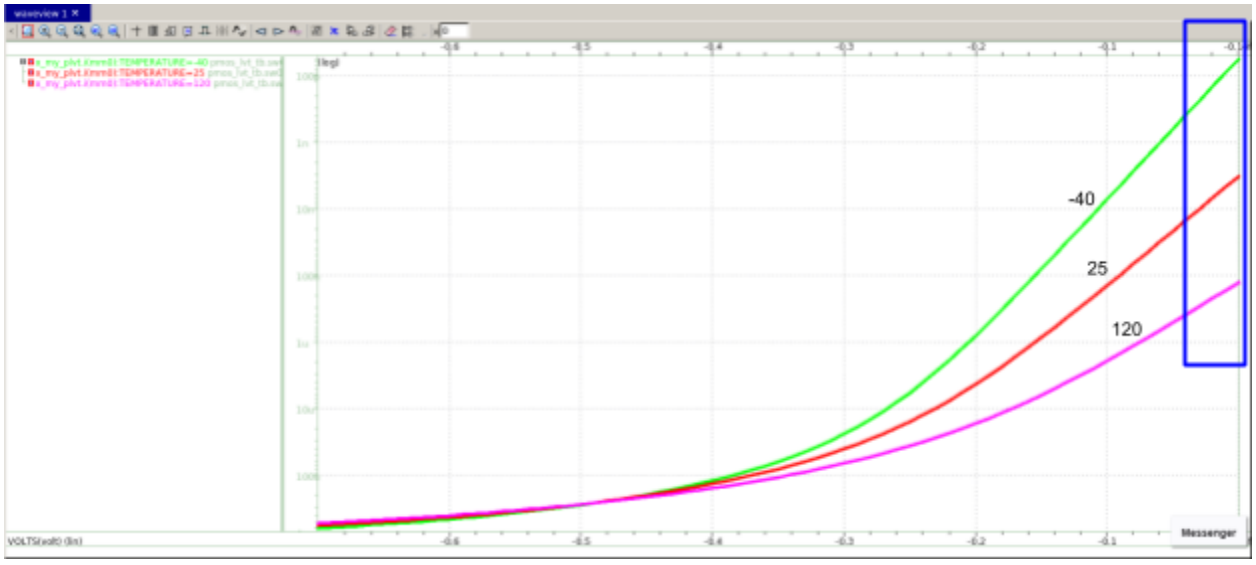
nmos_lvt.sp | nmos_lvt_tb.sp

```
.option ACCURATE
.option measdgt=5
.OPTIONS GMINDC= 1e-18
.option probe post=2
.option INGOLD=1
.OPTIONS RELTOL=.01

.inc "/usr/local2/ASAP7/afs/asu.edu/class/e/e/e/eee525b/asap7/asap7PDK/
models/hspice/7nm_TT.pm"

.include "./nmos_lvt.sp"
.TEMP 25
.option

.param Vgnd=0
.param Vvdd= 0.7
X_my_nlvt d g s nlvt

vS s 0 dc=Vgnd
vD d 0 dc=Vvdd
Vg g 0 dc=0
.DC Vg 0 0.7 0.01 TEMP POI 3 -40 25 120
.PROBE i(X_my_nlvt)
.PROBE i(*)
.PROBE v(*)
.option post
.end
```

(1) (plot in 1st quadrant) NMOS LVT device logIds v/s Vgs at -40° , 25° , and 120° C



(plot in 3rd quadrant) PMOS LVT device logIds v/s Vgs at -40° , 25° , and 120° C



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For plotting Ids vs Vgs at 25° C for all devices i.e. SLVT, LVT, RVT, SRAM , I used below test benches for NMOS and PMOS.

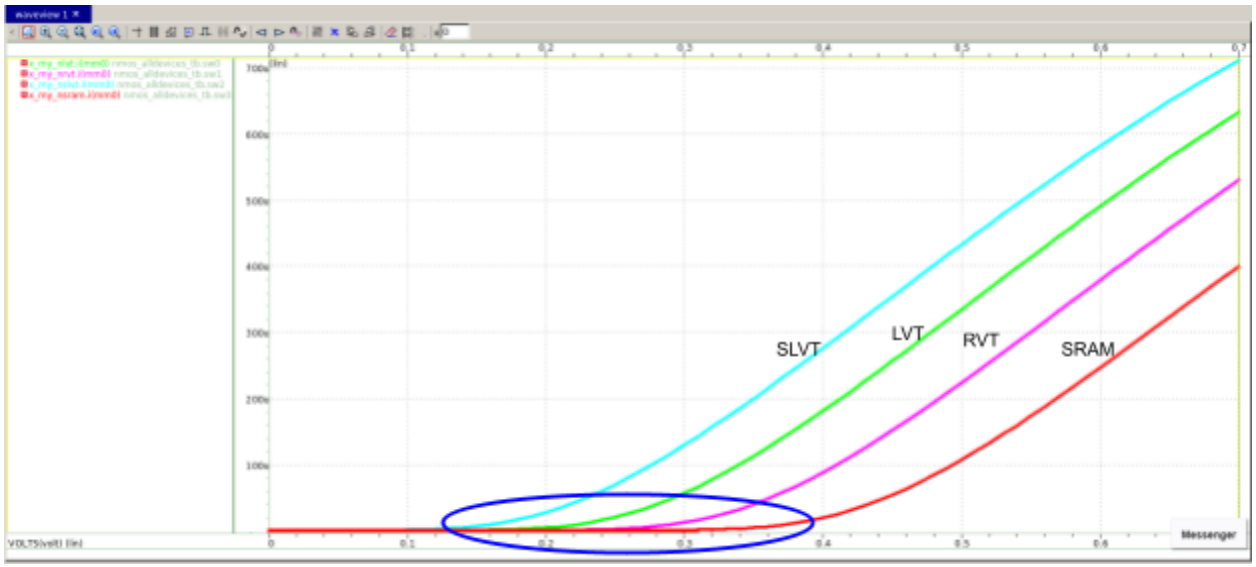
pmos_alldevices_tb.sp

```
.option ACCURATE
.option measdgt=5
.OPTIONS GMINDC= 1e-18
.option probe post=2
.option INGOLD=1
.OPTIONS RELTOL=0.01
.inc "/usr/local2/ASAP7/afs/asu.edu/class/e/e/e/eee525b/asap7/asap7PDK/
models/hspice/7nm_TT.pm"
.include "./pmos_lvt.sp"
.include "./pmos_rvt.sp"
.include "./pmos_slvt.sp"
.include "./pmos_sram.sp"
** default temperature **
.TEMP 25
** giving voltage values as variables**
.param Vgnd=0
.param Vvdd= 0.7
**all my devices instantiation **
X_my_plvt d g1 s1 plvt
X_my_prvt d g2 s2 prvt
X_my_pslvt d g3 s3 pslvt
X_my_psram d g4 s4 psram
** connecting voltage sources to all pins with values defined in
parmeters **
vS1 s1 0 dc=Vvdd
vS2 s2 0 dc=Vvdd
vS3 s3 0 dc=Vvdd
vS4 s4 0 dc=Vvdd
vD d 0 dc=Vgnd
Vgs1 g1 s1 dc=Vgnd
Vgs2 g2 s2 dc=Vgnd
Vgs3 g3 s3 dc=Vgnd
Vgs4 g4 s4 dc=Vgnd
**doing DC sweep **
.DC Vgs1 -0.7 0 0.01
.DC Vgs2 -0.7 0 0.01
.DC Vgs3 -0.7 0 0.01
.DC Vgs4 -0.7 0 0.01
**measuring current values **
.PROBE i(X_my_plvt)
.PROBE i(X_my_prvt)
.PROBE i(X_my_pslvt)
.PROBE i(X_my_psram)
.PROBE i(*)
.PROBE v(*)
.option post
.end
```

nmos_alldevices_tb.sp

```
.option ACCURATE
.option measdgt=5
.OPTIONS GMINDC= 1e-18
.option probe post=2
.option INGOLD=1
.OPTIONS RELTOL=0.01
.inc "/usr/local2/ASAP7/afs/asu.edu/class/e/e/e/eee525b/asap7/asap7PDK/
models/hspice/7nm_TT.pm"
.include "./nmos_lvt.sp"
.include "./nmos_rvt.sp"
.include "./nmos_slvt.sp"
.include "./nmos_sram.sp"
** default temperature **
.TEMP 25
** giving voltage values as variables**
.param Vgnd=0
.param Vvdd= 0.7
**all my devices instantiation **
X_my_nlvt d1 g1 s nlvt
X_my_nrvt d2 g2 s nrvt
X_my_nslvt d3 g3 s nslvt
X_my_nsram d4 g4 s nsram
** connecting voltAge sources to all pins with values defined in
parmeters **
vS s 0 dc=Vgnd
vD1 d1 0 dc=Vvdd
vD2 d2 0 dc=Vvdd
vD3 d3 0 dc=Vvdd
vD4 d4 0 dc=Vvdd
Vgs1 g1 s dc=Vgnd
Vgs2 g2 s dc=Vgnd
Vgs3 g3 s dc=Vgnd
Vgs4 g4 s dc=Vgnd
**doing DC sweep **
.DC Vgs1 0 0.7 0.01
.DC Vgs2 0 0.7 0.01
.DC Vgs3 0 0.7 0.01
.DC Vgs4 0 0.7 0.01
**measuring current values**
.PROBE i(X_my_nlvt)
.PROBE i(X_my_nrvt)
.PROBE i(X_my_nslvt)
.PROBE i(X_my_nsram)
.PROBE i(*)
.PROBE v(*)
.option post
.end
```

2) (plot in 1st quadrant) NMOS SLVT, LVT, RVT, and SRAM devices Ids v/s Vgs at 25° C



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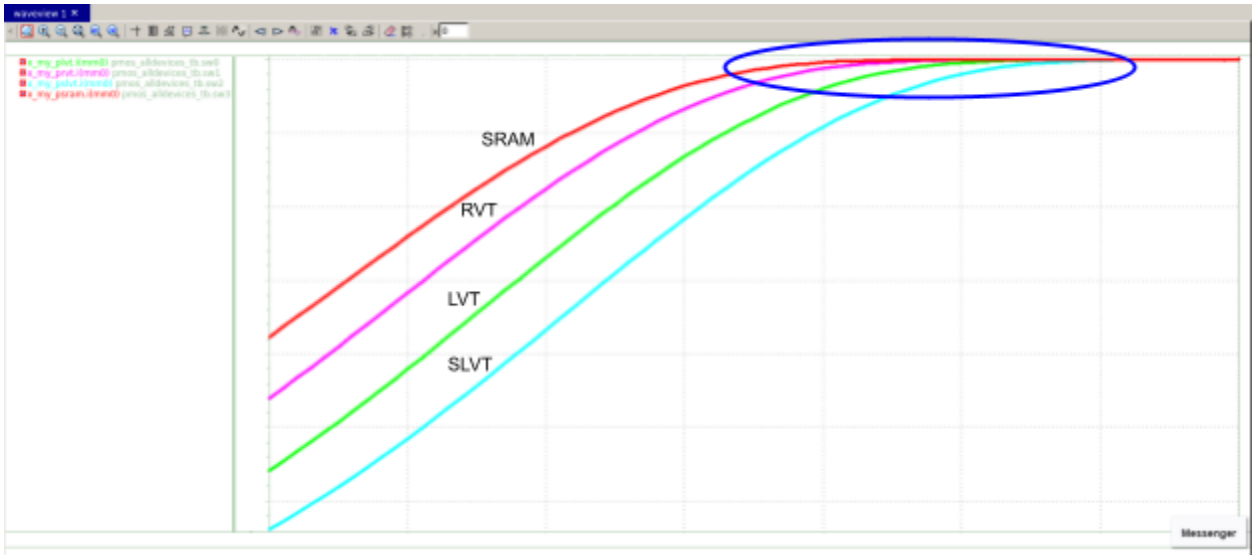
(plot in 3rd quadrant) PMOS SLVT, LVT, RVT, and SRAM devices Ids v/s Vgs at 25° C



a) Brief Explanation

In my testbench for LVT devices at 3 temperatures, I included my SPICE netlists of NMOS LVT and PMOS LVT which are nlvt and plvt and instantiated them as X_my_nlvt and X_my_plvt. Now, to connect the pins d, g, s which are drain, source and gate respectively, I used parameter variables for VDD and GND as Vvdd and Vgnd which are 0.7 V and 0 V respectively. Next, I used a DC sweep of Vgs which is voltage between g and s with 3 points of interest of temperatures i.e -40°, 25°, 120° C. Then, I measured currents and voltages through my devices using the .PROBE command.

For my testbench for all devices LVT, SLVT, RVT, SRAM for PMOS and NMOS at temperature 25° C, I included their respective SPICE netlists and instantiated them. Connected all the gate, drain, sources pins of each device to respective voltage sources. Next, applied DC sweep on Vgs and measured currents through all devices and plotted them in the Wave Viewer tool.

b) What is leakage current and what happens to the leakage current with temperature? What happens to the drive current with temperature? (Show it in your graph)

Leakage current is current that through transistor in cutoff region i.e Vgs< Vt for NMOS Vsg < |Vt| for PMOS. The leakage current is the Y-intercept of the straight line in the sub-threshold region. According to the graphs generated above in part 1, the leakage current is increasing with temperature(highlighted as a blue rectangle box). For PMOS, you see it on the right Y-axis as the current is negative and the plot is in the 3rd quadrant and the same trend is observed for PMOS i.e leakage current increases with temperature.

c) What are LVT, SLVT, RVT and SRAM devices and mention a use case for each device?

All the above mentioned devices have a different threshold voltage. Threshold voltage plays an important role in how fast the transistor can switch and leakage current. So, there will be tradeoffs between speed and power consumption. Below table summarizes the answer.

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Device	Explanation	Use case
LVT	Low Voltage Threshold transistors have a lower threshold voltage which allows for faster switching implies faster speed of operation, but with higher leakage current.	Used in high-speed CMOS logic circuits, high-performance CPU or GPU, high-speed clock buffers, data path logic.
SLVT	Super Low Voltage Threshold transistors with the lowest threshold voltage for ultra-fast switching but at the cost of maximum leakage current.	Used in ultra-high-speed circuits, clock distribution networks in high-end processors, high-frequency applications like telecom hardware, Server CPU.
RVT	Regular Voltage Threshold transistors have a moderate threshold voltage but offer a balance between speed and power consumption.	Used in general-purpose logic circuits in mobile processors, embedded systems, and consumer electronics like phones, tablets.
SRAM	SRAM PMOS transistors in pull-up paired with SRAM NMOS transistors for pull-down ensures stable and efficient memory storage with low leakage current.	Common in SRAM cells used for CPU cache (L1, L2, L3), buffer memory in network routers, FPGAs, and embedded systems where low-power operation is essential.

d) Based on simulation results, rank the above four devices according to how fast they operate.

How fast a device can operate depends on how fast you can turn it on, so the threshold voltage Vth which is minimum voltage to turn on the device should be low.
Threshold voltage is the point in the graph where with less increase in voltage there is huge increase in current(Ioff switched to Ion) i.e the inflection point.(highlighted in blue oval in Ids vs Vgs graphs at 25^{o}C)
For NMOS, I observed the below trend from the plots generated
NMOS : SLVT > LVT > RVT > SRAM, so, SLVT operates fastest of all and SRAM is slowest.
Similarly, for PMOS, I observed the below trend from the plots generated. As it is in the 3rd quadrant, we have to observe the modulus of current.
PMOS : SLVT > LVT > RVT > SRAM, so, SLVT operates fastest of all and SRAM is slowest.

e) What is the subthreshold slope? What would be an ideal subthreshold slope value.

When Vgs < Vt, Vsg < |Vt| for NMOS and PMOS respectively, there is a small current still flowing in the transistor even though the transistor is not on and that region of operation is called subthreshold region. The current in that region is exponentially dependent on Vgs or |Vsg| respectively. Therefore, when you take log(current in device) vs Vgs, there is a straight line dependence on Vgs in the subthreshold region. The slope of that line is the subthreshold slope. So, it is **voltage Vgs** required to increase the current through the device by **one decade** (a tenfold increase) when the transistor operates in the subthreshold region. An ideal subthreshold slope value = **16.67 decade/V** and ideal subthreshold swing value = 60 mV/decade which is inverse of subthreshold slope at 300 K. An ideal subthreshold slope is when slope of that line is maximum which is achievable by a transistor device and **fundamentally set by device doping concentrations, gate oxide control over channel and temperature.**

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f) Explain all the elements in the equation of subthreshold slope.

Subthreshold slope = Q/(NKT*ln(10))

Q is the electron charge value
K is the boltzmann's constant
T = temperature
ln(10) = constant
N is dependent on capacitance of the oxide and depletion region and equals 1+ C_{dep}/C_{ox}.

g) What is the importance of subthreshold slope and which parameter is it used to define?

Subthreshold slope is important because it tells how good our transistor device is in terms of how fast it can turn on and how much leakage current it has. There is a trade off between leakage current and how easily you can switch the transistor. So, a subthreshold slope defines the switching speed and leakage current through the device. Higher the slope, higher the switching speed and higher the leakage current. Higher the leakage current, higher the power consumption. So, the subthreshold slope defines the leakage current, switching speed, and power consumption of the transistor.
A faster transistor has a high subthreshold slope and maximum value of it is 16.67 decade/V.

h) Based on the above two questions if the on/off ratio of the transistor is 10^5 what would be Vg, if subthreshold swing is 60mv/decade?

The endpoints of the straight line in the subthreshold region in logIds vs Vgs plot, are (log Ioff, 0) and (log Ion , Vth). So, the slope of that line is the subthreshold slope(SS) = ΔVgs/(log(Ion)-log(Ioff)) Here, ΔVgs is Vth.
Or By using mathematical formula for calculating slope using two points gives :

(log Ion - log Ioff)/ (Vth - 0) => log(Ion/Ioff)/Vth = 1/60 => Vth = 5*60 = 300 mV

since subthreshold swing is reciprocal of subthreshold slope.

So, the amount of Vg to turn on the transistor is Vth and equal to 300 mV.(For NMOS since the source is connected to ground, For PMOS Vth = Vsg = 300 mV => Vg = 0.7 -0.3 =0.4V = 400 mV).

i) (Table) subthreshold slope (in mV/decade) values of NMOS and PMOS all devices (SLVT, LVT, RVT and SRAM) at -40,25 and 120 degrees. (Also include a screenshot of .measure commands used for this).

Below are the screenshots of results from HSPICE simulation at different temperatures for PMOS which are summarized in table.

```
$DATA1 SOURCE='HSPICE' VERSION='K-2015.06-2 linux64'
.TITLE '.option accurate'
 swinglvt         swingslvt        swingrvt         swingsram
 temper           alter#
   47.37453         47.58192         47.21173         46.60871
  -40.00000       1
```

```
$DATA1 SOURCE='HSPICE' VERSION='K-2015.06-2 linux64'
.TITLE '.option accurate'
 swinglvt         swingslvt        swingrvt         swingsram
 temper           alter#
   60.66446         61.67275         60.38074         59.60752
   25.00000       1
```

```
$DATA1 SOURCE='HSPICE' VERSION='K-2015.06-2 linux64'
.TITLE '.option accurate'
 swinglvt         swingslvt        swingrvt         swingsram
 temper           alter#
   82.37254         87.58788         80.33081         78.84020
  120.00000       1
```

Subthreshold Swing (mV/decade) PMOS

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Device \ Temp.	-40ºC	25ºC	120ºC
LVT	47.37	60.66	82.37
SLVT	47.58	61.67	87.58
RVT	47.21	60.38	80.33
SRAM	46.61	59.61	78.84

```
$DATA1 SOURCE='HSPICE' VERSION='K-2015.06-2 linux64'
.TITLE '.option accurate'
 swinglvt         swingslvt        swingrvt         swingsram
 temper           alter#
   48.81317         48.89762         48.73570         48.14842
  -40.00000       1
```

```
$DATA1 SOURCE='HSPICE' VERSION='K-2015.06-2 linux64'
.TITLE '.option accurate'
 swinglvt         swingslvt        swingrvt         swingsram
 temper           alter#
   62.41113         62.52064         62.31193         61.55950
   25.00000       1
```

```
$DATA1 SOURCE='HSPICE' VERSION='K-2015.06-2 linux64'
.TITLE '.option accurate'
 swinglvt         swingslvt        swingrvt         swingsram
 temper           alter#
   82.29389         83.04326         82.15179         81.16597
  120.00000       1
```

Subthreshold Swing (mV/decade) NMOS

Device \ Temp.	-40ºC	25ºC	120ºC
LVT	48.81	62.41	82.29
SLVT	48.89	62.52	83.04
RVT	48.73	62.31	82.15
SRAM	48.15	61.56	81.16

In your report, write the HSPICE measure commands you used for simulation. Note that log is regarded as log2 in HSPICE.

```
.PROBE LVT = deriv("log10(i(X_my_plvt.MM0))")
.meas swingLVT min "1000/abs(par(LVT))"

.PROBE SLVT = deriv("log10(i(X_my_pslvt.MM0))")
.meas swingSLVT min "1000/abs(par(SLVT))"

.PROBE RVT = deriv("log10(i(X_my_prvt.MM0))")
.meas swingRVT min "1000/abs(par(RVT))"

.PROBE SRAM = deriv("log10(i(X_my_psram.MM0))")
.meas swingSRAM min "1000/abs(par(SRAM))"
```

PMOS

```
.PROBE LVT = deriv("log10(i(X_my_nlvt.mm0))")
.meas swingLVT min "1000/abs(par(LVT))"

.PROBE SLVT = deriv("log10(i(X_my_nslvt.mm0))")
.meas swingSLVT min "1000/abs(par(SLVT))"

.PROBE RVT = deriv("log10(i(X_my_nrvt.mm0))")
.meas swingRVT min "1000/abs(par(RVT))"

.PROBE SRAM = deriv("log10(i(X_my_nsram.mm0))")
.meas swingSRAM min "1000/abs(par(SRAM))"
```

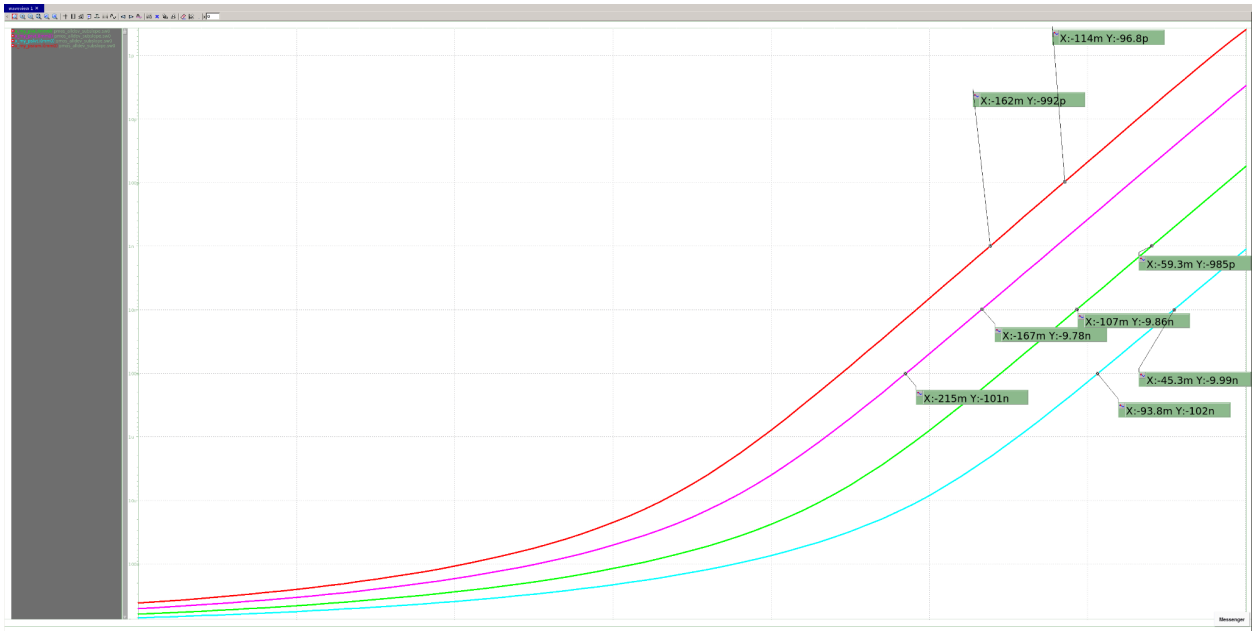
NMOS

Above measure commands are used for measuring subthreshold swing which is reciprocal of slope i.e $d\,log(I)/d\,V$ in the subthreshold region. To get slope in subthreshold region, we have to find I, V such that $d\,log(I)/d\,V$ is maximum which implies the reciprocal of that slope should be minimum. For example for LVT device, I measured variable called LVT which gives slope and then assigned

the minimum value of absolute value of its reciprocal to variable called swingLVT which is essentially subthreshold swing of LVT device in mV/decade (1000 in numerator is used to get in mV/decade).

j) (Plot separately for NMOS and PMOS) Show hand calculations using the values (x,y markings) shown on the plot for subthreshold slope values for NMOS and PMOS all devices (SLVT, LVT, RVT and SRAM) at -40.

PMOS



Device \ data points (X,Y)and slope	**point1(in Volts, Amperes)**	**point2(in Volts, Amperes)**	**swing(mV/decade)**
LVT	-107m, -9.86n	-59.3m, -985p	47.7
SLVT	-93.8m, -102n	-45.3m, -9.99n	48.5
RVT	-215m, -101n	-167m, -9.78n	48
SRAM	-162m, -992p	-114m, -96.8p	48

So, in the graph I took two points which are exactly one decade apart in the subthreshold region, so the subthreshold swing is **point2's x coordinate - point1's x coordinate** which gives in terms of mV/decade.

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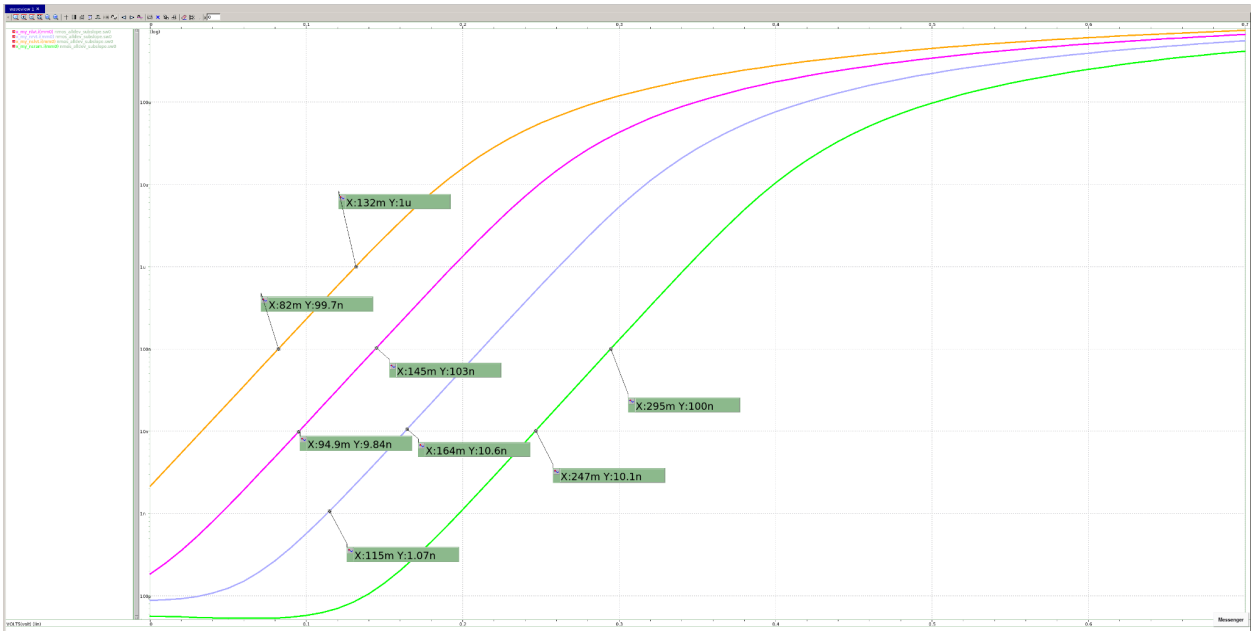
NMOS



Device \ data points (X,Y)and slope	point1(in Volts, Amperes)	point2(in Volts, Amperes)	swing(mV/decade)
LVT	94.9m, 9.84n	145m, 103n	50.1
SLVT	82m, 99.7n	132m, 1u	50
RVT	115m, 1.07n	164m, 10.6n	49
SRAM	247m, 10.1n	295m, 100n	48

k) (Table) Vt (in V) values of NMOS and PMOS all devices (SLVT, LVT, RVT and SRAM) at -40,25 and 120 degrees. (Also include a screenshot of .measure commands used for this). Show the calculations using the values shown on the plot.

```
.measure DC vthLVT when i(X_my_plvt.MM0) = "-14*533e-9"

.measure DC vthSLVT when i(X_my_pslvt.MM0) = "-14*533e-9"

.measure DC vthRVT when i(X_my_prvt.MM0) = "-14*533e-9"

.measure DC vthSRAM when i(X_my_psram.MM0) = "-14*533e-9"
```

In the above screenshot of measure commands, at each temperature, I got Vth i.e Vgs required to get current through PMOS device = -14*533e-9 (It's negative because current

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flows from source to drain in PMOS and multiplied by 14 because we have 14 fins). Also, Vth for PMOS devices is negative as reported which is expected.

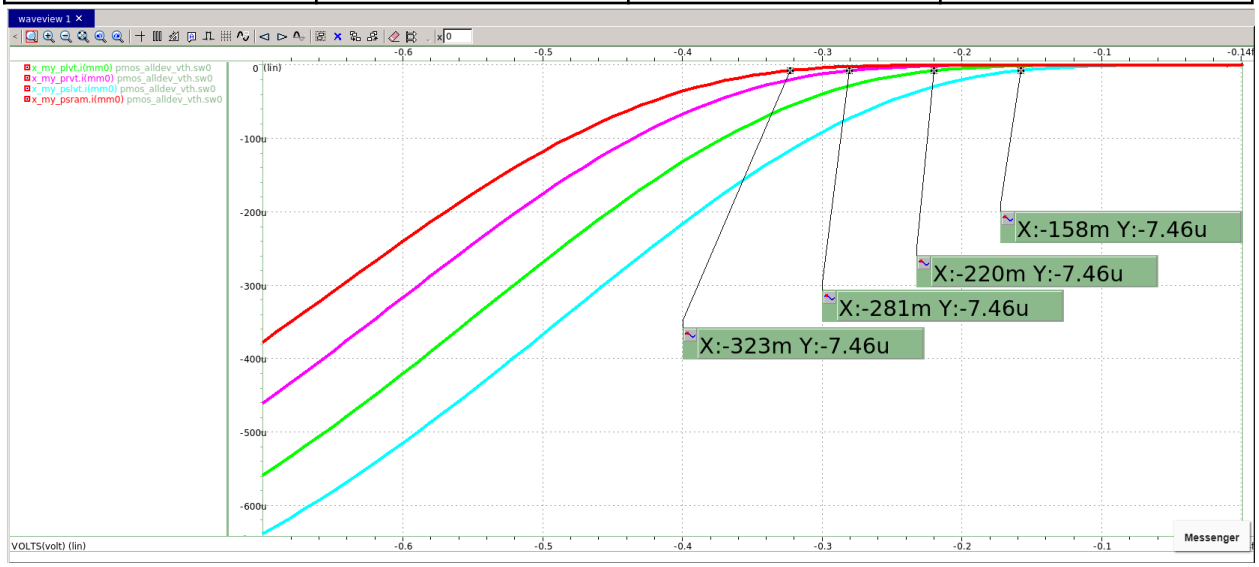
```
$DATA1 SOURCE='HSPICE' VERSION='K-2015.06-2 linux64'
.TITLE '.option accurate'
 vthlvt           vthslvt          vthrvt           vthsram
 temper           alter#
   -0.15868       -9.6253e-02        -0.22057         -0.26431
  120.00000       1
```

```
$DATA1 SOURCE='HSPICE' VERSION='K-2015.06-2 linux64'
.TITLE '.option accurate'
 vthlvt           vthslvt          vthrvt           vthsram
 temper           alter#
   -0.21999         -0.15806         -0.28084         -0.32276
   25.00000       1
```

```
$DATA1 SOURCE='HSPICE' VERSION='K-2015.06-2 linux64'
.TITLE '.option accurate'
 vthlvt           vthslvt          vthrvt           vthsram
 temper           alter#
   -0.25766         -0.19619         -0.31801         -0.35885
  -40.00000       1
```

PMOS Threshold Voltage in Volts

PMOS Device \ Temp.	-40ºC	25ºC	120ºC
LVT	-0.26	-0.22	-0.16
SLVT	-0.196	-0.16	-9.625e-02
RVT	-0.32	-0.28	-0.22
SRAM	-0.36	-0.323	-0.26



Also, plotted the points in above waveform where Ids through each device = -14*533 nA = -7.46uA and noted the X-coordinate values i.e threshold voltage values for all devices.

```
.measure DC vthLVT when i(X_my_nlvt.MM0) = "14*417e-9"
.measure DC vthSLVT when i(X_my_nslvt.MM0) = "14*417e-9"
.measure DC vthRVT when i(X_my_nrvt.MM0) = "14*417e-9"
.measure DC vthSRAM when i(X_my_nsram.MM0) = "14*417e-9"
```

In the above screenshot of measure commands, at each temperature, I got Vth i.e Vgs required to get current through NMOS device = 14*417e-9 (multiplied by 14 because we have 14 fins).

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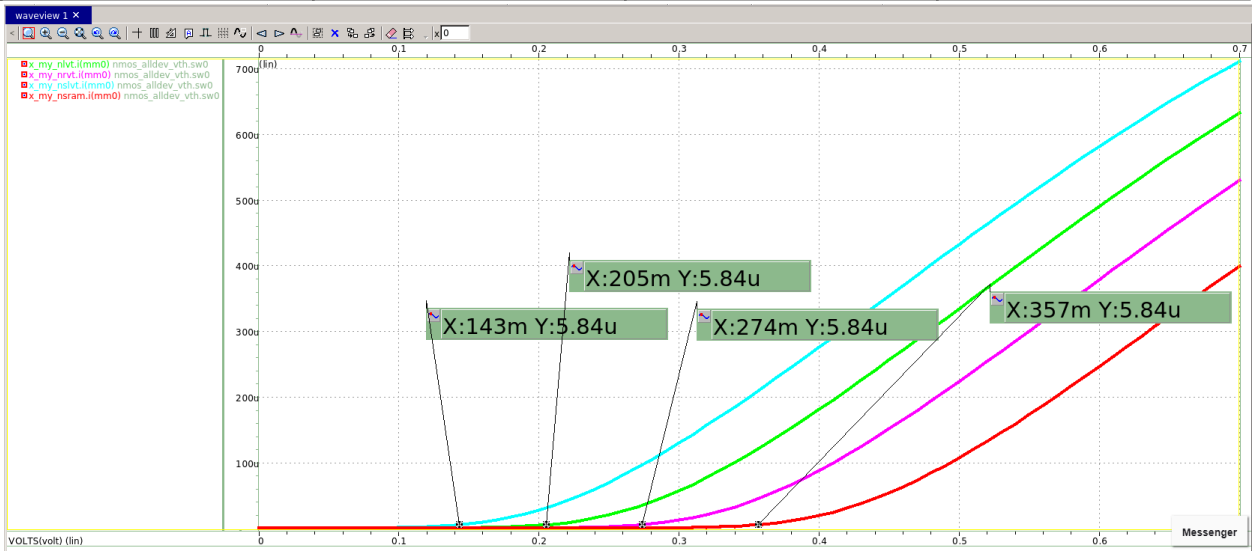
```
$DATA1 SOURCE='HSPICE' VERSION='K-2015.06-2 linux64'
.TITLE '.option accurate'
 vthlvt           vthslvt          vthrvt           vthsram
 temper           alter#
    0.23399          0.17203          0.30210          0.38387
  -40.00000       1
```

```
$DATA1 SOURCE='HSPICE' VERSION='K-2015.06-2 linux64'
.TITLE '.option accurate'
 vthlvt           vthslvt          vthrvt           vthsram
 temper           alter#
    0.20539          0.14299          0.27396          0.35667
   25.00000       1
```

```
$DATA1 SOURCE='HSPICE' VERSION='K-2015.06-2 linux64'
.TITLE '.option accurate'
 vthlvt           vthslvt          vthrvt           vthsram
 temper           alter#
    0.15997          9.6776e-02          0.22929          0.31296
  120.00000       1
```

NMOS Threshold voltage in Volts

NMOS Device \ Temp.	-40ºC	25ºC	120ºC
LVT	0.234	0.205	0.16
SLVT	0.17203	0.143	9.6776e-02
RVT	0.302	0.274	0.229
SRAM	0.3838	0.356	0.313



Also, plotted the points in above waveform where Ids through each device = 14*417 nA = 5.84uA and noted the X-coordinate values i.e threshold voltage values for all devices.

l) (Plot separate for NMOS and PMOS) Mark Vt values of NMOS and PMOS all devices (SLVT, LVT, RVT and SRAM) at 25 degrees on the plot.

So, in graphs, I took points where I observed a sudden increase in current as highlighted below in plots i.e when Ioff is changing to Ion for PMOS and NMOS devices.

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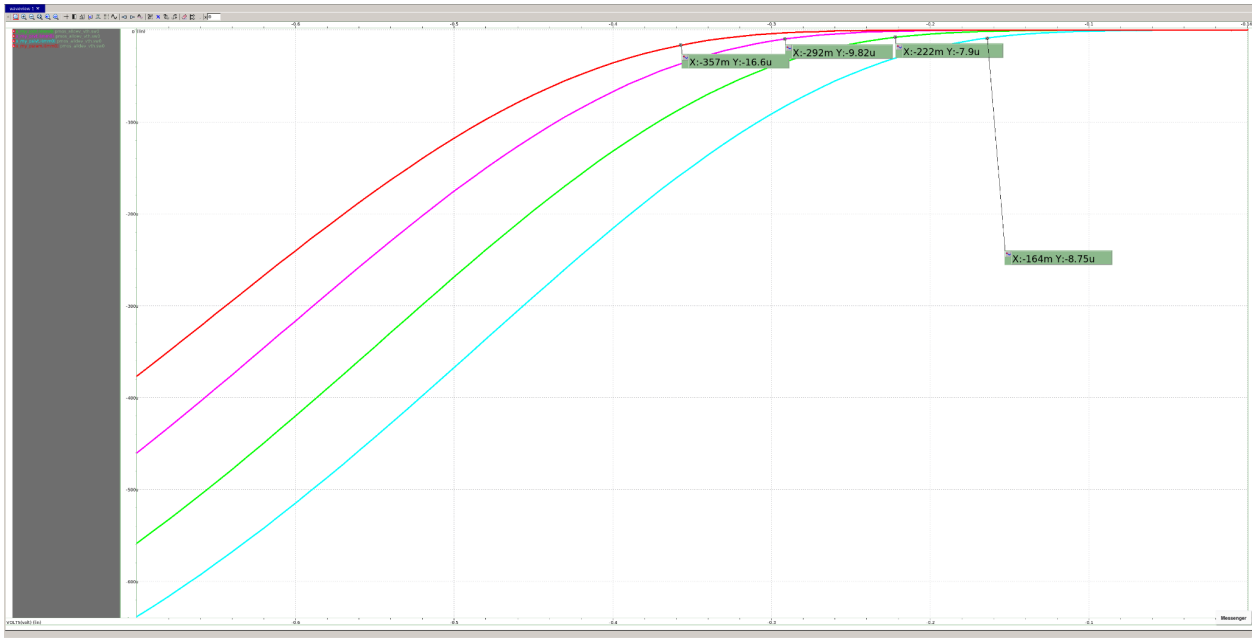
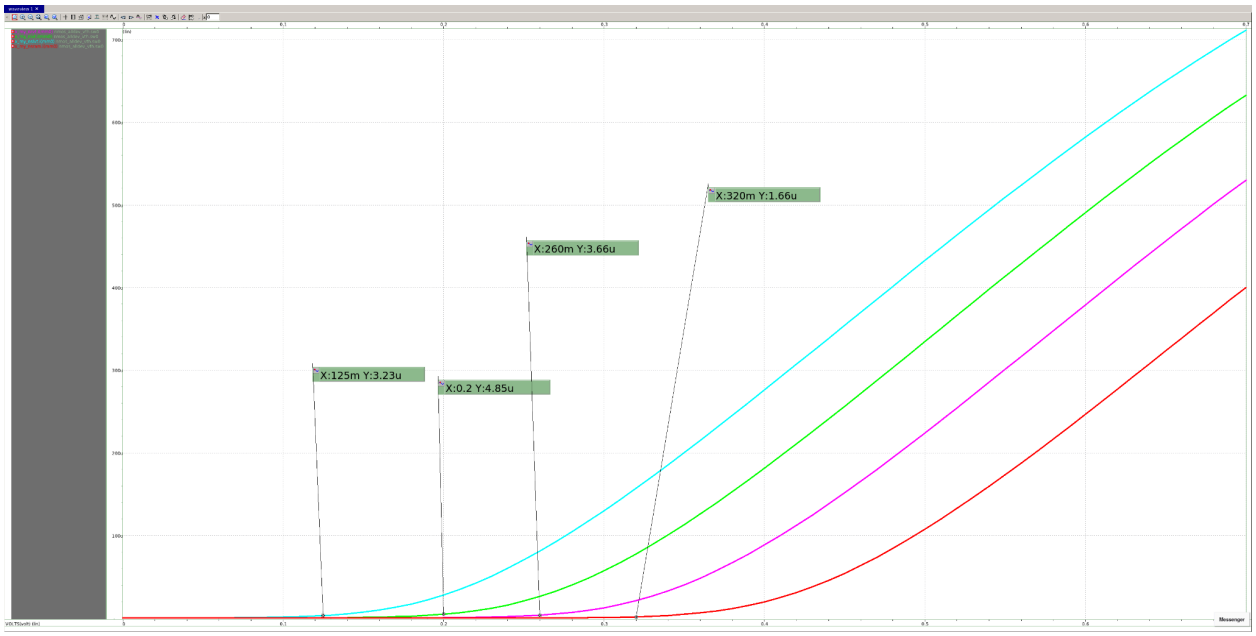


pmos Device at Temp 25	LVT	SLVT	RVT	SRAM
Vth in volts	-0.222	-0.164	-0.292	-0.357



nmos Device at Temp 25	LVT	SLVT	RVT	SRAM
Vth in volts	0.2	0.125	0.26	0.32

2.i. (plot in 1st quadrant) NMOS RVT device Ids v/s Vds at -40°, 25°, and 120° C

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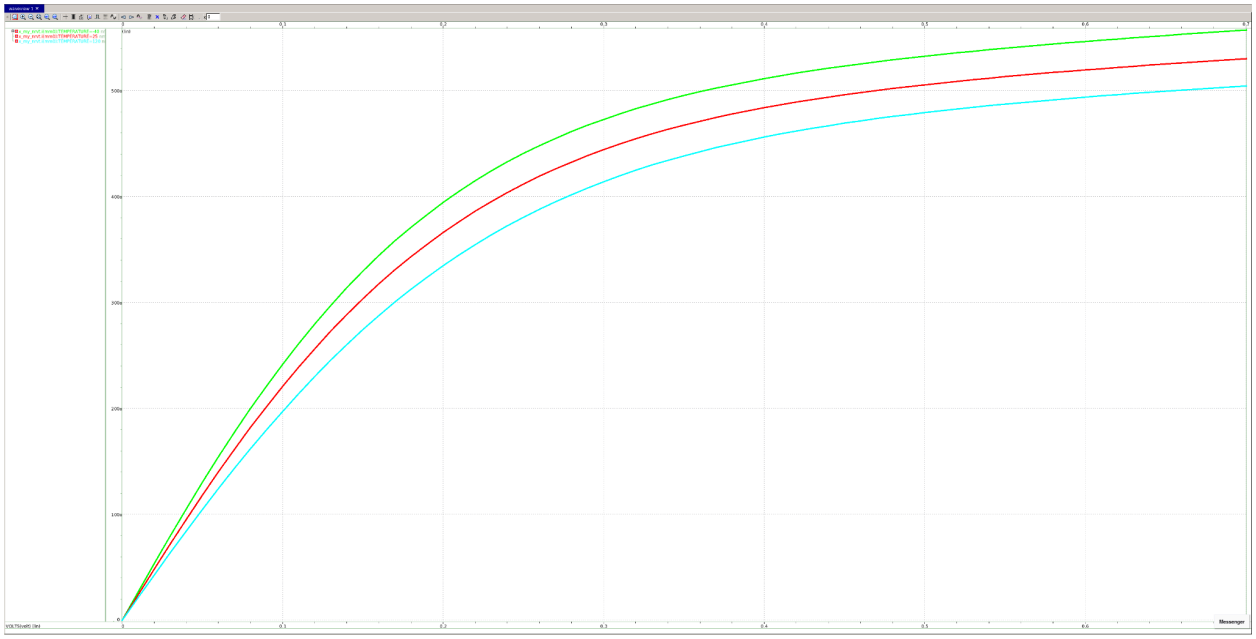
For, I need to DC sweep on VD at 3 three temperatures. Below are the commands I used.

.DC vD 0 0.7 0.01 TEMP POI 3 -40 25 120
.PROBE i(X_my_nrvt)

NMOS RVT

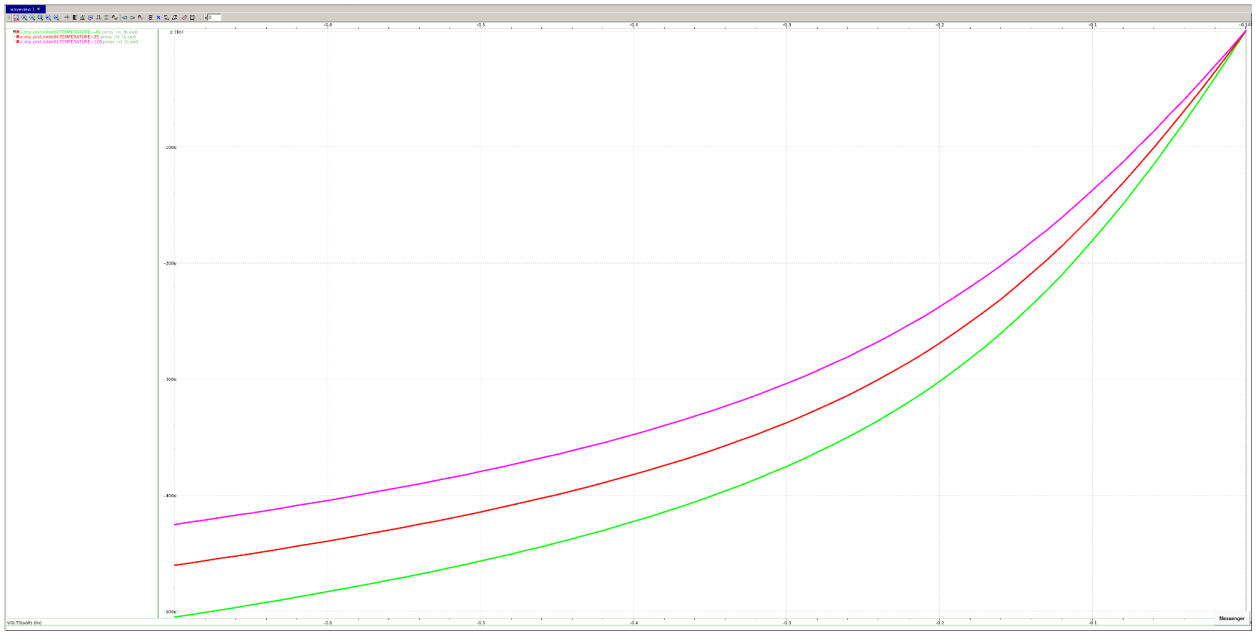


ii. (plot in 3rd quadrant) PMOS RVT device Ids v/s Vds at -40º, 25º, and 120º C

For, I need to DC sweep on Vds at 3 three temperatures. Below are the commands I used.

.DC Vds -0.7 0 0.01 TEMP POI 3 -40 25 120
.PROBE i(X_my_prvt)

PMOS RVT



(b) i. (plot in 1st quadrant) NMOS RVT device Ids v/s Vds at 25º Celsius with Ih and Il curves

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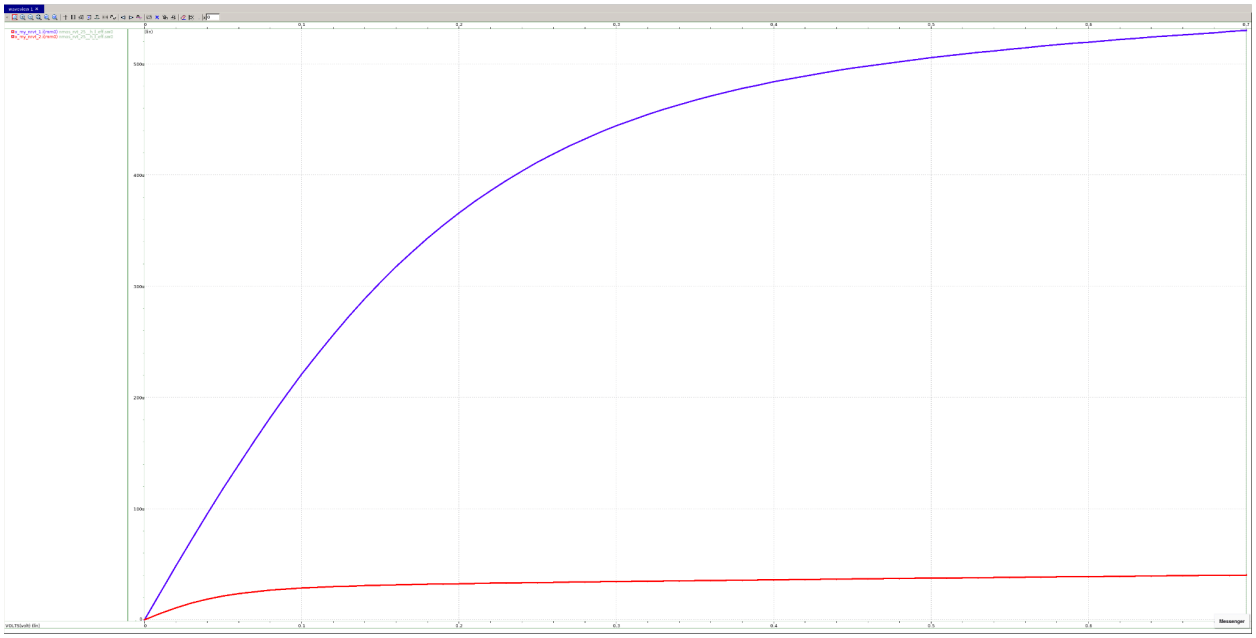

ii. (Table) Il,Ih, Ieff of NMOS RVT device at 25° Celsius (Also include screenshot of .measure commands a screenshot of outputs from your MS0 file). Provide a brief explanation.

```
.include "./nmos_rvt.sp"
.TEMP 25
.option

.param Vgnd=0
.param Vvdd= 0.7
X_my_nrvt_1 d g1 s nrvt
X_my_nrvt_2 d g2 s nrvt

vS s 0 dc=Vgnd
vD d 0 dc=Vgnd
Vgs1 g1 s dc=0.7
Vgs2 g2 s dc=0.35

.DC vD 0 0.7 0.01

.measure DC Ih find i(X_my_nrvt_1.MM0) when v(d) = "0.35"
.measure DC Il find i(X_my_nrvt_2.MM0) when v(d) = "0.7"
.measure Ieff param = "0.5*(Il+Ih)"
```

So, For this problem, I instantiated the NMOS RVT device twice as X_my_nrvt_1 and X_my_nrvt_2. For X_my_nrvt_1, Vgs is 0.7 V and measured current in it when Vds = Vd = 0.35 which implies that current is Ih as shown in the measure command above. For X_my_nrvt_2, Vgs is 0.35 V and measured current in it when Vds = Vd = 0.7 which implies that current is Il as shown in the measure command above. Then Ieff is the average of Ih and Il and measured that.

```
$DATA1 SOURCE='HSPICE' VERSION='K-2015.06-2 linux64'
.TITLE '.option accurate'
 ih               il               ieff             temper
 alter#
  4.6726e-04       4.0308e-05       2.5379e-04         25.00000
 1
```

Ih (in amperes)	Il (in amperes)	Ieff (in amperes)
4.6726e-04	**4.0308e-05**	**2.5379e-04**

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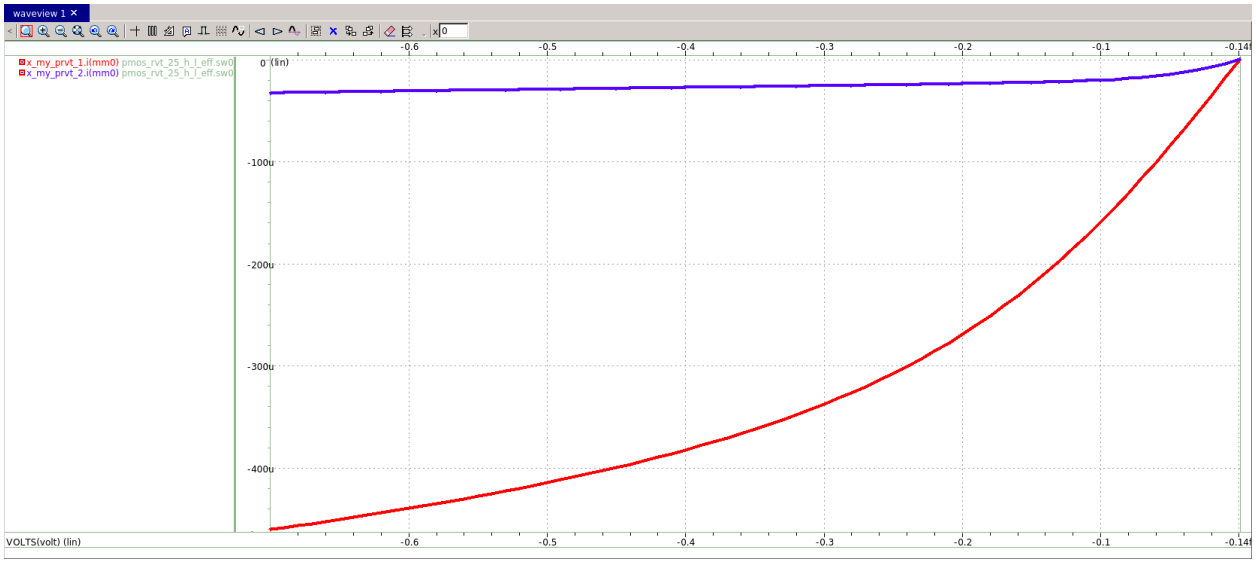
iii. (plot in 3rd quadrant) PMOS RVT device Ids v/s Vds at 25°Celsius with Ih and Il curves



iv. (Table) Il,Ih, leff of PMOS RVT device at 25°Celsius (Also include screenshot of .measure commands and screenshot of outputs from your MS0 file). Provide a brief explanation.

```
.include "./pmos_rvt.sp"
.TEMP 25
.option

.param Vgnd=0
.param Vvdd= 0.7
X_my_prvt_1 d g1 s prvt
X_my_prvt_2 d g2 s prvt

vS s 0 dc=Vvdd
Vds d s dc=Vgnd
Vsg1 s g1 dc=0.7
Vsg2 s g2 dc=0.35

.DC Vds -0.7 0 0.01

.measure DC Ih find i(X_my_prvt_1.MM0) when v(d) = "0.35"
.measure DC Il find i(X_my_prvt_2.MM0) when v(d) = "0"
.measure Ieff param = "0.5*(Il+Ih)"
```

So, For this problem, I instantiated the PMOS RVT device twice as X_my_prvt_1 and X_my_prvt_2. For X_my_prvt_1, Vsg is 0.7 V and measured current in it when Vds = -0.35 => Vd = 0.35 which implies that current is Ih as shown in the measure command above. For X_my_prvt_2, Vsg is 0.35 V and measured current in it when Vds = -0.7 => Vd = 0 which implies that current is Il as shown in the measure command above. Then Ieff is the average of Ih and Il and measured that.

```
$DATA1 SOURCE='HSPICE' VERSION='K-2015.06-2 linux64'
.TITLE '.option accurate'
 ih              il              ieff            temper
 alter#
 -3.6187e-04     -3.2484e-05     -1.9718e-04       25.00000
 1
```

Ih (in amperes)	Il (in amperes)	Ieff (in amperes)
-3.6187e-04	-3.2484e-05	-1.9718e-04