Experiment-4

Simulation of VHDL Models:

Tittle: Design a binary to gray code converter circuit in VHDL.

Objective: To design a binary to gray code converter and verify it using ISE simulator.

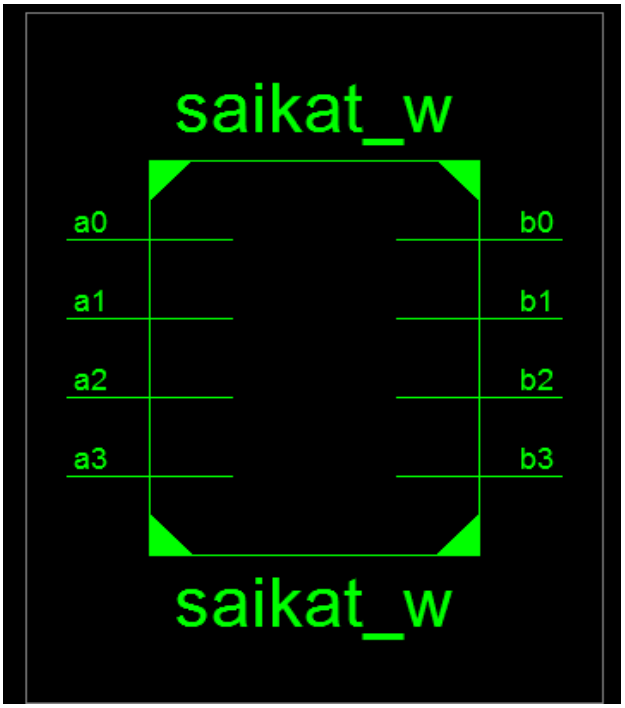
Theory: Gray code system is a binary number system in which every successful pair of numbers differs in only one bit. It is used in application in which the normal sequence of binary numbers generated by the hardware may produce an error or ambiguity during the transition from one number to next. For example, the states of a system my change from 3(011) to 4(100) as -011-001-101-100. Therefore, there is a high chance of a wrong state being read while the system changes from the initial state to the final state.

This could have serious consequences for the machine using the information. The gray code eliminates this problem since only bit changes its value during any transition between two numbers.

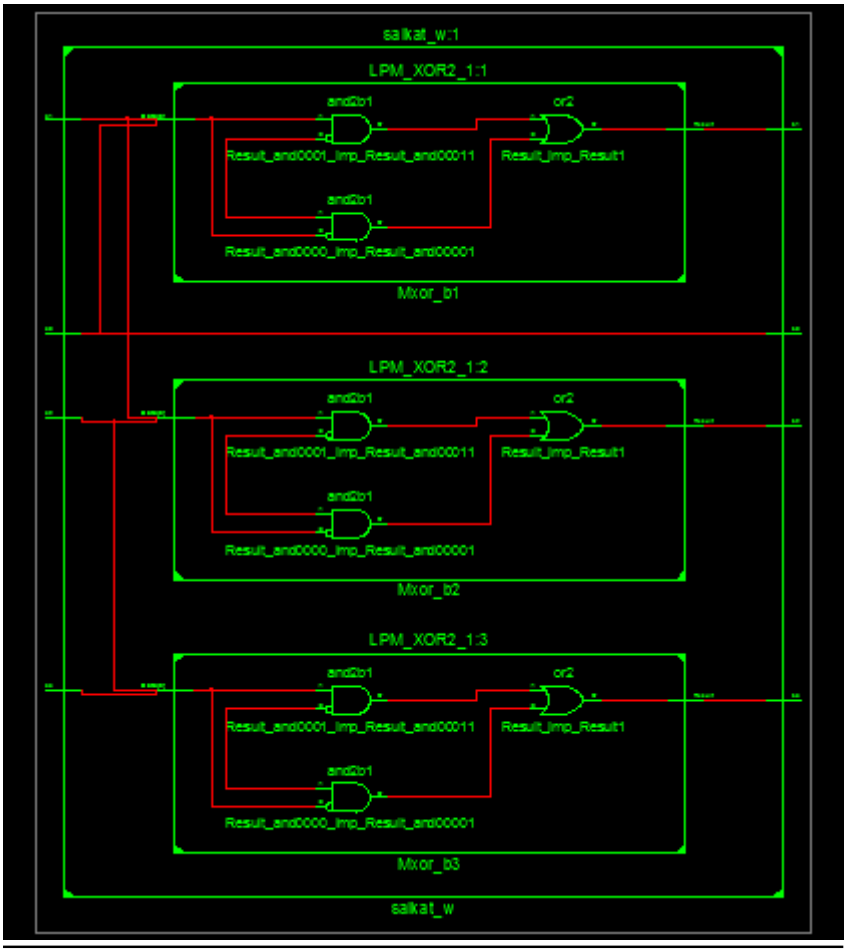
Code:

```
library IEEE;
 use IEEE.STD_LOGIC_1164.ALL;
entity saikat_w is
    Port ( a0 : in  STD_LOGIC;
           a1 : in  STD_LOGIC;
           a2 : in  STD_LOGIC;
           a3 : in  STD_LOGIC;
           b0 : out  STD_LOGIC;
           b1 : out  STD_LOGIC;
           b2 : out  STD_LOGIC;
           b3 : out  STD_LOGIC);
end saikat_w;
architecture Behavioral of saikat_w is
begin
b0 <= a0;
b1 <= a0 XOR a1;
b2 <= a1 XOR a2;
b3 <= a2 XOR a3;
end Behavioral;
```

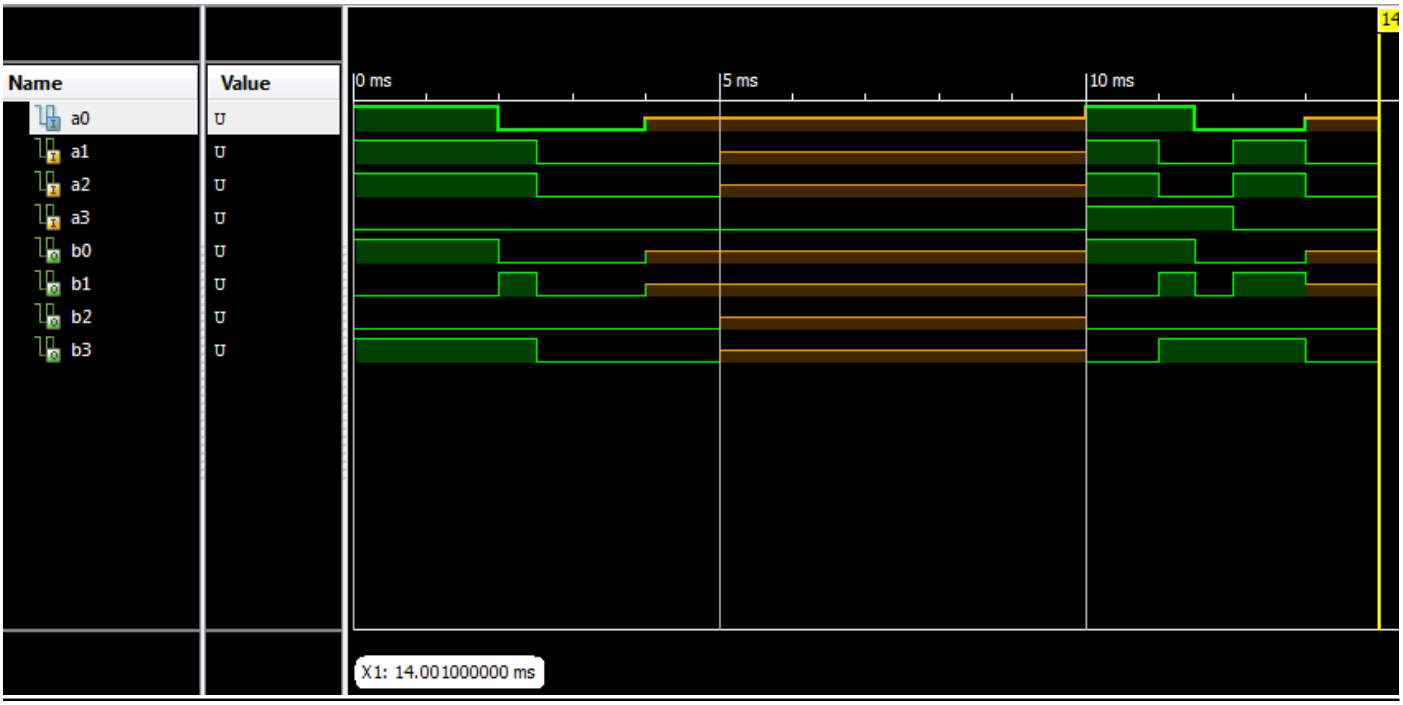
Entity Diagram:



Detailed Entity Diagram:



Output:



Result:

We have designed a binary to gray code converter circuit in VHDL and verified it by their truth table using the output wave-diagram.

Conclusion:

Thus, this is all about binary to gray code converter. From the above information finally, we can conclude that these converters play an essential role in performing different operations of digital electronics as well as communications among various number system.

Experiment-5

Simulation of VHDL Models:

Tittle: Design and simulate a 4:1 MUX in VHDL using variable.

Objective: To design and simulate a 4:1 MUX in VHDL using variable verify it using ISE simulator.

Theory: It is a combinational circuit which have many data inputs and single output depending on control or select inputs.

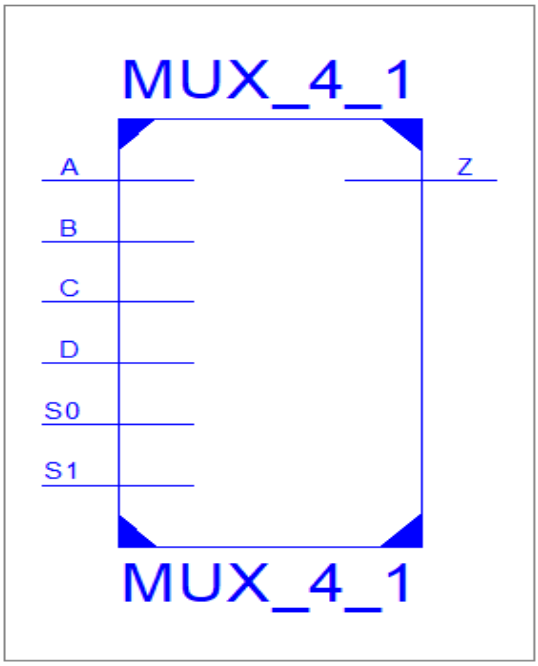
For N input lines, log n(base2) selection lines, or we can say that for 2^n input lines, n selection lines are required. Multiplexers are also known as “DATA n selector, parallel to series converter, many to one circuit, universal logic circuit”. Multiplexers are mainly used to increase amount of the data that can be sent over the network within certain amount of time and bandwidth.

Code:

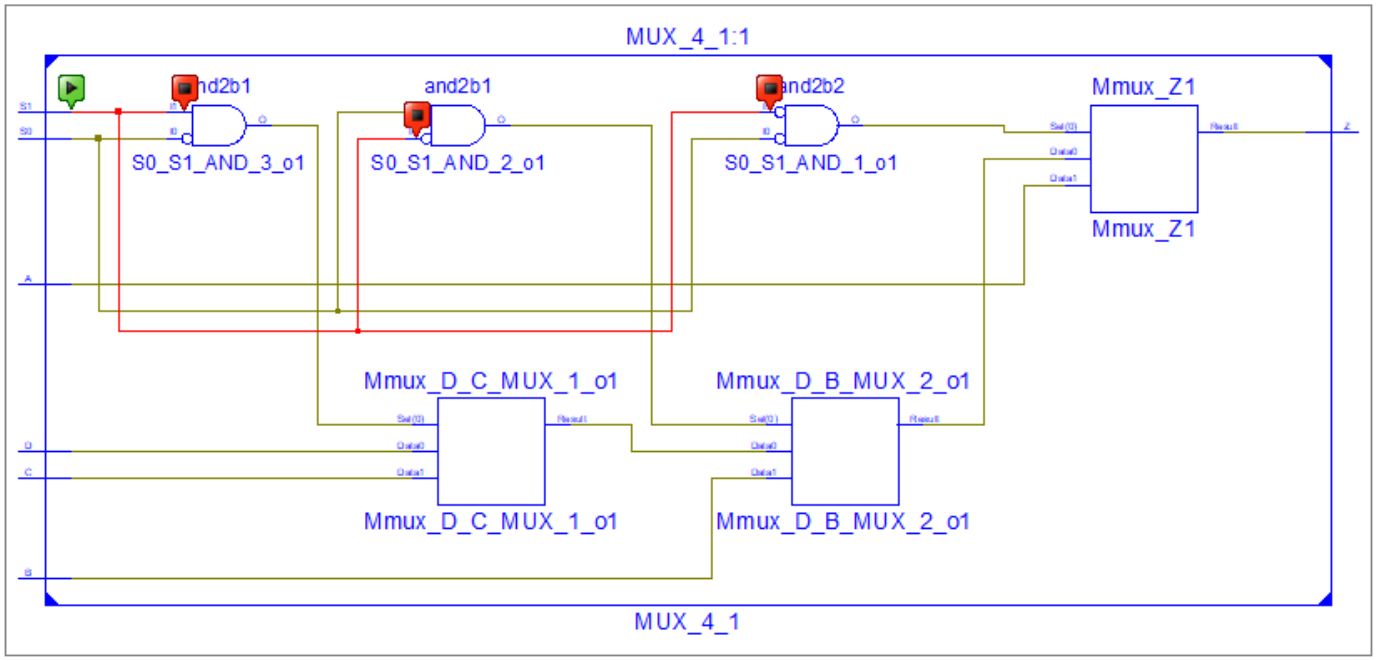
```
library IEEE;
use IEEE.STD_LOGIC_1164.all;
entity MUX_4_1 is
 port(
    A,B,C,D : in STD_LOGIC;
    S0,S1: in STD_LOGIC;
    Z: out STD_LOGIC
 );
end MUX_4_1;
architecture bhv of MUX_4_1 is
begin
process (A,B,C,D,S0,S1) is
variable Y: STD_LOGIC;
begin
  if (S0 ='0' and S1 = '0') then
     Y := A;
  elsif (S0 ='1' and S1 = '0') then
     Y := B;
  elsif (S0 ='0' and S1 = '1') then
     Y := C;
```

```
 else
    Y := D;
 end if;
Z <= Y;
end process;
end bhv;
```

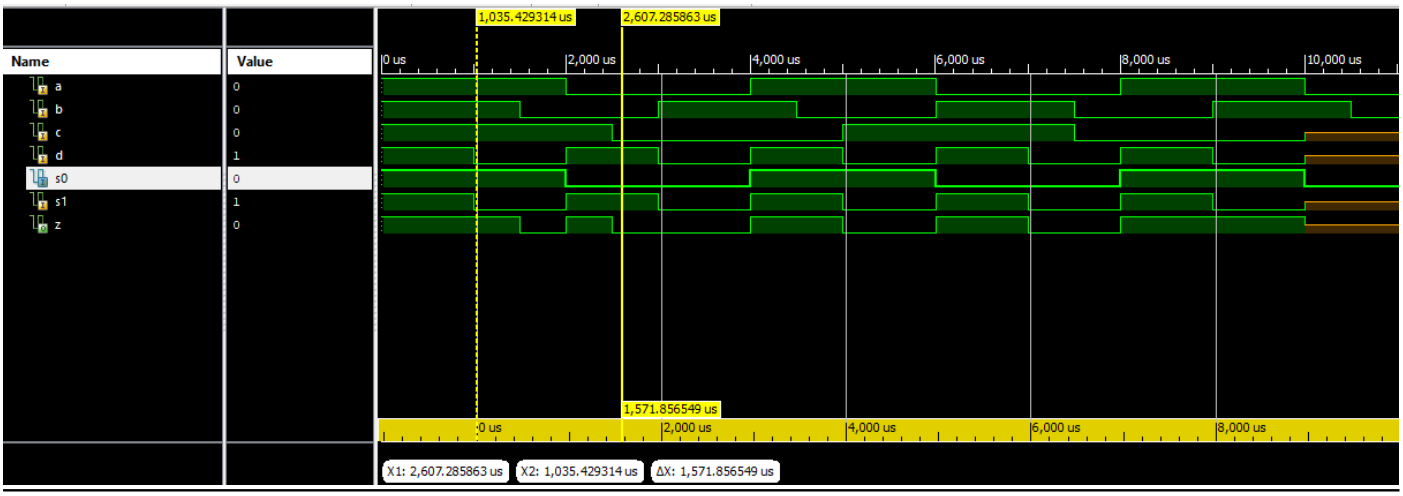
Entity Diagram:



Detailed Entity Diagram:



Output:



Result:

We have designed 4:1 MUX in VHDL using variable and verified it by their truth table using the output wave-diagram.

Conclusion:

In this experiment a 4:1 MUX has been designed, simulated and analyzed. We have learned how to design 4:1 multiplexer circuit in VHDL using variable and we have verified it by their truth table.