# Experiment-3

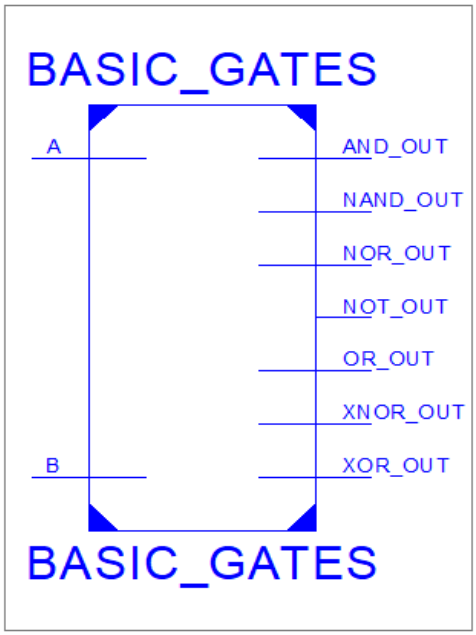
Question: Verify the Truth table of all the basic logic gates using VHDL.

## Code:

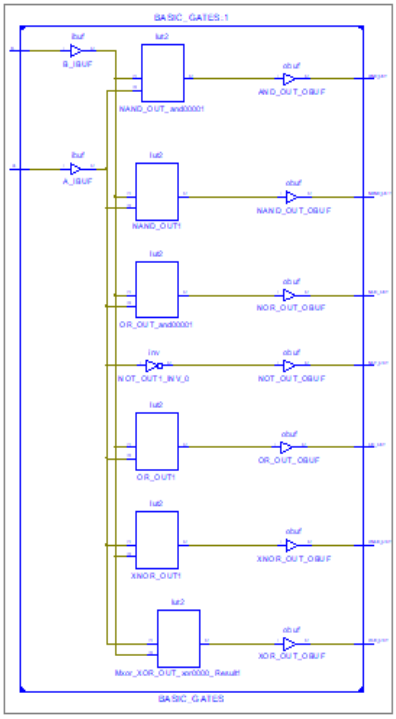
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity BASIC_GATES is
   Port ( A : in  STD_LOGIC;
          B : in  STD_LOGIC;
          AND_OUT : out  STD_LOGIC;
          OR_OUT : out  STD_LOGIC;
          NOT_OUT : out  STD_LOGIC;
          NAND_OUT : out  STD_LOGIC;
                                NOR_OUT : out  STD_LOGIC;
          XOR_OUT : out  STD_LOGIC;
                                XNOR_OUT: out STD_LOGIC);
end BASIC_GATES;

architecture Behavioral of BASIC_GATES is

begin

            process(A,B)
                        begin
                        if((A = '1') AND (B = '1')) THEN
                                    AND_OUT <= '1';
                        else
                                    AND_OUT <= '0';
                        end if;
                        if((A = '0') AND (B = '0')) THEN
                                    OR_OUT <= '0';
                        else
                                    OR_OUT <= '1';
                        end if;
                                    if((A = '0') AND (B = '0')) THEN
                                    NOR_OUT<= '1';
                        else
                                    NOR_OUT <= '0';
                        end if;

                        if(A = '1') THEN
```

```
                NOT_OUT <= '0';
        else
                NOT_OUT <= '1';
        end if;
        if((A = '1') AND (B = '1')) THEN
                NAND_OUT <= '0';
        else
                NAND_OUT <= '1';
        end if;
        if((A /= B)) THEN
                XOR_OUT <= '1';
        else
                XOR_OUT <= '0';
        end if;

        if((A /= B)) THEN
                XNOR_OUT <= '0';
        else
                XNOR_OUT <= '1';
        end if;
    end process;
end Behavioral;
```

Entity Diagram



Detailed Entity Diagram



## *Output:*