Experiment-8

Title: Implementation of a 4:1 MUX from 2:1 MUX.

Objective: To implement a 4:1 MUX using 2:1 MUX in VHDL using structural modelling.

Theory:

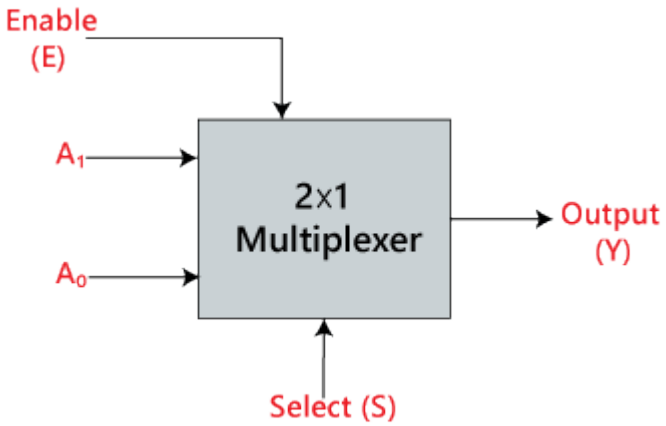
Multiplexer:

In electronics,a **multiplexer** (or **mux**; spelled sometimes as **multiplexor**), also known as a **data selector**, is a device that selects between several analog or digital input signals and forwards the selected input to a single output line. The selection is directed by a separate set of digital inputs known as select lines. A multiplexer of **2^n** inputs has **n** select lines, which are used to select which input line to send to the output.

2:1 Multiplexer:

In a 2:1 multiplexer, there are only two inputs, i.e., A_0 and A_1, 1 selection line, i.e., S_0 and single outputs, i.e., Y. On the basis of the combination of inputs which are present at the selection line S^0, one of these 2 inputs will be connected to the output. The block diagram and the truth table of the 2×1 multiplexer are given below.

Block Diagram:



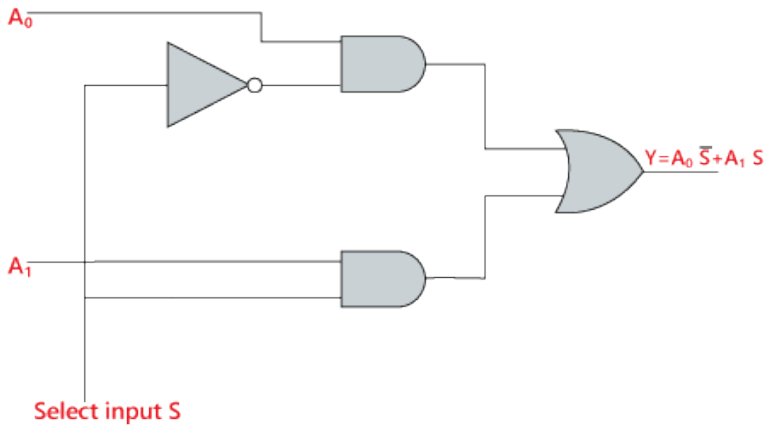
Truth Table:

INPUTS	Output
S_0	Y
0	A_0
1	A_1

The logical expression of the term Y is as follows:

$Y=S_0'.A_0+S_0.A_1$

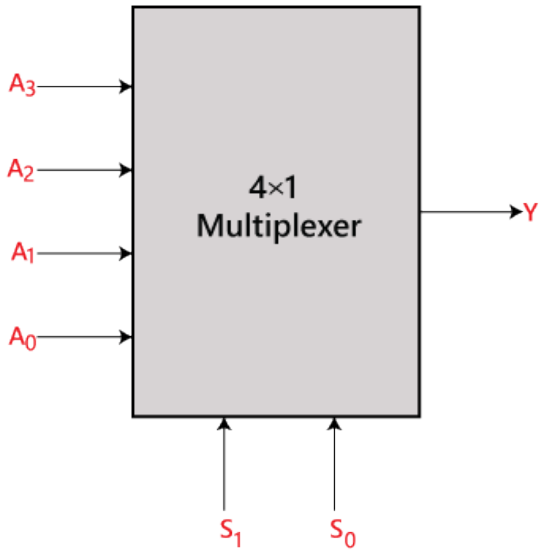
Logical circuit of the above expression is given below:



4×1 Multiplexer:

In the 4×1 multiplexer, there are a total of four inputs, i.e., A_0, A_1, A_2, and A_3, 2 selection lines, i.e., S_0 and S_1 and single output, i.e., Y. On the basis of the combination of inputs that are present at the selection lines S^0 and S_1, one of these 4 inputs are connected to the output. The block diagram and the truth table of the 4×1 multiplexer are given below.

Block Diagram:



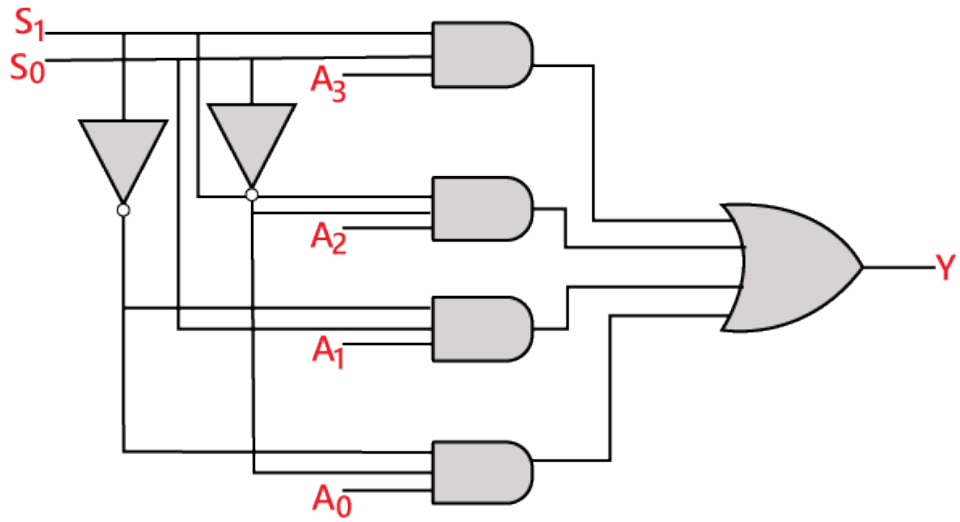
Truth Table:

INPUTS		Output
S_1	S_0	Y
0	0	A_0
0	1	A_1
1	0	A_2
1	1	A_3

The logical expression of the term Y is as follows:

$Y=S_1' S_0' A_0+S_1' S_0 A_1+S_1 S_0' A_2+S_1 S_0 A_3$

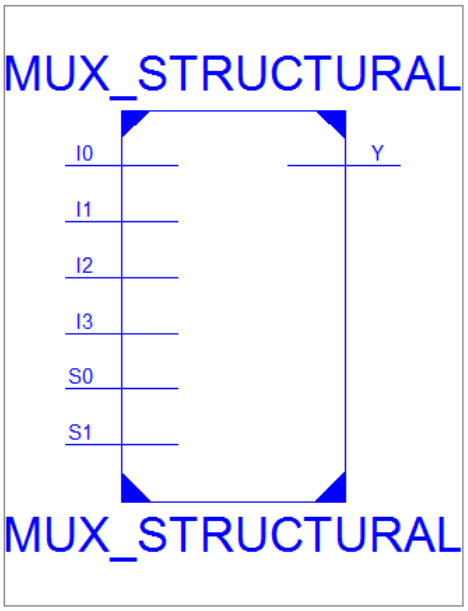
Logical circuit of the above expression is given below:



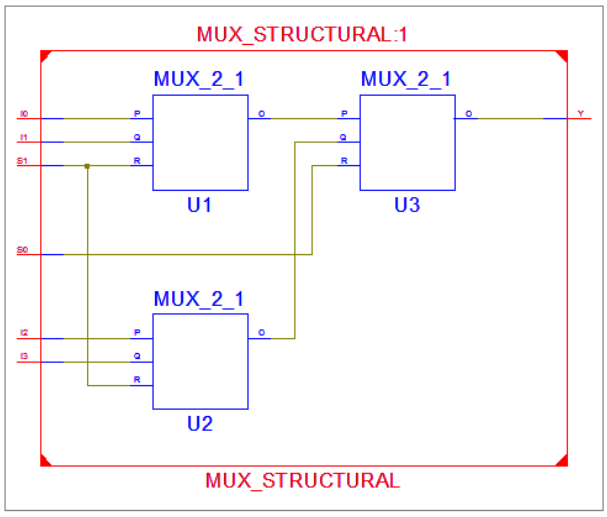
Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity MUX_4_1 is
    Port ( D0 : in  STD_LOGIC;
           D1 : in  STD_LOGIC;
           D2 : in  STD_LOGIC;
           D3 : in  STD_LOGIC;
           S0 : in  STD_LOGIC;
           S1 : in  STD_LOGIC;
           Y : out  STD_LOGIC);
end MUX_4_1;

architecture Structural of MUX_4_1 is
Component MUX_2_1 is
        Port(P, Q, R : in STD_LOGIC;
                       O : out STD_LOGIC);
end Component;

Signal P1,P2 : STD_LOGIC;

begin

        N1 : MUX_2_1 PORT MAP(D0,D1,S1,P1);
        N2 : MUX_2_1 PORT MAP(D2,D3,S1,P2);
        N3 : MUX_2_1 PORT MAP(P1,P2,S0,Y);

end structural;
```

Entity Diagram:



RTL Schematic:



Result:

We have implemented a 4:1 Multiplexer from 2:1 multiplexers in VHDL structural modelling, and the Entity Diagram and the RTL schematic are shown above.

Conclusion:

In this experiment, we learnt about structural modelling in VHDL and used it to implement a 4:1 Multiplexer.