Experiment -12

Tittle: Implementation of T – Flip Flop circuit in Behavioural Modelling.

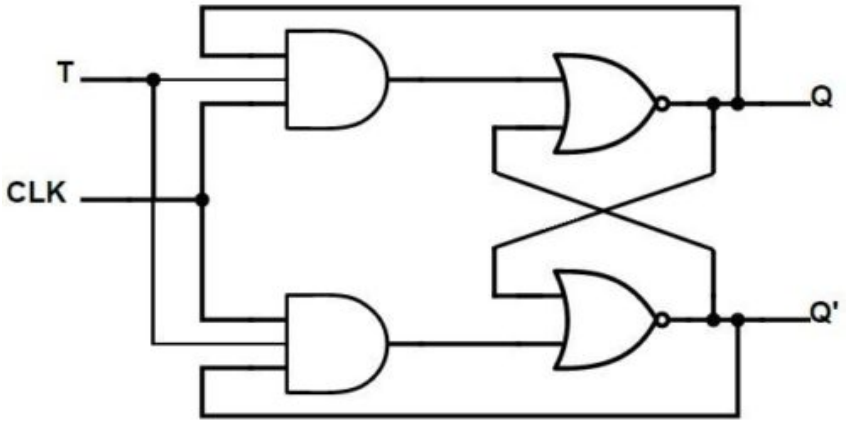
Objective: To understand the working of the T – Flip Flop circuit.

Theory: A T Flip-Flop is like a JK Flip-Flop. These are basically a single input version of JK Flip-Flops. This is modified form of JK Flip-Flop is obtained by connecting both inputs J and K together. It has only one input along with the clock input.

Truth Table:

T	Q	Q(t+1)
0	0	0
1	0	1
0	1	1
1	1	0

Circuit Diagram:

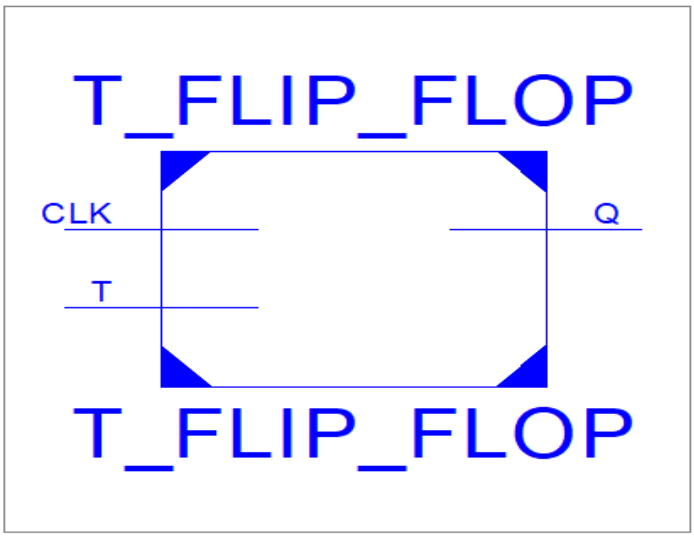


Code:

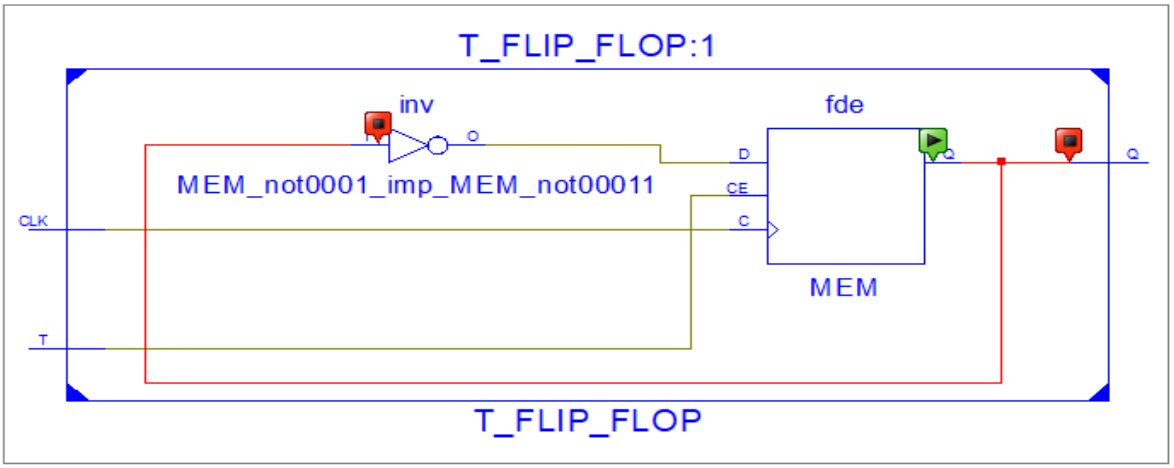
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity T_FLIP_FLOP is
 Port(T: In STD_LOGIC;
                CLK: In STD_LOGIC;
                Q: Out STD_LOGIC);
end T_FLIP_FLOP;
```

```
architecture Behavioral of T_FLIP_FLOP is
begin
process(CLK, T) is
        variable MEM: STD_LOGIC := '0';
        begin
        if(CLK = '1' and CLK'EVENT)then
                if(T = '1')then
                        MEM := NOT(MEM);
                end if;
        end if;
        Q <= MEM;
        end process;
end Behavioral;
```

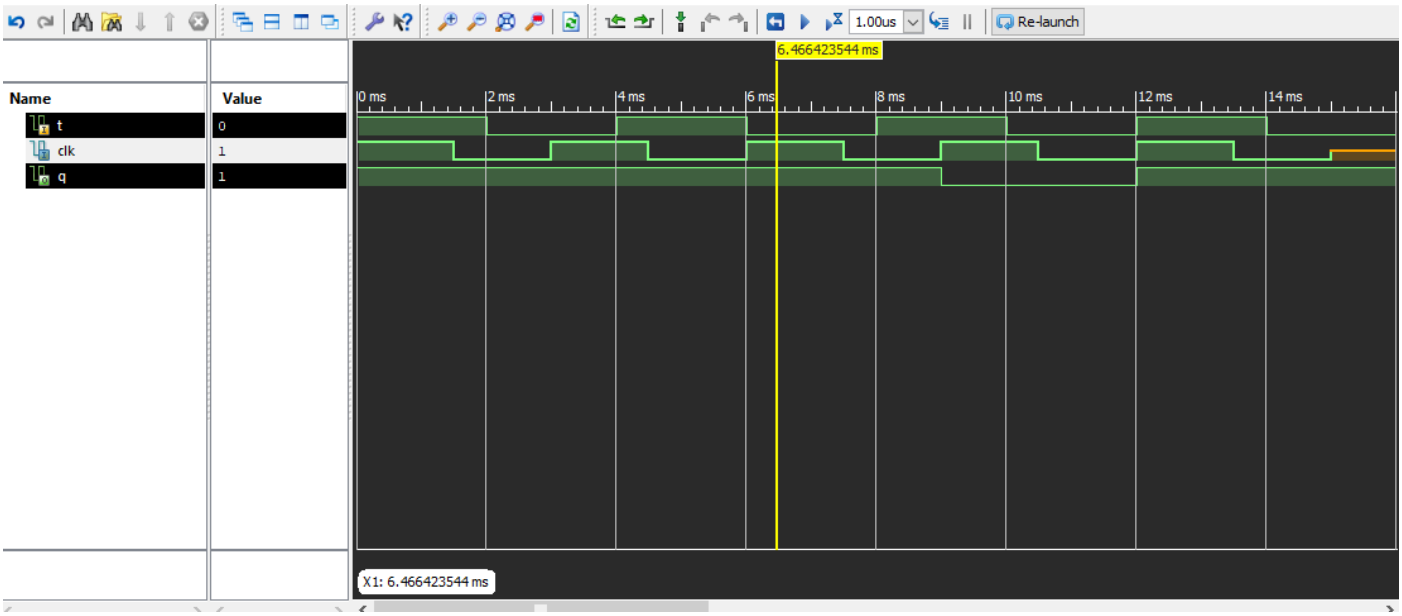
Entity Diagram:



RTL Schematic:



Output:



Result: We have implemented a T Flip-Flop circuit in Behavioural modelling using case statement , and the RTL Schematic and the Simulation Waveform are shown above.

Conclusion:

In this experiment , we learnt about case statement in VHDL and used it to implement a T Flip-Flop circuit.