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Year -> 2020-2024.

EXPERIMENT NO. – **6(A)**	TITLE ***CONSTRUCTION OF A SIMPLE ARITHMETIC CIRCUITS CIRCUIT - ADDER***	DATE OF EXPERIMENT

OBJECTIVE: *A) TO CONSTRUCT A HALF ADDER AND VERIFY ITS TRUTH TABLE.*
B) TO CONSTRUCT FULL ADDER USING TWO HALF ADDER AND VERIFY ITS TRUTH TABLE.

THEORY:

In electronics, an adder or summer is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic units, but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar operations.

Although adders can be constructed for many numerical representations, such as binary-coded decimal or excess-3, the most common adders operate on binary numbers. Other signed number representations require a more complex adder.

HALF ADDER:

The half adder adds two input bits and generates a carry and sum, which are the two outputs of a half adder. The input variables of a half adder are called the augend and addend bits. The output variables are the sum and carry.

The Truth Table for the half adder is:

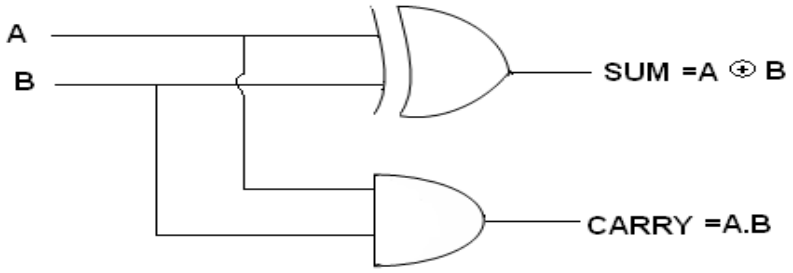
A	B	SUM	CARRY

0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Applying SOP for SUM and CARRY, we get the equations

SUM= A B' + A' B (*Logic o/p of EX-OR Gate*)
CARRY=A.B (*Logic o/p of AND Gate*)

So the logic diagram will be construct with the help of EX-OR Gate and AND Gate.



Logic diagram Of half adder

FULL ADDER:

*A **full adder** adds binary numbers and accounts for values carried in as well as out. A one-bit full adder adds three one-bit numbers, often written as A, B, and C_{in}; A and B are the operands, and C_{in} is a bit carried in from the previous less significant stage. The full adder is usually a component in a cascade of adders, which add 8, 16, 32, etc. bit binary numbers. A full adder can be implemented in many different ways such as with a custom transistor-level circuit or composed of other gates.*

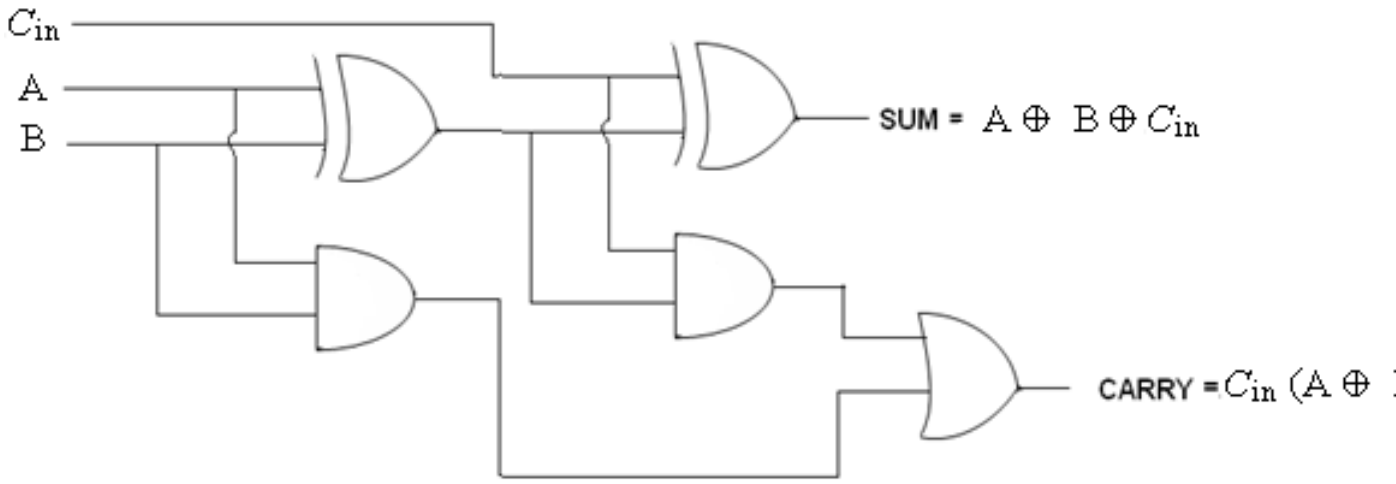
The circuit produces a two-bit output, output carry and sum typically represented by the signals C_{out} and S.

The Truth Table for the Full Adder is:

A	B	C_{in}	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1

1	1	1	1	1

So the logic diagram will be construct with the help of two Half Adder (EX-OR Gate, AND Gate and OR Gate).



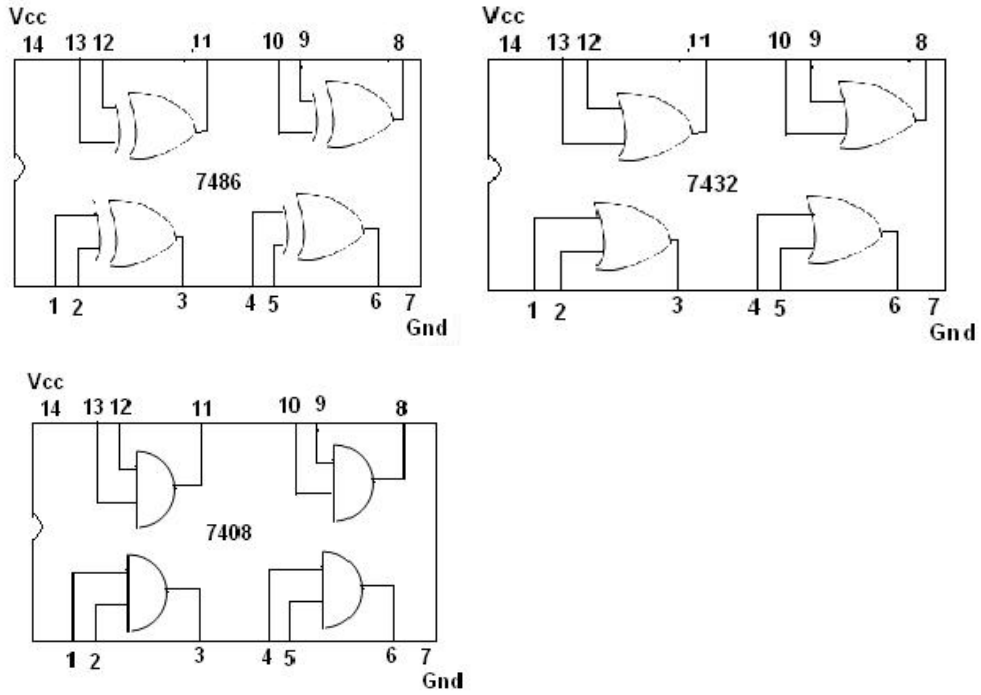
Logic diagram of full adder

APPARATUS REQUIRED:

SL NO	COMPONENTS / **EQUIPMENTS**	SPECIFICATION	**QUANTITY**
1	*Digital trainer kit*	*ST-2614*	1
2	*Quad 2-Input EXOR gate IC*	*74LS86*	1
3	*Quad 2-Input OR gate IC*	*74LS32*	1
4	*Quad 2-Input AND gate IC*	*74LS08*	1
5	*Patch cord*	-	-
6	*Bread Board*	-	1

EXPERIMENTAL PROCEDURE:

- *Do the connections as per the circuit diagram and follow the pin configarations of used ICs on breadboard, using connecting wires.*



Pin configuratio of used ICs 74LS86,74LS32,74LS08

PRECAUTIONS:

- *Connections of Circuits should be neat & clean, tight & compect.*
- *Avoid more connecting wires or patch cords.*
- *Never provide more than +5v to Vcc pin (No:14) of the Logic ICs.*

OBSERVATION TABLE FOR HALF ADDER:

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

OBSERVATION TABLE FOR FULL ADDER:

A	B	C_{in}	SUM	CARRY
0	0	0	0	0
0	0	1	1	0

0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Conclusion : So, from the above discussion, we can conclude that a half adder and full adder both performs the addition of the applied input bits. But half adder is used in a used in a lower degree of addition operations while full adder is used for a somewhat higher degree of addition operations.