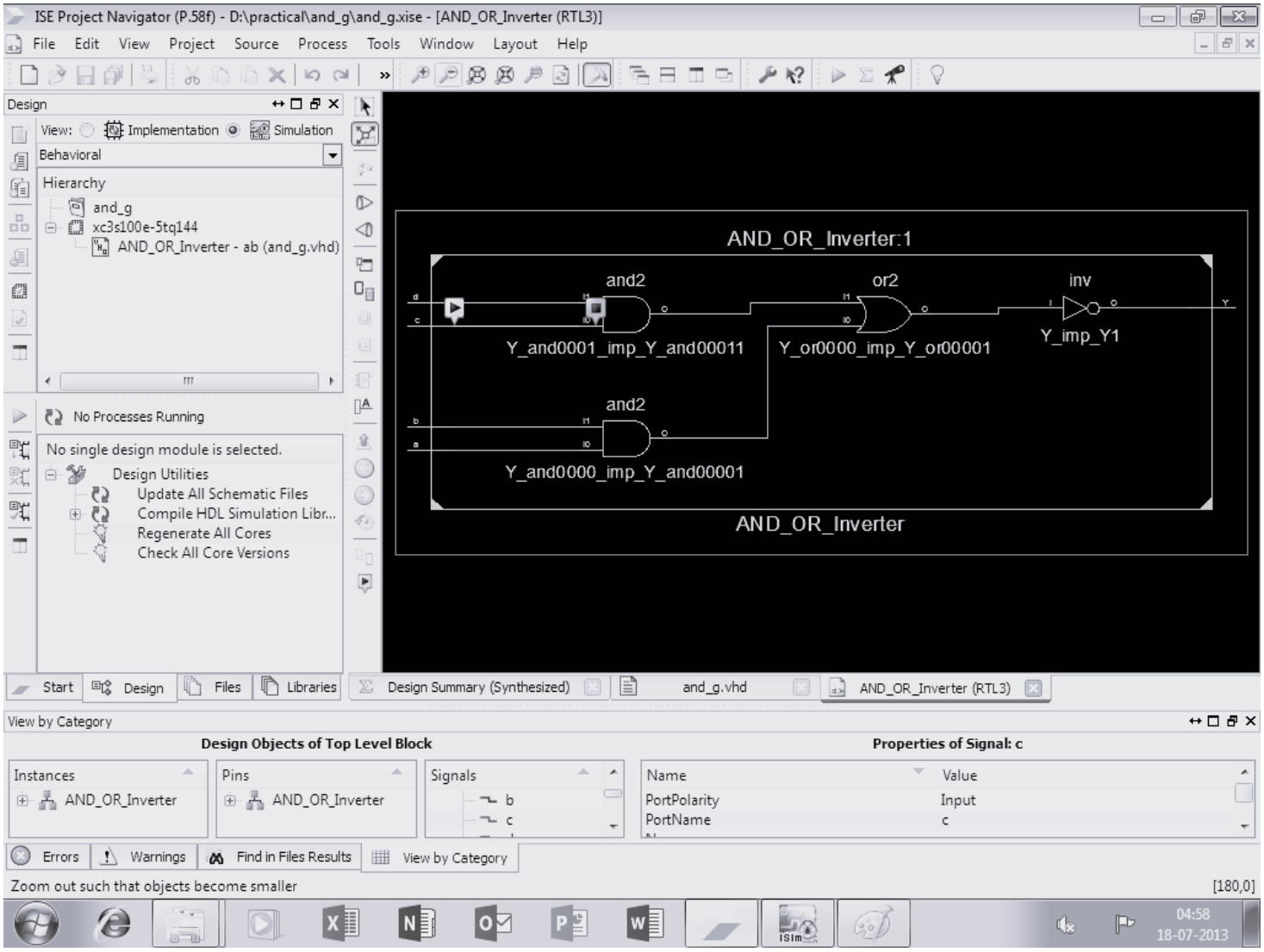
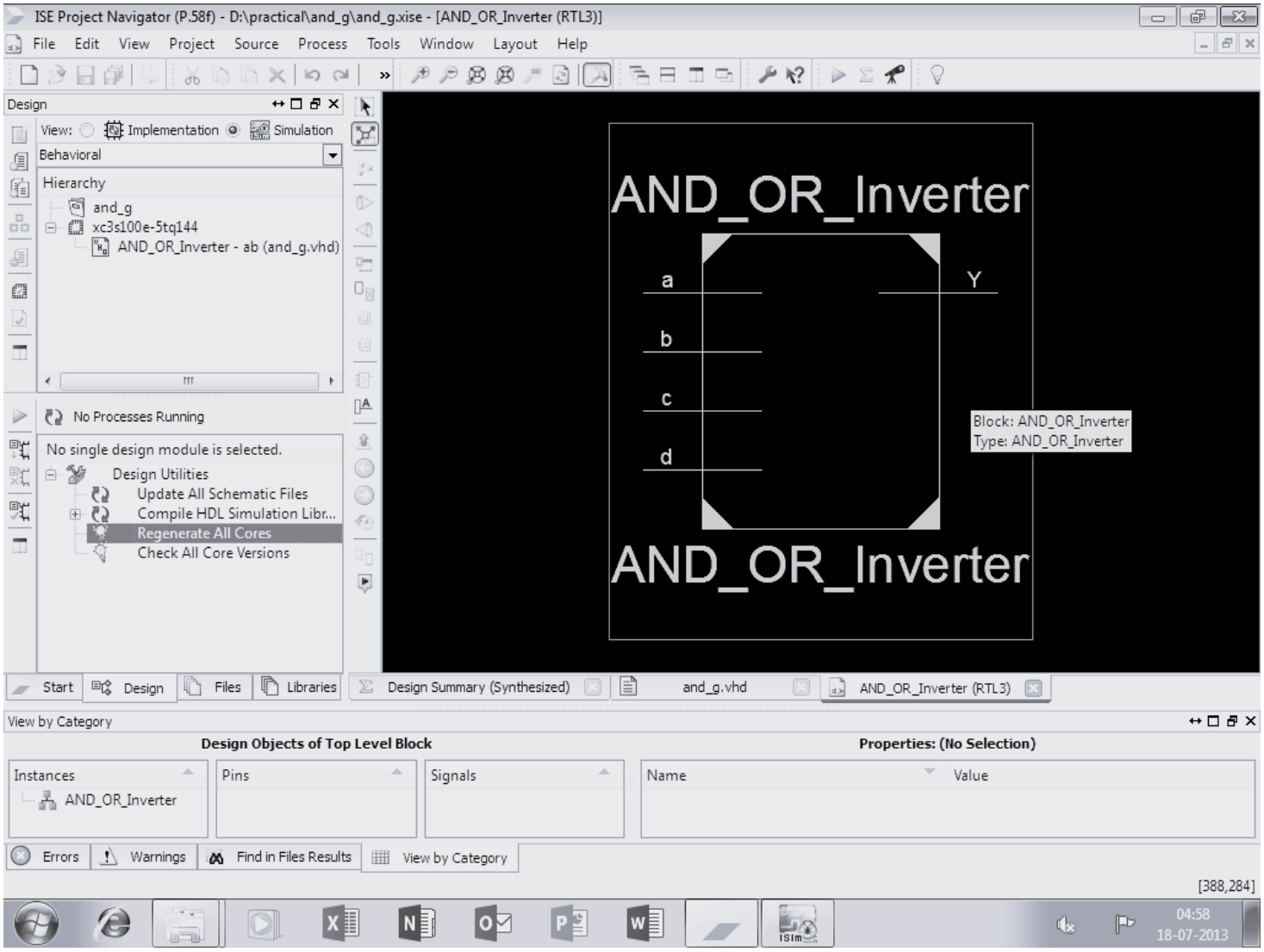
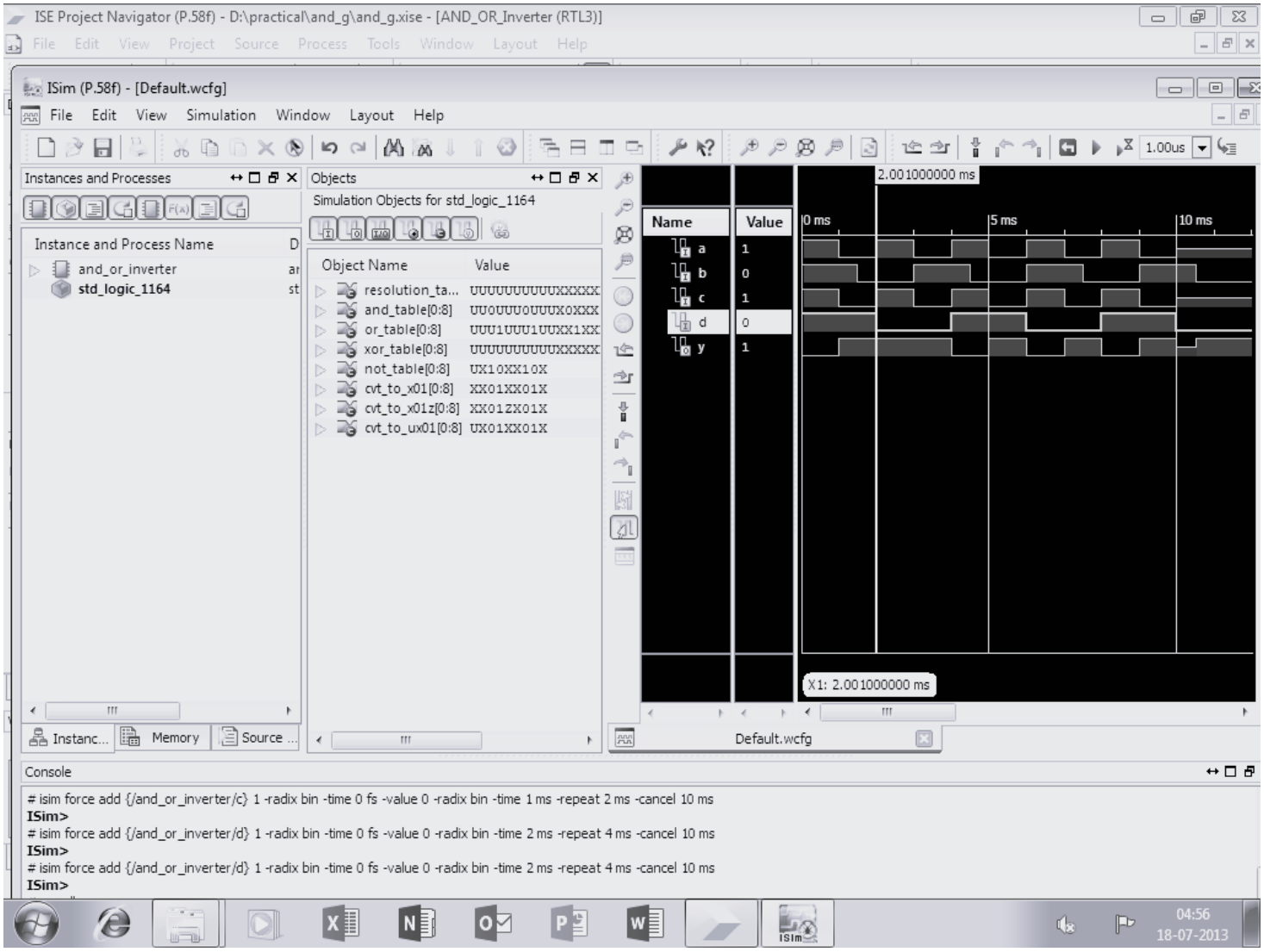

ISE Project Navigator (P.58f) - D:\practical\and_g\and_g.xise - [AND_OR_Inverter (RTL3)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
and_g
xc3s100e-5tq144
AND_OR_Inverter - ab (and_g.vhd)
No Processes Running
No single design module is selected.
Design Utilities
Update All Schematic Files
Compile HDL Simulation Libr...
Regenerate All Cores
Check All Core Versions
AND_OR_Inverter:1
and2
or2
inv
Y_and0001_imp_Y_and00011
Y_or0000_imp_Y_or00001
Y_imp_Y1
and2
Y_and0000_imp_Y_and00001
AND_OR_Inverter
Start Design Files Libraries
Design Summary (Synthesized)
and_g.vhd
AND_OR_Inverter (RTL3)
View by Category
Design Objects of Top Level Block
Properties of Signal: c
Instances
AND_OR_Inverter
Pins
AND_OR_Inverter
Signals
b
c
Name
Value
PortPolarity
Input
PortName
c
Errors Warnings Find in Files Results View by Category
Zoom out such that objects become smaller
[180,0]
04:58
18-07-2013


ISE Project Navigator (P.58f) - D:\practical\and_g\and_g.xise - [AND_OR_Inverter (RTL3)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
and_g
xc3s100e-5tq144
AND_OR_Inverter - ab (and_g.vhd)
No Processes Running
No single design module is selected.
Design Utilities
Update All Schematic Files
Compile HDL Simulation Libr...
Regenerate All Cores
Check All Core Versions
AND_OR_Inverter
a
b
c
d
Y
Block: AND_OR_Inverter
Type: AND_OR_Inverter
AND_OR_Inverter
Start Design Files Libraries
Design Summary (Synthesized)
and_g.vhd
AND_OR_Inverter (RTL3)
View by Category
Design Objects of Top Level Block
Properties: (No Selection)
Instances
AND_OR_Inverter
Pins
Signals
Name
Value
Errors Warnings Find in Files Results View by Category
[388,284]
04:58
18-07-2013


ISE Project Navigator (P.58f) - D:\practical\and_g\and_g.xise - [AND_OR_Inverter (RTL3)]
File Edit View Project Source Process Tools Window Layout Help
ISim (P.58f) - [Default.wcfg]
File Edit View Simulation Window Layout Help
1.00us
Instances and Processes
Instance and Process Name
and_or_inverter
std_logic_1164
Objects
Simulation Objects for std_logic_1164
Object Name
Value
resolution_ta...
and_table[0:8]
or_table[0:8]
xor_table[0:8]
not_table[0:8]
cvt_to_x01[0:8]
cvt_to_x01z[0:8]
cvt_to_ux01[0:8]
UX10XX10X
XX01XX01X
XX01ZX01X
UX01XX01X
Name
Value
a
b
c
d
y
2.001000000 ms
0 ms
5 ms
10 ms
X1: 2.001000000 ms
Instanc...
Memory
Source ...
Default.wcfg
Console
isim force add {/and_or_inverter/c} 1 -radix bin -time 0 fs -value 0 -radix bin -time 1 ms -repeat 2 ms -cancel 10 ms
ISim>
isim force add {/and_or_inverter/d} 1 -radix bin -time 0 fs -value 0 -radix bin -time 2 ms -repeat 4 ms -cancel 10 ms
ISim>
isim force add {/and_or_inverter/d} 1 -radix bin -time 0 fs -value 0 -radix bin -time 2 ms -repeat 4 ms -cancel 10 ms
ISim>
04:56
18-07-2013