Contribution

We made protocol for each week till week 5. But after that We needed to re_work on each diagram to make the project a little bit simpler . So, From week 5 , We worked on System design diagrams together on each team meeting .

Implementation Responsibilities :

UPPAAL : Amit Chakma and Ajoke Adijat Sulaiman did it together.

FreeRTOS : Saikot Das Joy wrote freeRTOS code . Amit Chakma and Saikot Das Joy simulated it on an ESP32 Micro-Controller.

Modelsim : Saikot Das Joy made FIFO(16x8) in VHDL and simulated it.

Documentation :

In documentation, which part is written by whom is described below:

Saikot Das Joy : State Machine Diagram , Sequence Diagram , freeRTOS Implementation and simulation , FIFO (16x8) memory in VHDL and simulation, Index.

Amit Chakma : Use case Diagram , Activity Diagram , Requirement Diagram.

Ajoke Adijat Sulaiman : Abstract , Introduction , UPPAAL, Summary.