Full adder

Full adder is a 3 input and 2 output adder . We can construct this full adder circuit using 2 half adders . It requires 3 xor gates , 2 and gates and one or gate.

TRUTH TABLE:

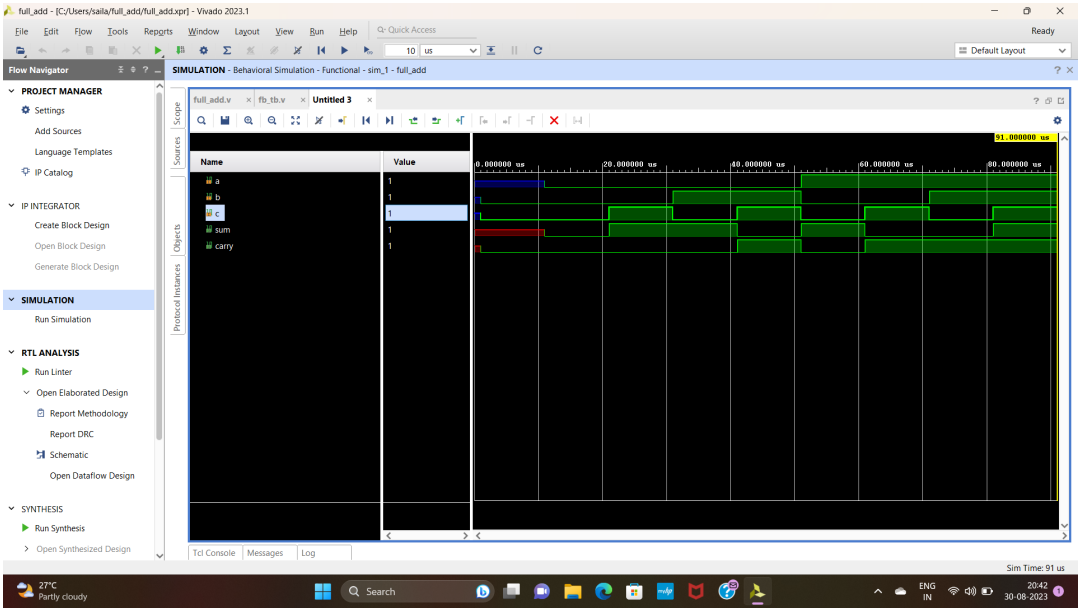
INPUT A	INPUT B	INPUT C	OUTPUT CARRY	OUTPUT SUM
0	0	0	0	0
0	0	1	0	**1**
0	1	0	0	**1**
0	1	1	**1**	0
1	0	0	0	**1**
1	0	1	**1**	0
1	1	0	**1**	0
1	1	1	**1**	**1**

VERILOG CODE:

```
//FULL ADDER USING DATA FLOW LEVEL OF ABSTRACTION

module full_add(input a,b,c, output sum,carry );
assign sum=a^b^c;
assign carry=(a|b) & (b|c) & (c|a);
Endmodule
```

SIMULATION OUTPUT:



SCHEMATIC DIAGRAM: