Theory and Practice (Analysis and Design) Peak Current Mode Control of High-Frequency DC-DC Converters

Xiaofan Cui*, *Student Member*, *IEEE*, and Al-Thaddeus Avestruz†, *Member*, *IEEE*

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Abstract:

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*X. Cui is with the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI, 48109, USA, e-mail: cuixf@umich.edu.

†A. T. Avestruz (corresponding author) is an assistant professor with the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI, 48109, USA, e-mail: avestruz@umich.edu, telephone number: (+1)617-290-4179.

1 Introduction

Although peak (or valley) current mode control (PCC) has been widely used in dc-dc voltage regulator control for a long time, high frequency [1] dc-dc converters using PCC are seldomly reported in the literature.

Parasitic ringing is an important bottleneck when implementing PCC for high-frequency dc-dc converters. The severe voltage spikes are common in a high frequency power converts using PCC as shown in 1. In one of our experiments, when these harsh parasitic ringings contaminate current measurements, the inner current loop of a current-mode buck converters using constant on-time (CM-COT) buck converter can actually be unstable. This phenomena challenges the traditional understanding that in CM-COT buck converters, the inner current loop is deadbeat and stable at all operating points [**?**]. In this paper, we provide new theoretical criteria which explain why and predict when this instability phenomena happen.

It is impossible to decrease the parasitic inductance under the level of nH under the constraints of the current pc board technology. Therefore, we solve this problem in another way: instead of eliminating parasitic ringings, we show three new compensation techniques which guarantee the PCC to work in harsh parasitic ringing conditions - analog comparator overdrive propagation delay (COPD), slope compensation and low-pass filter. We show that the overdrive propagation delay of the analog comparator can be eliminate the effect of parasitic ringing interference on the plant. We explain that the slope compensation, which is widely used in fixed-frequency PCC, can also be used in variable-frequency PCC to reject the parasitic ringing interference. We claim that a low-pass filter with cut-off frequency slower than switching frequency can still result in a good performance. Furthermore, unlike the traditional compensation design methods based on rule-of-thumbs and design experiences, we show a rigorous analysis tool to help designer with the design procedure.

PCC is advantageous in high-frequency and fast-transient-response dc-dc converters over the other traditional control methods including voltage-mode control and ripple-based control. Peak current mode control shows significantly faster transient response and is much easier to design than the voltage mode control [**?**]. Power converter plant in PCC architecture is usually a lower order system compared to voltage mode control because the PCC architecture eliminates the transient from duty cycle to inductor current by measuring and commanding inductor current [**?**]. A low order plant makes the compensator design easier and more robust. Peak current mode control is more robust to the output capacitor parasitic and can be applied in any types of dc-dc converters compared to the ripple-based method [**?**]. PCC sense and control the inductor current directly while the ripple-based control has to rely on the assumption that the capacitor voltage contains the information of inductor current. PCC does not rely on the output capacitor and load information, but the ripple-based method can even go in instability if the ESR or ESL is not appropriate. PCC can fix the switch-

[1] switching frequency $>$ 1 MHz

ing frequency more easily but ripple based control suffers a lot from the jittering in switching frequency. PCC can provide a tight DC voltage regulation. Another important benefit is that PCC naturally does cycle-by-cycle over current protection to the power stage, hence the fault protection design can be simplified.

Among many PCC architectures in literature, direct PCC using the mixed-signal hardware implementation is one of the most popular approach because it has both fast transient response and programmable flexibility. By whether the inductor current is sensed or not, state-of-the-art PCC can be direct PCC methods and indirect methods. Among direct PCC methods, mixed-signal implementation is the most promising because it shares the benefits of fast transient response and ability to be quickly online tuned to adapt to fast varying operating points. Analog implementation is the most traditional implementation method: The output voltage is processed by an error amplifier and the result is compared with the sensed current signal by an analog comparator [**?**]. Although the design methods are well-established and it is not hard to obtain high control bandwidth, good dynamic performance is not always guaranteed in a wide operating voltage range because electrical dynamics of circuits change with output voltage operating points and load conditions [**?**]. Digital implementation guarantees the programmable flexibility of the adaptive voltage regulation: An analog-to-digital converter (ADC) is added to discretize the sampled inductor current. Then the quantified current is compared with the current command in through digital logic. The implementation of the inductor current sampling can be referred to [**?**]. It is not suitable for high-frequency converter because a high-speed sampler is required. Mixed-signal hardware implementation [**?**] [**?**] combines the advantages of both analog and digital implementations. A common mixed-signal structure includes a digital voltage control loop and an analog current loop.

Because of the difficulties in measuring inductor current in high-frequency power converters, several indirect PCC are proposed. However, currently proposed indirect PCC still cannot outperform the direct PCC. Current-programmed control constructs the inductor current waveform using the priori-model and control the inductor current indirectly by duty ratio. The classic current-programmed control [**?**] is sensitive to the time-varying uncertainties of the inductor model and the input/output voltage measurement. Although [**?**] improves the method by measuring the actual current at two points every cycle and calculate slope, the prediction error is still inevitable because in some applications where the inductor current can go highly non-linear [**?**] [**?**]. Hence curve fitting using 2 sample points can cause significant errors. Another method in [**?**] claim a control algorithm which is stable under the incorrect current ramp estimation, but the proposed method cannot guarantee fast transient response. A V^2I_c method by [**?**] measures and control the capacitor current which contains the inductor current information. However, a complicated impedance matching network has to be designed to compensate the output capacitor parasitic [**?**]. Several derivative output ripple

voltage (DORV) techniques get the capacitor current information by differentiating the capacitor voltage [?] [?]. Although the methods avoid the complicated capacitor current measurement, it is vulnerable to noises because of derivative calculation. Several papers combine the aforementioned current mode control techniques with other control methods, for example, [?] combines the peak current mode control and the ripple-based control. [?] is the digital version of [?]. [?] and [?] combines ripple-based control with the current-programmed control and derivative output ripple voltage technique respectively. There also exist a few current-mode control methods which is not within the aforementioned category, for example, [?] uses the inductor current feed-forward in voltage mode control. [?] Implements a current-programmed control with an synchronously sampled output voltage.

Main factors which restrict the control bandwidth of dc-dc converters using PCC are low-loss switching devices, high-speed digital control devices and low circuit parasitics. Recently, the commercial GaN FET already has low enough switching losses which enables the high frequency DC-DC converter using hard switching [?]. People can get access to high speed digital control device. For example, a commercial ADC with precision over 10 bits can have sampling latency lower than 50 ns [?, ?], In the market, there are several types of DAC with settling time lower than 20 ns [?, ?] and FPGA with main clock higher than 400 MHz [?].

Circuit parasitic is more important in implementing direct PCC because the parasitic ringing causes the current measurement and current command error. However, the frequency and time constant of ringing are limited by the minimal parasitic inductance on PCB technology which is in the level of nH. The induced voltage spike is comparable to the voltage on the measurement resistor. Among a few existing works which tackles the high frequency PCC converters problem, either the power level or the power efficiency is sacrificed. Some paper decrease the power rating to avoid ringing interference, but this limited the application area. [?] shows a 5MHz converter on board with output power lower than 5 W. Some use integrated circuit to eliminate the parasitic, but this limit the power level of the circuit. [?] reports a 3MHz PCC buck converter on IC. Another method is introducing extra power losses to improve the signal to noise ratio. For example, using damper or snubber to attenuate the energy as well as the amplitude of the ringing. Increasing the sensing resistor value to get a much cleaner current ramp. However, considering the conduction loss is proportional to the square root of current $P_{\text{loss}} = I^2R$ but the signal-to-noise ratio is proportional to the current $V = IR$, this method does more harm than good in large output current applications like voltage regulator modules(VRMs).

In this paper, instead of trying to eliminate the parasitic ringing, we use several compensation techniques to stabilize the PCC high-frequency power converters even in harsh parasitic ringing conditions. We first exhibit a novel model on the mechanism of how ringing influences the power converter plant and control.

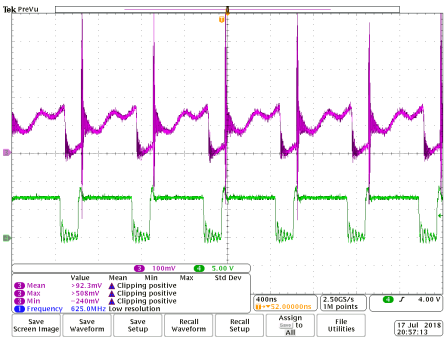

Fig. 1: Measured inductor current of a digitally-controlled CM-COT boost converter.

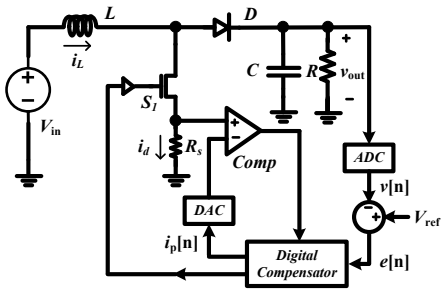

Fig. 2: Schematic diagram of a digitally-controlled CM-COT boost converter.

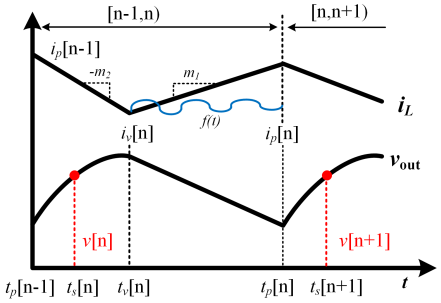

Fig. 3: Inductor current and capacitor voltage waveforms of a digitally-controlled CM-COT boost converter.

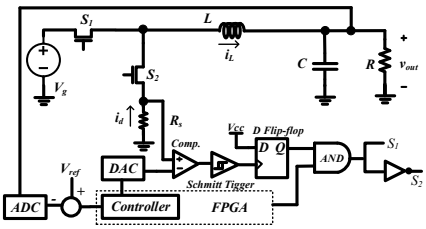

Fig. 4: Analog valley-current controller for constant-on-time current-mode buck.

Based on the model, we show the rigorous analysis tool to study stability and performance of practical DC-DC converter using PCC. Several compensation techniques are compared and discussed under the analysis tools.

2 Modeling

The traditional assumption of piece-wise linear inductor current is invalid in practical high-frequency dc-dc converters. Instead, it is more accurate to model the measured inductor current as a ramp added by an interference function. We illustrate a new model of interfered inner current loop. We found that the reasons of long-time settling and instability in the practical converter can be effectively explained by this model. We first define the interference function as following:

Definition 1. $f(t)$, the interference function in continuous time satisfies the following properties (i) $f(t)$ is cycle-invariant; (ii) $f(t)$ has a bounded amplitude of $[0, A_{\max}]$ and a bounded frequency spectrum of $[\omega_{\min}, \omega_{\max}]$.

The example converter plant we used is a current-mode boost converters using constant off-time (CM-COT boost converter) as shown in Fig. 2. $i_c[n]$ is the current command from the outer loop every cycle. Our

model of the interfered inner current loop can by described by following difference equations:

$$i_p[n] = i_p[n-1] - m_2 t_{\text{off}} + m_1 t_{\text{on}}[n], \tag{1}$$

$$i_c[n] = i_p[n] + f(t_{\text{on}}[n]). \tag{2}$$

The I_e and T_{on} at equilibrium can be obtained by letting $i_p[n+1] = i_p[n]$, $t_{\text{on}}[n+1] = t_{\text{on}}[n]$. I_e and I_c's relationship are govern by an implicit function $g(I_e, I_c) = 0$. We define an explicit mapping $\mathcal{T} : \mathcal{R}_+ \to \mathcal{R}_+$ from the inductor current command I_c to the actual inductor current I_e in steady state.

Although no assumptions mathematically guarantees that mapping $\mathcal{T}$ is a single-valued and monotonically non-decreasing explicit function. However, our special design using first-event-triggering mechanism guarantees these properties. As shown in Fig 5, the possibile triggering time instants can be t_1, t_2,t_3 or t_4. The D flip-flop in Fig 4 always latch the first comparator detection, which is then reset by the FPGA at the next switching cycle. This design guarantee t_1 to be the triggering time instant. A generic function $\mathcal{T}$ is like the shape in Fig 6. One defect of the function $\mathcal{T}$ is that it might includes jump discontinuity points. For $I_e \in [I_{f_1} - I_{f_2}]$ or $I_{f_3} - I_{f_4}$, there is no correct peak current command I_c which can position the real pwak current.

Definition 2. we define the *unreachable equilibrium set UE* $\triangleq [I_{f_1}, I_{f_2}] \cup [I_{f_3}, I_{f_4}], \ldots$. Lebesgue measure of the *UE* is $\lambda(UE)$.

We do not recommend having $\lambda(UE) \neq 0$ for control practice because the inner current loop will not be able to position the current to wherever the outer loop controller wants. We give the following theorem without proof to show the relationship between $\lambda(UE)$ and interference function $f(t)$.

Theorem 1. $\mathcal{T}$ is an onto-function if and only if the measured inductor current waveform $m_1 t + f(t)$ is strictly monotonic.

2.1 Stability

Under the condition of Theorem 1, we would like to study the stability of the equilibrium. Suppose the equilibrium is at $i_p[n] = I_e$, $t_{\text{on}}[n] = T_{\text{on}}$, $i_c[n] = I_c$, We translate the equilibrium to the origin by defining $\tilde{i}_p[n] = i_p[n] - I_e$, $\tilde{t}_{\text{on}}[n] = t_{\text{on}}[n] - T_{\text{on}}$, $\tilde{i}_c[n] = i_c[n] - I_c$.

$$\tilde{i}_p[n] = \tilde{i}_p[n-1] + m_1 \tilde{t}_{\text{on}}[n] \tag{3}$$

$$\tilde{i}_c[n] = \tilde{i}_p[n] + f(t_{\text{on}}[n]) - f(T_{\text{on}}). \tag{4}$$

We assume the peak current command $i_c[n]$ from outer voltage loop is fixed at I_c.

The resulting system can be formulated into a Lure system as shown in Fig 7. By applying the circle criterion, we prove the following theorem to show the stability conditions for the system (1) under any disturbance:

Theorem 2. The $A_{\max}\omega_{\max} < (m_1/2)$ if and only if the inner current loop is *globally asymptotically stable.*

Proof. □

2.2 Performance

In system (1), we view the current command sequence $\tilde{i}_c[n]$ as the input and the peak inductor current sequence $\tilde{i}_p[n]$ as the output. Ideally, the peak inductor current is assumed to follow the peak-current command with small overshoot and fast speed. However, with interference amplitude increasing, one could expect the convergence speed gradually slow down and overshoot gradually increases.

We show a Z-transform method to systematically analyze the performance of system (1) including settling time, overshoot and stability margin.

We linearize the system (1) and have

$$\tilde{i}_p[n] = \tilde{i}_p[n-1] + m_1\tilde{t}_{\text{on}}[n], \tag{5}$$

$$\tilde{i}_c[n] = \tilde{i}_p[n-1] + (f^{'}(T_{\text{on}}) + m_1)\tilde{t}_{\text{on}}[n]. \tag{6}$$

We define an equivalent local slope $s_0 = f^{'}(T_{\text{on}}) + m_1$, slope ratio $\beta = m_1/s_0$, and pole of inner current loop $a = 1 - \beta$. Then system (1) can be simplified as

$$\tilde{i}_p[n] = \beta\tilde{i}_c[n] + a\tilde{i}_p[n-1]. \tag{7}$$

Note that although the discretized data does not have a uniform corresponding to physical time domain, Z-transform can still be applied [**?**],

$$C_2(z) = \frac{\beta}{1 - az^{-1}}. \tag{8}$$

Ideally, $\beta = 1$, $a = 0$ and the pole of $C_2(z)$ locates at 0, meaning $C_2(z)$ is deadbeat. The larger the $|a|$ is, the longer transient under reference step the inner loop will have.

Because of the uncertainty of the derivative of f, While the operating points is moving, the pole a is within