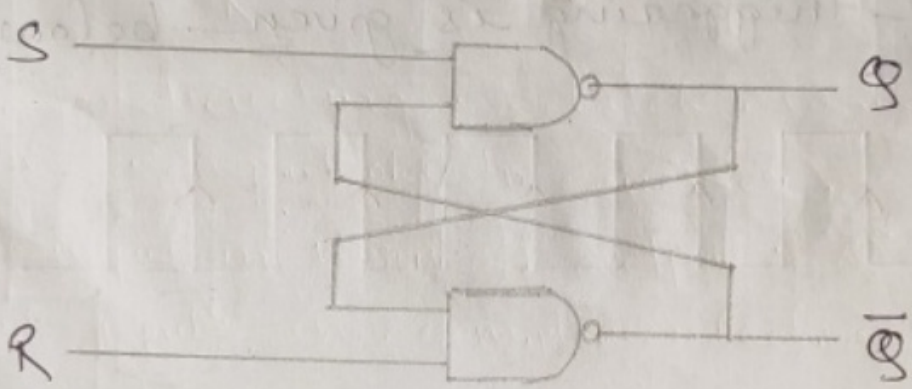
Latch

Latch is a basic building ~~block~~ element in sequential circuits. Latches do not have any clock signal, that is they are asynchronous sequential circuits. Latches continuously check all the inputs and correspondingly it changes its output when enabled.

Example - S-R latch is an example for simple latch.



Flip-Flop (FF)

The FF is also a building block of synchronous sequential circuits. It has two stable states. It can store one bit of information. Flip-Flops will have a clock signal. Their state changes depending on the clock pulse. Flip-Flop is edge sensitive. They will change their state when the clock signal transition occurs from Low to high or high to Low. When the clock is at constant 0 or 1, the state remains unchanged even if the input changes. A FF is also known as bistable multivibrator. Types – SR, JK, D and T flip-flop.

Latch Construction

There are two methods for constructing a latch –

1. By using 2 NOR gates.
2. By using 2 NAND gates.

1 Construction of Latch by using 2 NOR gates

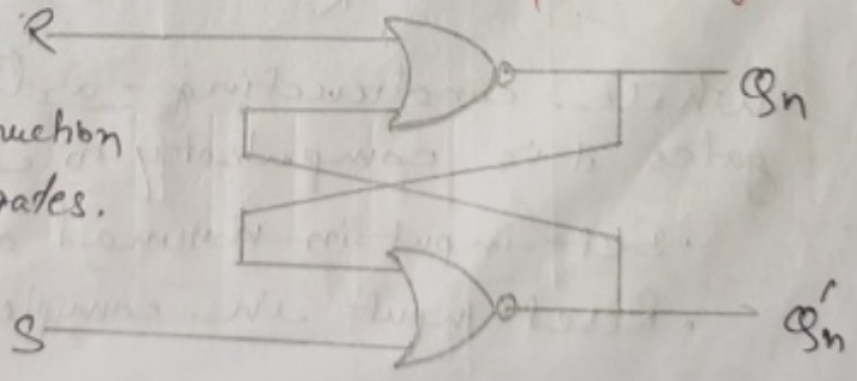


Fig- Latch construction using NOR gates.

While constructing a latch using NOR gates, it is compulsory to consider —

- Reset input R in normal output Q_n.
- Set input S in complemented output Q_n'

Truth table

S	R	Q	$\overline{Q}$
1	0	1	0
0	0	1	0
0	1	0	1
0	0	0	1
1	1	0	0 (Invalid)

* NOR Gates

A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

— . —

2. Construction of Latch by using 2 NAND gates.

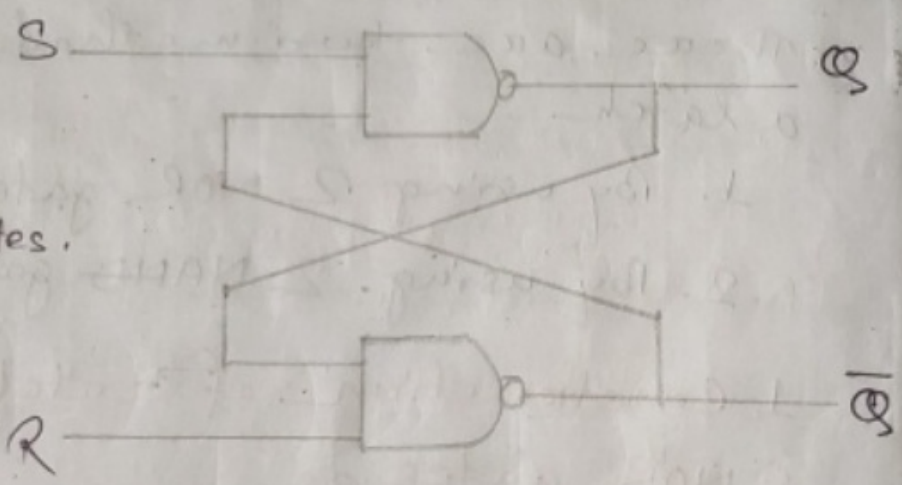


Fig- Latch construction using NAND gates.

While constructing a latch using NAND gates it is compulsory to consider

- Set input in normal output $\overline{Q}$ Q
- Reset input in complemented output $\overline{Q}$

Truth table

S	R	Q	$\overline{Q}$
1	0	0	1
1	1	0	1
0	1	1	0
1	1	1	0
0	0	1	1

* This type of flip-flop is some times called a direct coupled RS-flip-flop. or SR latch.

Clocked SR flip-flop

SR flip-flop is the simplest type of flip-flops. It stands for Set Reset flip-flop.
It is clocked flip-flop.

The clocked SR flip-flop consist of the basic NAND ~~gate~~ latch and two other NAND gates to provide clock pulse. clocked pulse is used for the synchronization and act as an additional control input.

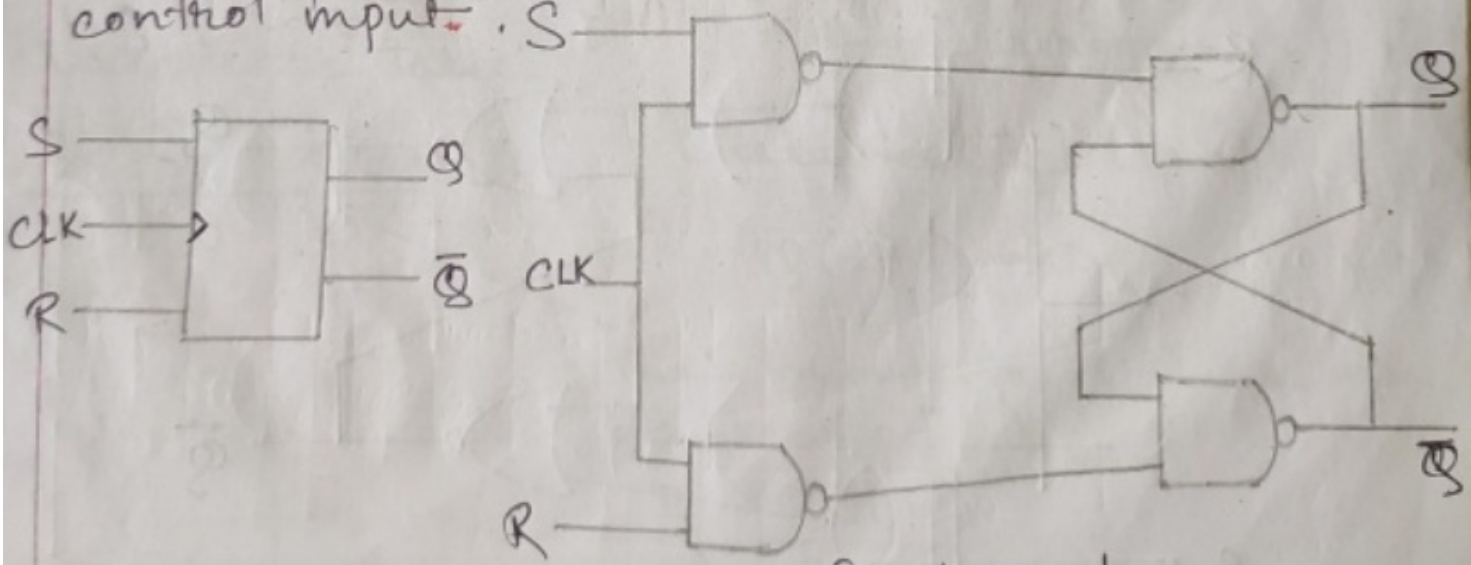
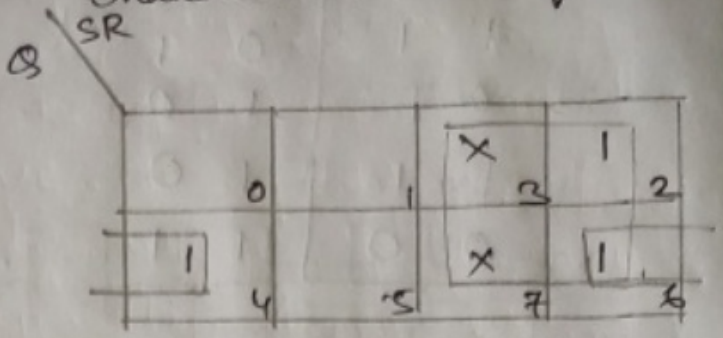


Fig. Logic diagram.

Characteristic table

Q	S	R	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	x
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	x

Characteristic Equation.

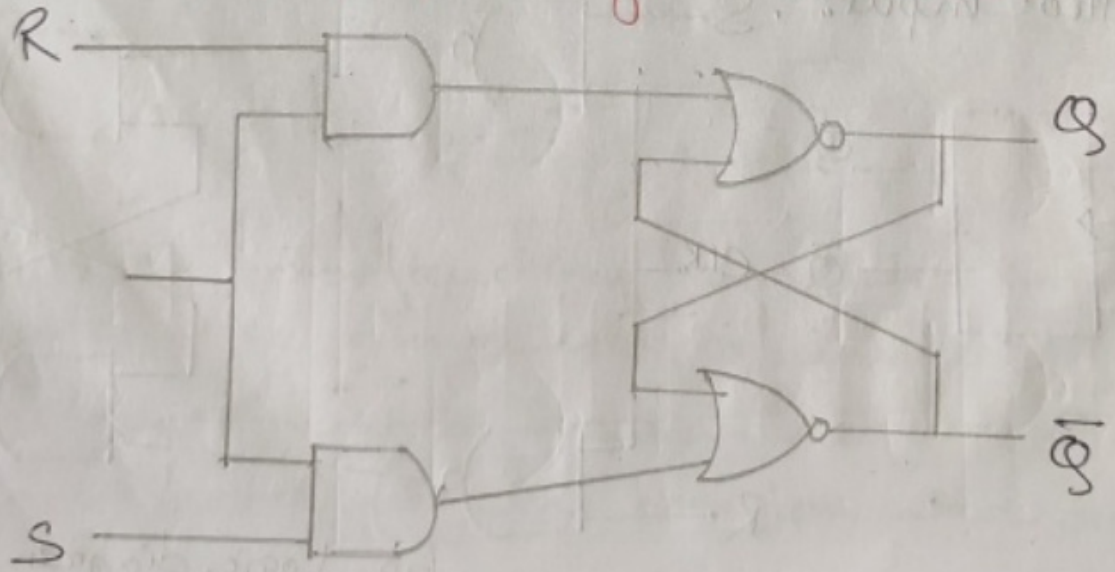


$$Q(t+1) = S + Q\bar{R}$$

The above characteristic table may be reduced as

S	R	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	x

* SR flip-flop using NOR Latch.



D Flip-Flop

A D flip-flop has a single data input in addition to the clock input. The D-flip-flop is a modification of the clocked SR flip-flop. Also called Delay flip-flop. The D input goes directly to S input and its complement through NOT gate, is applied to the R input. This kind of flip-flop prevents the value of D from reaching the output until a clock pulse occurs.

Fig- Block diagram.

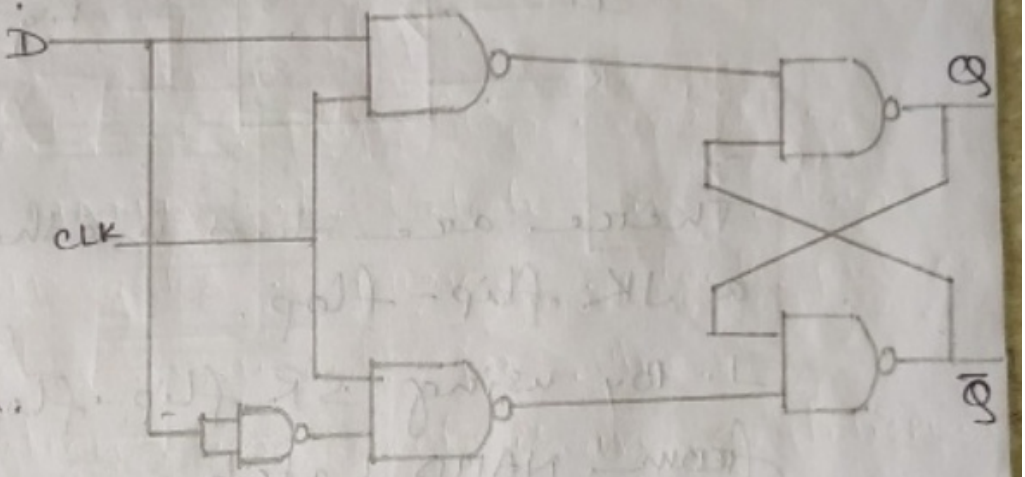


Fig – Logic diagram.

Characteristic Table

Q(t)	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

Characteristic Equation.

$$Q(t+1) = D$$

* The above truth table may be reduced as

D	Q(t+1)
0	0
1	1

JK Flip-Flop

One of the most useful and versatile flip-flop is the JK flip-flop.
A JK flip-flop is a refinement of the SR flip-flop to solve the problem of indeterminate state when both inputs are 1. In JK flip-flop inputs J and K behave like inputs S and R to Set and Reset the flip-flop.

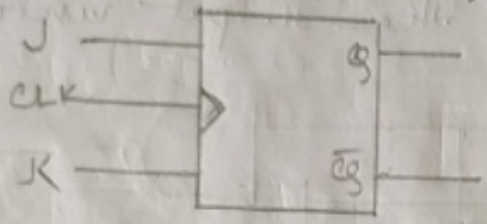


Fig - Block diagram.

There are two methods for constructing a JK flip-flop.

1. By using SR flip-flop constructed from NAND Latch.

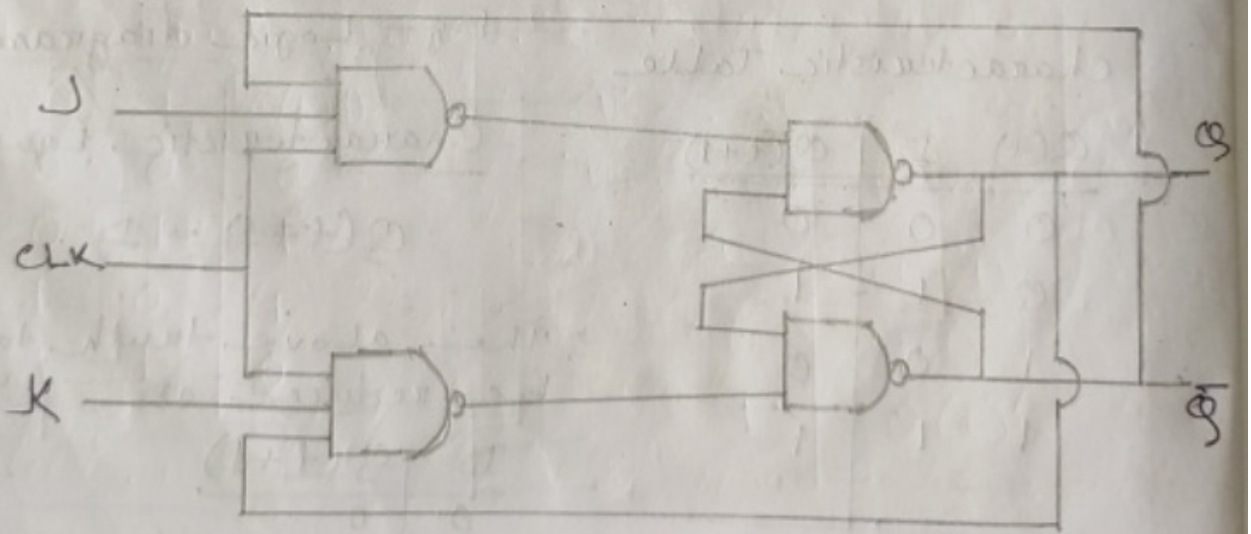


Fig - Logic diagram

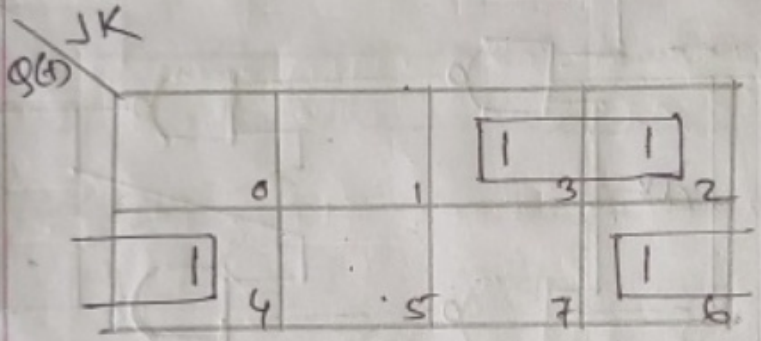
Characteristic table

Q(t)	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

The reduced truth table as

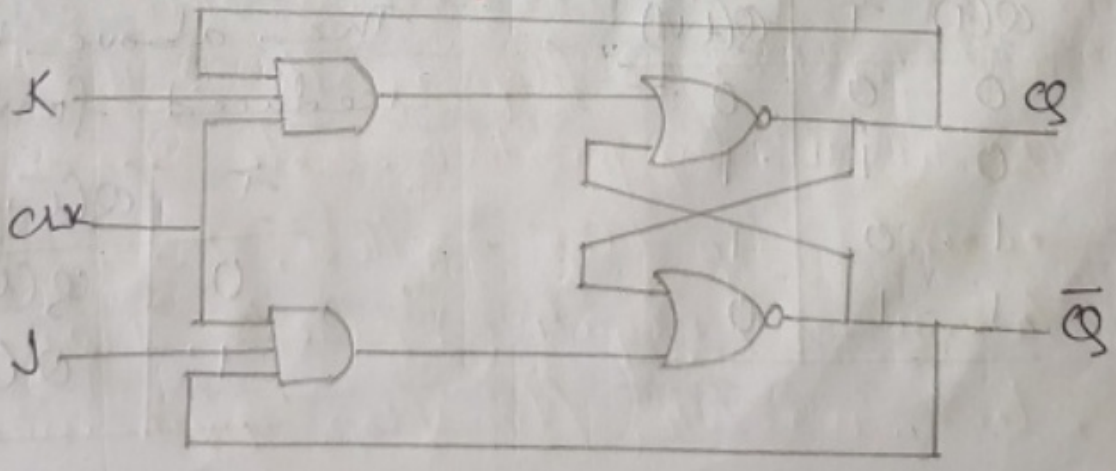
J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q(t)'

Characteristic equation.



$$Q(t+1) = \bar{Q}J + Q\bar{K}$$

* JK Flip-Flop using NOR gates Latch.



T Flip-Flop

T flip-flop is also known as Toggle flip-flop. Design the T-flip-flop by making simple modifications to the JK flip-flop. The T-flip flop is a single input device and hence by connecting J and K inputs together and giving them with single input called T. T-flip-flop is sometimes called as single input JK flip-flop.

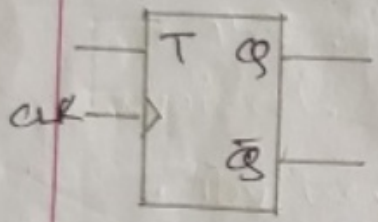


Fig:- Block diagram

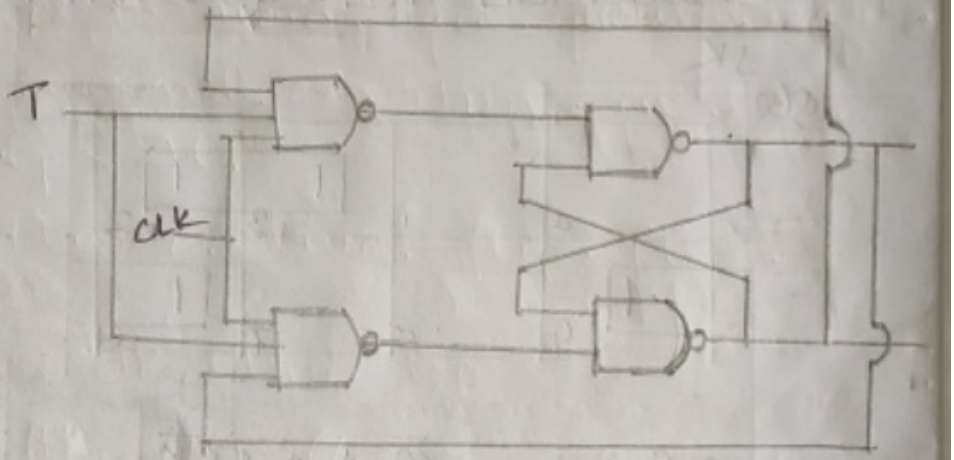


Fig:- Logic diagram.

Characteristic table.

Q(t)	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

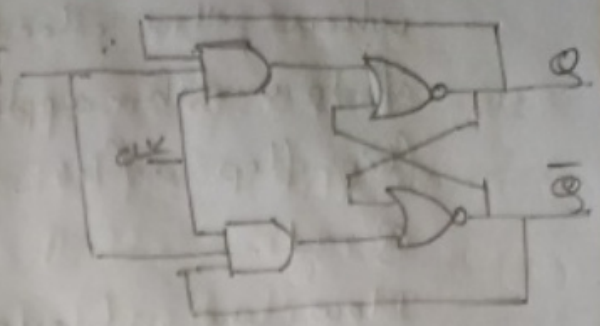
The above table in reduced from

T	Q(t+1)
0	Q(t)
1	Q(t)'

Characteristic equation

Q(t) \ T	0	1
0	0	1
1	2	3

$$Q(t+1) = Q\bar{T} + \bar{Q}T$$



Race around condition

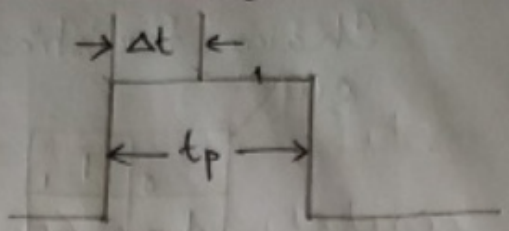
Race around condition occurs in JK flip-flop and it is undesirable. In SR flip-flop, when S=1, R=1, output was indeterminate. This problem was solved in JK-flip-flop by using the feedback connection from the output to the inputs. In JK flip-flop; when J=1, K=1; $Q(t+1) = \bar{Q}(t)$ (until clk=1).

If the clock pulse duration is more than the propagation delay of the flip-flop, output changes many times which causes unstability in the output this condition is called Race around condition.

Example :- J=1, K=1, Q=0, t_p is clock pulse width and Δt is the propagation delay through two NAND gates.

$\therefore \Delta t = 10$ sec
$T_p = 30$ sec
$Q(t+1) = 0, 1, 0$

when this clock pulse of tp width applied to the flip-flop after Δt time $Q = 1$.



Now we have $J = 1$, $K = 1$, $Q = 1$.
After next Δt time $Q = 0$
Hence the output will oscillate back and forth betn 0 and 1 in the duration tp of the clock pulse width.

There two steps to avoid race around condition
- The race around condition can be avoided if $t_p < \Delta t$.
- By using Master slave flip-flop.

Master - Slave JK Flip-flop

A master slave JK flip-flop is a basically a combination of two JK flip-flops connected together in a series configuration. The first flip-flop, called the master, is driven by positive clock. The second flip-flop, called the slave, is driven by negative clock. During positive clock master flip-flop gives intermediate

output, but the slave does not respond. During negative clock, slave flip-flop activate and it copied the previous output of master flip-flop and produces final output. The slave flip-flop output is feedback to inputs of the master flip-flop.

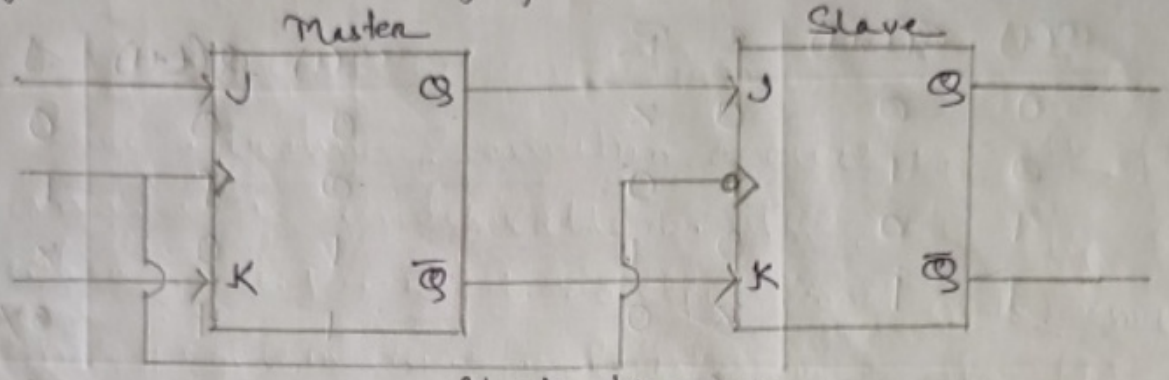


Fig - Block diagram.

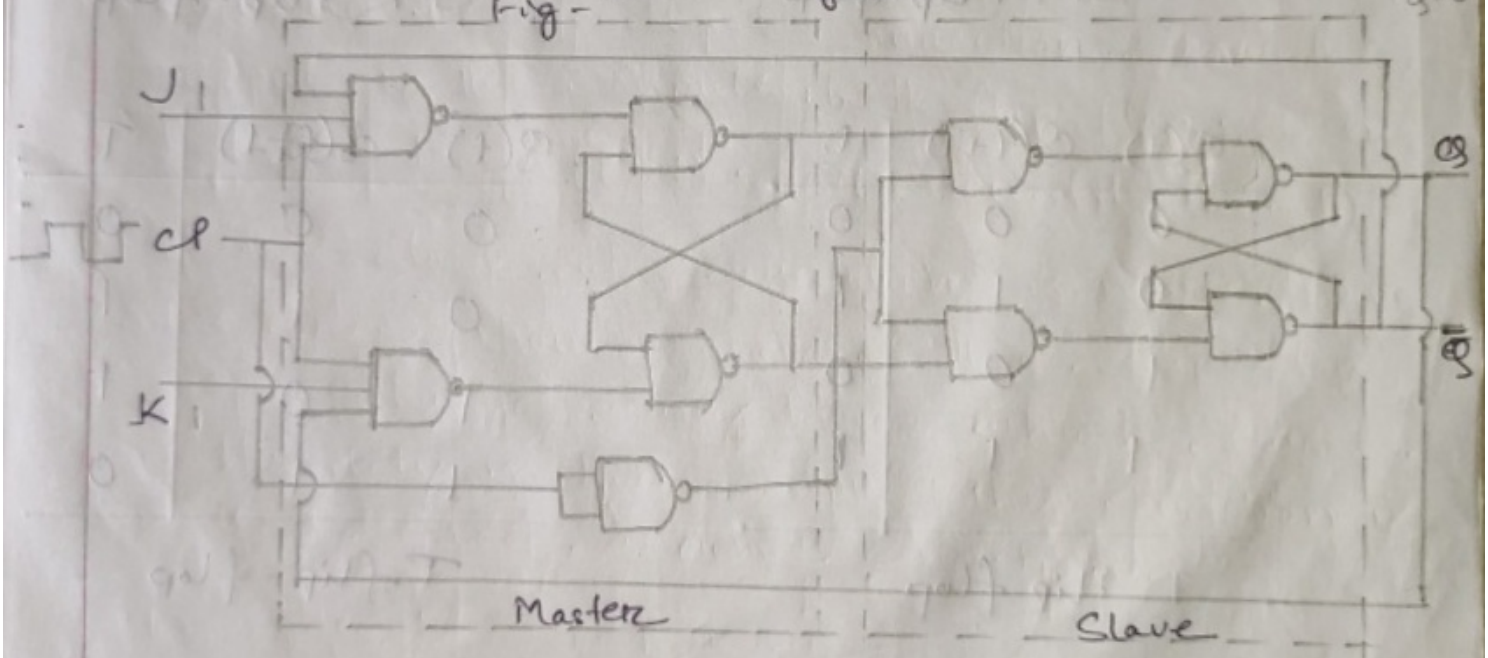


Fig - Master Slave flip flop using NAND gates.

Excitation Table

For a given combination of present state $Q(t)$ and next state $Q(t+1)$, excitation table tell the inputs required. The excitation table of any flip-flop is drawn using the truth table.

$Q(t)$	$Q(t+1)$	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

SR Flip flop

$Q(t)$	$Q(t+1)$	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

J K Flip-flop

$Q(t)$	$Q(t+1)$	D
0	0	0
0	1	1
1	0	0
1	1	1

D Flip flop

$Q(t)$	$Q(t+1)$	T
0	0	0
0	1	1
1	0	1
1	1	0

T flip-flop