FIELD EFFECTIVE TRANSISTOR (FET)

- Field effective transistor abbrivated as FET is an another Semi-Conductor device like BJT which can be used as an amplifier (or) switch.
- Like BJT, FET is also a three terminal device.
- The Operation of FET completely different from that of BJT.
- The three terminals of FET are: Drain(D), Source(S), Grate (G). Out of these three terminals gate terminal acts as controlling terminal.

Features of FET:-

Voltage Controlled Device:- In BJT, the output current (I_C) is controlled by the base current (I_B). Hence BJT is a current controlled device. But, In FET the voltage applied between gate and source (V_{GS}) controlls the drain current I_D. ∴ FET is a voltage Controlled Device.

- The name field effect is derived from the fact that, the output current flow is controlled by the electric field setup in the device by applying external voltage b/w gate and source terminals.

Unipolar Devices:- We know that, In BJT the current is calaculated by both electrons and holes. Hence, that is "Bipolar Junction Transistor". However in FET, current is carried by only one type charge particles, either electrons (or) holes. Hence, FET is called Unipolar device.

→ FET is more temperature stable as compare to the BJT.
→ FET has very high input impedence in the range of mega ohms.
→ FET require less space than that of BJT's. Hence, it is mainly used in design of integrated circuit's like processor.

Classification of FET:-

i) The FET's are divided into two groups:

1) Junction field effective transistor (JFET's)

2) Metal oxide semiconductor field effective transistor (MOSFET's).

- The JFET's further classified into N-channel JFET and P-channel JFET.

- MOSFET is further divided into

i) Depletion MOSFET - D-MOSFET

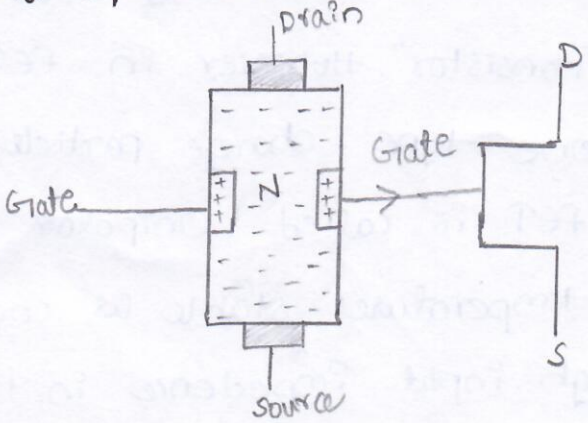
ii) Enhancement MOSFET - E-MOSFET.

Again these above two MOSFET's are further classified into N-channel, P-channel D-MOSFET's and N-channel, P-channel E-MOSFET's.

- In J-FET there is a direct electrical connection between the gate terminal and the channel of JFET.

- In MOSFET's the gate is insulated from the channel by a very thin layer of di-electric material SiO_2. Thus, in MOSFET's there is no dielectrical connection b/w the gate and the channel. Due to this extra layer the input resistance of MOSFET is very high.

Construction and Operation of N-channel JFET:-



→ A small bar of extrensic semiconductor material N-type is taken and two ohmic contacts are made which are drain and source terminals of FET.

→ Heavely dopped electrodes of P-type material are placed at the middle of the bar. which forms gate of the FET.

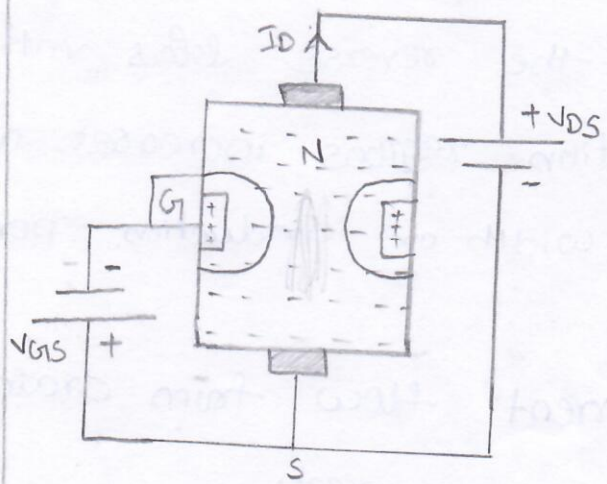
→ The region between the two P-gates are distance from the source to drain is called channel.

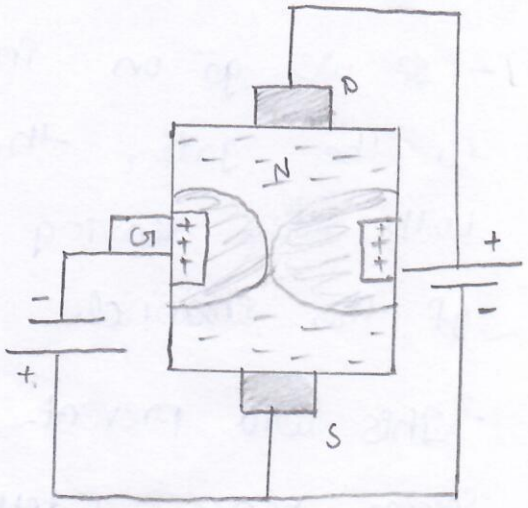
→ In above figure/bar the channel is formed with electrons.

∴ FET is called N-channel JFET.

Operation :- In J-FET, the P-N junction between gate and source is always kept in reverse bias. Since, the current in reverse bias P-N junction is extremely small, the gate current in FET is often neglected assumed to be zero.

- The bias diagram of N-channel J-FET at different gate voltages are shown in below figure;





- Let us Consider, when voltage (V_{DS}) is applied b/w drain and source, Gate terminal is kept Open due to this voltage the majority carriers that means electrons in N-type or holes in P-type starts flowing from the source to drain. This flow of electrons makes the drain current I_D.

- when, drain voltage V_{DS} is applied the drain current I_D flows in drain to source direction. But electrons moves from source to drain.

So, there is a constant flow of current b/w source and drain.

- In N-channel JFET, gate is directly connected to the source terminal with opposite polarity. whenever, gate is connected to negative voltage the junction between gate terminal and channel goes to reverse bias then, the carriers moves very less from source to drain.

- If we externally apply reverse bias voltage to the gate the reverse bias will further increase and hence increase the pentration of depletion region which reduces the width of the conducting portion of the channel.

∴ The channel reduces, the no. of electrons flowing from source to drain reduces. Hence, the current flowing from drain to source reduces.

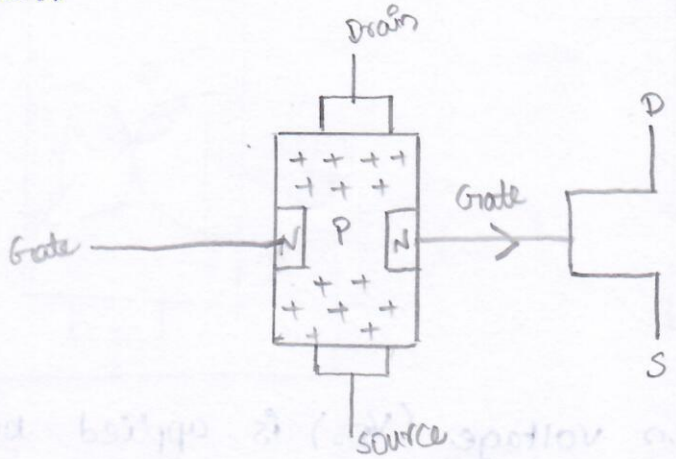
- If we go on increasing the reverse bias voltage to the gate, the depletion regions increases on both sides leaving zero width or conduction portion of the channel.

- This will prevent any current flow from drain to source hence, cutoff the drain current.

- The gate to source voltage that produces cutoff is known as cutoff voltage.

Construction and operation of P-channel JFET:-

Symbol:- The below structure and symbol represents P-channel JFET.



Construction:- → A small bar of extrensic semiconductor material P-type is taken and two ohmic contacts are made which are drain and source terminals of FET.

→ Heavely doped electrodes of N-type material are placed at the middle of the bar. which forms gate of the FET.

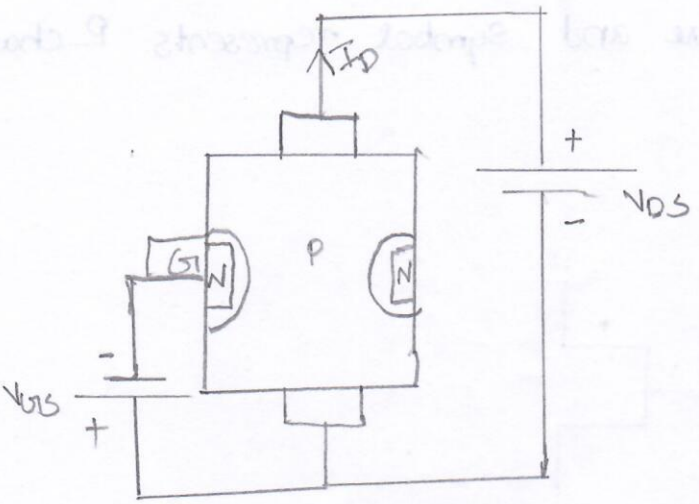
→ The region between the two N-gates are distance from the source to drain is known as channel.

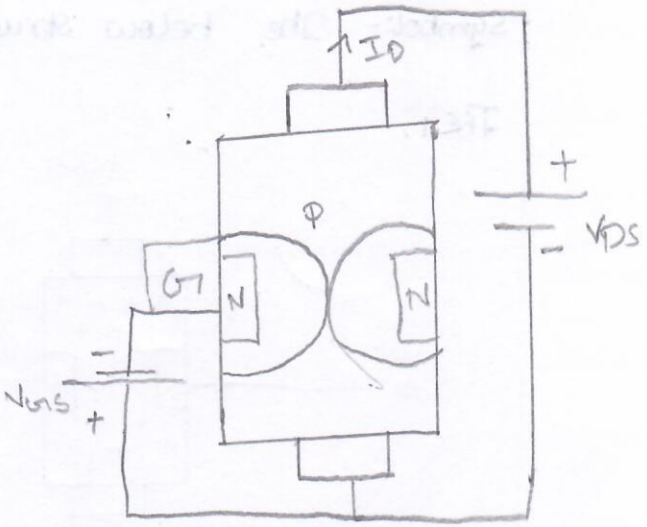
→ In above figure the channel is formed with holes.

∴ FET is called P-channel J-FET.

Operation and Circuit Diagram:- In J-FET the P-N junction between gate and source is always kept in reverse bias. Since, the current in reverse bias P-N junction is extremely small, the gate current in FET is often neglected assumed to be zero.

- The bias diagram of P-channel JFET at different gate voltages are shown in below figure;





→ Let us Consider, when voltage (V_{DS}) is applied between drain and source, Gate terminal is kept Open due to this voltage the majority carriers that means electrons in N-type or holes in P-type starts flowing from source to drain. This flow of holes makes the drain current I_D.

→ when, drain voltage V_{DS} is applied the drain current I_D flows in drain to source direction. But holes moves from source to drain.

→ so, there is a constant flow of current between source and drain.

→ In P-channel JFET, gate is directly connected to the source terminal with opposite polarity. Whenever, gate is connected to negative voltage the junction between gate terminal and channel goes to reverse bias then, the carriers moves very less from source to drain.

→ If we externally apply reverse bias voltage to the gate the reverse bias will further increase and hence increase the pentration of depletion region which reduces the width of the conducting portion of the channel.

∴ The channel reduces, the no. of holes flowing from source to drain reduces. Hence, the current flowing from drain to source reduces.

→ If we go on increasing the reverse bias voltage to the gate the depletion regions increases on both sides leaving zero width or conduction portion of the channel.

→ This will prevent any current flow from drain to source hence, cutoff the drain current.

– The gate to source voltage that produces cutoff is known as cutoff voltage.

Applications of JFET:-

1) JFET has high input impedance and low output impedance. then, they are used as buffer in measuring instruments.

2) Because of low noise they are used in Radio frequency amplifiers in FM tuners.

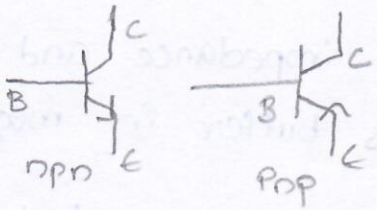
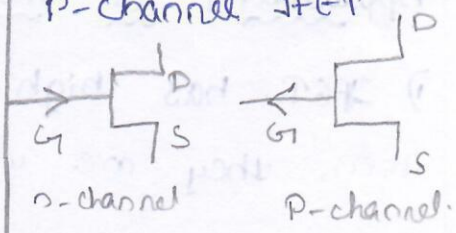
3) FET's are used in mixer circuits in FM and TV recievers.

4) Because of low frequency drift they are used in low frequency oscillators.

5) FETs are used in low frequency amplifiers.

6) FET's are used in Digital circuits.

Differences between BJT and FET:-

S.No	Parameter	BJT	FET
1)	Control element	Current controlled device - Input current I_B controls I_C	It is a voltage controlled device. - Input voltage V_{GS} controls drain current I_D.
2)	Device type	Current flows due to both majority and minority carriers. So, it is a bipolar device.	Current flows only due to majority carriers either electrons or holes. Hence, it is a unipolar device.
3)	Types	npn, Pnp	N-channel JFET P-channel JFET
4)	Symbol		
5)	Configuration	CE, CB, CC	CS, CD, CG
6)	Input resistance	less, compare to JFET	high, compare to BJT
7)	Size	bigger than JFET	Smaller than BJT
8)	Sensitivity	higher sensitivity to change in the applied signals	less sensitivity to change in applied voltage.
9)	Thermal stability	less	more
10)	ratio of output to input	$\beta = \frac{\Delta I_C}{\Delta I_B}$	$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$
11)	Thermal noise	more in BJT because of more junctions	much lower in JFET bcoz, few charge carriers cross the junction.

MOSFET:-

→ Metaloxide semiconductor field effective transistor. It is a second category of field effect transistor. In MOSFET the gate of the transistor is insulated from the channel by SiO_2 layer. Due to this the input resistance of MOSFET is very high. Because of this insulated gates MOSFET is also called IGFET (insulated gate field effective transistor).

- The two types of MOSFET's are Depletion MOSFET and Enhancement MOSFET:

Depletion MOSFET:- It is further divide into two types:-

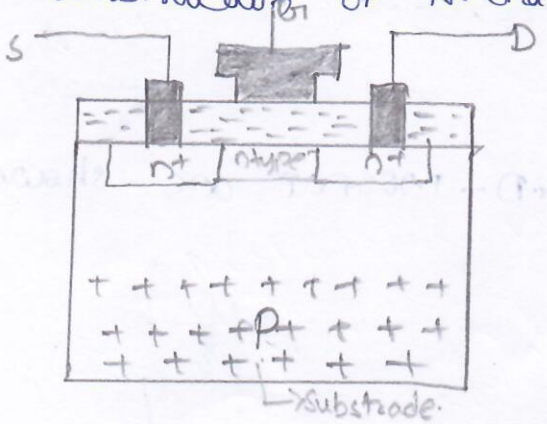
i) N-channel D-MOSFET

ii) P-channel D-MOSFET

i) N-channel D-MOSFET:-

- Two highly doped N-regions are diffused into a lightly doped P-type substrate is chalked depletion N-DMOSFET.

- The basic construction of N-channel D-MOSFET is below;



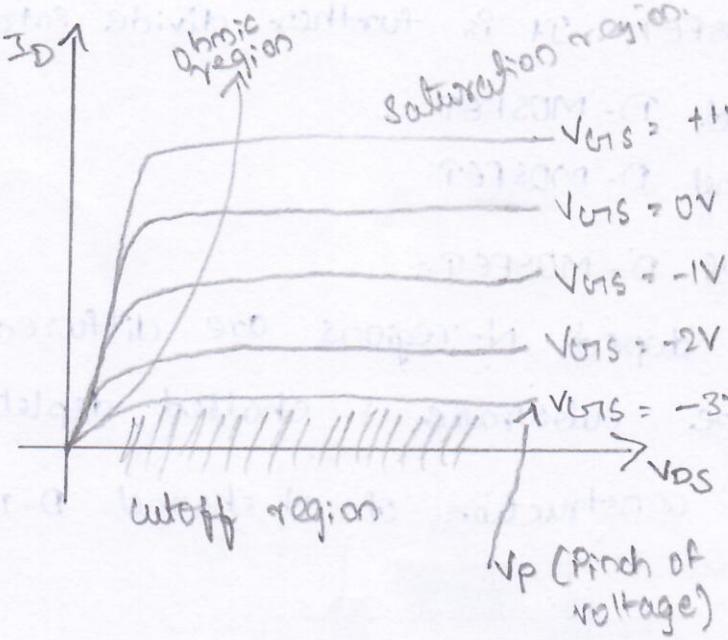
→ These two highly doped N-regions represent source and Drain. Usually substrate is connected to source terminal internally.

- The source and Drain terminals are connected to metallic contact.

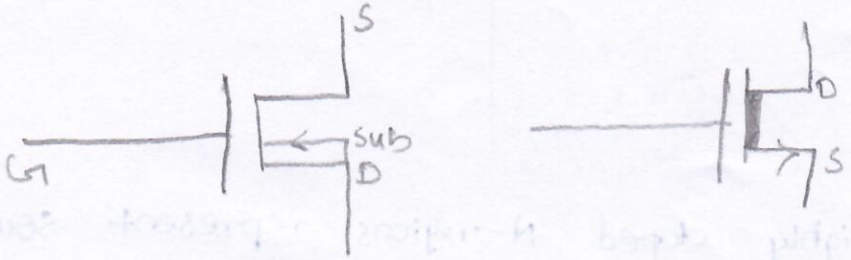
The gate is also connected to a metal contact by a very thin layer of dielectric material called SiO_2.

- The D-MOSFET always acts as an ON transistor. i.e., the channel is formed during manufacturing. If we apply -ve gate voltage, the -ve charges on the gate repel conduction electrons from the channel and attracts holes from the P-type substrate. In this process some of electrons are recombined with holes which depends on -ve voltage applied at the Gate.

- The drain characteristics of N-channel DMOSFET is;

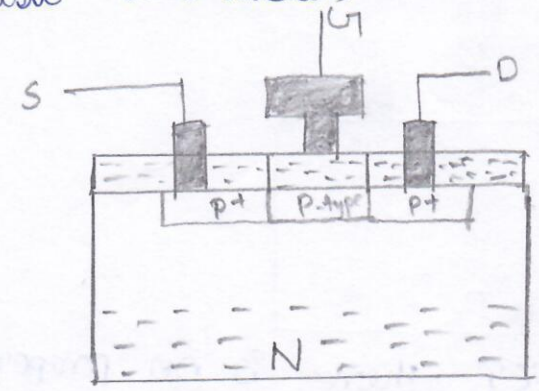


→ The symbols of N-D-MOSFET are shown below;



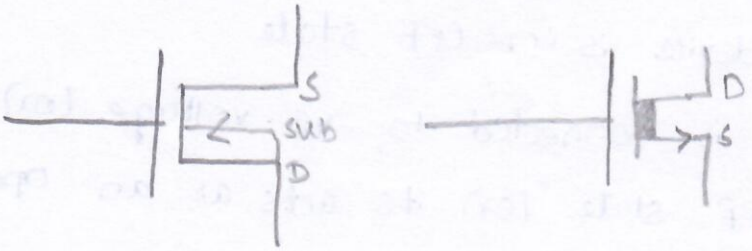
P-channel D-MOSFET:-

- Two highly doped P-regions are diffused into a lightly doped N-type substrate is known as P-channel D-MOSFET.
- The basic construction of P-channel D-MOSFET is below;

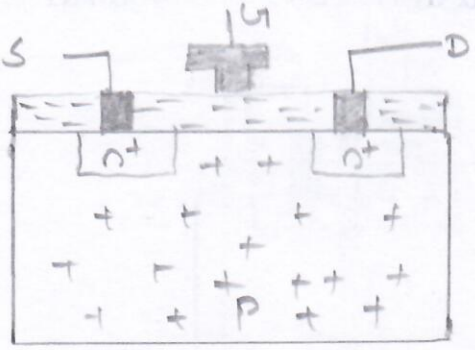


→ These two highly doped P-regions represent source and Drain. Usually substrate is connected to source terminal internally.

- The source and Drain terminals are connected to metallic. The gate is also connected to a metal contact surface but remains insulated from P-channel by a very thin layer of dielectric material called SiO_2.
- The D-MOSFET always acts as an ON Transistor. i.e., the channel is formed during manufacturing. If we apply +ve gate voltage, the +ve charges on the gate repel conduction holes from the channel and attracts electrons from the N-type substrate. In this process, some of holes are recombined with electrons which depends on -ve voltage applied at gate.
- The symbols of P-MOSFET are below;



N-channel E-MOSFET:- Like depletion MOSFET 2 highly doped n-regions are diffused into a lightly doped P-type substrade. The source and drains are taken out to metallic contacts. The construction of N-channel E-MOSFET is below;



- In N-channel E-MOSFET there is no proper channel b/w 2 n-regions. The SiO_2 layer is still present to isolate the gate metallic carriers b/w chain and source and it is separated by channel.

Operation:-

Case (i):- When gate is open which is not connected to any source, then there is flow of carriers b/w source and drain since, different carriers are placed at channel. Even the drain and source terminals are connected to different voltages then also there is no flow of carriers in the channel.

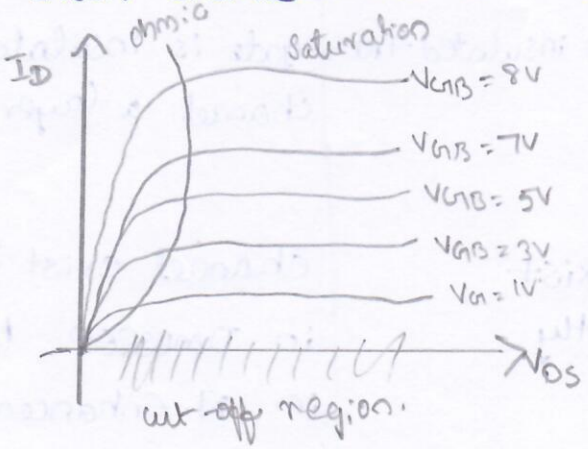
∴ The device is still in non-conducting mode.

Case(ii):- When gate is connected to -ve voltage, all the electrons are placed on SiO_2 layer these electrons attracts holes from P-type substrade towards channel. In this case also there is no charge carriers across the channel. Again the device is in OFF state.

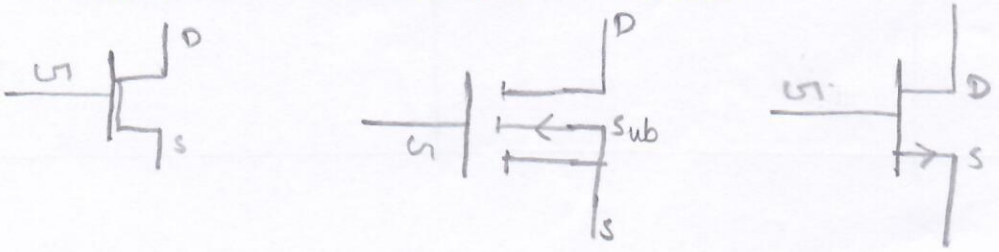
Note:- When N-MOSFET is connected to -ve voltage (or) logic 0 the device goes to OFF state (or) its acts as an open circuit.

Case iii):- When gate input is connected to +ve voltage of N-channel E-MOSFET, all the holes are placed $Si O_2$ layer. These holes attracts the minority carriers of P-substrate towards channel and repels majority carriers towards substrate Now, the channel is replaced by opposite carriers, then a layer is formed which is called inversion layer. The minimum voltage which is applied to gate terminal to establish a proper channel b/w source and drain is called Threshold voltage. When proper channel is placed based on applied voltage b/w chain and source the carriers moves from either source to drain (or) drain to source then we can say that the device is in ON state (or) the device acts as short circuit b/w source and drain.

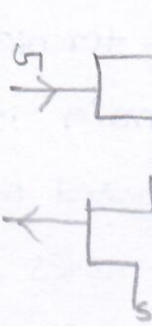
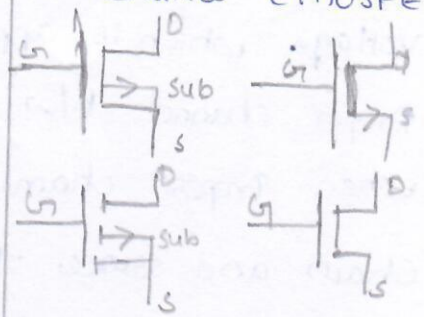
- The drain characteristics of N-E MOSFET:-



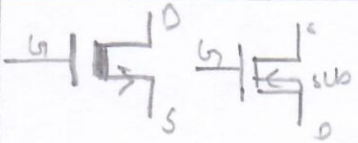
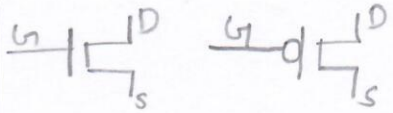
- Symbols of N-channel E MOSFET:-



Comparision b/w MOSFET and JFET:-

S.NO	Parameter	J-FET	MOSFET.
1.	Types	N-channel, P-channel	P-channel DMOSFET N-channel DMOSFET N-channel EMOSFET P-channel EMOSFET.
2.	Symbol		
3.	Operation mode.	Operated in depletion mode.	Operated in depletion and ~~Enhancement~~ modes
4.	Input impedence	High > 10mΩ	very high > 10,000mΩ
5.	Grate	Grate is not insulated from channel	gate is insulated from channel a layer of SiO_2.
6.	Channel	channel exist Permanently	channel exist permanently in DMOSFET but not in E. Enhancement MOSFET.

Comparsion b/w D-MOSFET and E-MOSFET:-

S.No	Parameter	Depletion type	Enhancement type
1.	Symbols		
2.	Channel	exist permanently	channel is physically absent. It is inducted after application of +ve voltage above threshold voltage for N-channel and -ve for P-channel EMOSFETs.
3.	Operation	It can be operated in depletion as well as enhancement.	It is operated in enhancement mode.
4.	Current flow	drain current flows b/w drain and source even $V_{GS}=0$	Practically no current for flow b/w drain and source at $V_{GS}=0$. But, current flows when $V_{GS}>$ threshold voltage.