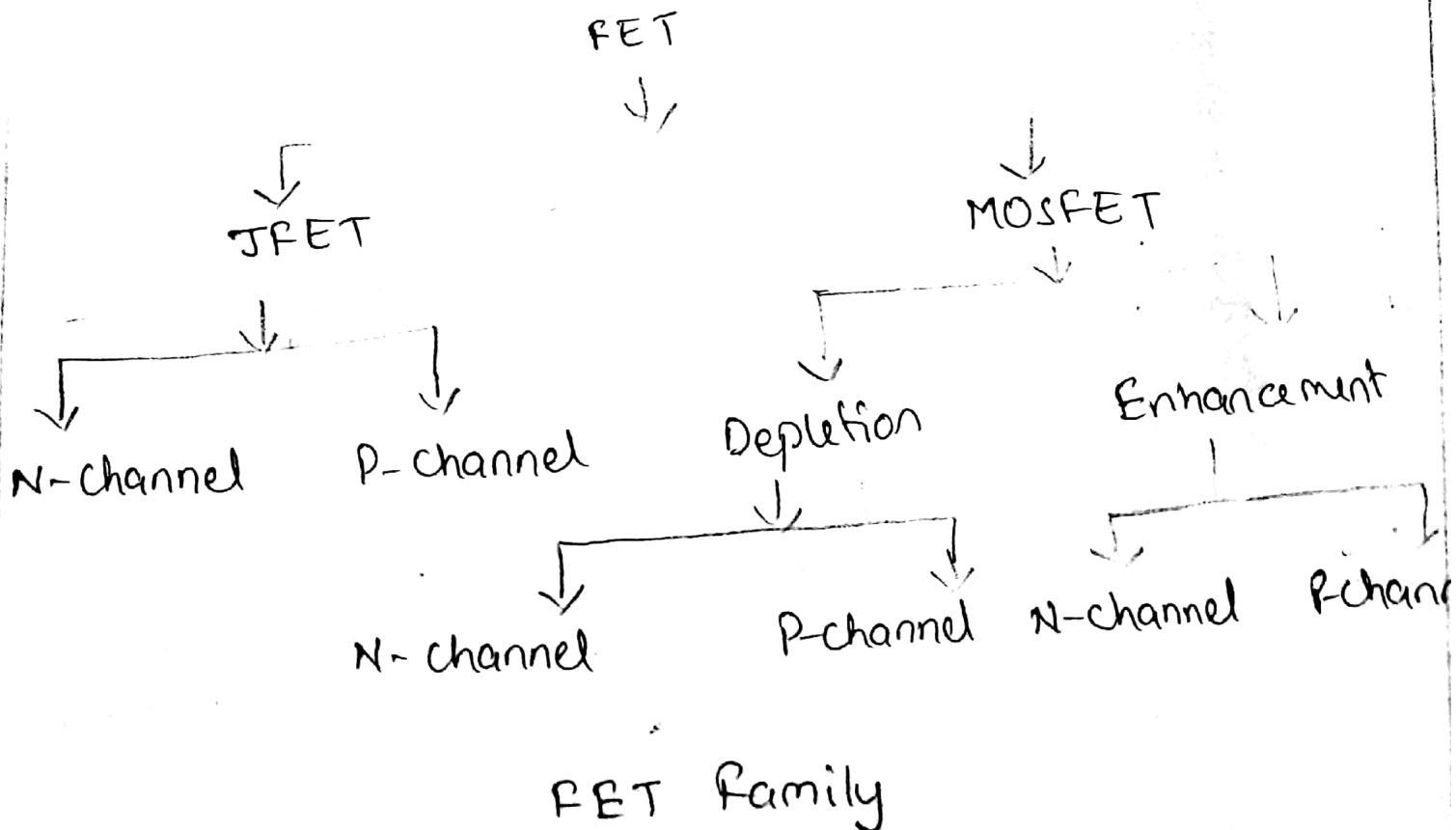


UNIT - V

1. Introduction to Field Effect Transistor (FET).

The Field Effect Transistor (FET). Like the bipolar junction transistor is a three terminal semiconductor device. However, the major functional difference between BJT & FET is that, the current through FET is controlled by voltage rather than by a current as in BJT. That is FET's are voltage-controlled devices. The base terminal of BJT draws a moderate current (1mA) from the signal source, so that internal resistance is low. But the corresponding gate terminal in FET draws no current and this gives, an extremely high input impedance, $10^7 - 10^{12}\Omega$. Unlike BJT, which is a bipolar device, the FET is a unipolar device. That is, FET operation depends upon the flow of majority carriers only.

The FET's are of two types. The JFET Transistor & the metal oxide semiconductor field Effect Transistor (MOSFET). The MOSFET is further divided into (i) depletion MOSFET & (ii) enhancement MOSFET. The FET family tree is shown below.



Features of FET :-

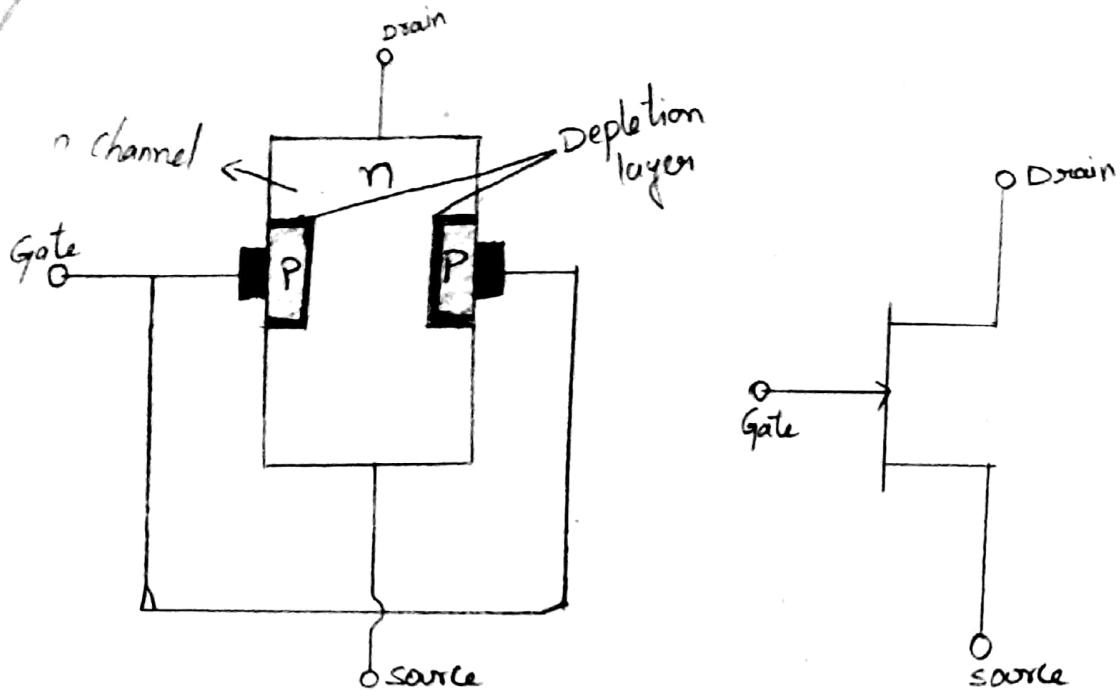
1. The operation of FET depends upon the flow of majority carriers only.
2. The input impedance of FET is very high, in the order of $M\Omega$.
3. The FET is less noisy than BJT.
4. It exhibits no offset voltage at zero drain current.
5. It is simple to fabricate.
6. It occupies less space in integrated circuits.

... Junction Field Effect Transistor (JFET) :

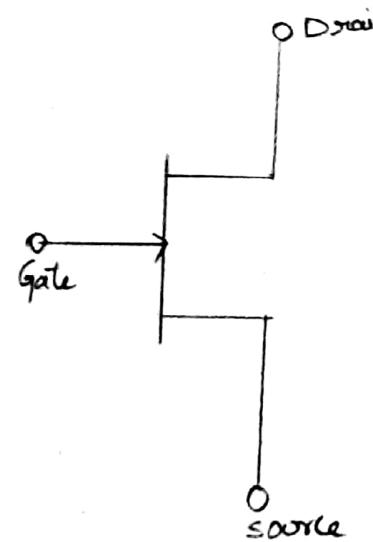
Construction.

The basic construction of the n-channel JFET is as follows. It consists of a n-type silicon bar surrounded by two small pieces of p-type material attached to its sides forming pn junctions. If the bar is of n-type the JFET functions as a n-channel JFET, & if the bar is of p-type it is called a p-channel JFET. The following figure shows schematic diagram of both types with their symbols.

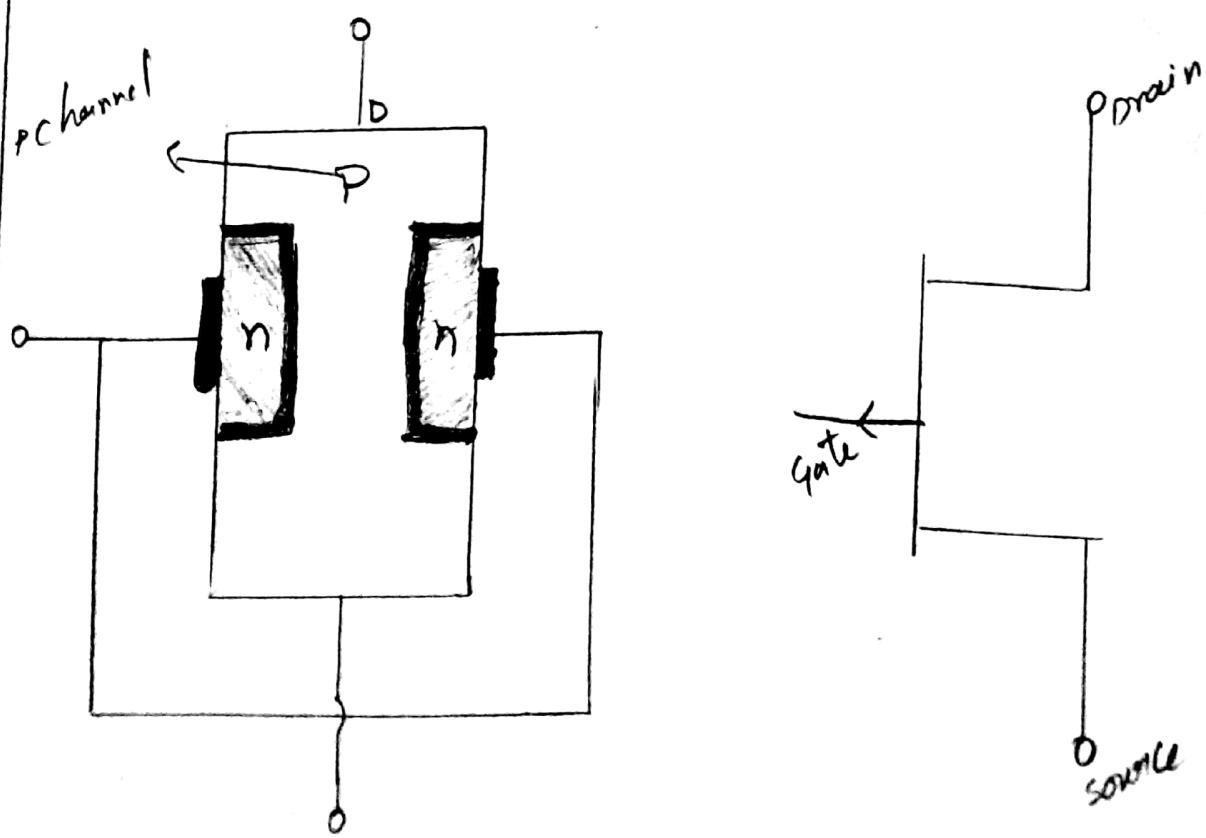
The channel ends are designated as source (S) and drain (D). The source 'S' is the terminal through which the majority carriers leave the bar. The two p-regions, which are formed by alloying or diffusion, are connected together and their terminal is called the gate. When no bias is applied to JFET, depletion regions are formed at two pn junctions as shown below. Recall that depletion region is a region depleted of charge carriers and therefore behaves as an insulator.



(a) *n* channel JFET



(b) symbol



JFET's and Their Symbols.

Operation of N-channel JFET.

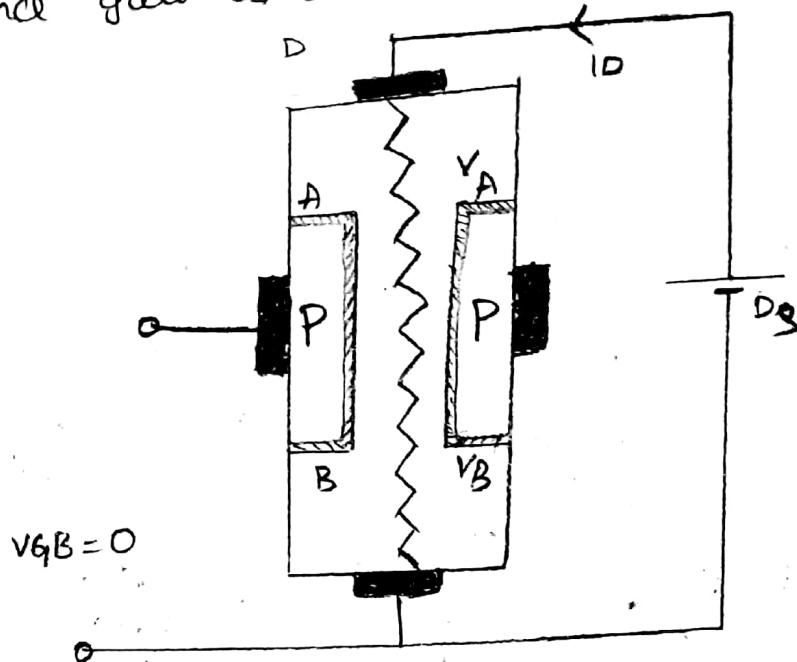
In this section we will study about the working of JFET for different biasing conditions.

1. When V_{DS} is some fixed positive value voltage is applied between the drain & source terminals. Due to this applied voltage electrons, will move through the n-type channel from source to drain, when the gate is negative biased with respect to source the pn junctions are reverse biased and depletion regions are formed. Since the channel is lightly doped compared to heavily doped region, the electrons penetrate deeply into the channel.

Q2: $V_{GS} = 0$, V_{DS} is varied

First assume that the gate source voltage (V_{GS}) is set to zero. When the drain source voltage V_{DS} is also zero the current flowing through FET is zero. That is $I_D = 0$. The instant the voltage V_{DS} is applied the electrons starts flowing from source to drain terminal, establishing the current I_D . Under this condition the channel between drain & source act as a resistance as shown below. The current I_D flowing through the channel cause a voltage drop between drain & source. Since gate is at zero potential and any point in the channel is at positive potential the gate-channel junction on the two sides are reverse biased. From below figure we can find that the voltage at a point A is more than the voltage at point B. Hence the upper region of P-type material is more reverse biased than the lower region. Recall that in a PN junction, the greater the applied reverse bias the wider the depletion region. Hence the depletion region is wider near the top of P material when compared to bottom P-region. As V_{DS} is increased there is further increase in the reverse bias applied to top of P-type material which further increases the width of the depletion regions from both sides. At some V_{DS} the depletion regions from two sides of the channel eventually meet at a point A as shown in following figure. At first glance, one is tempted to conclude, erroneously, that condition has been blocked since the channel has been pinched off.

NOTE :- Since gate is at zero,

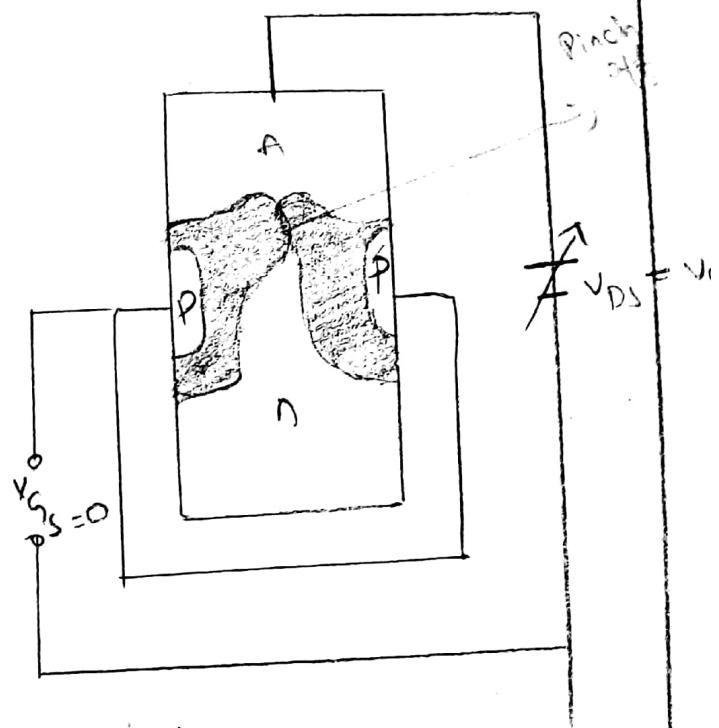
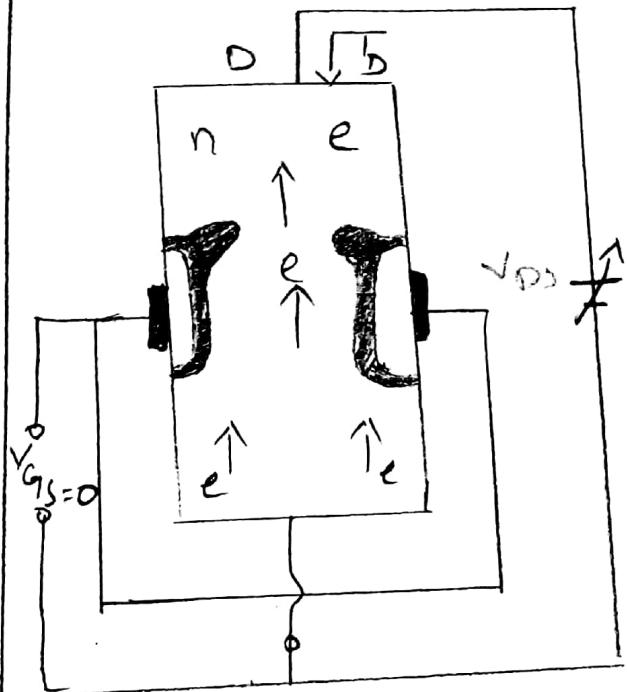


NOTE :- Since gate is at zero potential & any point in the channel is at positive potential the gate-channel junction on the two sides are reverse biased.

N-channel JFET, The Channel Behaving as a resistor

However, in reality a very small channel still exist, with a current of very high density and I_D maintains a saturation level. The drain current at this point with V_{DS} at zero is referred to as drain-source saturation current I_{DSs} . The drain-to-source voltage at which I_D reaches I_{DSs} is known as pinch-off voltage V_p . If V_{DS} is increased beyond V_p , I_D remains essentially same and JFET acts as a constant current source. If V_{DS} is increased further a stage is reached at which the gate-channel junction breaks down due to avalanche effect. At this point the drain current increases rapidly & the device may be destroyed.

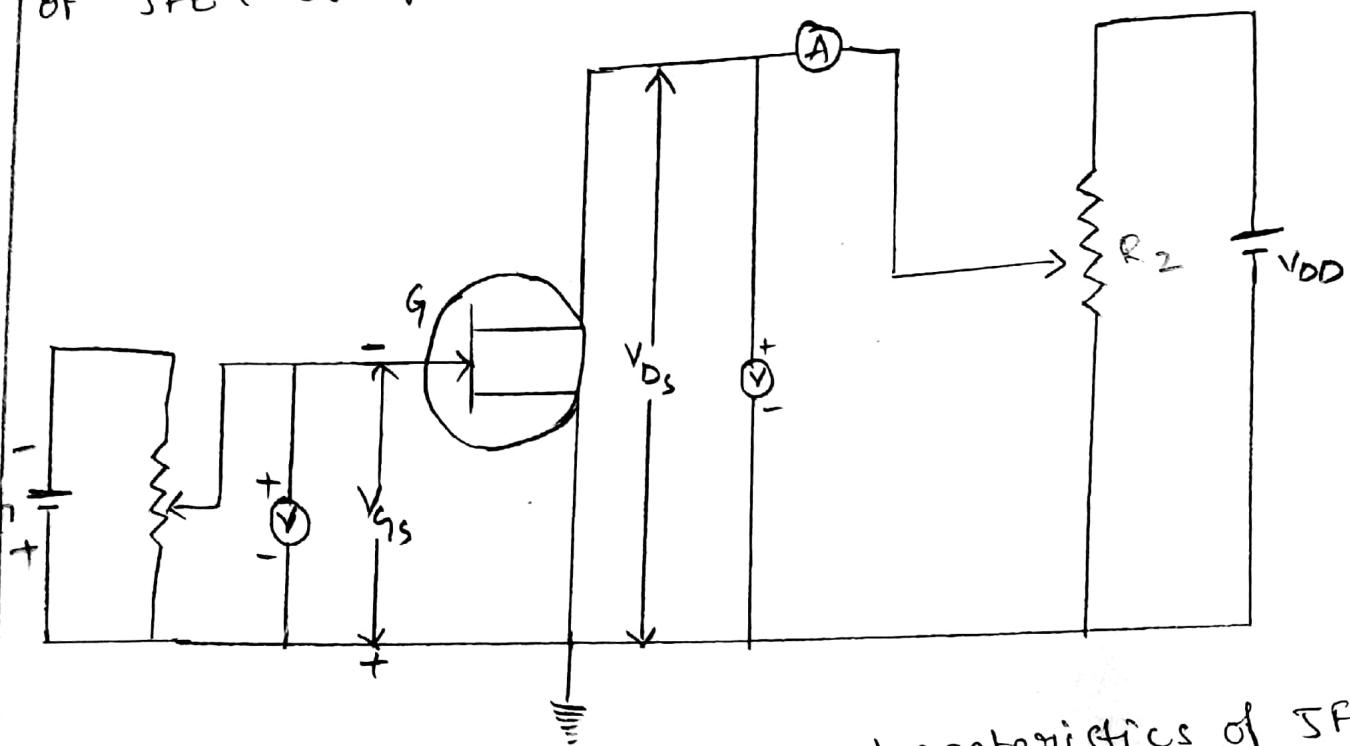
When an external bias say -1V is applied between the gate and source, the gate channel junction is reverse biased even when $V_{DS} = 0$ and the depletion region penetrates into the channel.



Working of N-channel JFET for
 $V_{GS} = 0$ and varied V_{DS} .

That is for same V_{DS} , the depletion region penetrates further and hence pinch-off voltage is reached at a lower I_D in case of $V_{GS} = -1V$ than when $V_{GS} = 0$. If V_{GS} is $V_{GS} = -1V$ than when $V_{GS} = 0$. If V_{GS} is increased further the pinch-off occurs at lower I_D and a stage is reached where $I_D = 0$. This happens when $V_{GS} = V_p$ (or $V_{GS(\text{off})}$)

4.15.3 Characteristic of JFET.
 The circuit diagram to obtain the characteristics of JFET as follows.



Circuit diagram to obtain characteristics of JFET
 The characteristics that we consider are

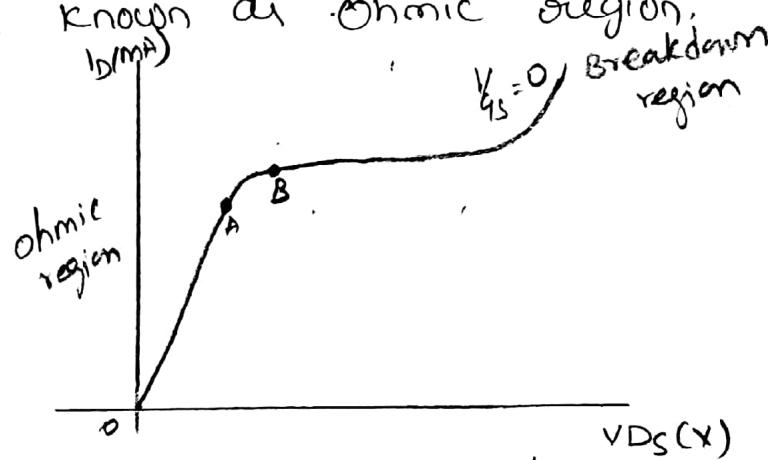
- (i) Drain characteristics
- (ii) Transfer characteristics

In drain characteristics the relation between I_D and V_{DS} for constant V_{GS} are different values of V_{GS} is plotted.

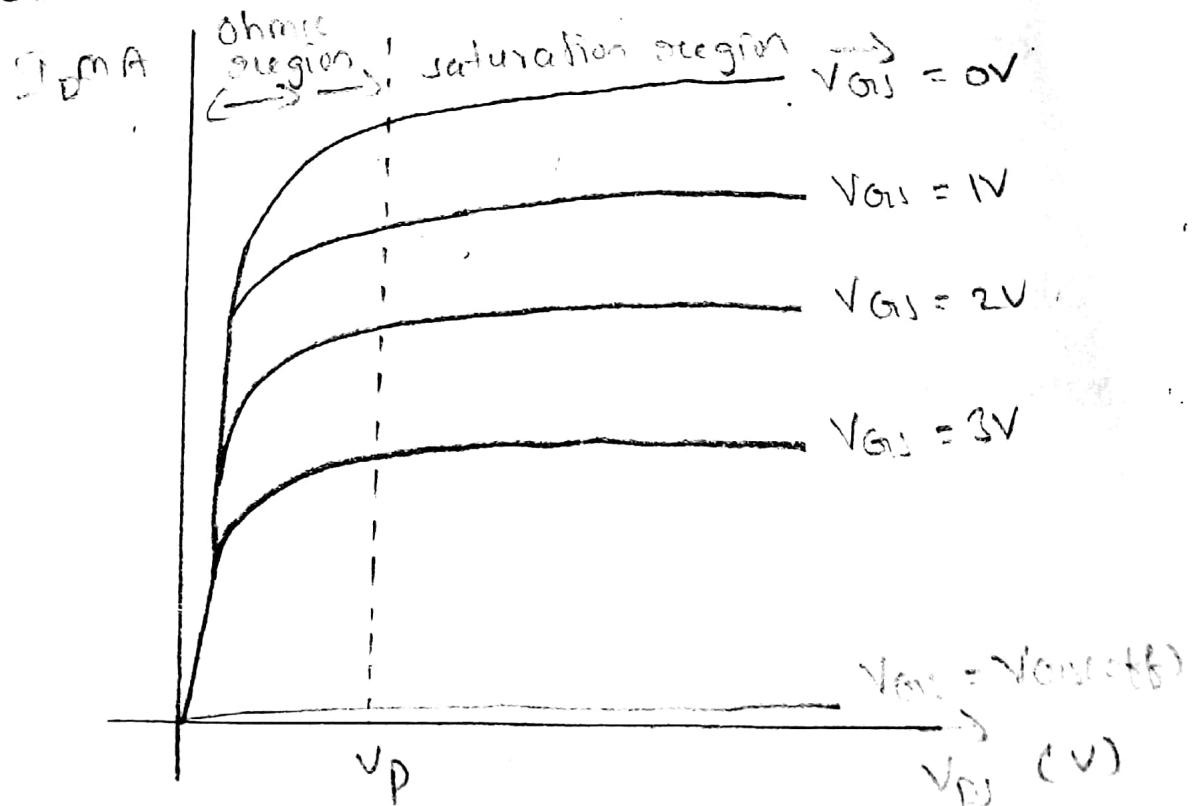
In transfer characteristics the relation between I_D and V_{GS} for constant V_{DS} are plotted.

JFET drain characteristics with $V_{GS} = 0$

The drain characteristic for $V_{GS} = 0$ is shown in figure. To plot this characteristic the gate to source voltage is kept at zero and V_{DS} is varied from zero. When V_{DS} is zero the drain current I_D is also zero. When V_{DS} is increased the drain current starts flowing through the channel and FET behaves like a resistor till point A. That is for low value of V_{DS} , current varies directly with voltage following Ohm's law... This portion of the characteristic where the FET behaves like a resistor is known as Ohmic region.



Characteristics of JFET for $V_{GS} = 0$



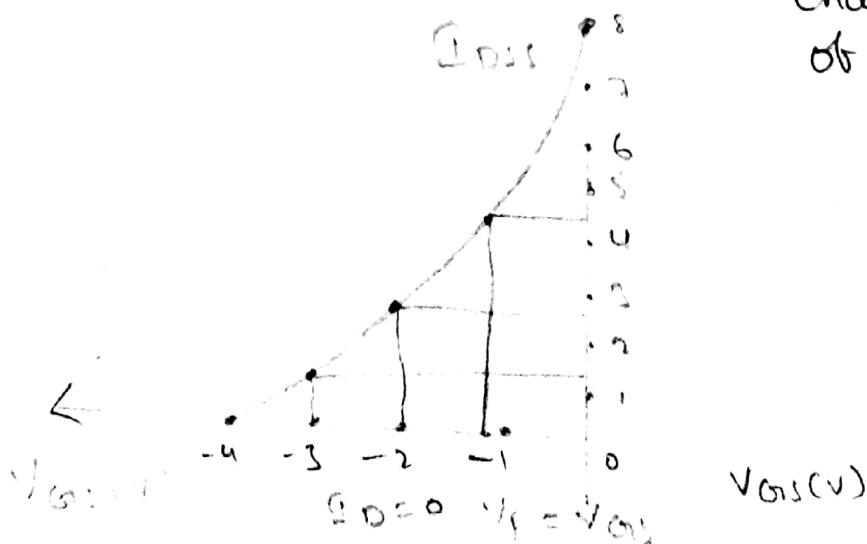
Characteristics of JFET for different values of V_{GS}

The FET can be used as a voltage variable resistor in this region. If we increase V_{DS} , a stage is reached at which pinch-off occurs and the drain current reaches a saturation level. The drain to source voltage at which pinch-off occurs is known as pinch-off voltage V_p and corresponding I_D is known as I_{DSS} . The point B at which pinch-off occurs is shown in the figure. Even if we increase V_{DS} further a stage is reached at which the gate channel junction of FET breakdown and I_D increases rapidly. This region in the characteristics is known as breakdown region. When an external bias (-V) is applied between gate and source the pinch-off occurs at less drain current less than I_{DSS} . The drain characteristics for different values of V_{GS} as shown in figure above.

4.15.4. Transfer characteristics.

It is a plot of drain current I_D versus V_{GS} for constant values of V_{DS} . To plot the characteristic V_{GS} is kept constant & and V_{DS} is varied, when $V_{GS} = V_{GS(\text{off})}$, the drain current flowing through FET is equal to I_{DSS} and when $V_{GS} \geq V_{GS(\text{off})}$, the drain current is zero.

Transfer characteristics of JFET



Shockley's equation.

The relation between V_{GS} and I_D can be represented by Shockley's equation,

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2$$

Using this mathematical expression, we can develop the plot of I_D versus V_{GS} for any JFET, provided the two parameters I_{DSS} and V_p are known.

4.16 JFET Parameters

The main parameters of JFET are

1. ac drain resistance.
2. Transconductance.
3. Current amplification factor.

1. ac drain resistance.

It is the ratio of change in drain source voltage to the change in drain current at constant gate-source voltage.

i.e.,

$$\text{ac drain resistance } r_d = \frac{\Delta V_{DS}}{\Delta I_D} \Big|_{V_{GS}} = \text{constant}$$

The ac drain resistance of a JFET has a larger value ranging from $10\text{k}\Omega$ to $1\text{m}\Omega$.

2. Transconductance.
It is the ratio of change in drain current to the change in gate-source voltage at constant drain-source voltage.

Transconductance.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \Big|_{V_{DS} = \text{constant}}$$

The Transconductance of JFET is usually expressed either in mA/volts or micromho. or Siemens (S).

3. Amplification factor.

It is the ratio of change in drain source voltage ΔV_{DS} to the change in gate source at constant drain current.

$$\text{Amplification factor } \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \Big|_{I_D = \text{constant}}$$

Relation among JFET parameters

$$\begin{aligned} \text{The Amplification factor } \mu &= \frac{\Delta V_{DS}}{\Delta V_{GS}} \\ &= \frac{\Delta V_{DS}}{\Delta I_D} \frac{\Delta I_D}{\Delta V_{GS}} \end{aligned}$$

$$\boxed{\mu = g_m r_d}$$

Amplification factor = ac drain resistance \times transconductance

4.17 Small Signal Model of JFET

From the operation of transistor we know that the drain current i_D is a function of gate source voltage V_{GS} and drain-source voltage V_{DS} . Hence we can write.

$$i_D = f(V_{GS}, V_{DS})$$

As both the gate and drain voltages are varied, the change in drain current is given by the first two terms in the Taylor's series expansion of equation,

$$\Delta i_D = \left. \frac{\partial i_D}{\partial V_{GS}} \right|_{V_{DS}} \Delta V_{GS} + \left. \frac{\partial i_D}{\partial V_{DS}} \right|_{V_{GS}} \Delta V_{DS}$$

In small signal notation the above equation can be written as

$$i_d = g_m V_{GS} + \frac{1}{r_d} V_{DS}$$

$$\text{where } g_m = \left. \frac{\partial i_d}{\partial V_{GS}} \right|_{V_{DS}} \text{ and } r_d = \left. \frac{\partial V_{DS}}{\partial i_d} \right|_{V_{GS}}$$

The parameter g_m is known as transconductance defined as the ratio of change in drain current to change in gate-source voltage keeping drain-source voltage constant. Similarly the parameter r_d is known as drain current for constant gate source voltage.

The amplification factor A_V is defined as the ratio of change in drain source voltage to change in gate source voltage.

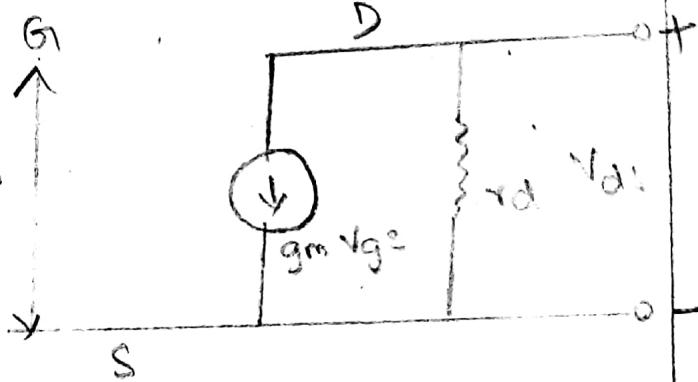
$$m = \frac{\partial V_{ds}}{\partial V_{gs}} = \frac{\partial V_{ds}}{\partial I_d} \cdot \frac{\partial I_d}{\partial V_{gs}}$$

$= r_d g_m$

$m = r_d g_m$

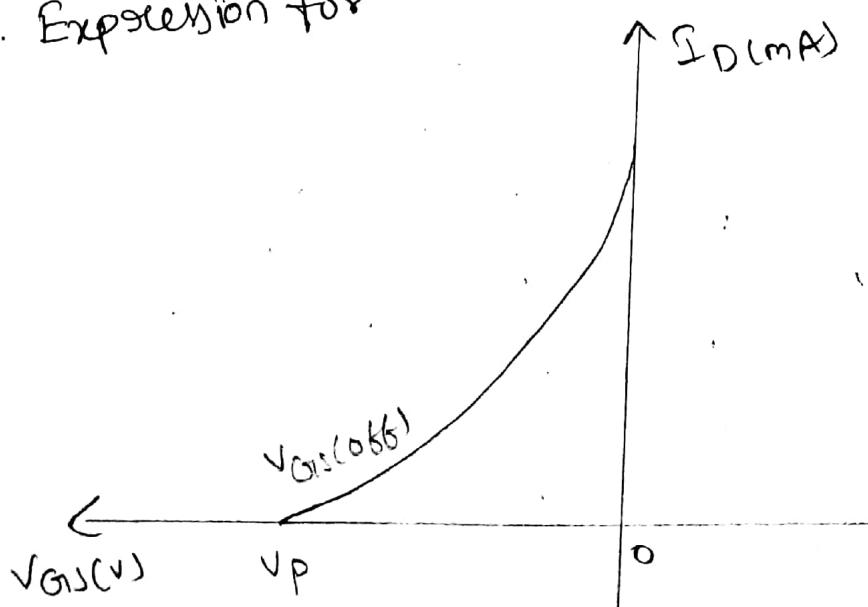
to find
source
voltage
(cont)

An FET circuit that satisfied equation is shown in figure. Since the input impedance of FET is very high it is represented by the open V_{gs} circuit at the input terminals. The current I_d is controlled by the gate source voltage. Hence a current source $g_m V_{gs}$ is connected from drain to source. The current source has its arrow pointing from drain to source.



small signal Model
for FET.

4.18. Expression for Saturation Drain Current.



Transfer characteristics of JFET.

To find transfer characteristics of JFET, the drain source voltage (V_{DS}) is kept constant and the gate source voltage (V_{GS}) is varied. For different values of V_{GS} , the corresponding drain current (I_D) is plotted. The gate source voltage V_{GS} is decreased from zero till I_D is reduced to zero. The transfer characteristic is shown in figure. The characteristics can be represented by Shockley's equation,

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2$$

where I_D is the drain current, I_{DSS} is the value of I_D when $V_{GS} = 0$ and V_p is pinch-off voltage.

The expression for saturation drain current can be obtained by differentiating with respect to V_{GS} .

$$\frac{\partial I_D}{\partial V_{GS}} = I_{DSS} \left[2 \left(1 - \frac{V_{GS}}{V_p}\right) \right] \left(\frac{-1}{V_p} \right)$$

$$= \frac{-2 I_{DSS}}{V_p} \left(1 - \frac{V_{GS}}{V_p}\right)$$

we know that $g_m = \frac{\partial I_D}{\partial V_{GS}}$ $V_{DS} = \text{constant}$

$$\therefore g_m = \frac{-2 I_{DSS}}{V_p} \left(1 - \frac{V_{GS}}{V_p}\right)$$

$$\text{at } V_{GS} = 0 \quad g_m = \frac{-2 I_{DSS}}{V_p} = g_{m0}$$

From the equation of Shockley's equation.

$$1 - \frac{V_{GS}}{V_p} = \sqrt{\frac{I_D}{I_{DSS}}}$$

Substituting the above equation in g_m

$$g_m = -2 \frac{I_{DSS}}{V_p} \sqrt{\frac{2D}{I_{DSS}}} = -2 \frac{I_D}{V_p} \sqrt{\frac{2D}{I_{DSS}}} = \frac{-2 I_D}{V_p}$$

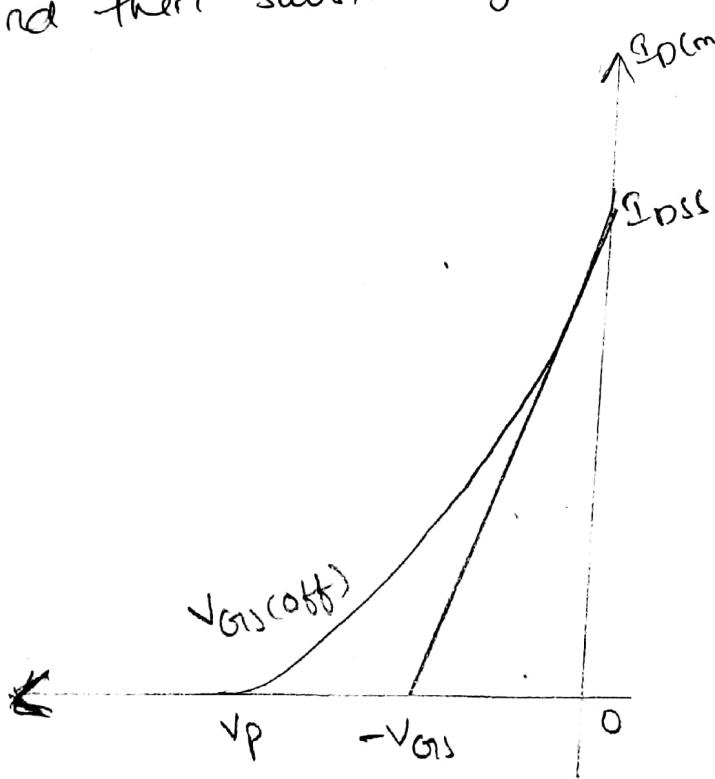
When $V_{GS} = 0$, $g_m = g_{m0}$

$$\Rightarrow g_{m0} = \frac{-2 I_{DSS}}{V_p}$$

From the previous equation of g_m , we can write

$$g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_p}\right)$$

4.19 Slope of the Transfer Characteristics at I_{DSS} .
 To find the slope of the transfer characteristics at I_{DSS} as shown in figure, the slope can be obtained by differentiating the equation representing by the transfer characteristics and then substituting $I_D = I_{DSS}$.



The Slope
 $= \frac{y_2 - y_1}{x_2 - x_1}$
 The point on I_D axis is
 $(0, I_{DSS})$

The point on V_{GS} axis is
 $(-V_{GS}, 0)$

The slope is $= \frac{I_{DSS}}{-V_{GS}}$

Transfer Characteristics of JFET with tangent drawn at I_{DSS}

We have

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2$$

The slope is

$$\begin{aligned} \frac{\partial I_D}{\partial V_{GS}} &= \frac{-2I_{DSS}}{V_p} \left(1 - \frac{V_{GS}}{V_p}\right) \\ &= \frac{-2I_{DSS}}{V_p} \sqrt{\frac{I_D}{I_{DSS}}} \end{aligned}$$

$$I_D = I_{DSS}$$

$$\frac{\partial I_D}{\partial V_{GS}} = \frac{-2I_{DSS}}{V_p} = \frac{I_{DSS}}{\left(\frac{-V_p}{2}\right)}$$

From the above equation we find that the tangent drawn to the curve at $I_D = I_{DSS}$ will have an intercept at $-\frac{V_p}{2}$ on the axis. Therefore to find the value of V_{GS} axis which is equal to V_p .

4.20 Comparison of BJT and FET.

1. In BJT, both majority and minority carriers contribute to current flow whereas in FET the current flow is carried by only one type of charge carriers.
2. BJT is a current controlled device. The current flowing in the base controls the collector current, $I_C = \beta I_B$. FET is a voltage controlled device. The voltage applied at the gate controls the current flowing through the channel.

3. FET's are much easier to fabricate than BJT.
4. FET gate currents are essentially zero, giving them input impedances that are far higher than that of BJT's. This makes it possible to build amplifier circuits having very high input impedance. The input impedance of BJT is comparatively low as some base current is required for operation.
5. The drain current of FET decreases with increasing temperature. That is the FET has a negative temperature coefficient. It prevents the FET from thermal runaway. But BJT has a positive temperature coefficient and hence subject to thermal runaway which leads to breakdown.
6. Construction of co-efficient BJT power transistor is much more difficult than FET power transistor.
7. FET circuit is superior to BJT in that there is no offset voltage with the FET turned on.
8. The FET chopper generally has a higher series resistance than the junction transistor.
9. FETs are less noisy than BJT.
10. FETs occupy less space than BJT.
11. In their active region FETs have much lower transconductance than BJT. In other words they have much lower gain than BJT. Hence it is more difficult to design high gain FET amplifier.
12. FET has relatively small gain bandwidth product when compared to BJT.
13. Minority carrier storage effects in BJT causes low switching speed. Since FET does not suffer from minority carrier effect it has higher switching speed.

4.21 Applications of JFET.

1. with its high input impedance, the FET play an important role in input circuit for instrument and audio applications.
2. FET can be used as voltage variable resistor in amplifiers.
3. The JFET can be used as level shifter between two operational amplifiers operated at different supply voltages.
4. The JFET can be used as nixie tube driver.

4.22 MOSFET

In previous section we studied the working of JFET. We know turn our attention to study the basic operation and characteristics of metal oxide semiconductor field effect transistor (MOSFET). The modes of operation of the MOSFET is divided into two types.

1. Depletion mode.
2. Enhancement mode

In depletion mode of operation the bias voltage on the gate reduce number of charge carriers in the channel and therefore reduce the drain current.

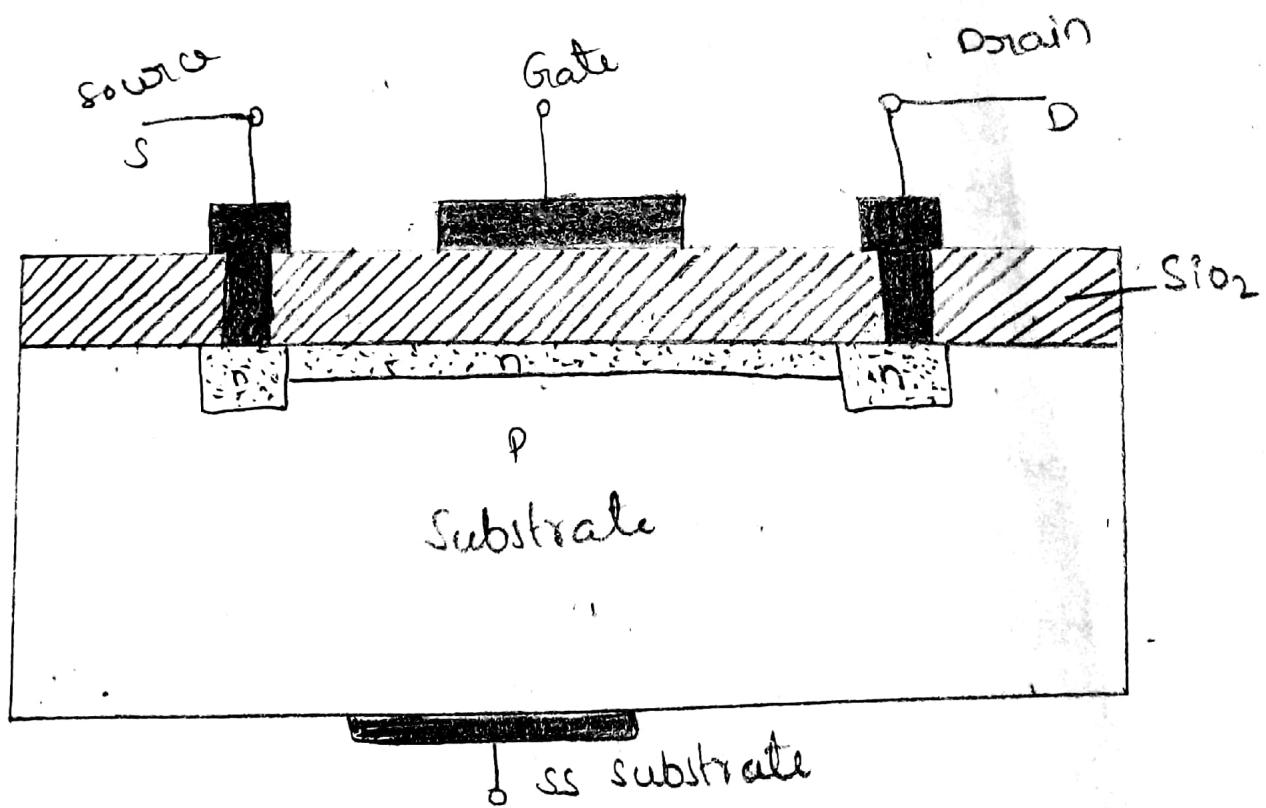
In enhancement mode of operation the bias

voltage on the gate increases the number of charge carriers in the channel and therefore increases the drain current.

In depletion MOSFET, operate in both depletion and enhancement modes whereas the enhancement MOSFET operate in enhancement mode only. In this section we study about depletion MOSFET.

4.23 Depletion MOSFET.

The construction of n-channel depletion MOSFET is shown in figure. It consists of a lightly doped P-type substrate in which two highly doped n-regions are diffused. The two heavily doped n-regions act as the source and drain. A lightly doped n-type channel is introduced between the two heavily doped source and drain. A thin layer of (1μm thick) silicon dioxide is coated on the surface. Holes are cut in the oxide layer to make contact with n-regions. Due to SiO_2 layer the gate is completely insulated from the channel. This permits operation with gate-source or gate-channel voltages above and below zero. In addition, the insulating layer of SiO_2 accounts for very high input impedance of MOSFET. In some MOSFETs the P-type substrate is internally connected to source, whereas in many devices an additional terminal is provided for substrate labeled SS.

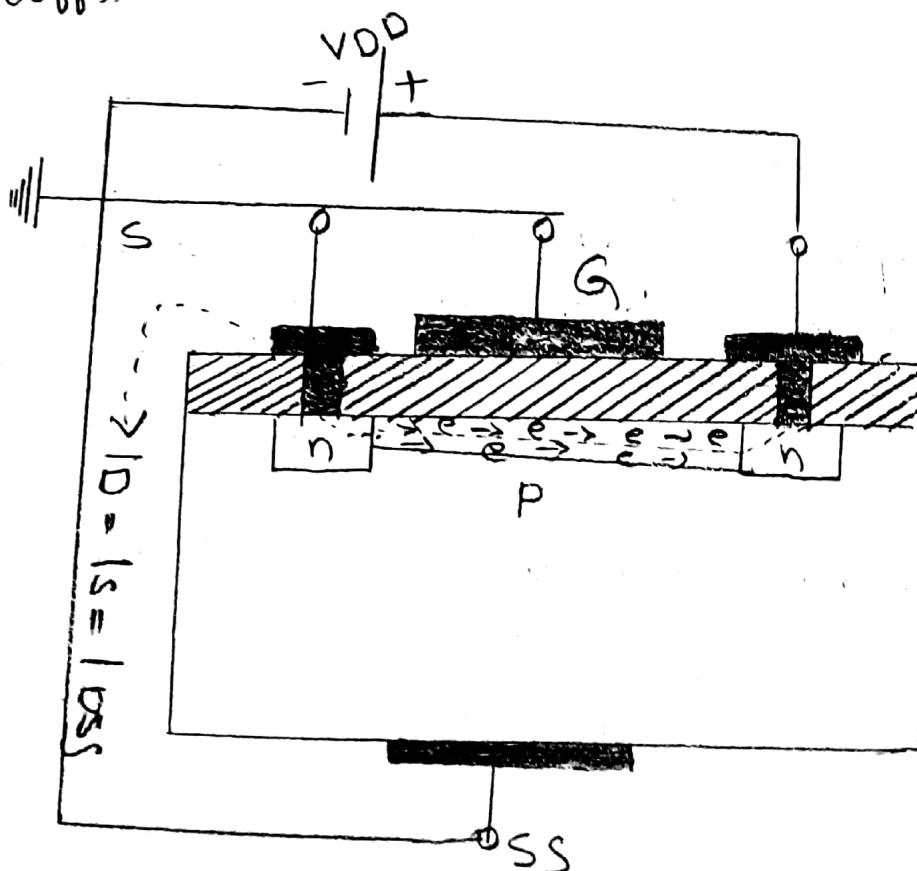


n-channel depletion MOSFET.

4.23.1 Basic Operation.

In the below figure a voltage V_{DS} is applied between the drain and source terminal and the gate-to-source voltage is set to zero. As a result, current is established from drain to source similar to that of JFET. Like in JFET, the saturated drain current I_{DSS} flows during pinch-off and it is labelled as I_{DSS} .

If a negative voltage is applied to gate with respect to source then holes are induced in the channel. These holes recombine with electrons and reduce the number of free electrons in the n-channel available for conduction. The more negative the bias, less the number of free electrons in the channel. Since the negative voltage on the gate deplete the channel the device is referred to as a depletion MOSFET. The depletion mode of operation is similar to JFET operation. When sufficient negative voltage is applied to gate the channel may be completely cutoff and the corresponding V_{GS} is called ($V_{GS(Off)}$).



If a positive voltage is applied to gate with respect to source then the electrons are induced in the channel. The induced electrons are induced to constitute additional current from source to drain. If we increase V_{GS} more in positive direction more number of electrons are induced, hence the drain current increases. That is the application of a positive gate-to-source voltage has enhanced the number of charge carriers compared to that when $V_{GS} = 0V$. For this reason the mode in which the MOSFET operates for positive values of gate-to-source voltage is known as enhancement mode.

4.23.2 Characteristics of depletion MOSFET.

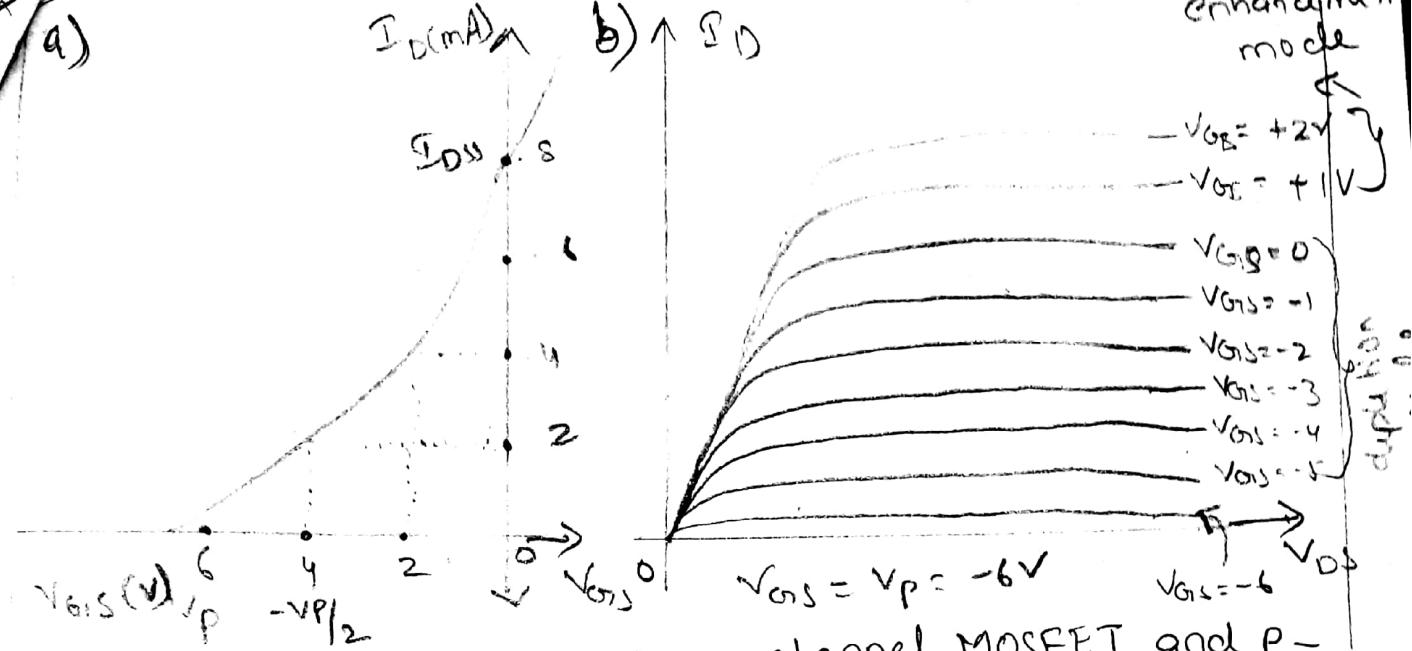
Drain characteristics.

It is a plot of drain current versus source voltage for various value of gate-source voltage. The drain characteristics of depletion MOSFET is similar to those N-channel JFET. If the gate is made positive additional carriers are introduced in the channel and the channel conductivity increases. Therefore, the depletion MOSFET consists of two regions of operation.

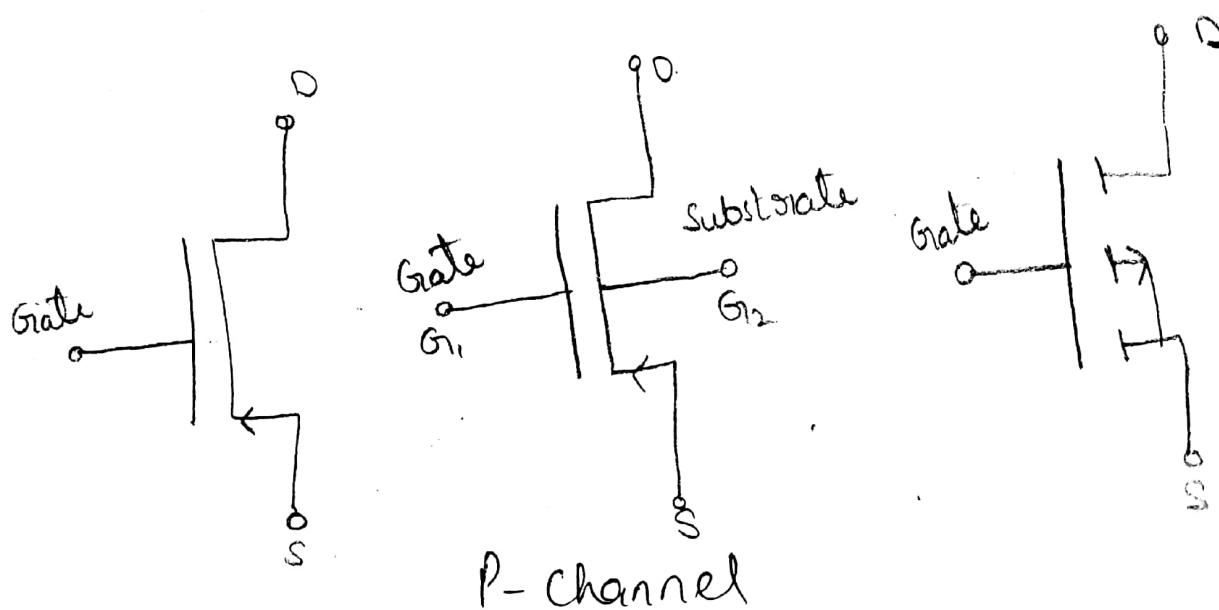
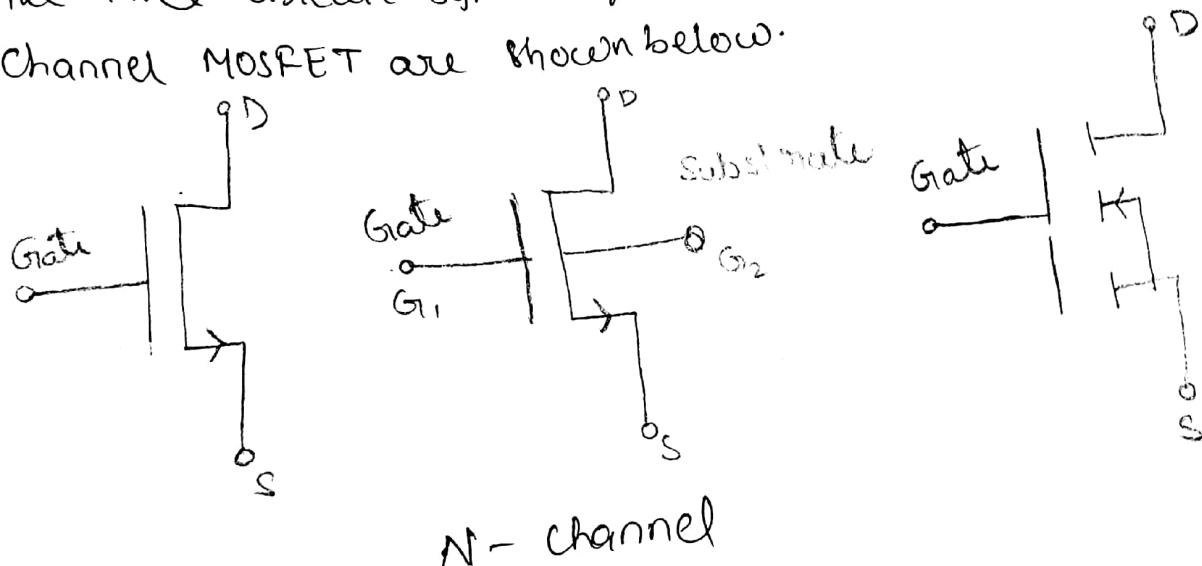
The transfer characteristics of depletion MOSFET is shown in the following figure. The general shape of the transfer characteristics is similar to those for the JFET. However the depletion MOSFET can be operated with $V_{GS} > 0$. As a result I_{DSS} is not maximum drain current as it is for JFET. The equation for the transfer characteristic curve of depletion MOSFET is same as that of JFET.

a) Transfer characteristics of N-channel depletion MOSFET.

b) Drain characteristics of N-channel depletion MOSFET



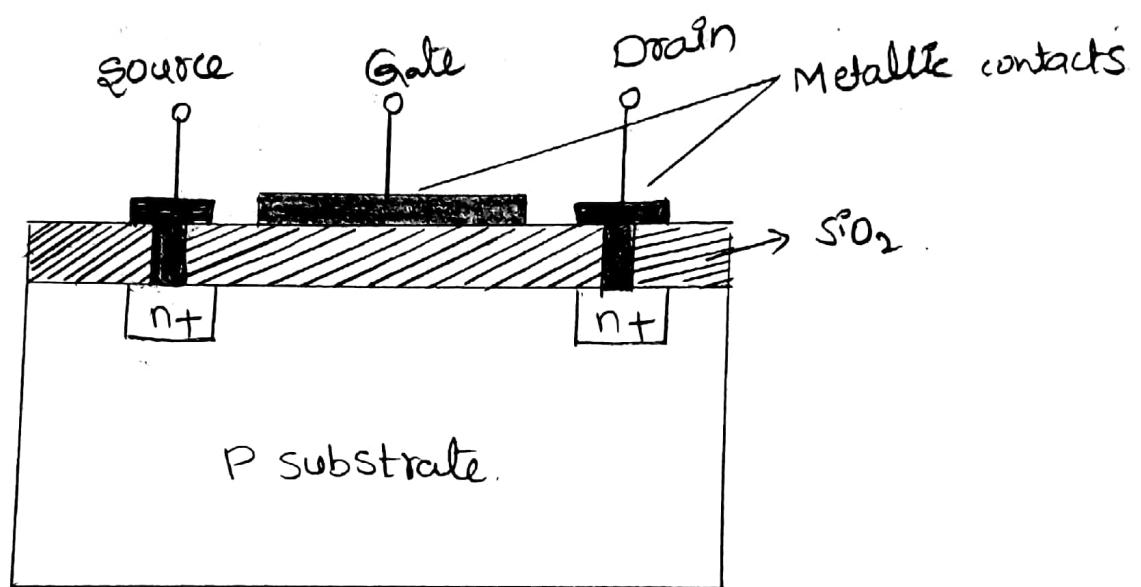
The three circuit symbols for n-channel MOSFET and p-channel MOSFET are shown below.



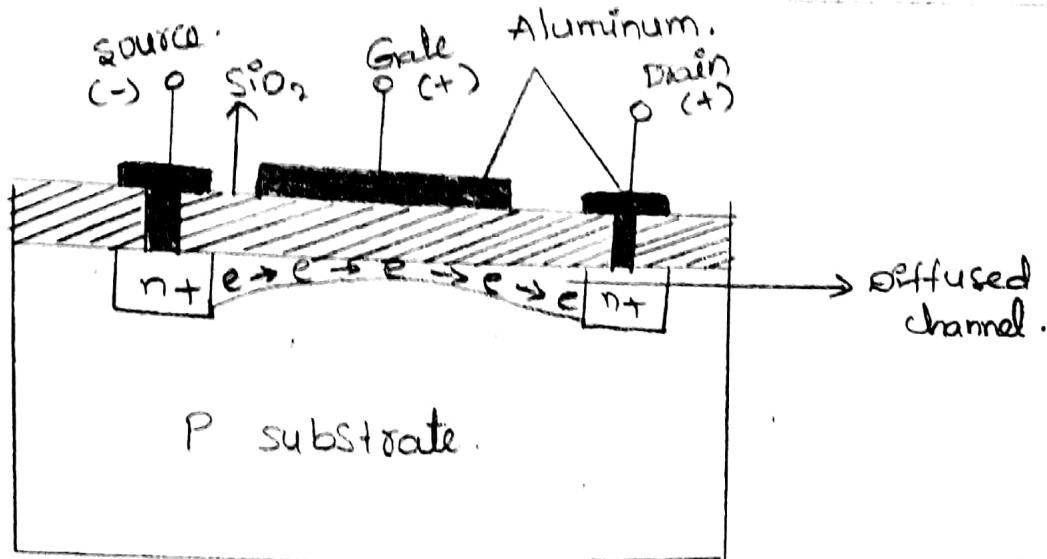
Symbol of N-channel and P-channel MOSFETs

4.24 Enhancement MOSFET.

The construction of n-channel enhancement MOSFET is shown in figure below. Like depletion MOSFET it also consists of a p-type substrate and two heavily doped n-regions that act as source and drain. The SiO_2 layer is present to isolate the gate from the region between the drain and source. The source and drain terminals are connected through metallic contacts to n-doped regions. But the enhancement MOSFET does not contain diffused channel between the source and drain.



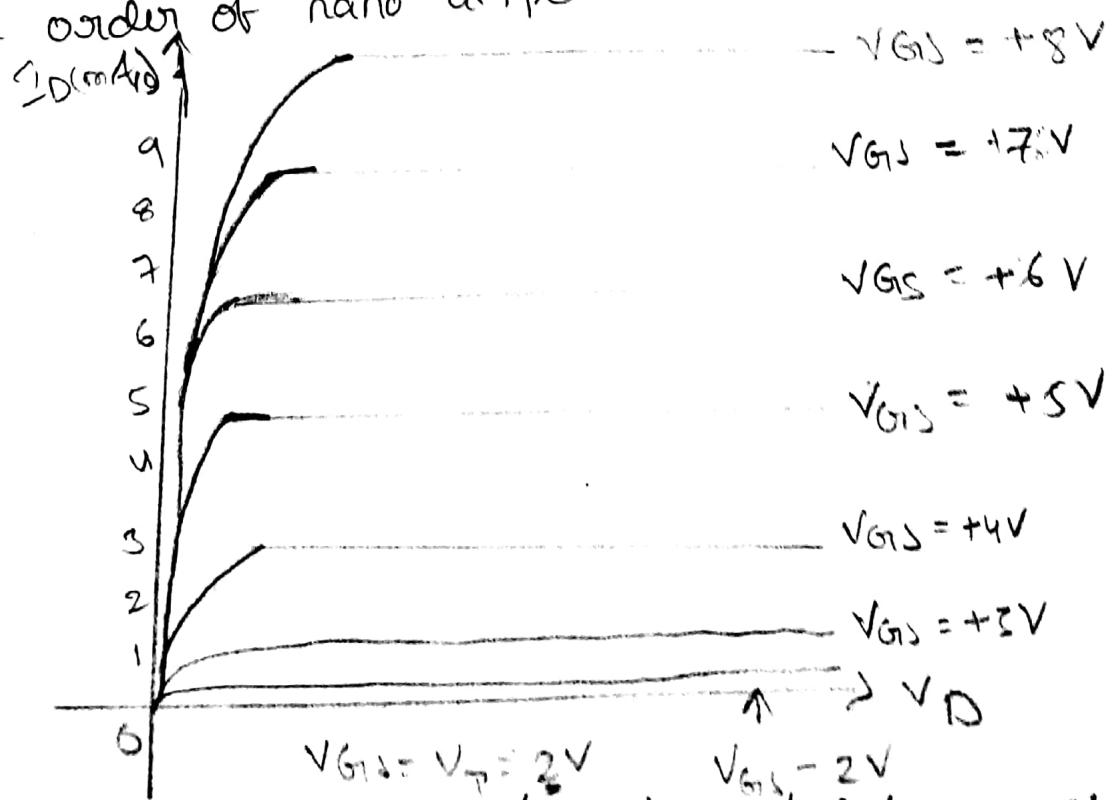
When the drain is made positive with respect to source and no potential is applied to gate, due to absence of the channel, a small drain current (i.e., a reverse leakage current) flows. If we apply a positive voltage to the gate with respect to source and substrate negative charge carriers are induced in the substrate. The negative charge carriers which are minority carriers in the p-type substrate form a "inversion layer". As the gate potential is increased more and more negative charge carriers are induced. These negative carriers that are accumulated between source and drain



constitute an n-type channel. Thus a drain current flows from drain to source through the induced channel. The magnitude of the drain current depends on the gate potential. Since the conduction of the channel is enhanced by the positive bias voltage on the gate the device is known as enhancement MOSFET.

4.24.1 Drain Characteristics.

The drain characteristics of enhancement MOSFET is shown below. The current I_{DSS} for $V_{GS} = 0$ is very small of the order of nano amperes shown below.

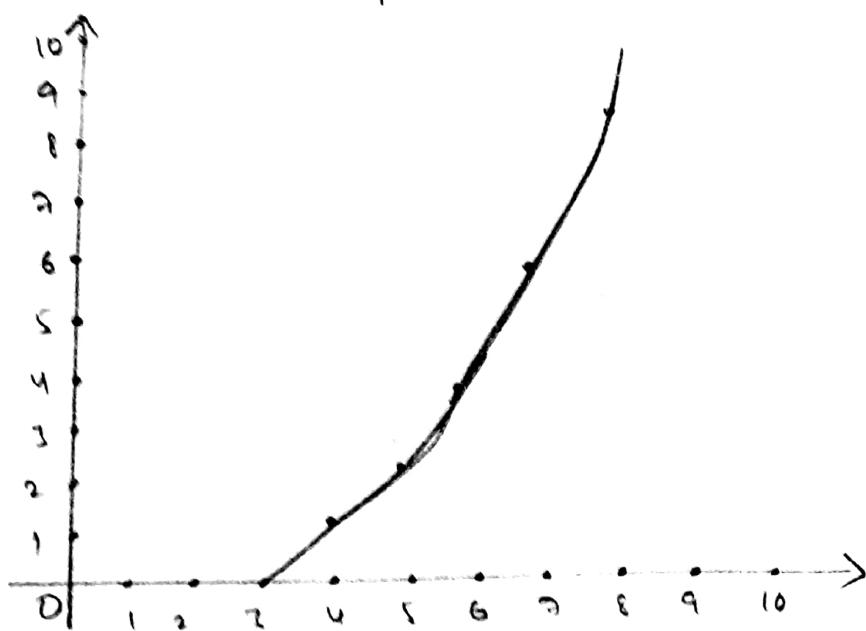


Drain characteristics of n-channel enhancement MOSFET.

NOTE : The drain current increases with positive increase in gate source bias voltage.

4.24.2 Transfer characteristic.

The n-channel enhancement MOSFET requires a positive gate to source voltage for its operation. Below figure shows the general transfer characteristics of n-channel MOSFET. Since the drain current is zero for $V_{GS} = 0$, the I_{DSS} is zero for this device. As V_{GS} is made positive the current I_D increases slowly at first and then more rapidly with an increase in V_{GS} . The gate source voltage at which there is significant increase in drain current is called the threshold voltage and is referred to as V_T or $V_{GS(th)}$. The equation for the transfer characteristics of enhancement MOSFET differs the curve starts at $V_{GS(th)}$ rather than V_{GS} . Here the equation for transfer characteristics is

$$I_D = K(V_{GS} - V_{GS(th)})^n$$


Transfer characteristic of n-channel enhancement MOSFET

4.25 Comparison between MOSFET and JFET.

JFET

1. The input resistance is the order of $10^9 \Omega$ since there is no insulating layer between gate and the conducting channel.
2. The gate leakage current is the order of 0.1 to 10 mA.
3. The drain resistance is the order of 0.1 to $1M\Omega$.
4. Electric field across the reverse biased pn junction controls the conductivity of the channel.
5. Operates only in depletion mode.
6. V_{GS} for an n-channel JFET cannot be allowed to go positive since that would forward bias the gate source p-n junction and cause a large gate current to flow.

MOSFET

1. The input resistance is very high in the order of $10^{13} \Omega$ due to presence of insulating layer between gate and conducting channel.
2. The gate leakage current is the order of 0.1 to 10 PA.
3. The drain resistance is the order of 1 to $50 K\Omega$.
4. Electric field across the insulating layer control the conductivity of the channel.
5. The depletion mode MOSFET operates both in enhancement & depletion modes.
 - Gate source voltage of a depletion mode MOSFET can be negative or positive.

In addition to above comparing to JFET, MOSFETs are easier to fabricate MOSFETs are widely used in digital VLSI circuits than JFETs. MOSFETs need special handling during installation.

- Handling Precautions for MOSFET.

The thin SiO_2 layer between the gate and the channel of MOSFET provide high input impedance to the device. But due to discharge of static electricity that accumulates on persons or surroundings, the very thin layer of SiO_2 at the gate breakdown and establish conduction through it. To avoid damage from electrostatic discharge, certain precautions should be taken when handling MOSFET.

1. MOSFET should be shipped and stored in conduction from rubber.
2. Prior to soldering, the technician should use a shorting strap to discharge his static electricity.
3. The soldering iron tip to be grounded.
4. MOSFETs should never be inserted into or remove from a circuit with the power ON.
5. The assembler should wear antistatic clothes and ground wrist bands.
6. All the instruments and metals benches used to test the MOS devices should be connected to ground.
7. Always avoid touching the device terminals and pick up the transistor by the casing.