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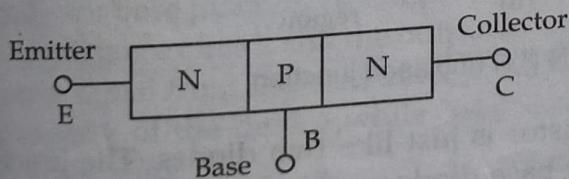
TRANSISTORS

6.1 THE BIPOLAR JUNCTION TRANSISTOR

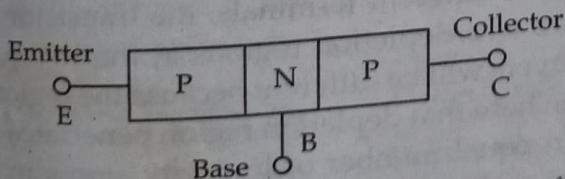
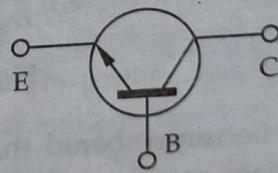
The transistor is a solid state device and is an essential ingredient of every electronic circuit. This is analogous to a vacuum triode. The main difference between a transistor and a vacuum triode is that transistor is a current device while a vacuum triode is a voltage device. The advantages of a transistor over a vacuum triode are long life, high efficiency, light weight, smaller in size, smaller power consumption, etc. The transistor was invented by John Bardeen and W.H. Brattain in 1948. A transistor is commonly known as Bipolar junction transistor (BJT). This is due to the fact that the current conduction in BJT is due to both types of charge carriers i.e., electrons and holes. Bipolar junction transistor is a three terminal, two junction device.

A junction transistor is simply a sandwich of one type of semiconductor material between two layers of the other type. Accordingly, there are two types of transistors: 1. N-P-N transistor and 2. P-N-P transistor.

When a layer of P type material is sandwiched between two layers of N-type material, the transistor is known as N-P-N transistor. This is shown in fig. [6.1 (a)]. Similarly, when a layer of N-type material is sandwiched between two layers of P-type material, the transistor is known as P-N-P transistor. This is shown in fig. [6.1 (b)]. Transistors are made either from silicon or germanium crystal. The symbols employed for N-P-N and P-N-P transistors are also shown in fig. (6.1).



(a) Structure and symbol of N-P-N transistor



(a) Structure and symbol of P-N-P transistor

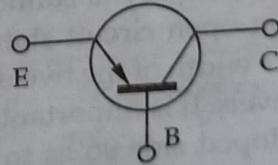


Fig. 6.1 N-P-N and P-N-P transistors

A transistor (N-P-N or P-N-P) has the following sections:

(i) **Emitter.** This forms the left hand section or region of the transistor. The main function of this region is to supply majority charge carriers (either electrons or holes) to the base and hence it is more heavily doped in comparison to other regions.

(ii) **Base.** The middle section of the transistor is known as base. This is very lightly doped and is very thin (10^{-6} m) as compared to either emitter or collector so that it may pass most of the injected charge carriers to the collector.

(iii) **Collector.** The right hand section of the transistor is called as collector. The main function of the collector is to collect majority charge carriers through the base. This is moderately doped.

Important points

- As regards the symbols, arrowhead is always at the emitter. The direction indicates the (conventional direction of current flow i.e., in case of N-P-N transistor it is from base to emitter (base is positive with respect to emitter) while in case of P-N-P transistor it is from emitter to base (emitter is positive with respect to base)).
- The emitter is heavily doped because it has to supply the majority carriers. The collector is less heavily doped. The base is lightly doped.
- In most of the transistors, the collector region is made physically larger than the emitter region. This is due to the fact that collector has to dissipate much greater power. Due to this difference, collector and emitter are not interchangeable. For the sake of convenience, it is customary to show emitter and collector to be of equal size.

6.1-1 UNBIASED TRANSISTOR

When no external supply is connected to a transistor, the transistor is said to be in unbiased condition. Fig. [6.1 (c)] shows an NPN unbiased transistor.

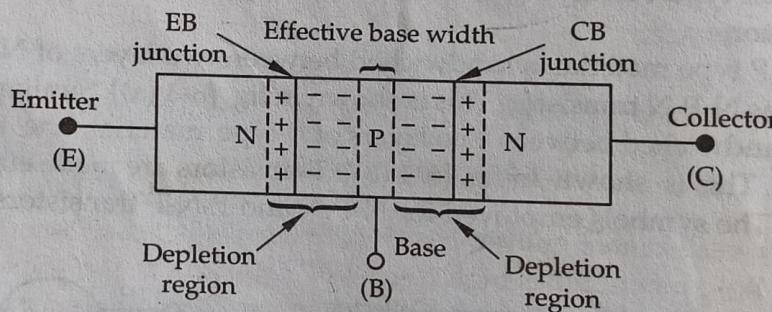


Fig. [6.1 (c)] N P N unbiased junction

It should be remembered that a transistor is just like two diodes. The junction between emitter and base may be called as emitter base diode or simply *emitter diode*. Similarly, the junction between base and collector may be called as collector base diode or simply *collector diode*. When no battery is connected between different terminals, the transistor is said to be unbiased or in open circuit state. There are two depletion regions at the two junctions of a transistor. The width of the two depletion layers will be different because the regions are doped at different levels. It is important to mention here that depletion region penetrates more deeply into lightly doped side so as to include an equal number of impurity atoms in each side of junction. Therefore, the depletion region at emitter junction penetrates less in heavily doped emitter and extends more in base region. Similarly, the depletion region at collector junction penetrates less in heavily doped collector and extends more in base region. So, the depletion layer formed at collector junction is larger than depletion layer formed at emitter junction.

6.1-2 TRANSISTOR BIASING

The transistor biasing is shown in fig. (6.2). The *emitter-base junction is always forward-biased while the collector base junction is always reverse-biased*. For this purpose a battery V_{EE} is

Transistors

connected between emitter and base while a battery V_{CC} is connected between collector and base. In fig. [6.2 (a)], the emitter-base junction of P-N-P transistor is forward-biased by connecting the positive terminal of V_{EE} to emitter and negative terminal to base. Similarly, in fig. [6.2 (b)], the emitter-base junction of N-P-N transistor is forward-biased by connecting the negative terminal of V_{EE} to emitter and positive terminal to base.

In fig. [6.2 (a)], the collector-base junction of a P-N-P transistor is reverse-biased by connecting the negative terminal of V_{CC} to collector while positive terminal to base. Similarly, in fig. [6.2 (b)], the collector-base junction of N-P-N transistor is reverse-biased by connecting the positive terminal of V_{CC} to emitter while negative terminal to base. The forward biasing of emitter-base junction allows a low resistance for emitter circuit and reverse-biasing of collector-base junction provides high resistance in the collector circuit.

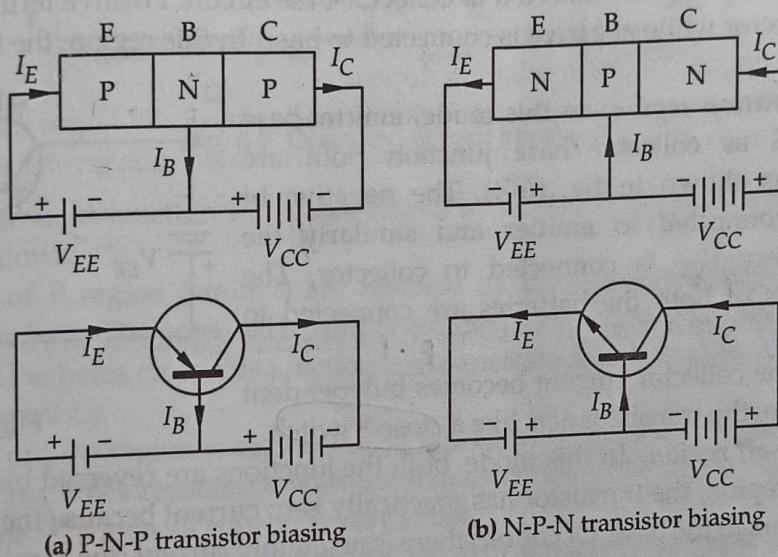


Fig. 6.2 Transistor biasing

We have seen that forward-biased emitter-base junction has a low resistance path whereas a reverse-biased collector base junction has high resistance path. In a transistor, a weak signal is introduced in low resistance circuit and the output is taken from the high resistance circuit. So a transistor transfers a signal from low resistance to high resistance. The prefix 'trans' means the signal transfer property of the device while 'istor' classifies as a solid element in the same general family with resistors.

6.1.3 DIFFERENT MODES OF OPERATION OF A TRANSISTOR

There are four possible ways of biasing a transistor. These are called as modes of operation of a transistor. These are listed below:

Cases	Emitter-base junction	Collector-base junction	Region of operation
I	Forward-biased	Reverse-biased	Active - amplifier
II	Forward-biased	Forward-biased	Saturation - closed switch
III	Reverse-biased	Reverse-biased	Cut-off - open switch
IV	Reverse-biased	Forward-biased	Inverted - inverter

Case I. Active region. In this mode, the emitter-base junction is forward-biased while collector-base junction is reversed-biased as shown in fig. (6.3). Here, we have considered the case of NPN transistor.

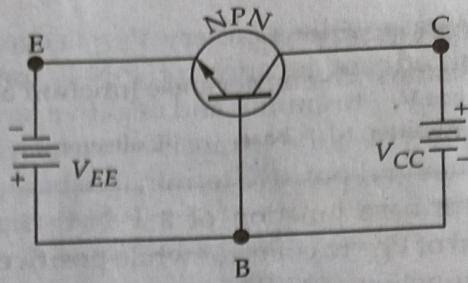


Fig. 6-3

In the emitter-base circuit, a battery V_{EE} is connected such that negative of the battery is connected to emitter while positive is connected to base.

Similarly, a battery V_{CC} is connected to collector-base circuit. Positive terminal of battery is connected to collector while negative is connected to base. In this region, the transistor is used for amplification.

Case II. Saturation region. In this mode, emitter-base junction as well as collector base junction both are forward-biased as shown in fig. (6.4). The negative of battery V_{EE} is connected to emitter and similarly the negative of battery V_{CC} is connected to collector. The positive terminals of both the batteries are connected to base.

In this case, the collector current becomes independent of base current. So, the transistor acts like a closed switch.

Case III. Cut-off region. In this mode, both the junctions are reverse-biased as shown in fig. (6.5). In this region, the transistor has practically zero current because the emitter does not emit charge carriers to the base. Of course, there is negligibly current due to minority carriers. In this situation, the transistor acts as open switch.

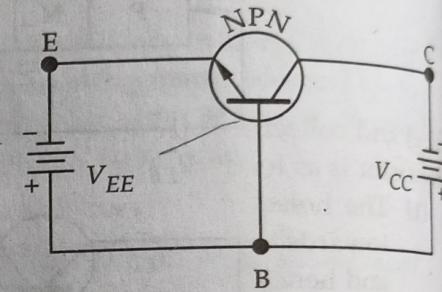


Fig. 6-4

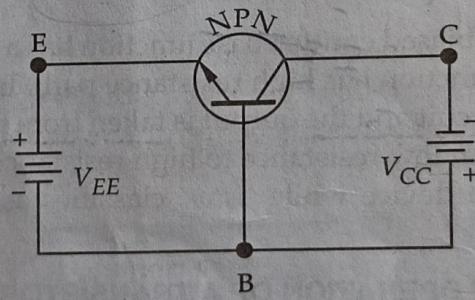


Fig. 6-5

Case IV. Inverted region. In this region, emitter-base junction is reverse-biased while collector base junction is forward-biased as shown in fig. (6.6). Here, the collector cannot inject the majority carriers into the base because the doping level of emitter and collector is not the same. In this region, the action of transistor is very poor.

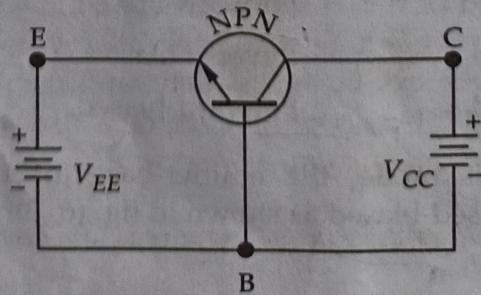


Fig. 6-6

6.2 OPERATION OF PNP TRANSISTOR

Figure (6.7) shows a PNP transistor with emitter-base junction as forward biased by dc source

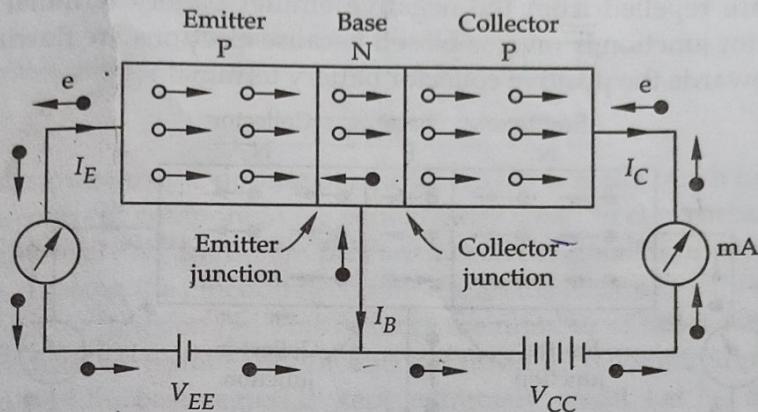


Fig. 6.7 Operation of PNP transistor

(V_{EE}) and collector-base junction as reverse-biased by dc source (V_{CC}). The operation of PNP transistor is as follows:

- (1) The holes of P region (emitter) are repelled by the positive terminal of battery V_{EE} towards the base. The potential barrier at emitter junction is reduced as it is forward bias and hence the holes cross this junction and penetrate into N -region. This constitute the emitter current I_E .
- (2) The width of base region is very thin and it is lightly doped and hence only two to five percent of the holes recombine with the free electrons of N -region. This constitute the base current I_B , which, of course, is very small.
- (3) The remaining holes (95% to 98%) are able to drift across the base and enter the collector region. They are swept up by the negative collector voltage V_{CC} . This constitutes the collector current I_C .
- (4) As each hole reaches the collector electrode, an electron is emitted from the negative terminal of battery and neutralizes the hole. Now, a covalent bond near the emitter electrode breaks down. The liberated electron enters the positive terminal of battery V_{EE} while the hole immediately moves towards the emitter junction. This process is repeated again and again.

Important Points

- (i) Current conduction within PNP transistor takes place by hole conduction from emitter to collector i.e., majority charge carriers in a PNP transistor are holes. The conduction in the external circuit is carried out by electrons.
- (ii) The collector current is slightly less than the emitter current. This is due to the fact that 2 to 5% of the holes are lost in recombination with electrons in base region. Thus the collector current is slightly less than emitter current.
- (iii) The collector current is a function of emitter current i.e., with the increase or decrease in the emitter current, a corresponding change in collector current is observed.

Beside hole current, there is electron current which flows from base region to emitter region. This current depends upon emitter-base potential. As the width of the base region is very small, the ratio of hole current to electron current is very small. So, for all practical purposes, the electron current may be neglected.

Thus only the hole current plays the important role in the operation of PNP transistor.

6.3 OPERATION OF NPN TRANSISTOR

The biasing of a NPN transistor is shown in fig. (6.8). The emitter junction is forward-biased because electrons are repelled from the negative emitter battery terminal V_{EE} towards the junction. The collector junction is reverse-biased because electrons are flowing away from the collector junction towards the positive collector battery terminal V_{CC} .

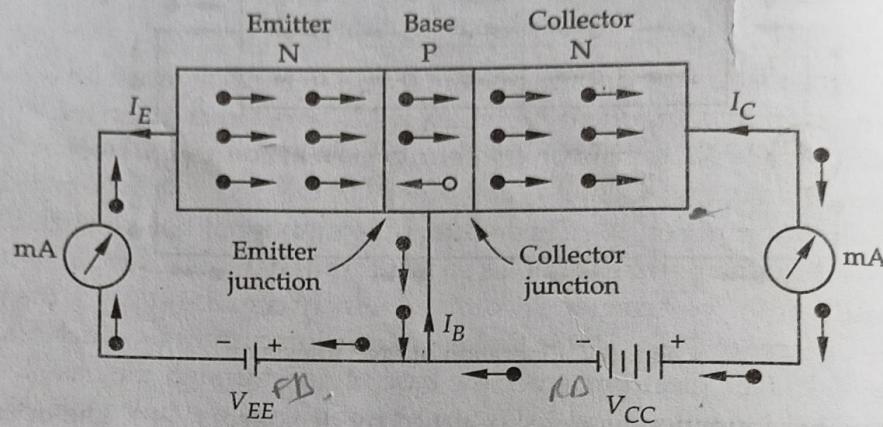


Fig. 6.8 Operation of NPN transistor

The operation of NPN transistor is as follows: —

- (1) The electron in the emitter region are repelled from the negative terminal of battery towards the emitter junction. Since, the potential barrier at the junction is reduced due to forward bias and base region is very thin and lightly doped, electrons cross the P-type base region.
- (2) A few electrons combine with the holes in P-region and are lost as charge carrier.
- (3) Now the electrons in N-region (collector region) readily swept up by the positive collector voltage V_{CC} .
- (4) For every electron flowing out the collector and entering the positive terminal of battery V_{CC} , an electron from the negative emitter battery terminal enters the emitter region. In this way electron conduction takes place continuously so long as the two junctions are properly biased.

So the current conduction in NPN transistor is carried out by electrons.

6.4 CURRENT COMPONENTS IN A TRANSISTOR

Figure (6.9) shows the various current components which flow across the forward-biased emitter junction and reverse-biased collector junction in PNP transistor.

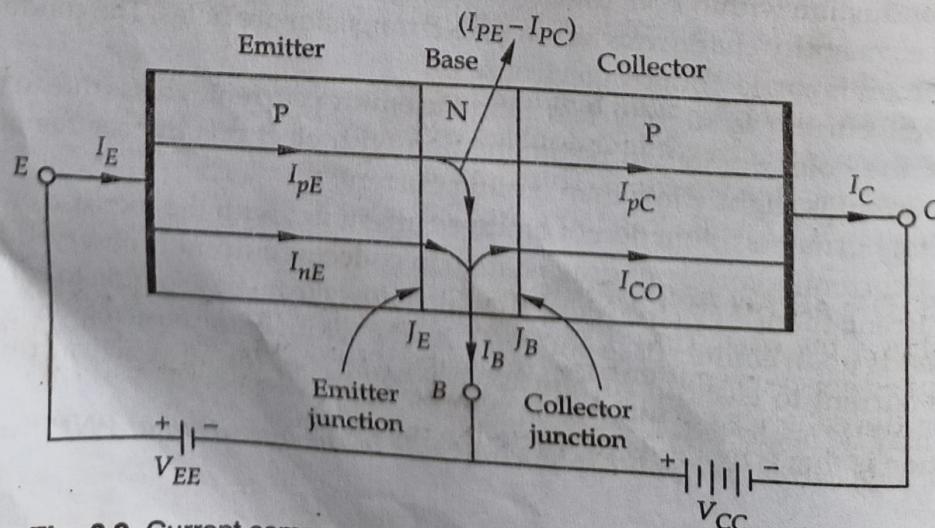


Fig. 6.9 Current components in a transistor with forward-biased emitter and reverse-biased collector

The emitter current consists of the following two parts:

- (i) Hole current I_{pE} constituted by holes (holes crossing from emitter into base),
- (ii) Electron current I_{nE} constituted by electrons (electrons crossing from base into the emitter).

\therefore Total emitter current

$$I_E = I_{pE} + I_{nE}$$

Majority Minority

In commercial transistors the doping of emitter region is made much heavier than base and hence the electron current component I_{nE} is negligibly small in comparison with hole current I_{pE} . Thus in a commercial PNP transistor, *the emitter current consists almost entirely of holes.*

A few of holes crossing the junction J_E combine with the electrons in N-type base and rest of them cross the collector junction J_C . This reduces the number of holes which ultimately reach the collector. To reduce the number of holes so lost through recombination with electrons in N-region, the width of the base region is kept extremely small. Let I_{pC} is the hole current at junction J_C . The difference ($I_{pE} - I_{pC}$) is the recombination current I_B which leaves the base as shown in fig. (6.9) In fact, electrons enter the base region through the base lead to replenish those electrons which have been lost by recombination with the holes injected into the base across J_E . The holes on reaching the collector junction cross this junction readily and enter the P-region of the collector.

If the emitter were open-circuited, then $I_E = 0$ i.e., I_{pC} would be zero. Under this condition, the base and collector together act as a reversed diode and the collector current I_C equals the reverse saturation current I_{CO} , which consists of the following two parts:

I_{nCO} caused by electrons moving across J_C from P-region to N-region.

I_{pCO} caused by holes moving across J_C from N-region to P-region.

$$I_{CO} = I_{nCO} + I_{pCO} \quad \dots(2)$$

In general

$$I_C = I_{pC} + I_{CO}$$

Majority Minority \quad \dots(3)

Thus for a PNP transistor

$$I_E = I_B + I_C \quad \dots(4)$$

Important points

Although both silicon and germanium are used in semiconductor devices but generally silicon is used due to the following reasons:

- (i) *Smaller I_{CBO} .* A silicon crystal has fewer free electrons than germanium crystal at room temperature. This shows that silicon will have much smaller collector cut-off current (I_{CBO}) than that of germanium.
- (ii) *Smaller variation of I_{CBO} with temperature.* I_{CBO} approximately doubles with each 8 to 10°C rise in germanium while it doubles with each 12°C rise for silicon.
- (iii) *Greater working temperature.* The normal working temperature of germanium is approximately 70°C while it is 150°C in case of silicon.

6.5 TRANSISTOR AS AN AMPLIFIER

Figure (6.10) shows the basic circuit of a transistor amplifier. Here, the weak signal to be amplified is applied between emitter-base circuit and the output is taken across the load resistor R_L connected in the collector circuit. A d.c. voltage V_{EE} is also connected in the input circuit. Now, the question is that why V_{EE} is connected in the circuit?

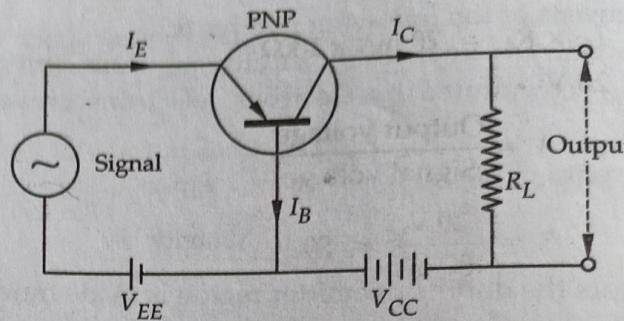


Fig. 6-10

Let, for the instant, V_{EE} is not connected in the circuit. Now for the negative peak of the applied signal, the emitter-base junction will be reverse-biased. This is not desirable because to achieve faithful amplification, the input circuit should always remain forward biased. For this purpose, emitter bias battery V_{EE} of such a magnitude that input circuit is always forward-biased regardless of the polarity of the signal is connected.

A small change in signal voltage produces an appreciable change in emitter current because the input circuit has low resistance. Now, due to the transistor action, the change in emitter current causes almost the same change in collector current. When the collector current flows through the load resistance R_L , a large voltage is developed across it. In this way, a weak signal applied in the input circuit appears in the amplified form across the output circuit.

Let a small voltage change ΔV_i between emitter and base causes a relatively large emitter-current change ΔI_E . We define by the symbol α that fraction of this current change which is collected and passes through R_L . Thus

$$\alpha = \frac{\Delta I_C}{I_E} \quad \text{i.e., } \Delta I_C = \alpha \cdot \Delta I_E$$

The change in output voltage across the load resistor

$$\begin{aligned}\Delta V_o &= R_L \times \Delta I_C \\ &= R_L \times \alpha \times \Delta I_E\end{aligned}$$

Under these circumstances, the voltage amplification

$$A = \frac{\Delta V_o}{\Delta V_i}$$

will be greater than unity and the transistor acts as an amplifier. If the dynamic resistance of the emitter junction be r_e , then $\Delta V_i = r_e \cdot \Delta I_E$

∴

$$A = \frac{R_L \times \alpha \times \Delta I_E}{r_e \cdot \Delta I_E}$$

or

$$A = \frac{\alpha R_L}{r_e}$$

Example A common base transistor amplifier has an input resistance of 20Ω and output resistance of $100 \text{ k}\Omega$. If a signal of 400 mV is applied between emitter and base, find voltage amplification. Assume α_{ac} to be nearly one.

The emitter current is given by

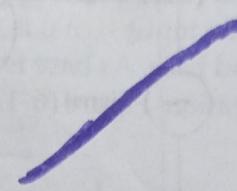
$$I_E = \frac{\text{Signal voltage}}{\text{Input resistance}} = \frac{400 \text{ mV}}{20 \Omega} = 20 \text{ mA}$$

$$I_C = \alpha I_E = 1 \times 20 \text{ mA} = 20 \text{ mA}$$

$$\text{Output voltage, } V_0 = I_C \times R_L = 20 \text{ mA} \times 1 \text{ k}\Omega = 20 \text{ V}$$

$$\therefore \text{Voltage amplification, } A = \frac{\text{Output voltage}}{\text{Signal voltage}}$$

$$\text{or } A = \frac{20 \text{ V}}{400 \text{ mV}} = 50$$



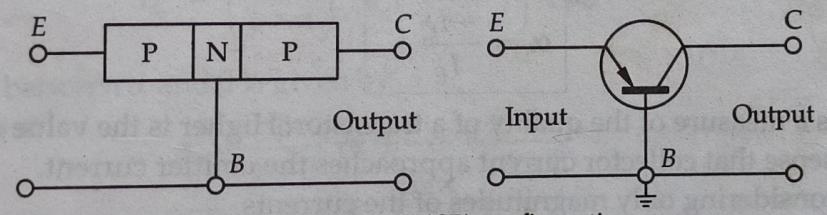
6.6 TRANSISTOR CIRCUIT CONFIGURATIONS

Following are the three types of transistor circuit configurations:

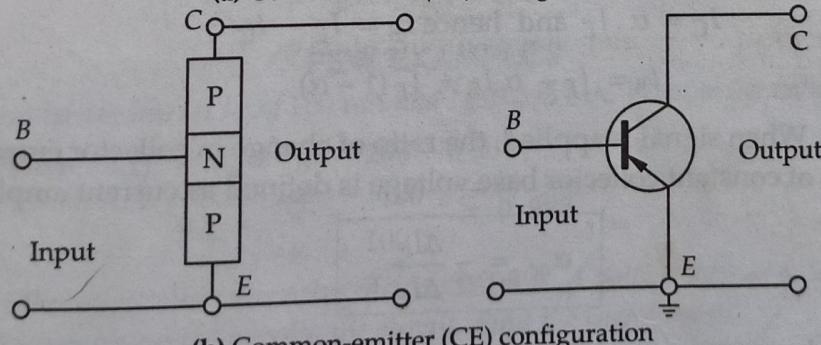
- (1) Common-base (CB)
- (2) Common-emitter (CE)
- (3) Common-collector (CC)

Here the term 'common' is used to denote the transistor lead which is common to the input and output circuits. This is because when a transistor is connected in a circuit, four terminals are required (two for input and two for output) while a transistor has only three terminals. This difficulty is removed by making one terminal of the transistor 'common' to both input and output terminals. The common terminal is generally grounded.

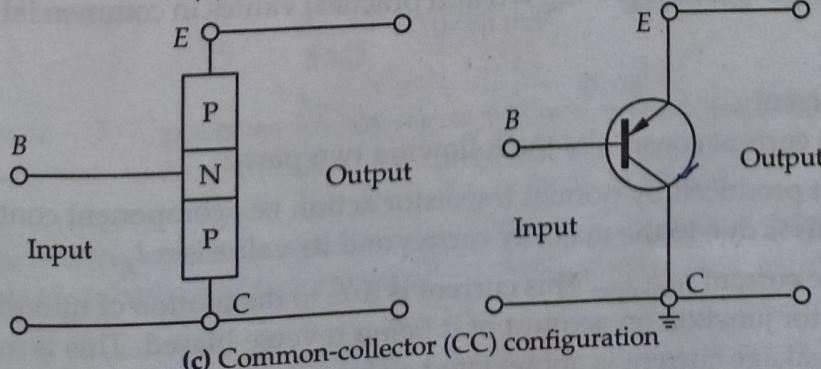
Each configuration has specific advantages and disadvantages. It should be remembered that regardless the circuit configuration, the emitter is always forward-biased while the collector is always reverse-biased. The different configurations of a PNP transistor are shown in fig. (6.11).



(a) Common-base (CB) configuration



(b) Common-emitter (CE) configuration



(c) Common-collector (CC) configuration

Fig. 6.11 Different configurations of PNP transistor

6.7 COMMON-BASE (CB) CONFIGURATION

In this configuration, the input signal is applied between emitter and base while the output is taken from collector and base. As base is common to input and output circuits, hence the name common-base configuration. Figure (6.12) shows the common-base PNP transistor circuit.

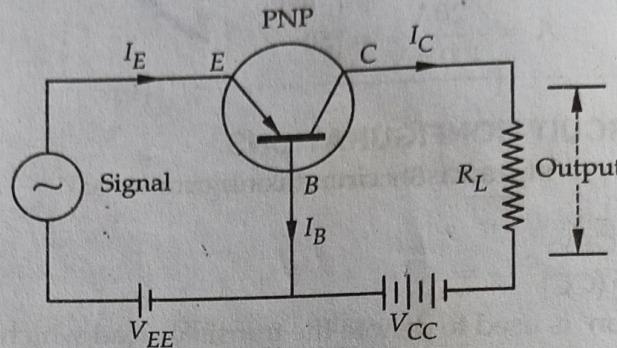


Fig. 6.12 Common-base PNP transistor amplifier

D.c current amplification factor (α) or dc gain. When no signal is applied, then the ratio of the collector current to the emitter current is called dc alpha (α_{dc}) of a transistor.

$$\alpha_{dc} = \frac{-I_C}{I_E}, \quad \begin{cases} \text{negative sign signifies that } I_E \text{ flows into} \\ \text{transistor while } I_C \text{ flows out of it} \end{cases}$$

If we write α_{dc} simply by α , then

$$\alpha = \frac{-I_C}{I_E}$$

α of a transistor is a measure of the quality of a transistor. Higher is the value of α , better is the transistor in the sense that collector current approaches the emitter current.

From eq. (1) considering only magnitudes of the currents

$$I_C = \alpha \cdot I_E \text{ and hence } I_B = I_E - I_C$$

$$\therefore I_B = I_E - \alpha I_E = I_E (1 - \alpha) \quad \dots(2)$$

A.c. current gain. When signal is applied, the ratio of change in collector current to the change in emitter current at constant collector base voltage is defined as current amplification factor

$$\alpha_{ac} = -\frac{\Delta I_C}{\Delta I_E} \quad \dots(3)$$

For all practical purposes, $\alpha_{dc} = \alpha_{ac} = \alpha$ and practical values in commercial transistors range from 0.9 to 0.99.

Total collector current

The total collector current consists of the following two parts:

- The current produced by normal transistor action i.e., component controlled by emitter current. This is due to the majority carrier and its value is αI_E .
- The leakage current $I_{leakage}$. This current is due to the motion of minority carriers across base-collector junction on account of it being reverse-biased. This is much smaller than αI_E . The leakage current is abbreviated as I_{CBO} i.e., collector-base current with emitter open. This is shown in fig. (6.13).

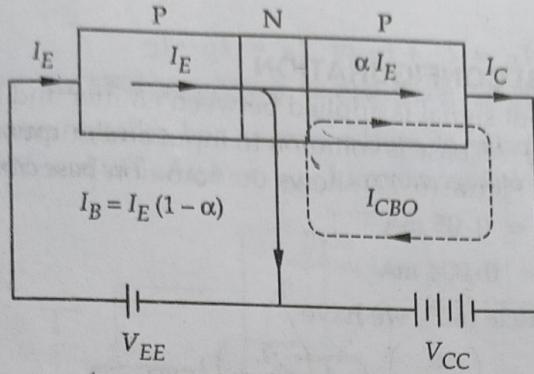


Fig. 6.13 Showing leakage current

∴ Total collector current

$$I_C = \alpha I_E + I_{CBO} \quad \dots(4)$$

Majority Minority

It is clear from eq. (4) that if $I_E = 0$ (emitter circuit is open), even there will be small leakage current in the collector circuit. The current I_{CBO} is usually small and may be neglected in transistor circuit calculations.

(iii) The collector current can also be expressed as

$$I_C = \alpha (I_C + I_B) + I_{CBO}$$

or $I_C (1 - \alpha) = \alpha I_B + I_{CBO}$

$$I_C = \left(\frac{\alpha}{1 - \alpha} \right) I_B + \left(\frac{1}{1 - \alpha} \right) I_{CBO} \quad \dots(5)$$

The relation between α and β is given by

$$\alpha = \frac{\beta}{1 + \beta} \quad \text{or} \quad 1 - \alpha = \frac{1}{1 + \beta}$$

$$I_C = \beta I_B + (1 + \beta) I_{CBO} \quad \dots(6)$$

FEW EXAMPLES

Example 1. A transistor has an I_C of 100 mA and I_B of 0.5 mA. What is the value of α_{dc} .

$$\text{Emitter current } I_E = I_C + I_B = 100 + 0.5 = 100.5 \text{ mA}$$

$$\alpha_{dc} = \frac{I_C}{I_E} = \frac{100}{100.5} = 0.995$$

Example 2. In CB configuration, the value of $\alpha = 0.98$. A voltage drop of 4.9 V is obtained across a resistor of 5 kΩ when connected in collector circuit. Find the base current.

Here

$$I_C = \frac{4.9 \text{ V}}{5 \text{ k}\Omega} = 0.98 \text{ mA}$$

Now,

$$\alpha = \frac{I_C}{I_E} \quad \text{or} \quad I_E = \frac{I_C}{\alpha} = \frac{0.98}{0.98} = 1 \text{ mA}$$

$$I_B = I_E - I_C = 1 - 0.98 = 0.02 \text{ mA}$$

Example 3. The emitter current I_E in a transistor is 3 mA. If the leakage current I_{CBO} is 5 μA and $\alpha = 0.98$, calculate the collector and base current.

$$I_C = \alpha I_E + I_{CBO}$$

$$= 0.98 \times 3 + 0.005 \quad (\because I_{CBO} = 5 \mu\text{A} = 0.005 \text{ mA})$$

$$= 2.945 \text{ mA}$$

Now

$$I_E = I_C + I_B \text{ or } I_B = I_E - I_C$$

$$\therefore I_B = 3 - 2.945 = 0.055 \text{ mA} = 55 \mu\text{A}$$

Example 4. Determine the value of emitter current and collector current of a transistor having $\alpha = 0.98$ and collector to base leakage current $I_{CBO} = 4 \mu\text{A}$. The base current is $50 \mu\text{A}$.

Given that, $I_B = 50 \mu\text{A} = 0.05 \text{ mA}$

and $I_{CBO} = 4 \mu\text{A} = 0.004 \text{ mA}$

According to eq. (5) of article (6.7), we have

$$\begin{aligned} I_C &= \left(\frac{\alpha}{1-\alpha} \right) I_B + \left(\frac{1}{1-\alpha} \right) I_{CBO} \\ &= \left(\frac{0.98}{1-0.98} \right) \times 0.05 + \left(\frac{1}{1-0.98} \right) + 0.004 \\ &= 2.45 \text{ mA} + 0.2 \text{ mA} = 2.65 \text{ mA} \end{aligned}$$

Now

$$I_E = I_C + I_B = 2.65 + 0.05 = 2.7 \text{ mA}$$

6.8 COMMON-EMITTER (CE) CONFIGURATION

In this configuration, the input signal is applied between base and emitter and the output is taken from collector and emitter. As emitter is common to input and output circuits, hence the name common emitter configuration. Figure (6.14) shows the common-emitter PNP transistor circuit.

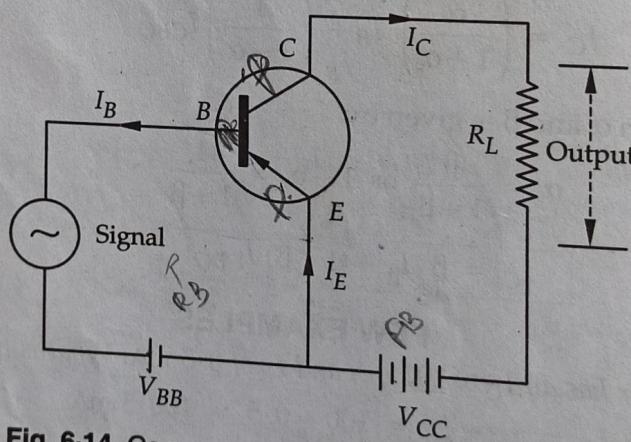


Fig. 6.14 Common-emitter PNP transistor amplifier

Base current amplification factor (β) or d.c. current gain. When no signal is applied, then the ratio of collector current to the base current is called dc beta (β_{dc}) of a transistor.

$$(\beta_{dc}) = \beta = \frac{I_C}{I_B}$$

...(1)

A.C. current gain. When signal is applied, the ratio of change in collector current to the change in base current is defined as base current amplification factor. Thus

$$(\beta_{ac}) = \beta_0 = \frac{\Delta I_C}{\Delta I_B}$$

$$I_C = \beta I_B$$

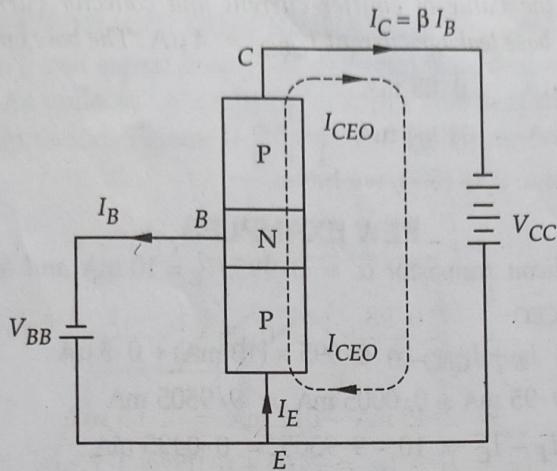
From eq. (1),

Almost in all transistors, the base current is less than 5% of the emitter current. Due to this fact, β is generally greater than 20. Usually, β ranges from 20 to 500. Hence this configuration is frequently used when appreciable current gain as well as voltage gain is required.

Transistors

Total collector current

The leakage current for this configuration is shown in fig. (6.15).

**Fig. 6.15** Showing leakage current

\therefore Total collector current

$$I_C = \beta I_B + I_{CEO} \quad \dots(3)$$

where I_{CEO} is the leakage current. It is obvious from eq. (3) that despite $I_B = 0$, there is a leakage current from collector to emitter. It is called I_{CEO} , the subscript CEO stands for collector to emitter with base open.

We know that

and

\therefore

$$I_E = I_B + I_C$$

$$I_C = \alpha I_E + I_{CBO}$$

$$I_C = \alpha(I_B + I_C) + I_{CBO}$$

$$I_C(1 - \alpha) = \alpha I_B + I_{CBO}$$

or

$$I_C = \frac{\alpha}{1 - \alpha} I_B + \frac{1}{1 - \alpha} I_{CBO} \quad \dots(4)$$

Comparing eqs. (3) and (4), we get

$$\beta = \frac{\alpha}{1 - \alpha} \quad \text{and} \quad I_{CEO} = \frac{1}{(1 - \alpha)} I_{CBO} \quad \dots(5)$$

Substituting the value of I_{CEO} in eq. (3), we get

$$I_C = \beta I_B + \left(\frac{1}{1 - \alpha} \right) I_{CBO} = \beta I_B + (\beta + 1) I_{CBO} \quad \dots(6)$$

Relation between α and β .

$$\text{We know that } \alpha = \frac{I_C}{I_E} \quad \text{and} \quad \beta = \frac{I_C}{I_B}$$

$$I_E = I_B + I_C \quad \text{or} \quad I_B = I_E - I_C$$

$$\text{Now } \beta = \frac{I_C}{I_E - I_C} = \frac{I_C / I_E}{1 - (I_C / I_E)}$$

or

$$\beta = \frac{\alpha}{(1 - \alpha)} \quad \dots(7)$$

Cross multiplying eq. (7), we get

$$\beta(1 - \alpha) = \alpha \text{ or } \beta - \beta\alpha = \alpha \text{ or } \beta = \alpha(1 + \beta)$$

∴

$$\alpha = \frac{\beta}{1 + \beta} \quad \dots(8)$$

It can be seen that

$$1 - \alpha = \frac{1}{1 + \beta} \quad \dots(9)$$

FEW EXAMPLES

Example 1. In a NPN silicon transistor $\alpha = 0.995$, $I_E = 10 \text{ mA}$ and leakage current I_{CBO} (for I_{CO}) = $0.5 \mu\text{A}$. Determine I_{CEO} .

We know,

$$\begin{aligned} I_C &= \alpha I_E + I_{CBO} = 0.995 \times (10 \text{ mA}) + 0.5 \mu\text{A} \\ &= 9.95 \text{ mA} + 0.0005 \text{ mA} = 9.9505 \text{ mA} \end{aligned}$$

Now

$$I_B = I_E - I_C = 10 - 9.9505 = 0.0495 \text{ mA}$$

$$\beta = \frac{\alpha}{1 - \alpha} = \frac{0.995}{1 - 0.995} = 199$$

∴

$$I_C = \beta I_B + I_{CEO} \text{ or } I_{CEO} = I_C - \beta I_B$$

or

$$\begin{aligned} I_{CEO} &= 9.9505 - 199 \times 0.0495 = 0.1 \text{ mA} \\ &= 100 \mu\text{A} \end{aligned}$$

Example 2. A germanium transistor with $\alpha = 0.98$ gives a reverse saturation current $I_{CBO} = 10 \mu\text{A}$ in common base configuration. When transistor is used in CE configuration with a base current of $0.22 \mu\text{A}$, calculate the collector current.

Given that, $I_{CBO} = 10 \mu\text{A} = 0.01 \text{ mA}$, $\alpha = 0.98$ and

$$I_B = 0.22 \mu\text{A} = 0.22 \times 10^{-3} \text{ mA}$$

According to eq. (4), we have

$$\begin{aligned} I_C &= \left(\frac{\alpha}{1 - \alpha} \right) I_B + \left(\frac{1}{1 - \alpha} \right) I_{CBO} \\ &= \left(\frac{0.98}{1 - 0.98} \right) \times 0.22 \times 10^{-3} + \left(\frac{1}{1 - 0.98} \right) \times 0.01 \\ &= 0.01078 + 0.5 = 0.51078 \text{ mA} \end{aligned}$$

Example 3. In common emitter configuration, if the voltage drop across $5 \text{ k}\Omega$ resistor connected in the collector circuit is 5 V , find the value of base current. $\beta = 50$

$$I_C = \frac{\text{Voltage drop across } R_L}{\text{Resistance of } R_L} = \frac{5 \text{ V}}{5 \text{ k}\Omega} = 1 \text{ mA}$$

$$\therefore I_B = \frac{I_C}{\beta} = \frac{1}{50} = 0.02 \text{ mA}$$

Example 4. A transistor is connected in CE configuration. Collector supply voltage $V_{CC} = 10 \text{ V}$, $R_L = 800 \Omega$, voltage drop across $R_L = 0.8 \text{ V}$ and $\alpha = 0.96$. What is base current? Also, determine the collector-emitter voltage.

$$\text{Here, } V_{CE} = V_{CC} - I_C R_L = 10 - 0.8 = 9.2 \text{ V}$$

$$I_C = \frac{0.8}{800} = 1 \text{ mA} \text{ and } \beta = \frac{\alpha}{1 - \alpha} = \frac{0.96}{1 - 0.96} = 24$$

$$I_B = \frac{I_C}{\beta} = \frac{1 \text{ mA}}{24} = 0.0416 \text{ mA} = 41.67 \mu\text{A}$$

6.9 COMMON-COLLECTOR (CC) CONFIGURATION

In this configuration, the input signal is applied between base and collector and the output is taken from the emitter. As collector is common to input and output circuits, hence the name common collector configuration. Figure (6.16) shows the common collector PNP transistor circuit.

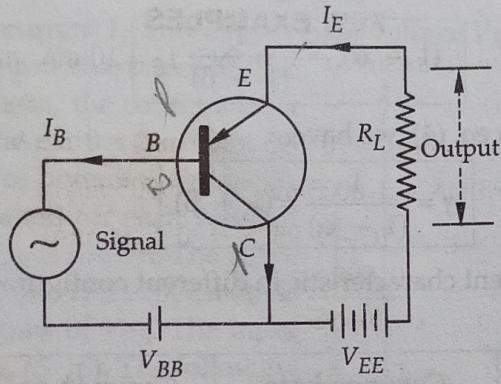


Fig. 6.16 Common collector PNP transistor amplifier

Current amplification factor (γ) or dc current gain. When no signal is applied, then the ratio of emitter current to the base current is called as dc gamma (γ_{dc}) of the transistor.

$$(\gamma_{dc}) = \gamma = \frac{I_E}{I_B} \quad \dots(1)$$

A.c. current gain. When signal is applied, then the ratio of change in emitter current to the change in base current is known as current amplification factor γ .

$$\gamma = \frac{\Delta I_E}{\Delta I_B} \quad \dots(2)$$

This configuration provides the same current gain as common emitter circuit as $\Delta I_E \approx \Delta I_C$ but the voltage gain is always less than one.

Total emitter current

We know that $I_E = I_B + I_C$

Also $I_C = \alpha I_E + I_{CBO}$

$$\therefore I_E = I_B + (\alpha I_E + I_{CBO}) = I_B + \alpha I_E + I_{CBO}$$

$$I_E(1 - \alpha) = I_B + I_{CBO}$$

$$I_E = \frac{I_B}{(1 - \alpha)} + \frac{I_{CBO}}{(1 - \alpha)}$$

or

$$I_E = (1 + \beta) I_B + (1 + \beta) I_{CBO} \quad \therefore \frac{1}{(1 - \alpha)} = (1 + \beta) \quad \dots(3)$$

Application. This configuration has very high input resistance ($\approx 750 \text{ k}\Omega$) and very low output resistance ($\approx 25 \Omega$) so the voltage gain is always less than one. Hence this configuration is seldom used for amplification. The most important use is for impedance matching i.e. for driving a low impedance load from a high impedance source.

Relation between γ and α

We know that $\gamma = \frac{I_E}{I_B}$ and $\alpha = \frac{I_C}{I_E}$

Also $I_B = I_E - I_C$

Now $\gamma = \frac{I_E}{I_E - I_C} = \frac{1}{1 - (I_C/I_E)} = \frac{1}{(1 - \alpha)}$... (4)

Relation between γ and β . According to eq. (8), we have

$$(1 - \alpha) = \frac{1}{(1 + \beta)}$$

Substituting this value in eq. (4), we have

$$\gamma = \frac{1}{(1 - \alpha)} = (1 + \beta) \quad \dots (5)$$

The comparison of different characteristic in different configurations is shown below in the tabular form

S. No	Characteristic	Common base	Common emitter	Common collector
1	Input resistance	low (about 100 Ω)	low (about 700 Ω)	very high
2	Output resistance	very high (about 400 k Ω)	high (about 50 k Ω)	low (about 50 Ω)
3	Voltage gain	about 150	about 150	less than 1
4	Applications	At high frequencies	At audio frequencies	impedance matching

6-10 CHARACTERISTICS OF COMMON BASE CIRCUIT

Figure (6.17) shows the circuit arrangement to draw the characteristics of a PNP transistor connected in common-base configuration.

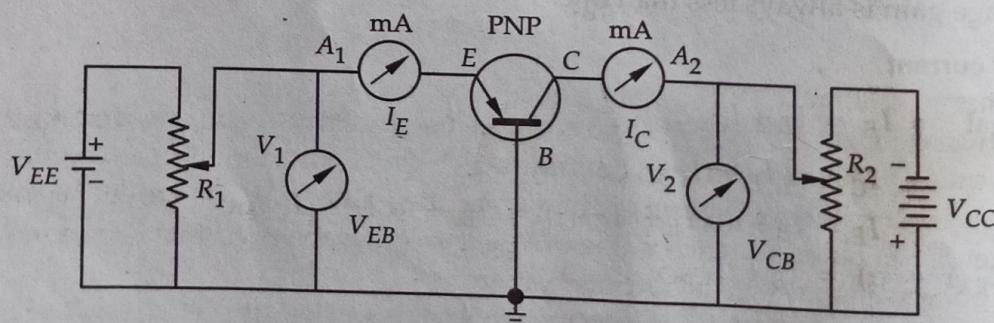


Fig. 6.17 PNP transistor connected in common base configuration

The battery V_{EE} supplies forward bias to the emitter-base junction through potential divider arrangement R_1 . Similarly, the battery V_{CC} supplies reverse-bias to the collector base junction through potential divider arrangement R_2 .

In the circuit, milliammeters are connected in series with emitter and collector to measure emitter current I_E and collector current I_C respectively. Similarly, voltmeters are connected in parallel across E and B to measure the voltage V_{EB} and across C and B to measure the voltage

V_{CB} respectively. Here, the quantities emitter to base voltage V_{EB} and emitter current I_E correspond to input circuit and collector to base voltage V_{CB} and collector current I_C to the output circuit.

The complete electrical behaviour of a transistor can be described by stating the relationship between different dc currents and voltages. These relationships can be displayed graphically and the curves thus obtained are known as characteristics of a transistor. Here we shall consider the *input characteristic* and *output characteristic*.

(1) Input characteristics

The curve between emitter current I_E and emitter base voltage V_{EB} at constant collector base voltage V_{CB} represents the input characteristic. For plotting the input characteristic, the collector base voltage V_{CB} is kept fixed. The emitter base voltage V_{EB} is varied with the help of potential divider R_1 and the emitter current is noted for each value of V_{EB} . A graph of I_E against V_{EB} is drawn. The curve is known as input characteristic. The experiment is repeated for other fixed values of V_{CB} . The input characteristic is shown in fig. (6.18). The following points are noted from the characteristic:

- (i) There exists a *cut in, offset or threshold voltage* V_{EB} below which the emitter current is very small.
- (ii) The emitter current I_E increases rapidly with small increase in emitter-base voltage V_{EB} . This shows that the input resistance is very small.

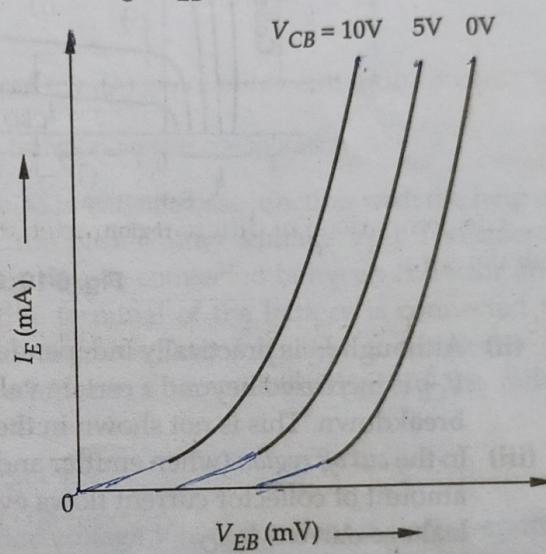


Fig. 6.18 Input characteristic

Input resistance. The ratio of change in emitter-base voltage (ΔV_{EB}) to the resulting change in emitter-current (ΔI_E) at constant collector-base voltage (V_{CB}) is defined as input resistance. This is denoted by r_i . Therefore,

$$r_i = \left. \frac{\Delta V_{EB}}{\Delta I_E} \right|_{V_{CB}=\text{constant}}$$

(2) Output characteristics

The curve between collector current I_C and collector base voltage V_{CB} at constant emitter current I_E represents the output characteristic. For plotting output characteristic, the emitter current I_E is kept fixed. With the help of potential divider R_2 , the value of V_{CB} is varied in steps and the collector current I_C is noted for each value of V_{CB} . Now a graph is drawn between I_C and V_{CB} . The curve so obtained is known as output characteristic.

The experiment is repeated for different fixed values of emitter current I_E . Figure (6.19) shows the output characteristic.

Following points are noted from the characteristic:

- (i) In the *active region* (when the collector junction is biased in reverse direction and the emitter junction in forward direction), the collector current is essentially independent of collector voltage and depends only upon the emitter current. Because α is less than, but almost equal to unity, the magnitude of collector current is slightly less than that of the emitter current.

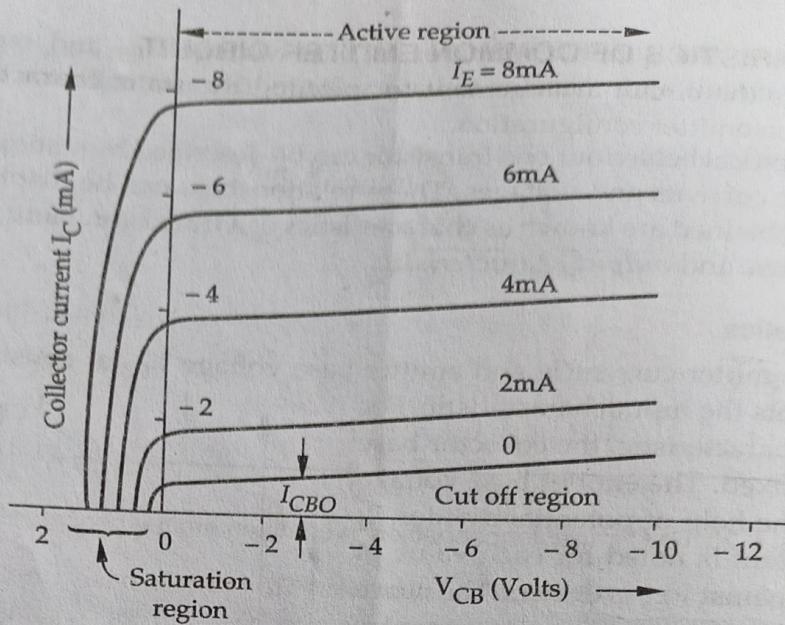


Fig. 6.19 Output characteristic

- (ii) Although I_C is practically independent of V_{CB} over the working range of transistor, yet if V_{CB} is increased beyond a certain value, I_C eventually increases rapidly due to avalanche breakdown. This is not shown in the characteristic.
- (iii) In the *cut off region* (when emitter and collector junctions are both reverse-biased), a small amount of collector current flows even when emitter current $I_E = 0$. This is the collector leakage current I_{CBO} .
- (iv) In the *saturation region* (when both emitter and collector junctions are forward-biased), the collector current I_C flows even when $V_{CB} \approx 0$. Actually, in PNP transistor, V_{CB} is slightly positive in this region and because of this forward biasing, there results large change in collector current with a small change in collector voltage. A forward bias implies that the P-type collector is made positive with respect to N-type base and hence hole current flows from collector side across the collector junction to base side. This hole current causes a positive increment in the collector current so that the collector current increases rapidly.

Output resistance. The ratio of change in collector-base voltage (ΔV_{CB}) to the resulting change in collector current (ΔI_C) at constant emitter current (I_E) is defined as output voltage. This is denoted by r_o . Therefore,

$$r_o = \left. \frac{\Delta V_{CB}}{\Delta I_C} \right|_{I_E = \text{constant}}$$

Example A transistor is connected in CB configuration. When the emitter voltage is changed by 200 mV, the emitter current changes by 5 mA. During this variation, the collector base voltage is kept fixed. Calculate the dynamic input resistance of the transistor.

We know that,

$$r_i = \left. \frac{\Delta V_{EB}}{\Delta I_E} \right|_{V_{CB} = \text{constant}}$$

$$r_i = \frac{200 \text{ mA}}{5 \text{ mA}} = 40 \Omega$$

6.11 CHARACTERISTICS OF COMMON Emitter CIRCUIT

Figure (6.20) shows the circuit arrangement for plotting the static characteristics of a PNP transistor in common emitter configuration.

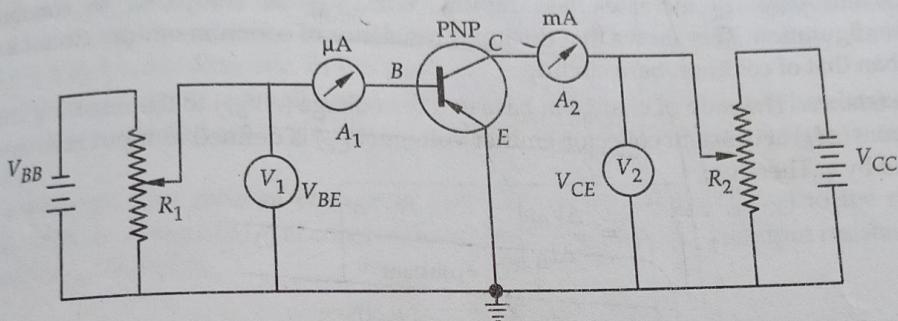


Fig. 6.20 PNP transistor connected in common emitter configuration

In the circuit, the battery V_{BB} provides forward bias to emitter-base junction with the help of potential divider R_1 . The voltmeter V_1 measures the base-emitter voltage V_{BE} . The microammeter A_1 measures the base current I_B . A battery V_{CC} is connected between collector and emitter through a potential divider R_2 . The positive terminal of the battery is connected to emitter while the negative terminal is connected to the collector so that the collector is reverse-biased. The voltmeter V_2 measures the collector-emitter voltage V_{CE} and the milliammeter A_2 measures the collector current.

(1) Input characteristics

The curve between base current I_B and base-emitter voltage V_{BE} at constant collector-emitter voltage V_{CE} represents the input characteristic. For plotting the input characteristic, the collector-emitter voltage V_{CE} is kept fixed. The base emitter voltage V_{BE} is varied with the help of potential divider R_1 and the base current I_B is noted for each value of V_{BE} . A graph of I_B against V_{BE} is drawn. The curve so obtained is known as input characteristic.

The experiment is repeated for other fixed values of V_{CE} . The input characteristic is shown in fig. (6.21).

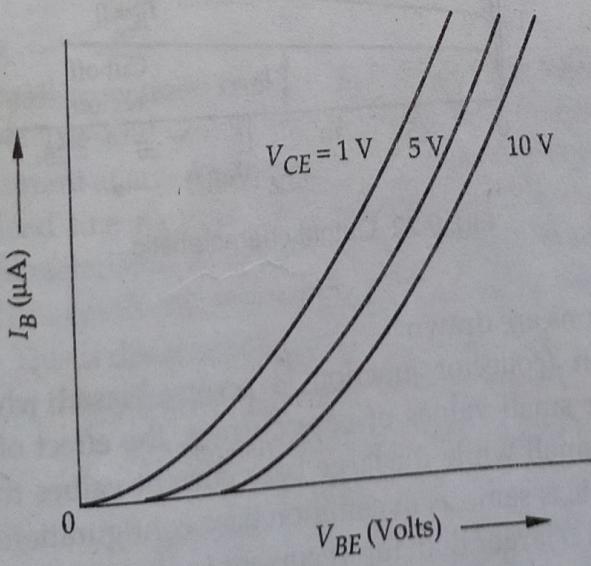


Fig. 6.21 Input characteristic

The following points are noted from the characteristics

- The characteristic resembles that of a forward-biased diode curve. This is expected because the base-emitter section of transistor is a diode and it is forward-biased.
- In this case, I_B increases less rapidly with V_{BE} as compared to common-base configuration. This shows that the input resistance of common-emitter circuit is higher than that of common-base circuit.

Input resistance. The ratio of change in base emitter voltage (ΔV_{BE}) to the resulting change in base current (ΔI_B) at constant collector-emitter voltage (V_{CE}) is defined as input resistance. This is denoted by r_i . Therefore,

$$r_i = \left. \frac{\Delta V_{BE}}{\Delta I_B} \right|_{V_{CE} = \text{constant}}$$

(2) Output characteristics

The curve between collector current I_C and collector emitter voltage V_{CE} at constant base current I_B represents the output characteristic. For plotting output characteristic, the base current I_B is kept fixed. With the help of potential divider R_2 , the value of V_{CE} is varied in steps and the collector current I_C is noted for each value of V_{CE} . A graph of I_C against V_{CE} is drawn. The curve so obtained is known as output characteristic.

The experiment is repeated for different values of I_B . Figure (6.22) shows the output characteristic.

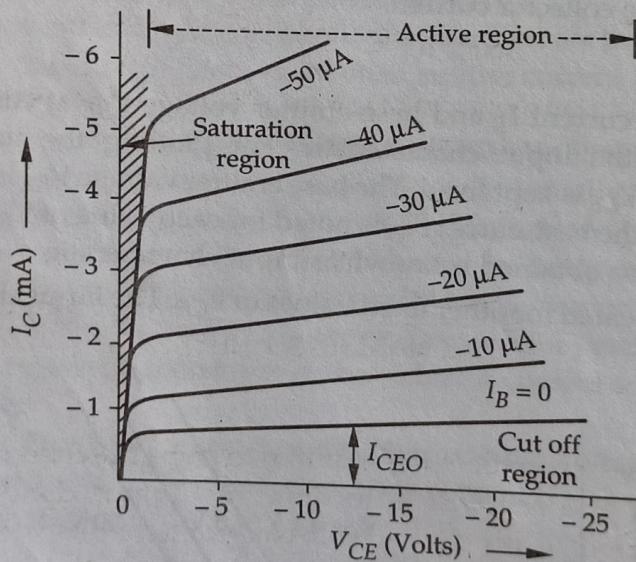


Fig. 6.22 Output characteristic

The following conclusions are drawn:

- In the active region (collector junction is reverse-biased while emitter junction is forward-biased), for small values of base current, the effect of collector voltage over collector current is small while for large base current values this effect increases. The shape of characteristic is same as in common base configuration but with the difference that collector current is larger than input current i.e., base current. Thus the current gain of this configuration is greater than unity. The operation of the transistor, when used as an amplifying device, must be restricted in the active region only, if much distortion is to be avoided.

- (ii) When V_{CE} has very low value (ideally zero), the transistor is said to be saturated and it operates in the saturation region of characteristic. In the saturated region, the change in base current I_B does not produce a corresponding change in collector current I_C .
- (iii) When V_{CE} is allowed to increase too far, collector-base junction completely breaks down and due to this avalanche breakdown, collector current increases rapidly. This is not shown in the characteristic. In this case, the transistor is damaged.
- (iv) In the cutoff region, a small amount of collector current flows even when base current $I_B = 0$. This is called I_{CEO} . Since main collector current is zero, the transistor is said to be cutoff.

Output resistance. The ratio of change in collector-emitter voltage (ΔV_{CE}) to the resulting change in collector current (ΔI_C) at constant base current I_B is defined as output resistance. This is denoted by r_o . Therefore,

$$r_o = \left. \frac{\Delta V_{CE}}{\Delta I_C} \right|_{I_B = \text{constant}}$$

Example 1. A change of 300 mV in base-emitter voltage causes a change of 100 μA in the base current. Determine the dynamic input resistance.

We know that,

$$r_i = \left. \frac{\Delta V_{BE}}{\Delta I_B} \right|_{V_{CE} = \text{constant}}$$

$$\therefore r_i = \frac{300 \times 10^{-3}}{100 \times 10^{-6}} = 3 \times 10^3 \Omega = 30 \text{ k}\Omega$$

Example 2. Increase in collector emitter voltage from 5 V to 8 V causes increase in collector current from 5 mA to 5.3 mA. Determine the dynamic output resistance.

We know that,

$$r_o = \left. \frac{\Delta V_{CE}}{\Delta I_C} \right|_{I_B = \text{constant}}$$

$$\therefore r_o = \frac{3 \text{ V}}{0.3 \text{ mA}} = \frac{3}{0.3 \times 10^{-3}} = 10 \times 10^3 = 10 \text{ k}\Omega$$

6.12 D.C. LOAD LINE

In a transistor circuit analysis, sometimes it is required to know the collector currents for various collector-emitter voltages. The one way is to draw the output characteristics and then to determine the collector current at any desired collector-emitter voltage. The other way, a more convenient method, is load line method. Here we shall consider a common emitter PNP transistor. The output characteristics are shown in fig. (6.22). For drawing dc load line of a transistor, we require only its cutoff and saturation points. Then the line joining these two points is known as dc load line. This is discussed below:

The voltage equation of the collector-emitter circuit is

$$V_{CC} = V_{CE} + I_C R_L$$

$$* I_C = \frac{V_{CC}}{R_L} - \frac{V_{CE}}{R_L} \quad \checkmark$$

*This is a linear equation similar to

$$y = -mx + c$$

The graph of the equation is straight line with slope $m = -1/R_L$

Here, V_{CC} and R_L are fixed values and hence it is a first degree equation which can be represented by a straight line. We now consider the cutoff and saturation points.

(i) When collector current $I_C = 0$, then collector-emitter voltage is maximum and is equal to V_{CC} i.e.,

$$V_{CE} = V_{CC} - I_C R_L = V_{CC}$$

This gives the cutoff point B as shown in fig. (6.23).

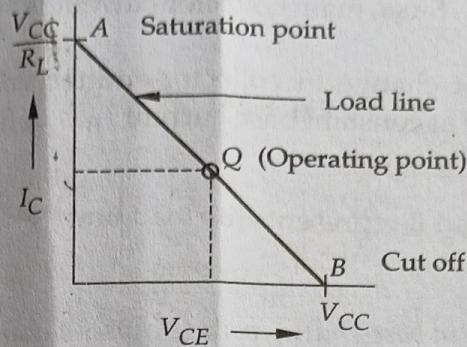


Fig. 6.23 d.c. Load line

(ii) When collector-emitter voltage $V_{CE} = 0$, then the collector current is maximum and is equal to V_{CC}/R_L i.e.,

$$V_{CE} = V_{CC} - I_C R_L$$

$$0 = V_{CC} - I_C R_L \text{ or } I_C = V_{CC} / R_L$$

This gives the saturation point A as shown in fig. (6.23).

The line joining the two points A and B is known as load line.

Operating point. This is a point on dc load line which represents the values of I_C and V_{CE} that exist in a transistor circuit when no signal is applied. This is also known as operating point or working point.

Suppose in the absence of the signal, the base current is $-10 \mu\text{A}$ (output characteristic is shown in fig. (6.22)). Then I_C and V_{CE} conditions in the circuit must be represented by some point on this characteristic. But I_C and V_{CE} conditions should also be represented by some point on d.c. load line.

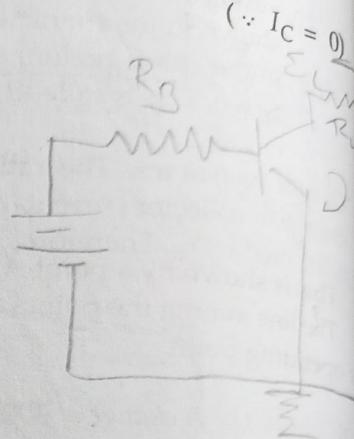
The intersection of the output characteristic for $-10 \mu\text{A}$ base current, and d.c. load line represents the actual state of affairs in the circuit and is called the operating point Q . This is shown in fig. (6.23).

The best position for this point is midway between cut off and saturation points. The selection of the operating point is done according to the use to which the device is put. For small signal amplifier, in which power is conserved, operating point should be selected as to give lowest quiescent value of collector current, while for an amplifier required to deliver sufficient amount of power, operating point is chosen so as to give quiescent current about one half of the maximum permissible collector current of the transistor.

Example 1. For the circuit shown in fig. [6.24 (a)], draw the dc load line and locate its quiescent or dc working point.

The load line and quiescent point are shown in fig. [6.24 (b)]. The cut off point lies on X-axis where $V_{CB} = V_{CC} = 25 \text{ V}$ (shown by point B). The saturation point lies on Y-axis where the saturation value of collector current is given by

$$(I_C)_{\text{Sat}} = V_{CC}/R_L = 25/5 \text{ K}\Omega = \frac{25}{5 \times 10^3} = 5 \times 10^{-3} = 5 \text{ mA.}$$



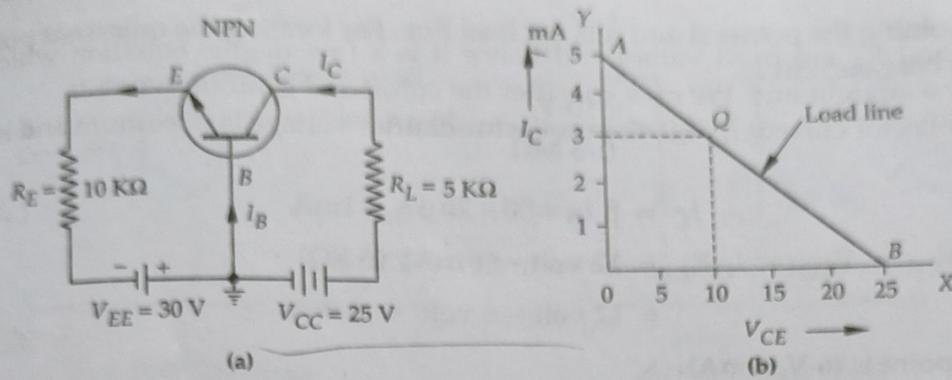


Fig. 6.24

This is shown by a point *A*.

The line joining the points *A* and *B* represents the load line. Now, we shall find the working or operating point.

$$I_E = V_{EE}/R_E = \frac{30}{10 \text{ k}\Omega} = 3 \text{ mA} \quad (\text{neglecting } V_{BE})$$

Now

$$I_C = \alpha I_E \approx I_E \approx 3 \text{ mA}$$

$$\begin{aligned} V_{CB} &= V_{CC} - I_C R_L = 25 - (3 \text{ mA})(5 \text{ k}\Omega) \\ &= 25 - 15 = 10 \text{ V} \end{aligned}$$

Hence *Q* point is located at (10 V, 3 mA).

Example 2. For the circuit shown in fig. [6.25 (a)], draw the dc load line and locate the quiescent or dc working point. Assume $\beta = 50$ and neglect V_{BE} .

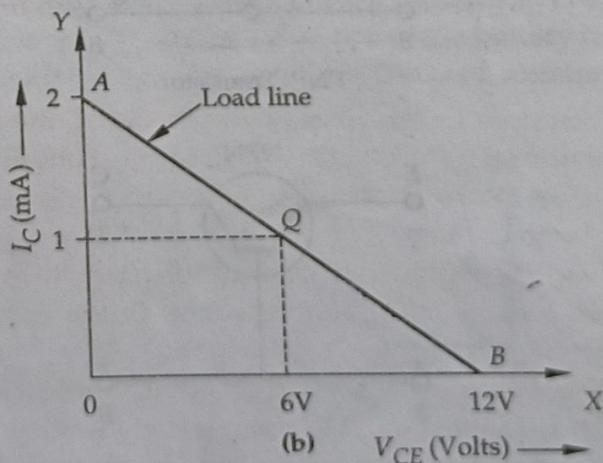
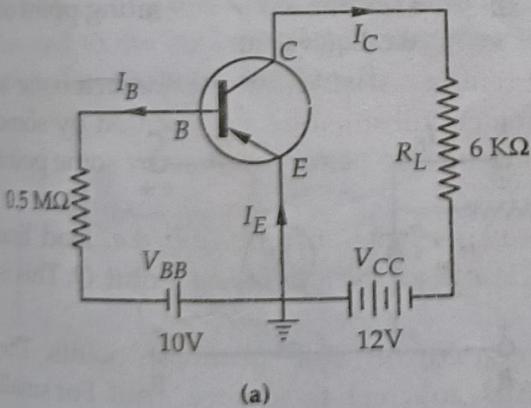


Fig. 6.25

The load line and quiescent point are shown in fig. [6.25 (b)].

The cutoff point *B* is located where

$$I_C = 0 \quad \text{and} \quad V_{CE} = V_{CC} = 12 \text{ volt}$$

The saturation point *A* lies, where

$$V_{CE} = 0 \quad \text{and} \quad (I_C)_{\text{sat}} = \frac{V_{CC}}{R_L} = \frac{12 \text{ V}}{6 \text{ k}\Omega} = 2 \text{ mA.}$$

The line joining the points A and B is the load line. For locating the quiescent point Q, let us calculate the base current I_B .

$$I_B = \frac{10 \text{ V}}{0.5 \text{ M}\Omega} = 20 \mu\text{A}$$

Now

$$I_C = \beta I_B = 50 \times 20 \mu\text{A} = 1 \text{ mA}$$

$$\begin{aligned} \text{Further } V_{CE} &= V_{CC} - I_C R_L = 12 \text{ volt} - (1 \text{ mA}) (6 \text{ k}\Omega) \\ &= 12 \text{ volt} - 6 \text{ volt} = 6 \text{ volt} \end{aligned}$$

Hence Q point is (6 V, 1 mA).

6.13 D.C. EQUIVALENT CIRCUIT

(1) Common-base circuit

In the common base circuit, the emitter diode acts like a forward-biased ideal diode, while collector diode acts as a current-source due to transistor action. Thus an ideal transistor* may be regarded as a rectifier diode in the emitter and a current source in the collector. The arrow in the current source points in the direction of conventional current. The dc equivalent circuits of a PNP and NPN transistors are shown in fig. (6.26).

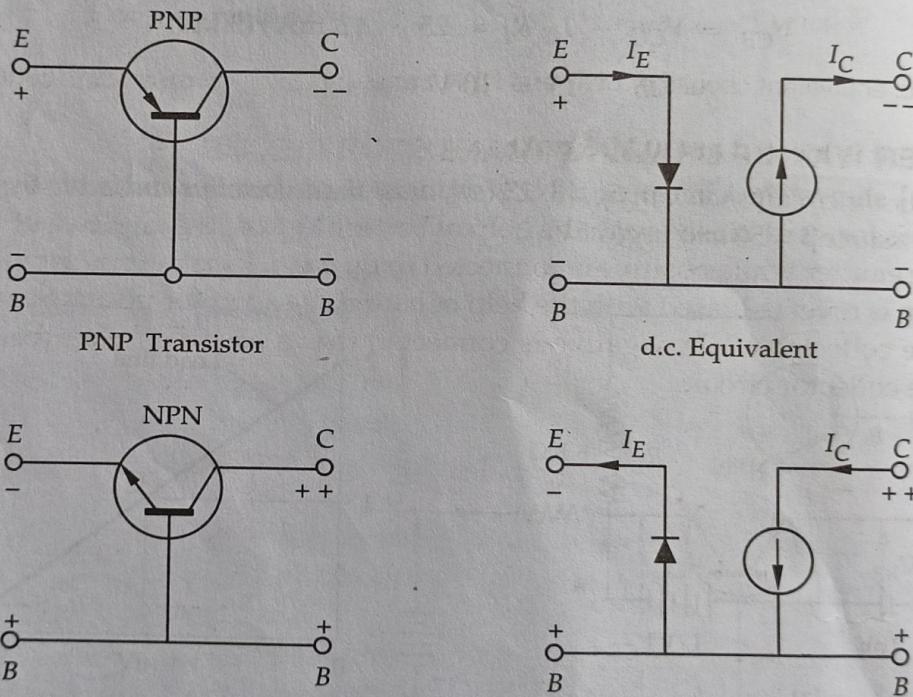


Fig. 6.26 d.c. equivalent circuits of PNP and NPN transistors in common-base configuration

(2) Common-emitter circuit

In this configuration, the ideal transistor may be regarded as a rectifier diode in the base circuit and a current source in the collector circuit. In the current source, the direction of the arrow points in the direction of conventional current. The d.c. equivalent circuits of a PNP and NPN transistors are shown in fig. (6.27).

* For an ideal transistor $\alpha = 1$ i.e., $I_C = I_E$

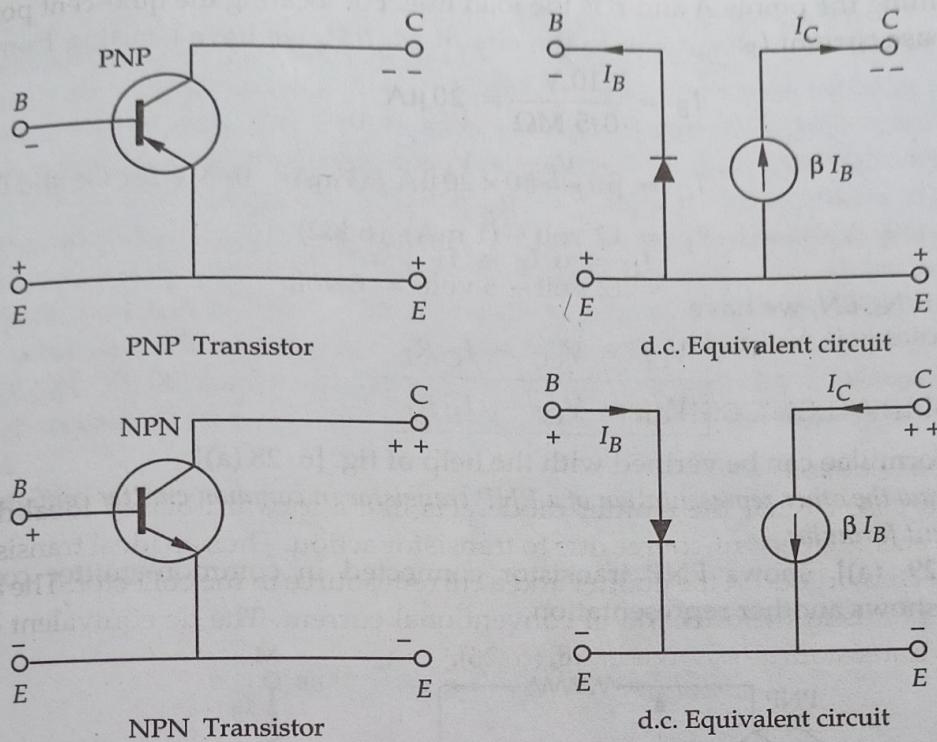


Fig. 6.27 d.c. equivalent circuits of PNP and NPN transistors in common-emitter configuration

6.14 ANOTHER WAY OF DRAWING TRANSISTOR CIRCUIT

Figure [6.28 (a)] shows the circuit of a NPN transistor in common-base configuration. The emitter junction is forward-biased with the help of battery V_{EE} i.e., the negative of the battery is connected to the emitter while positive is connected to the base. R_E is the emitter resistance. The collector junction is reverse-biased with the help of battery V_{CC} i.e., the positive of the battery is connected to the collector while negative is connected to the base. R_L being the load resistor connected in the collector circuit.

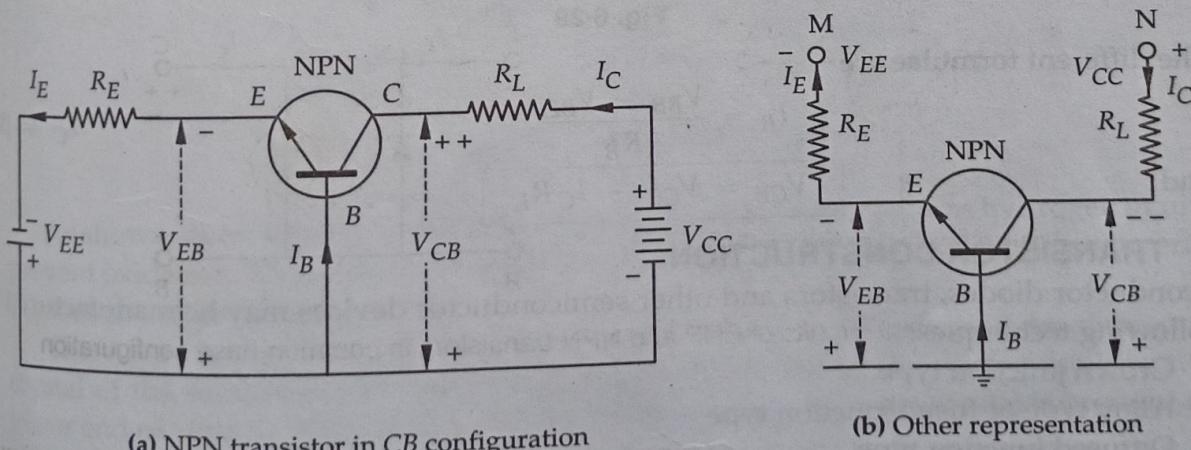


Fig. 6.28

Figure [6.28 (b)] shows a more popular way of drawing the circuit where only one terminal of the battery is shown and other terminal is understood to be grounded. For example, the positive terminal of V_{EE} and negative terminal of V_{CC} are supposed to be grounded.

The different voltages and currents shown in fig. [6.28 (b)] can be calculated in the following way:

Applying Kirchhoff's voltage law to the circuit MEBM, we have (starting from point B or ground)

$$-V_{EB} - I_E R_E + V_{EE} = 0$$

$$I_E = \frac{V_{EE} - V_{EB}}{R_E}$$

or

$$I_C = \alpha I_E \approx I_E$$

Now

From circuit NCBN, we have

$$V_{CB} = V_{CC} - I_C R_L$$

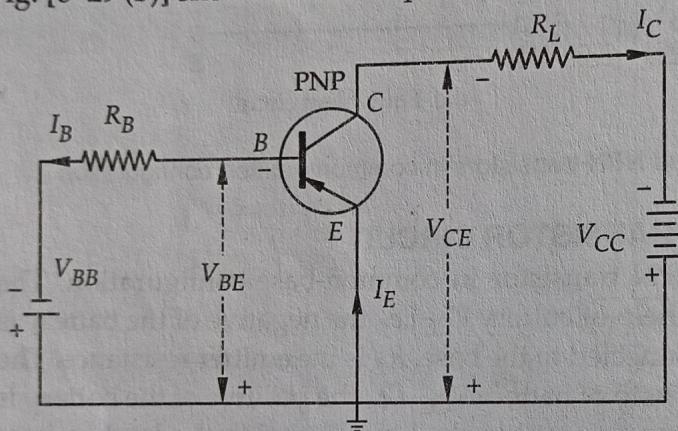
or

$$V_{CB} \equiv V_{CC} - I_E R_L$$

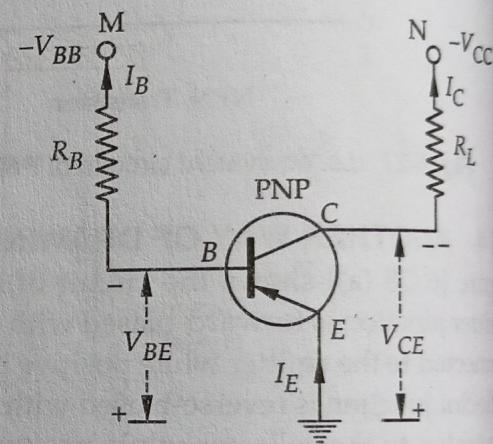
The same formulae can be verified with the help of fig. [6.28 (a)].

Example. Draw the other representation of a PNP transistor in common-emitter configuration. Write down the different formulae.

Figure [6.29 (a)] shows PNP transistor connected in common-emitter configuration. Fig. [6.29 (b)] shows another representation.



(a) NPN transistor in CB configuration



(b) Other representation

Fig. 6.29

The different formulae are

$$I_B = \frac{V_{BB} - V_{BE}}{R_B},$$

and

$$V_{CE} = V_{CC} - I_C R_L$$

$$I_C = \beta I_B$$

6.15 TRANSISTOR CONSTRUCTION

Semiconductor diodes, transistors and other semiconductor devices may be manufactured by the following techniques:

- (i) Grown junction type
- (ii) Alloy type or fused junction type
- (iii) Diffused junction type
- (iv) Epitaxial type, and
- (v) Mesa type.

Here, we shall discuss few of them.

(i) Grown junction diodes and transistors

We know that a junction cannot be formed simply by cementing N-type semiconductor with P-type semiconductor. There must be uniformity throughout the crystal lattice including the junction.

Transistors

In grown junction method, a diode is formed by first growing a crystal of say N-type from a melt of germanium or silicon and after a little later by adding P-type impurity in sufficiently large quantity. Similarly, a grown junction PNP transistor is manufactured by drawing a single crystal from a P-type melt of germanium or silicon and changing the impurity concentration during the crystal drawing operation first to N-type by adding N-type impurity and only a little later again to P-type by adding P-type impurity. Thus the transistor consists of a narrow layer of N-type semiconductor sandwiched between P-type material on its either side.

Grown junction diodes and transistors are manufactured through growing single large crystal which is slowly pulled from the melt in crystal growing furnace. This method is generally used for NPN transistors. The apparatus used for growing single large crystal is shown in fig. (6.30). This consists of furnace using r.f. heating coils. Thermocouple kept within the furnace records the temperature. The temperature of the furnace can thus be very closely controlled.

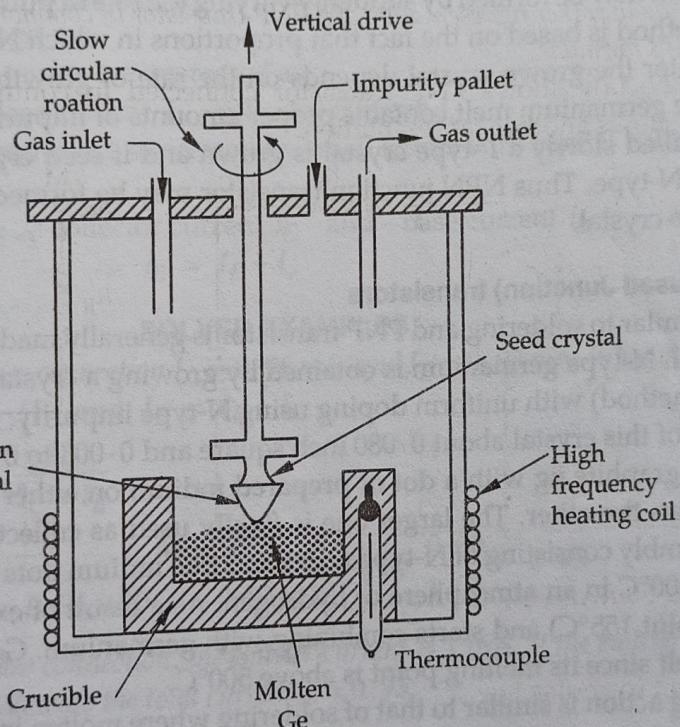


Fig. 6.30 Grown junction method

As shown, a crucible is placed in the chamber. The chamber contains hydrogen or nitrogen to prevent oxidation. The crucible contains the purified germanium or silicon at a temperature few degrees above its melting point.

There is a vertical shaft which can be rotated as well as pulled up. A small piece of single crystal of the semiconductor previously prepared, known as the seed crystal, is attached at lower end of vertical shaft. By lowering the vertical shaft, the seed crystal is brought in contact with the molten semiconductor.

The vertical shaft is rotated and pulled up at a very slow rate. The molten Ge or Si in contact with the seed crystal crystallizes and grows in a single crystal having uniform lattice structure.

During the growth of single crystals of semiconductor, appropriate impurities may be added to the melt to form either a P-type or an N-type semiconductor. Their concentrations are also controlled. In order to form a junction transistor, following two methods are used:

- (a) Impurity variation method, and (b) Speed variation method.

(a) Impurity variation method

In this method, the impurity content of the semiconductor is altered in its type as well as quantity. For example, in making NPN germanium grown junction transistor, a small quantity of N-type impurity is added to molten germanium and the crystal growth is started by dipping the seed crystal in the melt by lowering the shaft suitably. The part of the crystal that grows initially is the high resistivity N-type and forms the collector part of the transistor.

Now keeping the pulling continuous, enough P-type impurity is added to the melt to over-balance the N-type impurity. This forms the base of the transistor. This should be very thin. Hence the seed crystal is pulled to a very short distance after putting the P-type impurity. Further, a large amount of N-type impurity is added to the melt. The part of the crystal that now grows is a low resistivity N-type and forms the emitter of the transistor.

(b) Speed variation method

The grown junction may be formed by suddenly varying the rate of pulling the seed crystal from the melt. This method is based on the fact that proportions in which N and P-types impurities crystallise i.e., enter the grown crystal depends on the rate of growth i.e., rate of pulling the crystal. When the germanium melt contains proper amounts of impurities (N and P-type) and seed crystal is pulled slowly a P-type crystal is grown and if seed crystal is pulled fast, then crystal grown is N-type. Thus NPN junction transistor may be formed simply by altering the rate of pulling the crystal.

(ii) Alloy type (Fused Junction) transistors

This process is similar to soldering and PNP transistor is generally made by this process. In this method, first of all N-type germanium is obtained by growing a crystal (as described above in grown junction method) with uniform doping using N-type impurity.

Now a wafer of this crystal about 0.080 inch square and 0.003 to 0.005 inch thick is taken. This is placed in graphite jig with a dot of prepared indium on either side. One dot is larger, about 3 times, than the other. The larger one is finally used as collector while the smaller as emitter. This assembly consisting of N-type wafer and two indium dots is placed in furnace and heated to about 500°C in an atmosphere of hydrogen. As a result of extreme heat, the indium melts (melting point 155°C) and starts combining with germanium. Germanium, on the other hand does not melt since its melting point is above 500°C.

The combining action is similar to that of soldering where molten indium dissolves some of the germanium and forms a saturated solution. Now, the jig is removed from the furnace. On cooling molten germanium with indium content recrystallizes to form a crystal of P-type germanium at the solid-liquid interface. On further cooling, the rest of the indium solidifies as an alloy containing a little germanium.

Leads for emitter and collector are soldered to the dots making non-rectifying contacts as shown in fig. (6.31). Further, non-rectifying base contact is usually made by welding a strip or loop of gold plated wire to the base plate. The result is a PNP transistor. Large area collector junction helps in collecting most of the holes emitted from the emitter ensuring that the collector current almost equals the emitter current. The spacing between two junctions inside germanium wafer is very small and determines the electrical properties of the transistor.

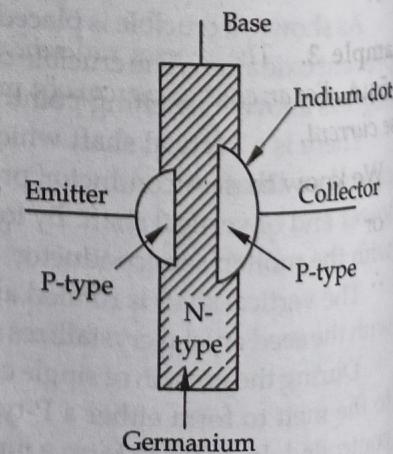


Fig. 6.31 Fused junction transistor

6.16 TRANSISTOR CURRENT AND VOLTAGE NOTATION

Standard circuit notation will be used in our transistor circuit analysis. Subscripts e or E, b or B and c or C will refer to emitter, base and collector quantities respectively. For dc quantities, we will use capital letters with capital subscripts as shown below:

Emitter current I_E , collector current I_C ,

Base current I_B , collector-emitter voltage V_{CE}

Emitter-base voltage V_{EB} , Emitter supply voltage V_{EE}

Collector supply voltage V_{CC} , Base supply voltage V_{BB}

The instantaneous value of time varying component will be identified by lower-case letters with lower subscripts as

Emitter current i_e , collector current i_c

Base current i_b , collector-emitter voltage v_{ce}

Emitter-base voltage v_{eb}

The rms values of ac currents are expressed as

Emitter current I_e , Base current I_b , collector current I_c

The total ac and dc currents are expressed by small letters with capital subscript as shown below:

Emitter current i_E , collector current i_C and base current i_B

For example $i_E = I_E + I_e$

SOLVED EXAMPLES

Example 1. In common base connection $I_C = 0.96 \text{ mA}$ and $I_B = 0.05 \text{ mA}$. What is the value of α .

We know that, $\alpha = I_C/I_E$ and $I_E = I_B + I_C$

$$\begin{aligned}\alpha &= \frac{I_C}{I_C + I_B} \\ &= \frac{0.96 \times 10^{-3}}{0.96 \times 10^{-3} + 0.05 \times 10^{-3}} = \frac{0.96}{1.01} = 0.95\end{aligned}$$

Example 2. In common base connection, the emitter current is 1 mA . If the emitter side is open, the collector current is $60 \mu\text{A}$. Calculate the total current $\alpha = 0.93$.

We know that

$$I_T = \alpha I_E + I_{C0}$$

$$\therefore I_T = 0.93 \times (1 \times 10^{-3}) + (60 \times 10^{-6}) = 0.99 \text{ mA}$$

Example 3. The reverse saturation current in NPN transistor in common base configuration is $15.5 \mu\text{A}$. For an emitter current of 4 mA , collector current is 2.47 mA . Find the value of current gain and base current.

We know that

$$I_C = \alpha I_E + I_{CBO}$$

$$\alpha I_E = I_C - I_{CBO}$$

$$\alpha = \frac{I_C - I_{CBO}}{I_E}$$

$$= \frac{2.47 \times 10^{-3} - 15.5 \times 10^{-6}}{4 \times 10^{-3}}$$

$$= \frac{(2.47 - 0.0155) \times 10^{-3}}{4 \times 10^{-3}} = 0.11$$

6.30

$$\text{Now, } I_B = I_E - I_C = 4 - 2.47 = 1.53 \text{ mA}$$

Example 4. A transistor has $I_B = 105 \mu\text{A}$ and $I_C = 2.05 \text{ mA}$. Find: (a) β of transistor, (b) α of transistor, (c) emitter current I_E , (d) Now, if I_B changes by $27 \mu\text{A}$ and I_C changes by $+0.65 \text{ mA}$, find the new value of β .

(a) We know that, $\beta = I_C/I_B$

$$\therefore \beta = \frac{2.05 \times 10^{-3}}{105 \times 10^{-6}} = 19.5$$

$$(b) \alpha = \frac{\beta}{1+\beta} = \frac{19.5}{1+19.5} = 0.95$$

$$(c) I_E = I_B + I_C = [(105 \times 10^{-6}) + (2.05 \times 10^{-3})] \text{ amp} \\ = (0.105 + 2.05) \times 10^{-3} = 2.155 \times 10^{-3} \text{ amp.} = 2.155 \text{ mA}$$

(d) Given that, $\Delta I_B = 27 \mu\text{A}$ and $\Delta I_C = 0.65 \text{ mA}$

$$\text{Now, } I_B = 105 \mu\text{A} + 27 \mu\text{A} = 132 \mu\text{A}$$

and

$$I_C = 2.05 \text{ mA} + 0.65 \text{ mA} = 2.70 \text{ mA}$$

$$\therefore \beta = \frac{I_C}{I_B} = \frac{2.7 \times 10^{-3} \text{ A}}{132 \times 10^{-6} \text{ A}} = 20.5$$

Example 5. The emitter current I_E in a transistor is 4 mA . If the leakage current I_{CBO} is 6 mA and $\alpha = 0.98$, find the collector and base currents.

We know that, $I_C = \alpha I_E + I_{CBO}$

$$\therefore I_C = 0.98 \times (4 \times 10^{-3}) + 0.006 \times 10^{-3} \\ = 3.926 \times 10^{-3} = 3.926 \text{ mA}$$

Now

$$I_B = I_E - I_C = (4 \times 10^{-3}) - (3.926 \times 10^{-3}) \\ = 0.074 \times 10^{-3} = 0.074 \text{ mA}$$

Example 6. In a transistor circuit $I_E = 5 \text{ mA}$, $I_C = 4.95 \text{ mA}$, $I_{CEO} = 200 \mu\text{A}$. Calculate β and leakage current I_{CBO} .

$$\begin{aligned} \beta &= \frac{I_C}{I_B} = \frac{I_C}{I_E - I_C} \\ &= \frac{4.95 \times 10^{-3}}{5 \times 10^{-3} - 4.95 \times 10^{-3}} = \frac{4.95}{5 - 4.95} = \frac{4.95}{0.05} = 99 \end{aligned}$$

Further $I_{CEO} = (1 + \beta) I_{CBO}$

$$\therefore I_{CBO} = \frac{I_{CEO}}{1 + \beta} = \frac{200 \mu\text{A}}{100} = 2 \mu\text{A}$$

Example 7. A germanium transistor used as an amplifier has a collector cut off current $I_{CBO} = 10 \mu\text{A}$ at a temperature 27°C and $\beta = 50$.

(a) What is the collector current when the base current is 0.25 mA ?

(b) Assuming that β does not change with temperature, what would be the value of new collector current, if the transistor's temperature rises to 50°C ?

(a) We know that, $I_C = \beta I_B + (1 + \beta) I_{CBO}$

$$\therefore I_C = 50 \times (0.25 \times 10^{-3}) + (1 + 50) \times (10 \times 10^{-6}) \text{ A} \\ = 13.01 \times 10^{-3} \text{ A} = 13.01 \text{ mA}$$

(b) We know that I_{CBO} doubles for every rise in temperature. Therefore,

$$(I_{CBO})_{50} = I_{CBO} \times 2^{(T_2 - T_1)/10} \\ = 10 \times 2^{(50 - 27)/10} \mu\text{A} \\ = 10 \times 2^{2.3} = 49.2 \mu\text{A} = 49.2 \times 10^{-6} \text{ A}$$

$$\text{Now } (I_C)_{50} = \beta I_B + (1 + \beta)(I_{CBO})_{50} \\ = [50 \times (0.25 \times 10^{-3}) + 51 \times (49.2 \times 10^{-6})] \text{ A} \\ = 15.01 \times 10^{-3} \text{ A} = 15.01 \text{ mA}$$

EXERCISES AND PROBLEMS

1. What is a transistor? Why is it so called? How it is biased?
2. Explain the mechanism of current flow in a PNP and NPN transistors.
3. Explain the following:
 - (i) Why is a transistor low powered device?
 - (ii) Why is collector wider than emitter and base?
 - (iii) Why is base made thin?
 - (iv) Why is collector current slightly less than emitter current?
 - (v) In a transistor operating in active region, although the collector junction is reverse-biased, the collector current is quite large. Explain.
4. Show different current components in a transistor and prove

$$I_C = I_{pC} + I_{CO}$$

 majority minority
5. Name the three possible transistor connections. Explain the operation of transistor as an amplifier.
6. (i) Define α . Show that it is always less than unity.
(ii) Define β . Show that

$$\beta = \frac{\alpha}{(1 - \alpha)}$$
7. For a PNP transistor biased in active region, indicate and discuss the various electron and

TRANSISTOR BIASING AND THERMAL STABILIZATION

10.1 TRANSISTOR BIASING

Among the basic functions of a transistor is its amplification. For faithful amplification (amplified magnitude of signal without any change in shape), the following three conditions must be satisfied:

- (i) the emitter-base junction should be forward biased,
- (ii) the collector-base junction should be reverse biased, and
- (iii) there should be proper zero signal collector current.

The proper flow of zero signal collector current (proper operating point of a transistor) and the maintenance of proper collector-emitter voltage during the passage of signal is known as *transistor biasing*.

When a transistor is not properly biased, it works inefficiently and produces distortion in the output signal. Hence a transistor should be biased correctly. A transistor is biased either with the help of battery or associating a circuit with the transistor. The latter method is generally employed. The circuit used with the transistor is known as *biasing circuit*.

10.2 STABILISATION

The maintenance of the operating point stable is known as *stabilisation*.

There are two factors which are responsible for shifting the operating point. Firstly, many of the transistor parameters are markedly temperature sensitive and secondly when a transistor is replaced by another of the same type, there is a wide spread in the values of transistor parameters. The problem of operating point instability is not faced in case of vacuum tubes. The reason is that the tube parameters are almost independent of working temperature and it is also possible to manufacture tubes with identical characteristics. So, stabilization of the operating point is necessary due to the following reasons:

- (a) Temperature dependence of I_C ,
- (b) Individual variations and
- (c) Thermal runaway.

(a) Temperature dependence of I_C . The instability of I_C^* is principally caused by the following three sources:

- (i) The collector leakage current I_{CO} is greatly influenced by temperature changes. The I_{CO} doubles for every 10°C rise in temperature.
- (ii) Increase of β with increase of temperature.
- (iii) Variation of V_{BE} (Base to emitter voltage) with temperature. Here it should be remembered that V_{CE} also changes with temperature but the change is very small. Hence I_C is almost independent of V_{CE} .

* $I_C = \beta I_B + I_{CO}(\beta + 1)$

(b) **Individual variations.** When a transistor is replaced by another transistor of the same type, the value of β and V_{BE} are not exactly the same. Hence, the operating point is changed. So, it is necessary to stabilise the operating point irrespective of individual variations in transistor parameters.

(c) **Thermal runaway.** Depending upon the construction of a transistor, the collector junction can withstand a maximum temperature. The range of temperature lies between 60°C to 100°C for Ge transistor and 150°C to 225°C for Si transistor. If the temperature increases beyond this range then the transistor burns out. The increase in the collector junction temperature is due to thermal runaway. When a collector current flows in a transistor, it is heated i.e., its temperature increases. If no stabilization is done, the collector leakage current also increases. This further increases the transistor temperature. Consequently, there is a further increase in collector leakage current. The action becomes cumulative and the transistor may ultimately burn out. The self-destruction of an unstabilized transistor is known as thermal runaway.

The following two techniques are used for stabilization

- (i) **Stabilization techniques.** The technique consists in the use of a resistive biasing circuit which permits such a variation of base current I_B as to maintain I_C almost constant inspite of variation of I_{CO} , β and V_{BE} .
- (ii) **Compensation techniques.** In this technique temperature sensitive devices such as diodes, transistors, thermistors etc. are used. Such devices produce compensating voltages and currents in such a way that the operating point is maintained stable.

10.3 STABILITY FACTOR

The stability factor S is defined as the rate of change of collector current I_C with respect to the reverse saturation current I_{CO} , keeping β and V_{BE} constant, i.e.,

$$S = \frac{\partial I_C}{\partial I_{CO}} \approx \frac{\Delta I_C}{\Delta I_{CO}} \quad \dots(1)$$

This expression shows that smaller is the value of S , higher is the stability. So, the stability factor S should be kept as small as possible. The lowest value of S that can be obtained is unity since I_C must include I_{CO} . Closer is the value of S to unity, lesser will be the variation of operating point with temperature.

In the definition of S , β and V_{BE} are assumed to be constant while they vary with temperature. Hence we define the following two other stability constants:

- (i) **Stability factor S_β .** This is defined as the rate of change of I_C with β keeping I_{CO} and V_{BE} constant, i.e.,

$$S_\beta = \frac{\partial I_C}{\partial \beta} \approx \frac{\Delta I_C}{\Delta \beta} \quad \dots(2)$$

- (ii) **Stability factor S_V .** This is defined as the rate of change of I_C with V_{BE} , keeping I_{CO} and β constant, i.e.,

$$S_V = \frac{\partial I_C}{\partial V_{BE}} \approx \frac{\Delta I_C}{\Delta V_{BE}} \quad \dots(3)$$

Expression for stability factor S.

When a transistor is biased in the active region of its characteristics, the collector current I_C is related to the base current I_B by the following expression

$$I_C = \beta I_B + (1 + \beta) I_{CO} \quad \dots(4)$$

Differentiating eq. (4) with respect to I_C considering β to be constant, we get

Transistor Biasing and Thermal Stabilization

$$1 = \beta \frac{dI_B}{dI_C} + (1 + \beta) \frac{\partial I_{CO}}{\partial I_C}$$

or

$$1 = \beta \frac{dI_B}{dI_C} + (1 + \beta) \cdot \frac{1}{S} \quad \left(\because S = \frac{\partial I_C}{\partial I_{CO}} \right)$$

or

$$1 - \beta \frac{dI_B}{dI_C} = (1 + \beta) \cdot \frac{1}{S}$$

$$S = \frac{(1 + \beta)}{1 - \beta \frac{dI_B}{dI_C}}$$

... (5)

The value of dI_B/dI_C depends upon the type of biasing arrangement. The stability factor S gives a measure of the change in I_C with respect to I_{CO} whether the change is the result of temperature variation or due to the transistor being replaced by another of the same type.

Expression for stability factor S_β .

Differentiating eq. (4) with respect to I_C and assuming I_{CO} to be constant, we get

$$1 = \beta \frac{dI_B}{dI_C} + I_B \frac{\partial \beta}{\partial I_C} + I_{CO} \frac{\partial \beta}{\partial I_C}$$

or

$$\frac{\partial \beta}{\partial I_C} [I_{CO} + I_B] = 1 - \beta \frac{dI_B}{dI_C}$$

or

$$\frac{I_{CO} + I_B}{S_\beta} = 1 - \beta \frac{dI_B}{dI_C} \quad \left(\because S_\beta = \frac{\partial I_C}{\partial \beta} \right)$$

$$S_\beta = \frac{I_{CO} + I_B}{1 - \beta \frac{dI_B}{dI_C}}$$

... (6)

With the help of this equation we can find out variation in I_C as a result of variation in β .

Stability factor for common base configuration

In case of common base configuration, the collector current I_C is given by

$$I_C = \alpha I_E + I_{CO} \quad ... (7)$$

where I_E = emitter current

I_{CO} = reverse saturation current

Differentiating eq. (7) with respect to I_{CO} , we get

$$\frac{dI_C}{dI_{CO}} = 0 + 1 \quad \text{or} \quad \frac{dI_C}{dI_{CO}} = 1$$

$$S = 1$$

or
(e) This shows that common base configuration is highly stable.

Stability factor for common emitter configuration

In this configuration, the collector current I_C is given by

$$I_C = \beta I_B + (1 + \beta) I_{CO}$$

$$\frac{dI_C}{dI_{CO}} = (1 + \beta)$$

or

If $\beta = 50$, then $S = 51$.

$$S = (1 + \beta)$$

This shows that the collector current changes 51 times when there is a change in reverse saturation current. So, the collector current is highly dependent on I_{CO} (which depends on temperature). Therefore, for this configuration, bias stabilisation is very important to improve the stability factor.

10.4 DIFFERENT METHODS FOR TRANSISTOR BIASING

From the point of view of simplicity and economy, only one source of supply (instead of two V_{BB} and V_{CC}) in the output circuit (*i.e.*, V_{CC}) is used. Some of the methods used for providing bias for a transistor are as follows:

- (1) *Base resistor method.*
- (2) *Collector to base bias.*
- (3) *Base bias with collector and emitter feedbacks.*
- (4) *Voltage divider bias.*

The basic principle involved in all the above methods is to obtain the required base current (*i.e.*, collector current) from V_{CC} in zero signal conditions. The value of collector load is selected in such a way that the voltage between collector and emitter should not fall below 0.5 volt for germanium transistor and 0.7 volt for silicon transistor.

10.5 BASE RESISTOR METHOD

Figure (10.1) shows an NPN transistor connected in *CE* configuration with resistor biased. In this method, a high resistance R_B is connected between positive terminal of supply V_{CC} and base of the transistor. Here, it should be remembered that if the transistor is PNP, then R_B

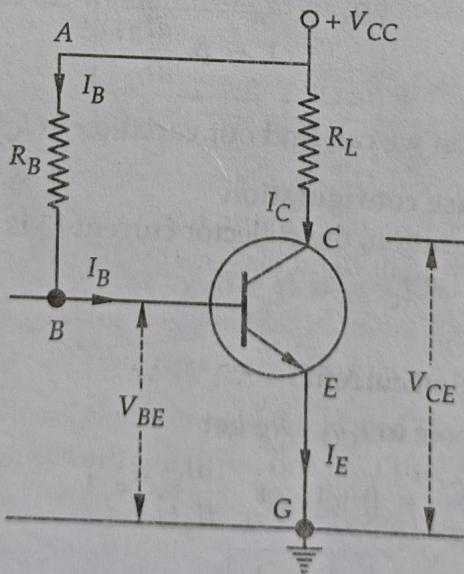


Fig. 10.1 *CE*, NPN transistor with base resistor biased

is connected between negative terminal of supply V_{CC} and base of the transistor. Here, the required zero signal base current flows through R_B and is provided by V_{CC} . In fig. (10.1), the base-emitter junction is forward biased because the base is positive w.r.t. emitter. By a proper selection of R_B , the required zero signal base current (and hence $I_C = \beta I_B$) can be made to flow.

Circuit analysis

Here, we shall find the value of R_B such that the required collector current flows under zero signal conditions. Let I_C be the required zero signal collector current.

Considering the closed circuit ABEGA and applying the Kirchhoff's voltage law, we have

$$I_B R_B + V_{BE} = V_{CC}$$

$$I_B R_B = V_{CC} - V_{BE}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} \quad \dots(1)$$

Further

$$I_B = \frac{I_C}{\beta} \quad \dots(2)$$

Substituting the value of I_B from eq. (2) in eq. (1), we get

$$R_B = \frac{(V_{CC} - V_{BE}) \beta}{I_C} \quad \dots(3)$$

The value of V_{BE} can be seen from the transistor manual. Using eq. (3), the value of R_B can be calculated. As V_{BE} is generally very small as compared to V_{CC} , hence

$$R_B = \frac{\beta V_{CC}}{I_C} \quad \dots(4)$$

From eq. (4), the value of R_B can be found directly. Hence, this method is sometimes called as fixed-bias method.

Stability factor S

The stability factor S is given by

$$S = \frac{(1 + \beta)}{1 - \beta (dI_B/dI_C)}$$

In base resistor method, the base current I_B * is independent of collector current I_C . So, the stability factor S is given by

$$S = (1 + \beta) \quad \dots(5)$$

If $\beta = 100$, then $S = 101$. This shows that I_C changes 101 times as much as any change in I_C . Thus, I_C is very dependent upon I_C and hence upon temperature. The value of S is the highest that can be obtained. Hence the circuit has very poor stability. This is the main disadvantage of base resistor method or fixed bias method. Due to this fact this method is rarely used.

SOLVED EXAMPLES

Example 1. Figure (10.2) shows the base bias with emitter feedback. Obtain an expression for I_C .

Considering the closed circuit ABEGA, and applying the Kirchhoff's law, we get

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E \quad \dots(1)$$

Now $I_B = I_C/\beta$ and $I_E \equiv I_C$

Substituting these values in eq. (1), we get

$$V_{CC} \equiv R_B (I_C/\beta) + V_{BE} + I_C R_E$$

$$V_{CC} - V_{BE} \equiv I_C [R_E + (R_B/\beta)]$$

or

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{V_{CC}}{R_B}$$

From eq. (1)

So, I_B is independent of I_C .

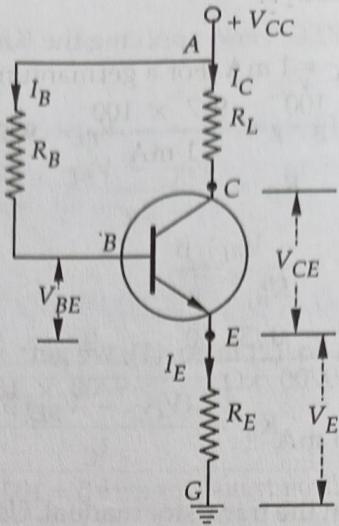


Fig. 10-2

$$\therefore I_C \approx \frac{V_{CC} - V_{BE}}{[R_E + (R_B/\beta)]} \quad \dots(2)$$

As V_{BE} is negligibly small as compared to V_{CC} , hence

$$I_C \approx \frac{V_{CC}}{[R_E + (R_B/\beta)]} \quad \dots(3)$$

Example 2. Calculate the stability factor for base bias with emitter feedback.

In case of base bias with emitter feedback, we have

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$

Further,

$$I_E = I_B + I_C$$

∴

$$V_{CC} = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

or

$$I_B = \frac{V_{CC} - V_{BE} - I_C R_E}{R_E + R_B} \quad \dots(1)$$

Differentiating eq. (1) with respect to I_C , we get

$$\frac{dI_B}{dI_C} = \frac{0 - 0 - R_E}{R_E + R_B} = -\frac{R_E}{R_E + R_B}$$

Now, the expression for stability factor S is given by

$$\begin{aligned} S &= \frac{1 + \beta}{1 - \beta \left(\frac{dI_B}{dI_C} \right)} = \frac{1 + \beta}{1 - \beta \left(-\frac{R_E}{R_E + R_B} \right)} \\ &= \frac{1 + \beta}{1 + \beta [R_E/(R_E + R_B)]} \quad \dots(2) \end{aligned}$$

Example 3. (i) A germanium transistor is to be operated at zero signal $I_C = 1$ mA. If the collector supply $V_{CC} = 10$ V, what is the value of R_B in base resistor method? Take $\beta = 100$.

(ii) If another transistor of the same batch with $\beta = 50$ is used, what will be the new value of zero signal I_C for the same R_B .

(i) The value of R_B is given by

$$R_B = \frac{(V_{CC} - V_{BE}) \beta}{I_C}$$

Here, $V_{CC} = 10 \text{ V}$, $\beta = 100$ and $I_C = 1 \text{ mA}$. For a germanium transistor $V_{BE} = 0.3 \text{ V}$.

$$\therefore R_B = \frac{(10 - 0.3) 100}{1 \text{ mA}} = \frac{9.7 \times 100}{1 \text{ mA}} = 9700 \text{ k}\Omega$$

(ii) The value of I_C is given by

$$\begin{aligned} I_C &= \frac{(V_{CC} - V_{BE}) \beta}{R_B} \\ &= \frac{(10 - 0.3) 50}{9700 \text{ k}\Omega} = \frac{9.7 \times 50}{9700 \times 10^3 \Omega} \\ &= 0.5 \text{ mA} \end{aligned}$$

Example 4. Figure (10.3) shows a silicon transistor with $\beta = 100$ and biased by base resistor method. Determine the operating point.

The value of I_C is given by

$$I_C = \frac{(V_{CC} - V_{BE}) \beta}{R_B}$$

Here, $V_{CC} = 10 \text{ V}$, $V_{BE} = 0.7 \text{ V}$ (Silicon transistor), $\beta = 100$ and $R_B = 930 \text{ k}\Omega$.

$$\therefore I_C = \frac{(10 - 0.7) 100}{930 \text{ k}\Omega} = 1 \text{ mA.}$$

$$\begin{aligned} \text{Now, } V_{CE} &= V_{CC} - I_C R_L \\ &= 10 - 1 \text{ mA} \times 4 \text{ k}\Omega \\ &= (10 - 4) \text{ volt} \\ &= 6 \text{ V} \end{aligned}$$

∴ Operating point is (6 V, 1 mA).

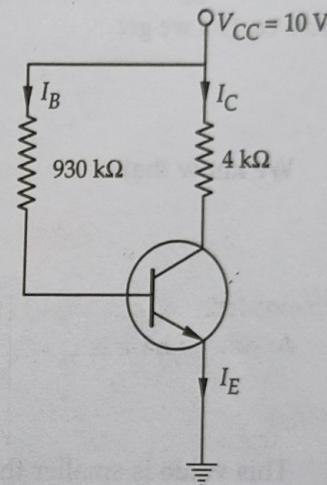


Fig. 10.3

10.6 COLLECTOR TO BASE BIAS

The circuit of an NPN transistor connected in CE configuration with collector to base bias is shown in fig. (10.4). This circuit is same as base bias circuit except that the base resistor R_B is returned to collector rather than to V_{CC} supply. Using this circuit, there is considerable improvement in the stability. If the collector current I_C tends to increase (either as a result of rise in temperature or as a result of transistor being replaced by another of larger β), the d.c. voltage drop across R_L increases and consequently V_{CE} decreases. As a result, the base current I_B also reduces. This will tend to compensate for the original increase. The compensation is never exact.

Circuit analysis

The required value of R_B needed to give the zero signal current I_C can be calculated as follows:

$$\text{Voltage drop across } R_L = (I_C + I_B) R_L \equiv I_C R_L \quad \dots(1)$$

$$\text{From the figure, } I_C R_L + I_B R_B + V_{BE} = V_{CC}$$

or

$$I_B R_B = V_{CC} - V_{BE} - I_C R_L$$

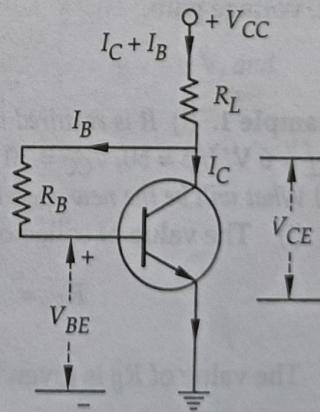


Fig. 10.4

$$\therefore R_B = \frac{V_{CC} - V_{BE} - I_C R_L}{I_B}$$

$$\text{or } R_B = \frac{(V_{CC} - V_{BE} - I_C R_L) \beta}{I_C} \quad \dots(2)$$

Stability factor S. Applying KVL to the circuit of fig. (10.4), we have

$$(I_B + I_C) R_L + I_B R_B + V_{BE} = V_{CC}$$

or

$$I_B (R_L + R_B) + I_C R_L + V_{BE} = V_{CC}$$

∴

$$I_B = \frac{V_{CC} - V_{BE} - I_C R_L}{R_L + R_B} \quad \dots(3)$$

Since V_{BE} is almost independent of collector current ($V_{BE} = 0.7$ for Si and 0.3 V for Ge), then from eq. (3), we get

$$\frac{dI_B}{dI_C} = - \frac{R_L}{R_L + R_B} \quad \dots(4)$$

We know that

$$S = \frac{1 + \beta}{1 - \beta(dI_B/dI_C)}$$

∴

$$S = \frac{1 + \beta}{1 + \beta \left(\frac{R_L}{R_L + R_B} \right)} \quad \dots(5)$$

This value is smaller than $(1 + \beta)$ which is obtained for fixed-bias circuit. Thus there is an improvement in the stability.

The circuit of fig. (10.4) provides a negative feedback. This reduces the gain of the amplifier. So the increased stability of the collector to base bias circuit is obtained at the cost of a.c. voltage gain.

SOLVED EXAMPLES

Example 1. (i) It is required to set the operating point by biasing with feedback resistor at $I_C = 1$ mA, $V_{CE} = 6$ V. If $\beta = 50$, $V_{CC} = 10$ V, $V_{BE} = 0.3$ V, how will you do it?

(ii) What will be the new operating point if $\beta = 50$, all other circuit values remaining the same?

(i) The value of collector load R_L is given by

$$R_L = \frac{V_{CC} - V_{CE}}{I_C} = \frac{10 \text{ V} - 6 \text{ V}}{1 \text{ mA}} = 4 \text{ k}\Omega \quad \dots(1)$$

The value of R_B is given by

$$\begin{aligned} R_B &= \frac{(V_{CC} - V_{BE} - I_C R_L) \beta}{I_C} \\ &= \frac{(10 - 0.3 - (1 \times 10^{-3} \times 4 \times 10^3)) 100}{1 \times 10^{-3}} \\ &= 570 \times 10^3 \Omega = 570 \text{ k}\Omega \end{aligned} \quad \dots(2)$$

(ii) In this case $\beta = 50$. Substituting the values in eq. (2), we have

$$570 \text{ k}\Omega = \frac{(10 - 0.3 - I_C \times 4 \text{ k}\Omega) 50}{I_C}$$

$$570 I_C = 9.3 \times 50 - I_C \times 200$$

$$770 I_C = 9.3 \times 50 \quad \text{or} \quad I_C = \frac{9.3 \times 50}{770 \text{ k}\Omega}$$

or

$$\therefore I_C = 0.66 \text{ mA}$$

Now, Collector-emitter voltage

$$\begin{aligned} V_{CE} &= V_{CC} - I_C R_L \\ &= 10 - 0.66 \text{ mA} \times 4 \text{ k}\Omega = 7.36 \text{ V} \end{aligned}$$

 \therefore New operating point = 7.36 V, 0.66 mA

Example 2. Determine the bias resistor R_B for fixed bias and collector to base bias and compare the stability factor S for both of them. Given

$$V_{CC} = 12 \text{ V}, R_L = 330 \text{ ohms}, I_B = 0.3 \text{ mA}, \beta = 100, V_{CEQ} = 6 \text{ V}$$

$$\text{For a fixed bias, } R_B \approx \frac{V_{CC}}{I_B} = \frac{12 \text{ V}}{0.3 \text{ mA}} = 40 \text{ k}\Omega$$

$$\text{For collector to base bias, } R_B \approx \frac{V_{CEQ}}{I_B} = \frac{6 \text{ V}}{0.3 \text{ mA}} = 20 \text{ k}\Omega$$

$$S \text{ for fixed bias} = 1 + \beta = 1 + 100 = 101$$

S for collector to base bias is given by

$$\begin{aligned} S &= \frac{1 + \beta}{1 + \beta \left(\frac{R_L}{R_L + R_B} \right)} = \frac{1 + 100}{1 + 100 \left(\frac{330}{330 + 20 \times 10^3} \right)} \\ &= \frac{101}{1 + 1.65} = 38.2 \end{aligned}$$

This shows that this biasing arrangement is considerably more stable as far as variations in Q point are concerned due to temperature causing I_{CO} to change.

Example 3. A PNP transistor with $\beta = 50$ is used in CE amplifier with collector to base bias. The collector circuit resistance $R_L = 2.5 \text{ k}\Omega$ and $V_{CC} = 10 \text{ V}$. Assume $V_{BE} = 0$, find

- (i) suitable value of R_B so as to make quiescent collector to emitter voltage $V_{CE} = -5 \text{ V}$, and
- (ii) the stability factor S .

(i) In case of PNP transistor

$$I_C \approx \frac{-V_{CC} - V_{CE}}{R_L} = \frac{-10 - (-5)}{2.5 \times 10^3} = -2 \text{ mA}$$

$$I_B = \frac{I_C}{\beta} = \frac{-2 \text{ mA}}{25} = -80 \mu\text{A}$$

$$R_B = \frac{V_{CE} - V_{BE}}{I_B} = \frac{-5 - 0}{-80 \times 10^{-6}} = 62.5 \text{ k}\Omega$$

(ii) The stability factor S is given by

$$\begin{aligned} S &= \frac{1 + \beta}{1 + \beta \left(\frac{R_L}{R_L + R_B} \right)} = \frac{1 + 25}{1 + 25 \left(\frac{2.5 \times 10^3}{2.5 \times 10^3 + 62.5 \times 10^3} \right)} \\ &= \frac{26}{1 + 25 \times (2.5/65)} = 13.32 \end{aligned}$$

10.7 BASE BIAS WITH COLLECTOR AND EMITTER FEEDBACKS

The circuit of base bias with collector and emitter feedbacks is shown in fig. (10.5). Using R_E , the circuit sensitivity to changes in β is reduced. Let β increase. Now, emitter voltage increases

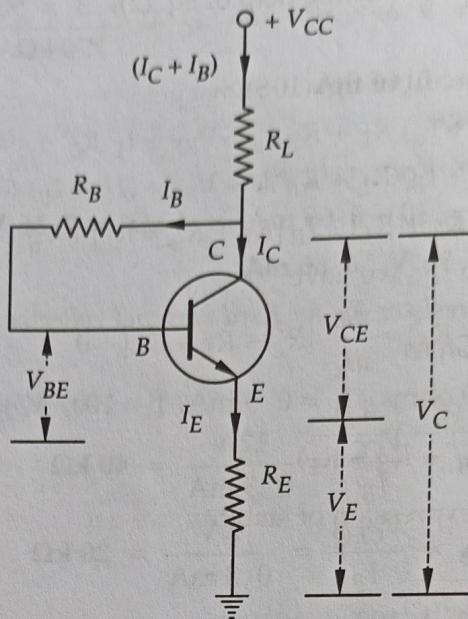


Fig. 10-5 Base bias with collector and emitter feedbacks

but collector voltage decreases. So the voltage across R_B is also reduced. This causes I_B to decrease thereby partially offsetting the increase in β .

Let there be a rise in temperature. Now, leakage current increases. As a result, the collector as well as emitter current increases. So, the voltage drop across R_E also increases. This provides negative feed back to the base and hence the base current reduces. We know that $I_B + I_C/\beta$. When I_B is reduced, then I_C is automatically reduced as β is constant. So, the rising tendency of I_C is checked as shown below in fig. (10.6).

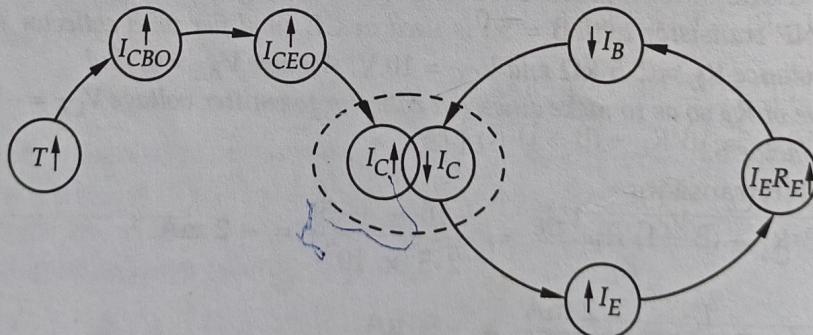


Fig. 10-6 Rising temperature is checked

Circuit Analysis

Assuming I_B to be negligibly small, the saturated collector current is given by

$$(I_C)_{\text{sat}} = \frac{V_{CC}}{R_E + R_L} \quad \dots(1)$$

The actual value of I_C can be calculated by applying KVL to the left of circuit of fig. (10.5) i.e.,

$$V_{CC} = I_C R_L + I_B R_B + I_E R_E + V_{BE}$$

$$\text{or } V_{CC} = I_C R_L + (I_C/\beta) R_B + I_C R_E + V_{BE} \quad (\because I_E \approx I_C)$$

$$I_C = \frac{V_{CC} - V_{BE}}{R_L + R_E + (R_B/\beta)} \quad \dots(2)$$

The value of R_B can be calculated with the help of eq. (2).

Stability factor S

Applying KVL to the left of the circuit of fig. (105), we get

$$\begin{aligned} V_{CC} &= (I_C + I_B) R_L + R_B I_B + V_{BE} + I_E R_E \\ &= (I_C + I_B) R_L + R_B I_B + V_{BE} + (I_C + I_B) R_E \\ &= I_C [R_L + R_E] + I_B [R_L + R_B + R_E] + V_{BE} \end{aligned}$$

Differentiating with respect to I_C , we have

$$0 = (R_L + R_E) + \frac{dI_B}{dI_C} [R_L + R_B + R_E] + 0$$

$$\text{or } \frac{dI_B}{dI_C} = -\frac{(R_L + R_E)}{(R_L + R_B + R_E)}$$

Putting this value in general expression of stability, we get

$$\begin{aligned} S &= \frac{(1 + \beta)}{1 - \beta (dI_B/dI_C)} \\ \text{or } S &= \frac{(1 + \beta)}{\left[1 + \beta \left\{ \frac{(R_L + R_E)}{(R_L + R_B + R_E)} \right\} \right]} \end{aligned} \quad \dots(3)$$

SOLVED EXAMPLES

Example 1. A transistor with $\beta = 45$ is used with collector to base resistor R_B biasing with quiescent value of 5 V for V_{CE} . If $V_{CC} = 24$ V, $R_1 = 10 \text{ k}\Omega$, $R_E = 270 \Omega$, find the value of R_B .

See fig. (10-7). Applying KVL to collector and emitter loop, we have

$$V_{CC} - I_C R_L - V_{CE} - R_E I_E = 0$$

$$\text{or } V_{CC} - V_{CE} = I_C R_L + R_E I_E$$

$$\text{or } V_{CC} - V_{CE} = [\beta R_L + (\beta + 1) R_E] I_B$$

$$\text{or } I_B = \frac{V_{CC} - V_{CE}}{\beta R_L + (\beta + 1) R_E}$$

$$= \frac{24 - 5}{45 \times 10 + 50 \times 0.27}$$

$$= 0.041 \text{ mA}$$

Further, $V_{CC} - R_L I_C - R_B I_B - V_{BE} - I_E R_E = 0$

$$\text{or } V_{CC} - V_{BE} = R_L \beta I_B + R_B I_B + (\beta + 1) R_E I_B$$

$$\text{or } 24 - 0.7 = I_B [45 \times 10 + R_B + 50 \times 0.27]$$

$$\text{or } 23.3 = 0.041 [450 + R_B + 12.42]$$

Solving for R_B , we get

$$R_B = 105.87 \text{ k}\Omega$$

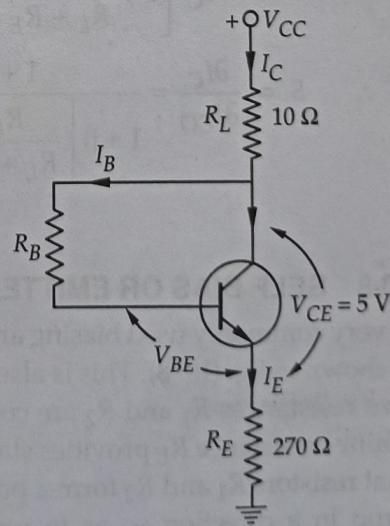


Fig. 10-7

Example 2. In the circuit shown in fig. (10.5), $V_{CC} = 24 \text{ V}$, $R_L = 10 \text{ k}\Omega$ and $R_E = 270 \Omega$. If the silicon transistor is used with $\beta = 45$ and if under quiescent conditions $V_{CE} = 5 \text{ V}$, determine R_B and stability factor S .

Let $I_E = (I_C + I_B)$ be the current flowing through R_L . Applying Kirchhoff's voltage law to the right side of the circuit, we have

$$\begin{aligned} V_{CC} &= R_L I_E + V_{CE} + R_E I_E = V_{CE} + I_E (R_L + R_E) \\ \therefore I_E &= \frac{V_{CC} - V_{CE}}{R_L + R_E} = \frac{24 - 5}{(10 + 0.270) \cdot 10^3} \\ &= 1.85 \text{ mA} \end{aligned}$$

We know that $\beta = I_C/I_B$

$$\therefore \beta + 1 = \frac{I_C}{I_B} + 1 = \frac{I_C + I_B}{I_B} = \frac{I_E}{I_B}$$

$$\text{or } I_B = \frac{I_E}{\beta + 1} = \frac{1.85 \text{ mA}}{46} = 0.04 \text{ mA}$$

Applying KVL to CBE loop, we get

$$V_{CB} = V_{CE} - V_{BE} = 5 - 0.7 = 4.3 \text{ V}$$

$$\text{So, } R_B = \frac{V_{CB}}{I_B} = \frac{4.3}{0.04 \text{ mA}} = 107 \text{ k}\Omega$$

Further,

$$V_{CC} = (I_B + I_C)[R_L + R_E] + I_B R_B + V_{BE}$$

or

$$V_{CC} = I_B [R_L + R_E + R_B] + I_C (R_L + R_E) + V_{BE}$$

∴

$$I_B = \frac{V_{CC} - V_{BE} - I_C (R_L + R_E)}{R_L + R_E + R_B}$$

Substituting, $I_C = \beta I_B + (1 + \beta) I_{CO}$

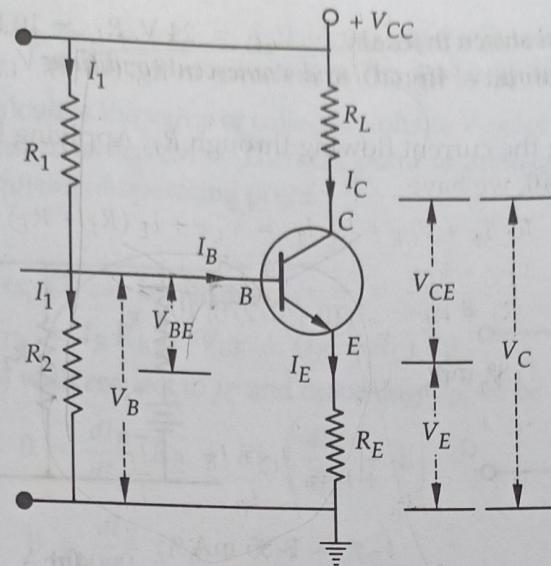
Substituting this value in the above equation, we get

$$\begin{aligned} I_C \left[1 + \frac{\beta (R_L + R_E)}{R_L + R_E + R_B} \right] &= (1 + \beta) I_{CO} + \frac{\beta (V_{CC} - V_{BE})}{R_L + R_E + R_B} \\ \therefore S = \frac{\partial I_C}{\partial I_{CO}} &= \frac{1 + \beta}{1 + \beta \left[\frac{R_L + R_E}{R_L + R_B + R_E} \right]} = \frac{1 + 45}{1 + 45 \left[\frac{(10 \times 10^3) + 270}{(10 \times 10^3) + (107 \times 10^3) + 270} \right]} \\ &= 9.3. \end{aligned}$$

10.8 SELF BIAS OR Emitter Bias (VOLTAGE DIVIDER BIAS)

A very commonly used biasing arrangement is self-bias or emitter bias. The circuit arrangement is shown in fig. (10.8). This is also known as universal bias stabilization circuit. In this method two resistances R_1 and R_2 are connected across supply voltage V_{CC} and provide biasing. The emitter resistance R_E provides stabilization. The name voltage divider is derived due to the fact that resistors R_1 and R_2 form a potential divider across V_{CC} . The resistance R_E causes a voltage drop in a direction so as to reverse-bias the emitter junction. Since the junction must be forward-biased, the base voltage is obtained from the supply through $R_1 - R_2$ network. The net forward bias across the emitter junction is equal to V_b minus the d.c. voltage drop across R_E .

The improvement in the operating point stability may be explained as follows: Let there be a rise in temperature. This causes a rise in I_{CO} i.e., a rise in I_C . Now, the current in R_E increases.

**Fig. 10-8** Voltage divider bias

As a result, the voltage drop across R_E increases and consequently the base current decreases. This decreases the collector current. Thus the presence of R_E reduces the increase in I_C and improves the operating point stability. In case of amplifiers, to avoid the loss of ac signal gain (because of the feedback caused by R_E) a capacitor of large capacitance is connected across R_E . The condenser offers a very small reactance to ac signal and hence it passes through the condenser.

Circuit analysis

Let current I_1 flows through R_1 . As the base current I_B is very small, the current flowing through R_2 can also be taken as I_1 . The calculation of collector current I_C is as follows:

The current I_1 flowing through R_1 or R_2 is given by

$$I_1 = \frac{V_{CC}}{(R_1 + R_2)} \quad \dots(1)$$

The voltage V_2 developed across R_2 is given by

$$V_2 = \left(\frac{V_{CC}}{R_1 + R_2} \right) R_2 \quad \dots(2)$$

Applying KVL to the base circuit, we have

$$\begin{aligned} V_2 &= V_{BE} + V_E = V_{BE} + I_E R_E \\ \text{or } V_2 &= V_{BE} + I_C R_E \quad (\because I_E \approx I_C) \\ I_C &= \frac{V_2 - V_{BE}}{R_E} \quad \dots(3) \end{aligned}$$

Here, I_C is almost independent of transistor parameters and hence good stabilization is ensured.

The collector emitter voltage V_{CE} can be calculated as follows:

Applying KVL to the collector side we have

$$\begin{aligned} V_{CC} &= I_C R_L + V_{CE} + I_E R_E \\ &= I_C R_L + V_{CE} + I_C R_E \\ V_{CE} &= V_{CC} - I_C (R_L + R_E) \quad \dots(4) \end{aligned}$$

Circuit analysis using Thevenin's theorem.

The Thevenin equivalent circuit of fig. (10.8) is shown in fig. (10.9).

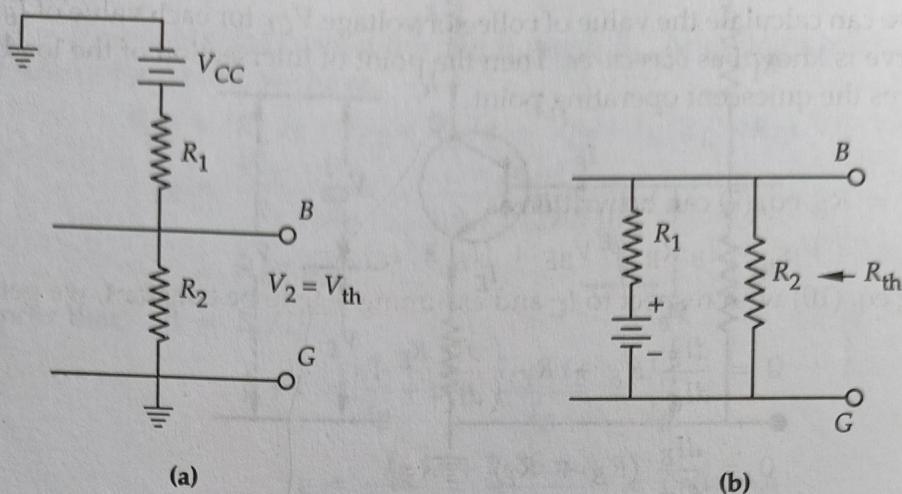


Fig. 10.9 Simplified equivalent circuit

From fig. (10.9), we have

$$V_2 = V_{Th} = \left(\frac{R_2}{R_1 + R_2} \right) V_{CC} \quad \dots(5)$$

$$R_{Th} = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2} \quad \dots(6)$$

Applying KVL to the base-emitter circuit, we have

$$V_{Th} = I_B R_{Th} + V_{BE} + (I_B + I_C) R_E \quad \dots(7)$$

Applying KVL to the emitter-collector circuit, we have

$$V_{CE} = V_{CC} - I_C (R_L + R_E) \quad (\because I_C \gg I_B) \quad \dots(8)$$

From eq. (8), we have

$$I_C = \frac{V_{CC} - V_{CE}}{(R_L + R_E)}$$

Substituting this value of I_C in eq. (7), we have

$$V_{Th} = I_B R_{Th} + V_{BE} + R_E \left[I_B + \frac{V_{CC} - V_{CE}}{R_L + R_E} \right]$$

or

$$V_{Th} = I_B R_{Th} + V_{BE} + R_E I_B + \frac{R_E V_{CC}}{R_L + R_E} - \frac{R_E V_{CE}}{R_L + R_E} \quad \dots(9)$$

From eq. (9), we can calculate the value of collector voltage V_{CE} for each value of I_B and plot the curve. The curve is known as *bias curve*. Then the point of intersection of the load line and this bias curve gives the quiescent operating point.

Stability factor

Considering $R_{Th} = R_B$, eq. (7) can be written as

$$V_{Th} = I_B R_B + V_{BE} + (I_B + I_C) R_E \quad \dots(10)$$

Differentiating eq. (10) with respect to I_C and assuming V_{BE} to be constant, we get

$$0 = \frac{dI_B}{dI_C} R_B + R_E \left(\frac{dI_B}{dI_C} + 1 \right)$$

or

$$0 = \frac{dI_B}{dI_C} (R_B + R_E) + R_E$$

$$\therefore \frac{dI_B}{dI_C} = \frac{-R_E}{(R_B + R_E)} \quad \dots(11)$$

We know that the stability factor S is given by

$$S = \frac{1 + \beta}{1 - \beta (dI_B/dI_C)} \quad \dots(12)$$

Substituting the value of dI_B/dI_C from eq. (11) in eq. (12), we get

$$S = \frac{1 + \beta}{1 + \beta \left(\frac{R_E}{R_B + R_E} \right)} \quad S = \frac{1}{\frac{R_E}{R_B + R_E}} = \frac{R_B + R_E}{R_E} \quad \dots(13)$$

Equation (13) can also be written as

$$S = (1 + \beta) \frac{(R_B + R_E)}{R_B + R_E + \beta R_E} = (1 + \beta) \frac{\frac{(R_B/R_E) + 1}{R_E}}{\frac{R_B}{R_E} + 1 + \beta} \quad \dots(14)$$

This expression shows that smaller the value of R_B , better is the stability. If R_B/R_E is very small then S approaches 1 which is best for S .

Let us reduce eq. (14) is another form. From eq. (14), we have

$$S + S\beta + S(R_B/R_E) = 1 + \beta + (R_B/R_E) + \beta(R_B/R_E)$$

$$S + S\beta - 1 - \beta = (R_B/R_E) + \beta(R_B/R_E) - S(R_B/R_E)$$

or

$$(S - 1)(1 + \beta) = (R_B/R_E)[1 + \beta - S]$$

$$\frac{R_B}{R_E} = \frac{(S - 1)(1 + \beta)}{(1 + \beta - S)}$$

...(15)

This equation can be used in solving many problems.

SOLVED EXAMPLES

Example 1. A silicon transistor uses potential divider method of biasing. $V_{CC} = 12$ V, $R_1 = 10$ k Ω , $R_2 = 5$ k Ω , $R_L = 1$ k Ω and $R_E = 3$ k Ω . Determine the operating point using Thevenin's theorem.

Refer to figs. (10.8) and (10.9)

Here $V_{Th} = \left(\frac{R_2}{R_1 + R_2} \right) V_{CC} = \left(\frac{5}{10 + 5} \right) 12 = 4 \text{ volt}$

and $R_{Th} = \frac{R_1 R_2}{R_1 + R_2} = \frac{10 \times 5}{10 + 5} = 3.3 \Omega$

From fig. [9.9 (c)], we have

$$\begin{aligned} V_{Th} &= I_B R_{Th} + V_{BE} + (I_B + I_C) R_E \\ &= I_B R_{Th} + V_{BE} + I_C R_E \\ &= I_B R_{Th} + V_{BE} + \beta I_B R_E \end{aligned} \quad (I_C \gg I_B)$$

Solving we get $I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + \beta R_E}$

\therefore Collector current $I_C = \beta I_B$

or $I_C = \frac{\beta (V_{Th} - V_{BE})}{R_{Th} + \beta R_E} = \frac{V_{Th} - V_{BE}}{\frac{R_{Th}}{\beta} + R_E}$

or $I_C \approx \frac{V_{Th} - V_{BE}}{R_E} \quad (\because R_E \gg R_{Th} \beta)$

so $I_C = \frac{4 - 0.7}{3 \text{ k}\Omega} = \frac{3.3}{3 \text{ k}\Omega} = 1.1 \text{ mA}$

Now

$$\begin{aligned} V_{CE} &= V_{CC} - I_C (R_L + R_E) \\ &= 12 - 1.1 \text{ mA} \times 4 \text{ k}\Omega = (12 - 4.4) \text{ V} \\ &= 7.6 \text{ volt} \end{aligned}$$

\therefore Operating point is (7.6 volt, 1.1 mA)

Example 2. A silicon transistor with $(V_{BE})_{sat.} = 0.8 \text{ V}$, $\beta = 100$, $(V_{CE})_{sat.} = 0.2 \text{ V}$. Find the maximum value of R_C for which transistor remains in saturation (see fig. 10.10).

Applying KVL to base-emitter circuit

$$5 - 200 I_B - 0.8 = 0$$

$$\therefore I_B = \frac{4.2}{200} = 0.021 \text{ mA}$$

$$\text{So, } I_C = \beta I_B = 100 \times 0.021 = 2.1 \text{ mA}$$

$$\text{But } I_C = \frac{V_{CC} - (V_{CE})_{sat.}}{R_C}$$

$$\therefore R_C = \frac{10 - 0.2}{2.1} = \frac{9.8}{2.1} = 4.667 \text{ k}\Omega$$

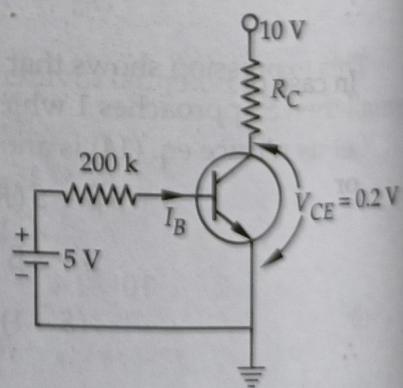


Fig. 10-10

Example 3. Find emitter current for the transistor with self bias circuit having $\beta = 100$, $V_{CC} = 20 \text{ V}$, $R_1 = 12 \text{ k}$, $R_2 = 8 \text{ k}$, $R_C = 2 \text{ k}$ and $R_E = 1 \text{ k}$.

Let us first calculate V_{Th} and R_{Th} to draw the Thevenin's equivalent circuit. We have

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$$V_{Th} = \left(\frac{V_{CC}}{R_1 + R_2} \right) \times R_2 = \left(\frac{20}{12 + 8} \right) \times 8 \text{ volt} = 8 \text{ volt}$$

$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2} = \frac{12 \times 8}{12 + 8} = 4.8 \text{ k}\Omega$$

The Thevenin's equivalent circuit is shown in fig. (10.11).
Applying KVL to input side

$$V_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

$$8 - 4.8 I_B - 0.7 - I_B (1 + 100) 1 = 0$$

Solving for I_B , we get

$$I_B = 0.0689 \text{ mA}$$

$$\text{Now } I_E = I_B (1 + \beta)$$

$$= 0.0689 (1 + 100) = 6.96 \text{ mA}$$

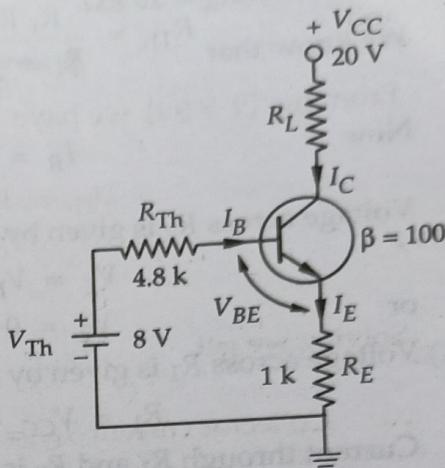


Fig. 10.11

Example 4. In a germanium transistor using potential divider method of biasing, the operating point is chosen such that $I_C = 2 \text{ mA}$, $V_{CE} = 4 \text{ V}$. If $R_L = 2 \text{ k}\Omega$, $V_{CC} = 10 \text{ V}$ and $\beta = 50$, determine the values of R_1 , R_2 and R_E . Assume $I_1 = 10 I_B$.

As I_B is very small as compared to I_1 so we can assume that the same current (I_1) is flowing through R_2 .

$$\text{Now base current } I_B = \frac{I_C}{\beta} = \frac{2 \text{ mA}}{50} = 0.04 \text{ mA}$$

∴ Current flowing through R_1 and R_2 is given by

$$I_1 = 10 I_B = 10 \times 0.04 = 0.4 \text{ mA}$$

$$\text{We know that } I_1 = \frac{V_{CC}}{R_1 + R_2}$$

$$\therefore (R_1 + R_2) = \frac{V_{CC}}{I_1} = \frac{10 \text{ V}}{0.4 \text{ mA}} = 25 \text{ k}\Omega \quad \dots(1)$$

In case of potential divider bias

$$V_{CC} = I_C R_L + V_{CE} + I_E R_E \quad (\because I_C \approx I_E)$$

$$V_{CC} = I_C R_L + V_{CE} + I_C R_E$$

$$10 = 2 \text{ mA} \times 2 \text{ k}\Omega + 4 \text{ V} + 2 \text{ mA} \times R_E$$

$$10 - 4 - 4 = 2 \text{ mA} \times R_E$$

$$\therefore R_E = \frac{2 \text{ V}}{2 \text{ mA}} = 1 \text{ k}\Omega \quad \dots(2)$$

The voltage across R_2 is given by

$$V_2 = V_{BE} + V_E = V_{BE} + R_E \times I_C$$

$$\text{or } V_2 = 0.3 + 1 \text{ k}\Omega \times 2 \text{ mA} = 0.3 + 2 \text{ V} = 2.3 \text{ volt}$$

$$\therefore \text{Resistance } R_2 = \frac{V_2}{I_1} = \frac{2.3 \text{ V}}{0.4 \text{ mA}} = 5.75 \text{ k}\Omega \quad \dots(3)$$

Now according to eq. (1)

$$R_1 = 25 \text{ k}\Omega - R_2 = 25 \text{ k}\Omega - 5.75 \text{ k}\Omega = 19.25 \text{ k}\Omega \quad \dots(4)$$

Example 5. A NPN transistor circuit uses the potential divider method of biasing has $\alpha = 0.985$ and $V_{BE} = 0.3$ V. If $V_{CC} = 15$ V, Calculate R_1 and R_L to place Q point at $I_C = 2$ mA and $V_{CE} = 4$ volts. $R_E = 2$ k Ω and $R_2 = 20$ k Ω .

We know that $\beta = \frac{\alpha}{1 - \alpha} = \frac{0.985}{1 - 0.985} = 66$

Now $I_B = \frac{I_C}{\beta} = \frac{2 \text{ mA}}{66} = 0.03 \text{ mA}$

Voltage across R_2 is given by

$$V_2 = V_{BE} + V_E = 0.3 + I_C \times R_E$$

or

$$V_2 = 0.3 + 2 \text{ mA} \times 2 \text{ k}\Omega = 0.3 + 4 = 4.3 \text{ volt}$$

Voltage across R_1 is given by

$$R_1 = V_{CC} - V_2 = 15 - 4.3 = 10.7 \text{ volt}$$

Current through R_1 and R_2 is given by

$$I_1 = \frac{V_2}{R_2} = \frac{4.3 \text{ V}}{20 \text{ k}\Omega} = 0.215 \text{ mA}$$

$$\therefore \text{Resistance } R_1 = \frac{\text{Voltage across } R_1}{I_1} \\ = \frac{10.7}{0.215 \text{ mA}} = 49.7 \text{ k}\Omega$$

$$\begin{aligned} V_L &= \text{Voltage across } R_L = V_{CC} - V_{CE} - V_E \\ &= 15 - 4 - R_E \times I_C \\ &= 15 - 4 - 2 \text{ k}\Omega \times 2 \text{ mA} \\ &= 15 - 4 - 4 = 7 \text{ V} \end{aligned}$$

$$\therefore R_L = \frac{\text{Voltage across } R_L}{I_C} = \frac{V_L}{I_C} \\ = \frac{7 \text{ V}}{2 \text{ mA}} = 3.5 \text{ k}\Omega$$

Example 6. In the CE amplifier of fig. (10.8), $I_E = 1$ mA, $R_E = 1000 \Omega$ and $\beta = 49$. Find the values of R_1 and R_2 such that the stability factor does not exceed 5. Assume $V_{CC} = 5$ volts and $V_{BE} = 0$.

We know that the stability factor S is given by

$$S = \frac{\beta + 1}{1 + \beta \left(\frac{R_E}{R_B + R_E} \right)}$$

Substituting the given values, we get

$$5 = \frac{49 + 1}{1 + 49 \left(\frac{1000}{R_B + 1000} \right)}$$

Solving we get $R_B = 4444 \Omega$

Further $R_B = \frac{R_1 R_2}{R_1 + R_2} = R_{Th}$

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...(1)

$$4444 = \frac{R_1 R_2}{R_1 + R_2}$$

Now, voltage drop across R_E is given by

$$V_E = I_E \times R_E = 1 \text{ mA} \times 1000 \Omega = 1 \text{ volt}$$

The voltage between base and ground is given by

$$\begin{aligned} V_{BG} &= V_{Th} = V_{BE} + V_E \\ &= 0 + 1 \text{ volt} = 1 \text{ volt} \end{aligned}$$

We know that

$$\begin{aligned} V_{Th} &= \left(\frac{R_2}{R_1 + R_2} \right) V_{CC} \\ 1 &= \left(\frac{R_2}{R_1 + R_2} \right) 5 \\ \frac{R_2}{R_1 + R_2} &= \frac{1}{5} \end{aligned} \quad \dots(2)$$

From eq. (2)

Substituting this value in eq. (1), we get

$$4444 = \frac{1}{5} \times R_1, \therefore R_1 = 4444 \times 5 = 22,220 \Omega$$

From eq. (2), $R_1 + R_2 = 5 R_2$ or $R_2 = R_1/4$

$$R_2 = \frac{22,220 \Omega}{4} = 5555 \Omega$$

Example 7. A common-emitter amplifier with self bias arrangement is shown in fig. (10.12). This employs an NPN transistor having $\beta = 99$. If this circuit is required to have a stability factor of 5, calculate the values of R_1 , R_2 and R_E , if the values of resistance R_L and various voltages are as shown in the figure.

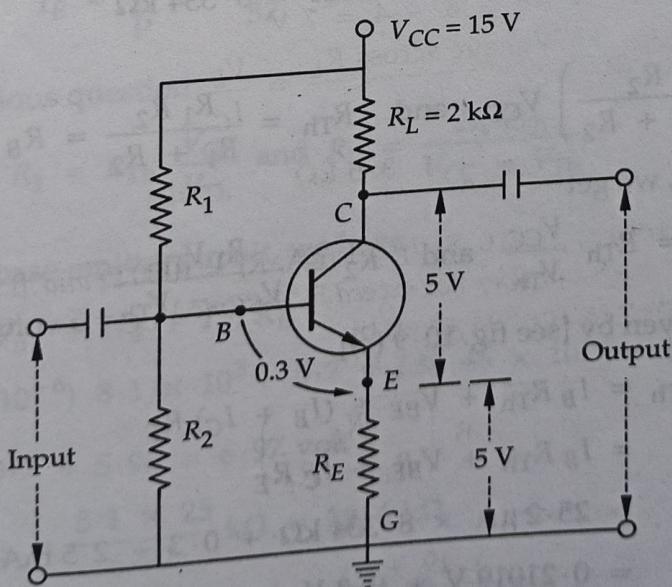


Fig. 10.12 CE amplifier with self bias arrangement

The collector potential with respect to ground G is given by

$$V_{CG} = V_{CE} + V_{EG}$$

$$V_{CG} = 5 + 5 = 10 \text{ V}$$

or

∴ Voltage drop across R_L is given by

$$V_L = V_{CC} - V_{GG} = 15 \text{ V} - 10 \text{ V} = 5 \text{ V}$$

$$\therefore \text{Collector current } I_C = \frac{V_L}{R_L}$$

$$\text{or } I_C = \frac{5 \text{ V}}{2 \text{ k}\Omega} = 2.5 \text{ mA}$$

The corresponding base current is given by

$$I_B = \frac{I_C}{\beta} = \frac{2.5 \text{ mA}}{99} = 25.2 \mu\text{A}$$

Since, this current is very small as compared to collector current I_C , hence, it may be assumed that the emitter current consists of collector current component only. Thus

$$R_E = \frac{V_E}{I_C} = \frac{5 \text{ V}}{2.5 \text{ mA}} = 2 \text{ k}\Omega$$

We know that

$$S = \frac{1 + \beta}{1 + \beta \left(\frac{R_E}{R_B + R_E} \right)} = (1 + \beta) \frac{(R_B/R_E) + 1}{(R_B/R_E) + 1 + \beta}$$

$$\therefore \frac{R_B}{R_E} = \frac{(1 + \beta)(S - 1)}{(1 + \beta - S)} = \frac{(1 + 99)(5 - 1)}{(1 + 99 - 5)}$$

$$\text{or } \frac{R_B}{R_E} = \frac{400}{95} = 4.167$$

$$\text{or } R_B = 4.167 \times R_E = 4.167 \times 2 \text{ k}\Omega = 8.334 \text{ k}\Omega$$

We know that

$$V_{Th} = \left(\frac{R_2}{R_1 + R_2} \right) V_{CC} \quad \text{and} \quad R_{Th} = \frac{R_1 R_2}{R_1 + R_2} = R_B$$

Solving for R_1 and R_2 , we get

$$R_1 = R_{Th} \frac{V_{CC}}{V_{Th}} \quad \text{and} \quad R_2 = \frac{R_1 V_{Th}}{V_{CC} - V_{Th}}$$

The value of V_{Th} is given by [see fig. 10.9 (c)]

$$\begin{aligned} V_{Th} &= I_B R_{Th} + V_{BE} + (I_B + I_C) R_E \\ &= I_B R_{Th} + V_{BE} + I_C R_E \quad (\text{negricting } I_B) \\ &= 25.2 \mu\text{A} \times 8.334 \text{ k}\Omega + 0.3 + 2.5 \text{ mA} \times 2 \text{ k}\Omega \\ &= 0.21019 \text{ V} + 0.3 \text{ V} + 5 \text{ V} \approx 5.5 \text{ V} \end{aligned}$$

$$\therefore R_1 = \frac{8.334 \times 15}{5.5} = 22.7 \text{ k}\Omega$$

$$R_2 = \frac{22.7 \times 5.5}{15 - 5.5} = 13.1 \text{ k}\Omega$$

Example 8 A silicon transistor having $\beta = 52$ and $V_{BE} = 0.7$ V is used in the circuit of fig. (10-8). $V_{CC} = 25$ V and $R_L = 5 \text{ k}\Omega$. The operating point is required to be established at $V_{CE} = 10$ volt and $I_C = 2 \text{ mA}$ and with stability factor S not exceeding 4. Find the values of R_1 , R_2 and R_E .

Considering the collector circuit, we have

$$V_{CC} - V_{CE} = I_C (R_L + R_E) \quad (\because I_C + I_B \approx I_C)$$

$$25 - 10 = 2 \text{ mA} (R_L + R_E)$$

$$R_L + R_E = \frac{15 \text{ V}}{2 \text{ mA}} = 7.5 \text{ k}\Omega$$

$$R_E = (7.5 \text{ k}\Omega - R_L) = 7.5 \text{ k}\Omega - 5 \text{ k}\Omega = 2.5 \text{ k}\Omega$$

or
We know that stability factor S is given by

$$S = (1 + \beta) \frac{(R_B/R_E) + 1}{(R_B/R_E) + 1 + \beta}$$

The maximum permitted value of S is 4, so

$$4 = (1 + 52) \frac{(R_B/R_E) + 1}{(R_B/R_E) + 1 + 52}$$

Solving we get $\frac{R_B}{R_E} = \frac{159}{49}$ or $R_B = R_E \times \frac{159}{49}$

$$R_B = 2.5 \text{ k}\Omega \times \frac{159}{49} = 8.1 \text{ k}\Omega = R_{Th}$$

The value of base current I_B is given by

$$I_B \approx \frac{I_C}{\beta} = \frac{2 \text{ mA}}{52} = 38.46 \mu\text{A}$$

As did in the previous question

$$R_1 = R_{Th} \frac{V_{CC}}{V_{Th}} \text{ and } R_2 = \frac{R_1 V_{Th}}{V_{CC} - V_{Th}}$$

Applying KVL to base-emitter circuit, we have

$$\begin{aligned} V_{Th} &= I_B R_B + V_{BE} + (I_B + I_C) R_E \\ &= (38.46 \times 10^{-6}) 8.1 \times 10^3 + 0.7 + (38.46 \times 10^{-6} + 2 \times 10^{-3}) 2.5 \times 10^3 \\ &= 0.312 + 0.7 + 5.96 = 6.97 \text{ volt} \end{aligned}$$

$$R_1 = \frac{8.1 \times 25}{6.97} \text{ k}\Omega = 29.4 \text{ k}\Omega$$

$$\text{and } R_2 = \frac{29.4 \times 6.97}{25 - 6.97} = \frac{204.92}{18.03} = 11.3 \text{ k}\Omega$$

Example 9. Determine quiescent currents and collector to emitter voltage for a silicon PNP transistor with $\beta = 50$. The circuit components in self biasing arrangements are $V_{CC} = -20$ V, $R_L = 2 \text{ k}\Omega$, $R_E = 0.1 \text{ k}\Omega$, $R_1 = 100 \text{ k}\Omega$ and $R_2 = 5 \text{ k}\Omega$ (See fig. (10-13)) Find also stability factor.

Let us consider the Thevenin's equivalent circuit. Here

$$V_{Th} = - \left(\frac{V_{CC}}{R_1 + R_2} \right) \times R_2$$

$$\text{or } V_{Th} = - \left(\frac{20}{100 + 5} \right) \times 5 = - 0.952 \text{ volt}$$

$$\text{and } R_{Th} = \left(\frac{R_1 R_2}{R_1 + R_2} \right) = \frac{100 \times 5}{100 + 5} = 4.76 \text{ k}\Omega$$

The Thevenin's equivalent circuit is shown in fig. (10.14). Applying KVL to input side, we have

$$\begin{aligned} -R_E I_E - V_{BE} - I_B R_{Th} + V_{Th} &= 0 \\ -R_E I_B (1 + \beta) - V_{BE} - I_B R_{Th} + V_{Th} &= 0 \\ -0.1 I_B (1 + 50) - 0.7 - I_B \times 4.76 + 0.952 &= 0 \end{aligned}$$

Solving we get

$$I_B = 0.0256 \text{ mA}$$

$$I_C = \beta I_B = 50 \times 0.0256 = 1.28 \text{ mA}$$

$$\begin{aligned} \text{and } I_E &= I_B (1 + \beta) = 0.0256 \times 51 \\ &= 1.3056 \text{ mA} \end{aligned}$$

Applying KVL to output side

$$\begin{aligned} -I_E R_E - V_{CE} - I_C R_L + V_{CC} &= 0 \\ -1.3056 \times 0.1 - V_{CE} - 1.28 \times 2 + 20 &= 0 \end{aligned}$$

$$\text{or } V_{CE} = 17.31 \text{ volt}$$

So, the operating point is (1.28 mA, 17.31 V)

$$\begin{aligned} \text{Further } S &= \frac{(1 + \beta)(1 + R_B/R_E)}{1 + \beta + (R_B/R_E)} \\ &= \frac{(1 + 50)(1 + 4.76/0.1)}{1 + 50 + (4.76/0.1)} = 25.13 \end{aligned}$$

Example 10. Design selfbias circuit for C.E. amplifier having $\beta = 99$ and $S = 5$. The other values are $V_{CE} = 6 \text{ V}$, $V_{RE} = 5.5 \text{ V}$, $V_{CC} = 15 \text{ V}$, $R_C = 2.5 \text{ k}\Omega$ and $V_{BE} = 0.3 \text{ V}$.

See fig. (10.15).

Applying KVL to output circuit

$$V_{CC} - I_C R_L - V_{CE} - I_E R_E = 0$$

$$\therefore I_C R_L = V_{CC} - V_{CE} - I_E R_E$$

$$\text{or } I_C = \frac{V_{CC} - V_{CE} - I_E R_E}{R_L}$$

$$\text{or } I_C = \frac{15 - 6 - 5.5}{2.5} = 1.4 \text{ mA}$$

$$\text{Now } I_B = \frac{I_C}{\beta} = \frac{1.4}{99} = 14 \mu\text{A}$$

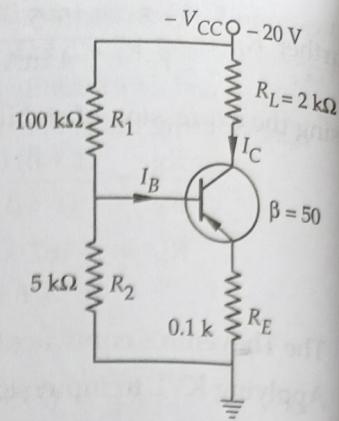


Fig. 10.13

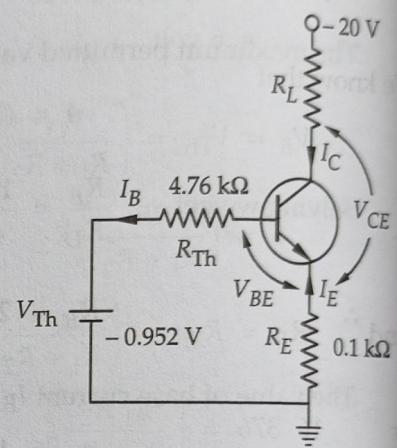


Fig. 10.14

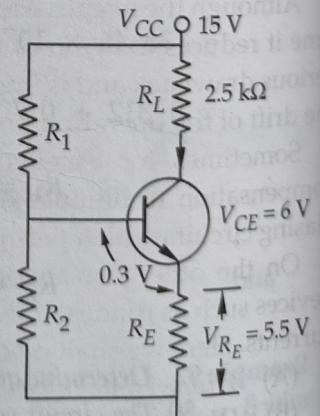


Fig. 10.15

$$\text{Further } R_E = \frac{5.5}{I_E} \approx \frac{5.5}{1.4 \text{ mA}} = 3.93 \text{ k}\Omega$$

Using the expression of stability, we have

$$\frac{R_B}{R_E} = \frac{(1 + \beta)(S - 1)}{(1 + \beta - S)} = \frac{(1 + 99)(5 - 1)}{(1 + 99 - 5)} = \frac{400}{95} = 4.167$$

$$R_B = 4.167 \times R_E = 4.167 \times 3.93 = 16.376 \text{ k}\Omega.$$

The Thevenin's equivalent circuit is shown in fig. (10-16).

Applying KVL to input side, we have

$$V_B - I_B R_B - V_{BE} - I_E R_E = 0$$

$$\begin{aligned} \text{or } V_B &= I_B R_B + V_{BE} + I_E R_E \\ &= 0.014 \text{ mA} \times 16.376 \text{ k}\Omega + 0.3 + 5 \text{ V} \\ &= 6 \text{ volt} \end{aligned}$$

We know that

$$V_B = V_{Th} = \left(\frac{V_{CC}}{R_1 + R_2} \right) R_2$$

$$\text{or } 6 = \left(\frac{15}{R_1 + R_2} \right) R_2 \quad \dots(a)$$

$$\text{And } R_B = R_{Th} = \left(\frac{R_1 R_2}{R_1 + R_2} \right)$$

$$\text{or } 16.376 = \left(\frac{R_1 R_2}{R_1 + R_2} \right) \quad \dots(b)$$

Solving eqs. (a) and (b), we get

$$R_1 = 40.94 \text{ k}\Omega \text{ and } R_2 = 27.29 \text{ k}\Omega.$$

10-9 BIAS COMPENSATION

So far we have studied the various biasing methods and operating point stability provided by them. We have seen that self bias circuit provides better operating point stability than a fixed bias circuit. In both arrangements the stabilization action occurs due to the negative feedback action offered by the circuit.

Although the negative feedback improves the stability of the operating point but at the same time it reduces the gain of the amplifier. In certain applications, the loss in the gain becomes serious drawback and is intolerable. In such cases, compensation techniques are used to reduce the drift of the operating point.

Sometimes for excellent bias and thermal stabilization, both stabilization as well as compensation techniques are used. The stabilization techniques refer to the use of resistive biasing circuits which permit I_B to vary so as to keep I_C relatively constant.

On the other hand, compensation techniques refer to the use of temperature-sensitive devices such as diodes, transistors, thermistors, sensistor etc to compensate for the variation in currents. Here we shall discuss the following compensation techniques :

- (A) Diode compensation for instability due to V_{BE} variation.
- (B) Diode compensation for instability due to I_{CO} variation.
- (C) Thermistor compensation.
- (D) Sensistor compensation.

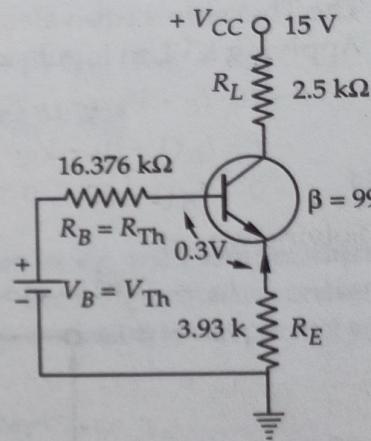
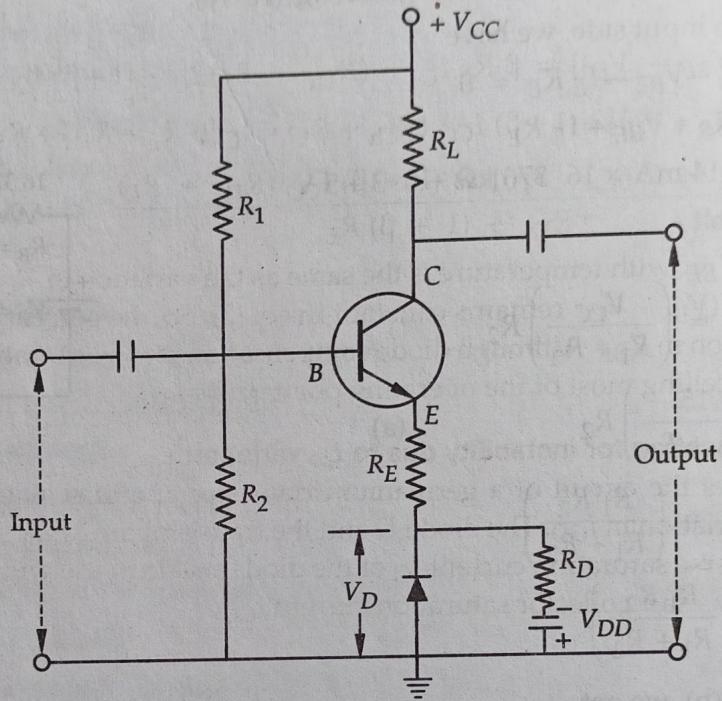


Fig. 10-16

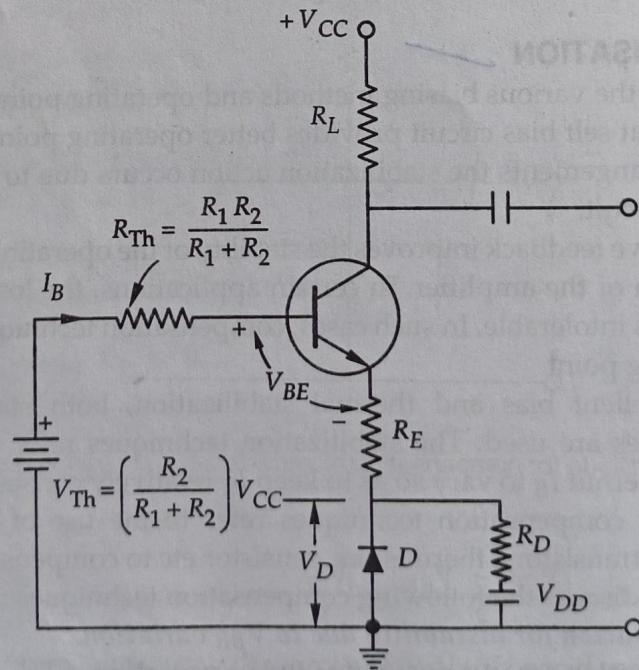
... (b)

(A) Diode compensation for instability due to V_{BE} variation

For germanium transistor, changes in I_{CO} with temperature contribute more serious problem than for silicon transistor. On the other hand, in a silicon transistor, the changes of V_{BE} with temperature possesses significantly to the changes in I_C . A diode may be used as compensation element for variation in V_{BE} or I_{CO} . Figure [10.17 (a)] shows the circuit of self bias stabilization technique with a diode compensation for V_{BE} . The Thevenin's equivalent circuit is shown in fig. [10.17 (b)]. The diode D used here is of the same material and type as the transistor. Hence, the voltage V_D across the diode has same temperature coefficient (-2.5 mV/deg. C) as V_{BE} of the transistor. The diode D is forward-biased by the source V_{DD} and resistor R_D .



(a) Self-bias with stabilization and compensation



(b) Thevenin's equivalent circuit

Fig. 10.17

Transistor Biasing and Thermal Stabilization

Applying Kirchhoff's voltage law to the base circuit of fig. [10.17 (b)], we get

$$V_{Th} - V_{BE} + V_D = I_B R_{Th} + R_E (I_B + I_C) \quad \dots(1)$$

$$I_C = \beta I_B + (1 + \beta) I_{CO} \quad \dots(2)$$

But
From eq. (1), we have

$$V_{Th} - V_{BE} + V_D = R_E I_C + (R_{Th} + R_E) I_B$$

Substituting the value of I_B from eq. (2), we get

$$V_{Th} - V_{BE} + V_D = R_E I_C + (R_{Th} + R_E) \left[\frac{I_C - (1 + \beta) I_{CO}}{\beta} \right]$$

$$\text{or } \beta [V_{Th} - (V_{BE} - V_D)] = \beta R_E I_C + (R_{Th} + R_E) I_C - (1 + \beta) I_{CO} (R_{Th} + R_E)$$

$$\text{or } \beta [V_{Th} - (V_{BE} - V_D)] + (1 + \beta) I_{CO} (R_{Th} + R_E) = I_C [\beta R_E + R_{Th} + R_E]$$

$$\therefore I_C = \frac{\beta [V_{Th} - (V_{BE} - V_D)] + (1 + \beta) I_{CO} (R_{Th} + R_E)}{R_{Th} + (1 + \beta) R_E} \quad \dots(3)$$

Since variation in V_{BE} with temperature is the same as the variation in V_D with temperature, hence the quantity $(V_{BE} - V_D)$ remains constant in eq. (3). So, the current I_C remains constant despite of the variation in V_{BE} . Although diode compensation for V_{BE} variation is not perfect yet it is effective in cancelling most of the operating point drift.

B) Diode Compensation for instability due to I_{CO} variation

Figure (10.18) shows the circuit of a germanium transistor amplifier with diode D used for compensation of variation in I_{CO} . The diode D and the transistor are of the same type and same material. So the reverse saturation current I_O of the diode will increase with temperature at the same rate as the transistor collector saturation current I_{CO} .

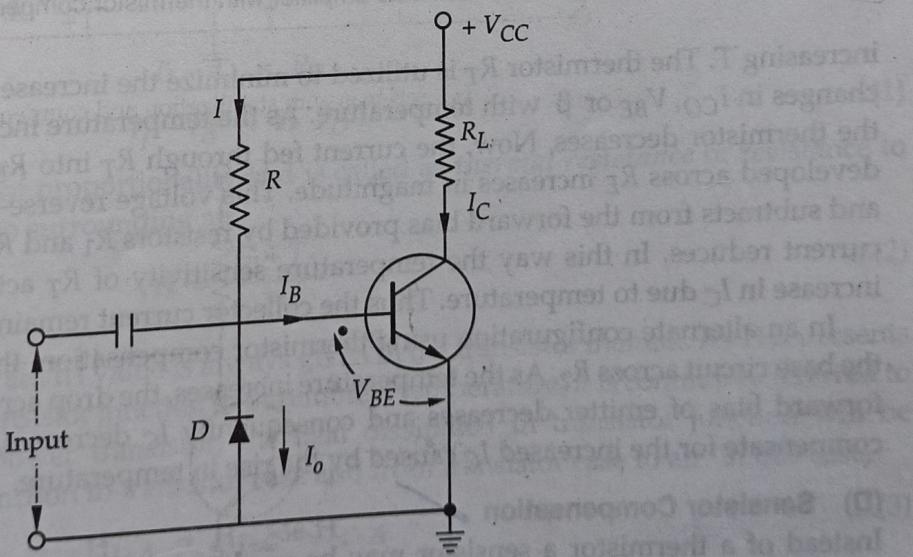


Fig. 10.18 Diode for compensation of variation in I_{CO} in germanium transistor

From fig. (10.18)

$$I = \frac{V_{CC} - V_{BE}}{R} \approx \frac{V_{CC}}{R} = \text{Constant} \quad \dots(4)$$

The diode D is reverse biased by V_{BE} . We know that in case of germanium transistor V_{BE} is 0.3 volt. So, the current through D is the reverse saturation current I_O .

$$\dots(5)$$

Now base current $I_B = I - I_O$

Substituting the value of I_B from eq. (5) in eq. (2), we get

$$I_C = \beta(I - I_O) + (1 + \beta)I_{CO}$$

If $\beta \gg 1$,

$$I_C \approx \beta I - \beta I_O + \beta I_{CO}$$

In expression (6), I is almost constant and if I_O of diode D and I_{CO} of transistor track each other over the operating temperature range, then I_C remains constant.

(C) Thermistor Compensation

Figure (10.19) shows the self-bias CE amplifier with thermistor R_T . The thermistor has negative temperature coefficient of resistance, i.e., its resistance decreases exponentially with increasing temperature.

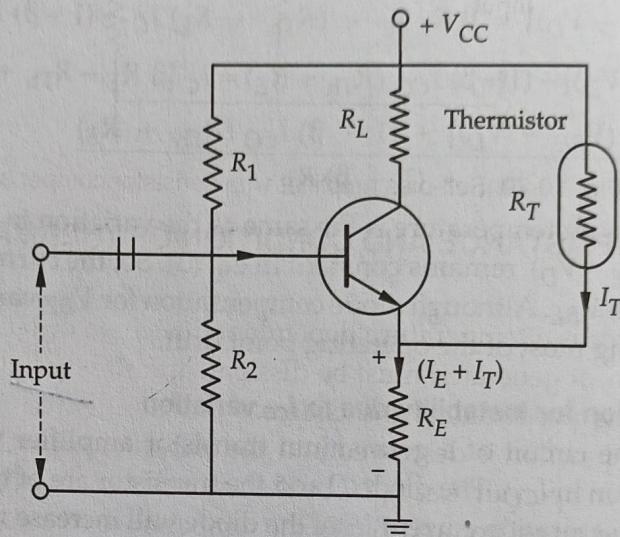


Fig. 10.19 Self-bias amplifier with thermistor compensation

increasing T . The thermistor R_T is utilized to minimize the increase in collector current due to changes in I_{CO} , V_{BE} or β with temperature. As the temperature increases, the resistance of the thermistor decreases. Now, the current fed through R_T into R_E increases. So, the voltage developed across R_E increases in magnitude. This voltage reverse-biases the emitter junction and subtracts from the forward bias provided by resistors R_1 and R_2 . As a result, the collector current reduces. In this way the temperature sensitivity of R_T acts so as to compensate the increase in I_C due to temperature. Thus the collector current remains fairly constant.

In an alternate configuration using thermistor compensation, thermistor may be placed in the base circuit across R_2 . As the temperature increases, the drop across R_T decreases. So the forward bias of emitter decreases and consequently I_C decreases. This reduced I_C tends to compensate for the increased I_C caused by the rise in temperature.

(D) Sensistor Compensation

Instead of a thermistor a sensistor may be used for operating point stability. Sensistor is a temperature sensitive resistor having positive temperature coefficient of resistance like a metal. It is a heavily doped semiconductor. The sensistor may be used either in parallel with R_E [as shown in fig. 10.20] or in parallel with (or in place of) R_E . As the temperature increases, the resistance of the sensistor increases. Thus the resistance of the parallel combination ($R_1 \parallel R_E$) increases. Now the voltage drop across R_2 decreases. Due to the decrease of this voltage, the forward emitter bias decreases. As a result I_C decreases. This reduced I_C compensates for the increased I_C caused by the increase in I_{CO} , V_{BE} or β due to temperature.

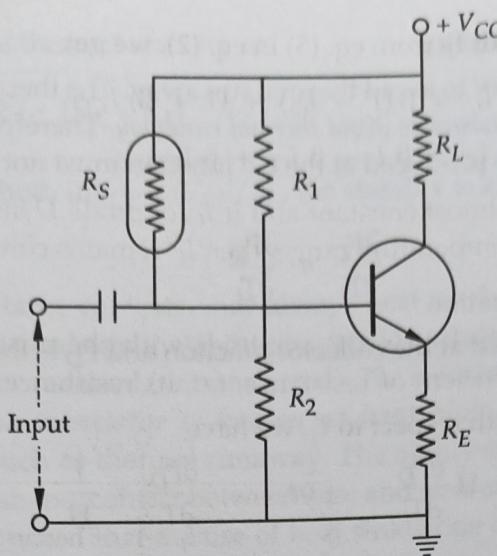


Fig. 10.20 Self-bias amplifier with transistor compensation

10.10 THERMAL RESISTANCE AND CONDITION OF THERMAL STABILITY

Thermal resistance

We know that transistor is a temperature dependent device. In order to keep the temperature within the limits, the heat generated must be dissipated to the surroundings. Most of the heat within the transistor is produced at the collector junction. If the temperature exceeds the permissible limit, this junction is destroyed and the transistor is rendered useless. Consider a transistor is operating in open air. Let T_A °C be the ambient temperature i.e., the temperature of surrounding air around transistor and T_J °C, the temperature of collector-base junction of the transistor. As $T_J > T_A$ i.e., difference $T_J - T_A$ is greater, the power dissipated in the transistor P_D will be greater. Thus

$$T_J - T_A \propto P_D \quad \dots(1)$$

$$T_J - T_A = H P_D$$

where H is the constant of proportionality and is called as *thermal resistance* or resistance to heat flow from junction to surrounding air.

$$H = \frac{T_J - T_A}{P_D} \quad \dots(2)$$

The unit of H is °C/watt. Its value is always given in the transistor manual. As H represents total resistance from a transistor junction to the ambient temperature, it is commonly referred to as H_{J-A} . However in power transistor, the heat dissipated in transistor junction will be conducted away from junction to transistor case and from transistor case to air. In this case,

$$H_{J-A} = H_{J-C} + H_{C-A} \quad \dots(3)$$

$$P_D = \frac{T_J - T_A}{H_{J-C} + H_{C-A}} \quad \dots(4)$$

Here, H_{C-A} is determined by surface area of the case and its contact with air. If the effective surface area of the transistor case could be increased, the resistance to heat flow (H_{C-A}) could be decreased. We know that a low thermal resistance means that it is easy for heat to flow from junction to surrounding air. So, larger is the transistor case, the lower is the thermal resistance and vice versa. This can be achieved by the use of heat sink.

Condition for thermal stability

For a transistor, it is necessary to avoid thermal run away. The thermal stability of a transistor is defined as the ability of a transistor to avoid thermal runaway. Therefore, the required condition is that the rate at which heat is produced at the CB junction must not exceed the rate at which the heat can be dissipated i.e.,

$$\frac{\partial P_C}{\partial T_j} < \frac{\partial P_D}{\partial T_j} \quad \dots(5)$$

where P_C is the heat produced at the collector junction and P_D is the heat dissipated at collector junction.

Differentiating eq. (1) with respect to T_j , we have

$$1 = H \frac{\partial P_D}{\partial T_j} \quad \text{or} \quad \frac{\partial P_D}{\partial T_j} = \frac{1}{H} \quad \dots(6)$$

From eqs. (5) and (6), we get the following condition that must be satisfied to prevent thermal runaway:

$$\frac{\partial P_C}{\partial T_j} < \frac{1}{H} \quad \dots(7)$$

Let us consider a more practical expression of thermal stability by considering a potential divider method as shown in fig. (10.21). Here, we express the left hand side of eq. (1) as

$$\frac{\partial P_C}{\partial T_j} = \frac{\partial P_C}{\partial I_C} \times \frac{\partial I_C}{\partial T_j} \quad \dots(8)$$

Considering the self-bias circuit, the value of P_C (heat produced at collector-base junction) is given by

$$P_C = V_{CC} I_C - I_C^2 R_L - I_E^2 R_E$$

$$\text{or} \quad P_C = V_{CC} I_C - I_C^2 [R_L + R_E] \quad (\because I_E \approx I_C)$$

Here, $V_{CC} I_C$ is the power taken from supply source.

$$\therefore \frac{\partial P_C}{\partial I_C} = V_{CC} - 2 I_C [R_L + R_E] \quad \dots(9)$$

We know that, $S = \frac{\partial I_C}{\partial I_{Co}} = \frac{\partial I_C}{\partial T_j} \times \frac{\partial T_j}{\partial I_{Co}}$

$$\text{or} \quad \frac{\partial I_C}{\partial T_j} = S \times \frac{\partial I_{Co}}{\partial T_j} \quad \dots(10)$$

Substituting the values of $(\partial P_C / \partial I_C)$ and $(\partial I_C / \partial T_j)$ from eq. (9) and eq. (10) in eq. (8), we get

$$\frac{\partial P_C}{\partial T_j} = V_{CC} - 2 I_C [R_L + R_E] \times S \left(\frac{\partial I_{Co}}{\partial T_j} \right) \quad \dots(11)$$

$$\text{or} \quad \frac{\partial P_C}{\partial T_j} = V_{CC} - 2 I_C [R_L + R_E] \times S \times (0.07 I_{Co})$$

$$\left(\because \frac{\partial I_{Co}}{\partial T_j} = 0.07 I_{Co} \right)$$

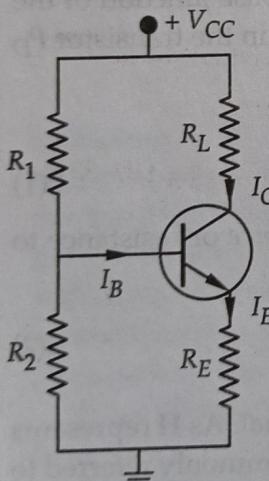


Fig. 10.21

Therefore, the condition of thermal stability is

$$V_{CC} - 2 I_C [R_L + R_E] \times S \times (0.07 I_{Co}) < \frac{1}{H} \quad \dots(12)$$

In a potential divider method, if $V_{CE} < (V_{CC}/2)$, the stability is automatically ensured.

10.11 HEAT SINK

As power transistors handle large currents, they always heat up during operation. Generally, power transistors are mounted in large metal case to provide a large area from which the heat generated by the device may be radiated (or transferred). The metal sheet that helps to dissipate the additional heat from the transistor is known as heat sink. The heat sink avoids the undesirable thermal effects such as thermal runaway. The ability of heat sink depends on the material used, volume, area, shape, contact between case and sink and movement of air around the sink. It should be further noted that the use of heat sink alone can not be sufficient to stop thermal runaway under all conditions. The consideration should also be given to the selection of (i) operating point, (ii) ambient temperature and (iii) type of transistor used.

The variation of maximum collector dissipation with case temperature is an important characteristic supplied by transistors manufacturers. A typical curve is shown in fig. (10.22). It is clear from fig. (10.22) that the transistor can dissipate safely the rated maximum power (P_D)_{max} below temperature (T_A)₀. However, the maximum allowable power dissipation decreases with increasing value of temperature higher than that of (T_A)₀ as indicated in fig. (10.22). The phenomenon is called derating of power curve.

A typical physical connection of transistor with heat sink is shown in fig. (10.23).

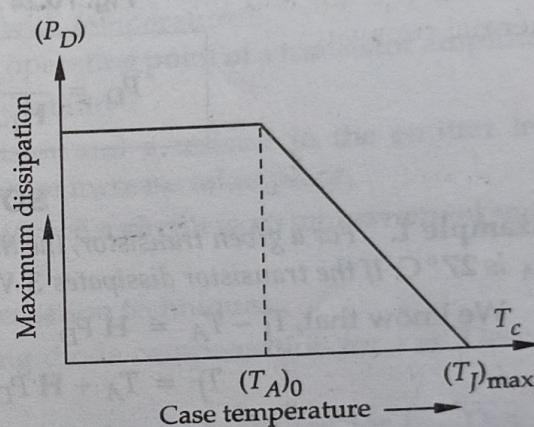


Fig. 10.22

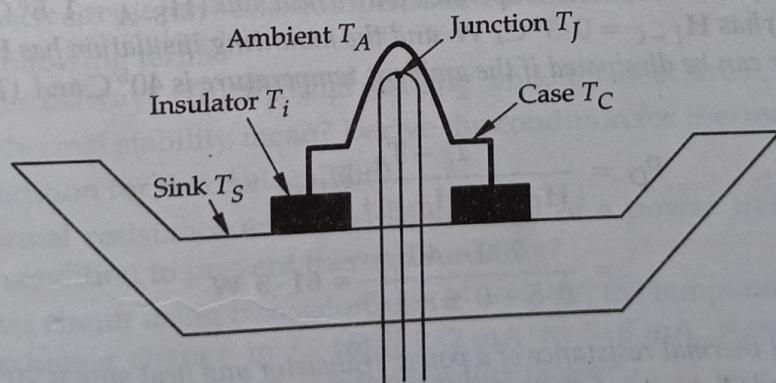


Fig. 10.23 Transistor with heat sink

We have already mentioned that

$$H_{J-A} = H_{J-C} + H_{C-A} \quad \dots(5)$$

where, H_{J-C} is thermal resistance between junction and case and H_{C-A} is thermal resistance between case and ambient. The circuit designer has no control over H_{J-C} . So, a proper approach to dissipate heat from case to ambient is through heat sink. Hence, thermal resistance H_{C-A} is broken into two parts as:

$$H_{C-A} = H_{C-S} + H_{S-A} \quad \dots(6)$$

So, including heat sink, we have

$$H_{J-A} = H_{J-C} + H_{C-S} + H_{S-A} \quad \dots(7)$$

Figure (10.24) shows the electrical circuit of heat sink. A heat sink can now be seen to provide a low thermal resistance between case and air. Therefore

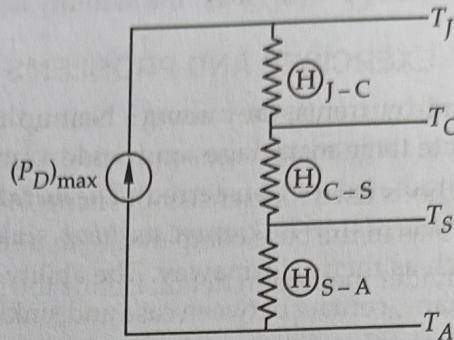


Fig. 10.24 Electrical circuit of heat sink

$$P_D = \frac{T_J - T_A}{H_{J-C} + H_{C-S} + H_{S-A}} \quad \dots(8)$$

SOLVED EXAMPLES

Example 1. For a given transistor, the thermal resistance is $8^\circ\text{C}/\text{W}$ and for the ambient temperature T_A is 27°C . If the transistor dissipates 3 W of power, calculate the junction temperature T_J .

We know that, $T_J - T_A = H P_D$

$$\begin{aligned} \therefore T_J &= T_A + H P_D \\ &= 27^\circ\text{C} + (8^\circ\text{C}/\text{W}) (3\text{ W}) \\ &= 27^\circ\text{C} + 24^\circ\text{C} = 51^\circ\text{C} \end{aligned}$$

Example 2. A silicon power transistor is operated with a heat sink ($H_{S-A} = 1.5^\circ\text{C}/\text{W}$). The transistor rated at 150 W (25°C) has $H_{J-C} = 0.5^\circ\text{C}/\text{W}$ and the mounting insulation has $H_{C-S} = 0.6^\circ\text{C}/\text{W}$. What maximum power can be dissipated if the ambient temperature is 40°C and $(T_J)_{\text{max}} = 200^\circ\text{C}$?

We know that

$$\begin{aligned} P_D &= \frac{T_J - T_A}{H_{J-C} + H_{C-S} + H_{S-A}} \\ &= \frac{200 - 40}{0.5 + 0.6 + 1.5} \approx 61.5 \text{ W} \end{aligned}$$

Example 3. The total thermal resistance of a power transistor and heat sink is $20^\circ\text{C}/\text{W}$. The ambient temperature is 25°C and $(T_J)_{\text{max}} = 200^\circ\text{C}$. If $V_{CE} = 4\text{ V}$, find the maximum collector current that the transistor can carry without destruction. What will be the allowed value of collector current if ambient temperature rises to 75°C ?

We know that, $P_D = \frac{T_J - T_A}{H}$

$$\therefore P_D = \frac{200 - 25}{20} = 8.75 \text{ W}$$

Now

$$V_{CE} I_C = 8.75 \text{ or } I_C = 8.75/4 = 2.19 \text{ A}$$

When temperature rises to 75°C , we have

$$P_D = \frac{T_J - T_A}{H} = \frac{200 - 75}{20} = 6.25 \text{ W}$$

$$I_C = 6.25/4 = 1.56 \text{ A}$$

EXERCISES AND PROBLEMS

What do you understand by transistor biasing? Name the different types of transistor biasing and state their advantages and disadvantages. What is meant by self-biasing in transistor biasing. What is meant by collector feedback biasing?