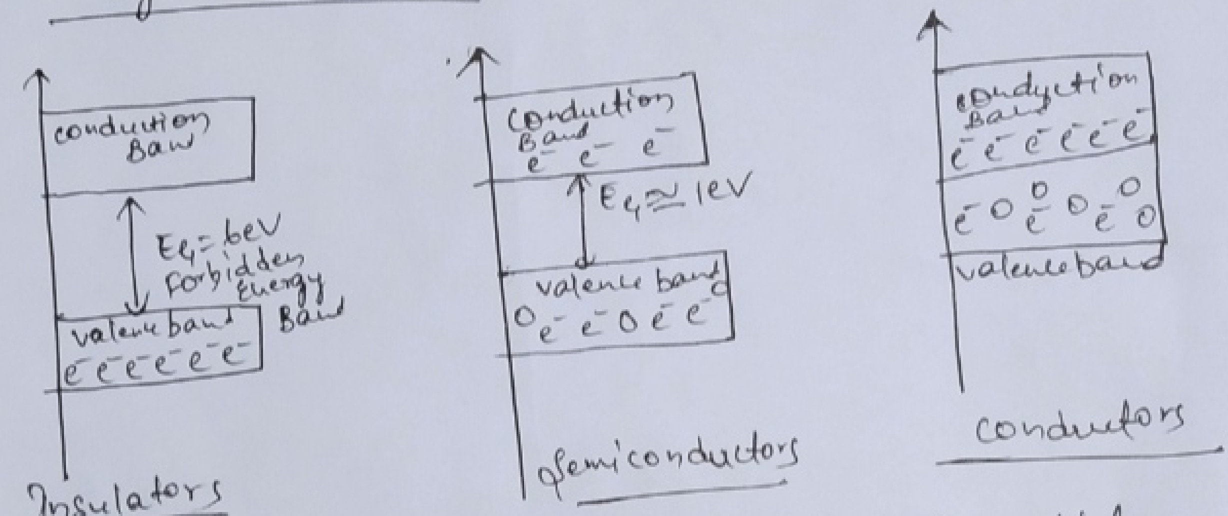
ELECTRONIC DEVICES UNIT-I SUMMARY

Introduction to Semiconductor physics

Energy Band Theory



$e^- \rightarrow$ Electrons - Negatively charged particle

$o \rightarrow$ Hole - Positively charged particle.

Valence Band: the outermost orbital that the Electrons occupy in an atom is known as valence Band.

Forbidden Band: the Energy gap between the conduction band and valence band is known as Forbidden Band

conduction Band: the delocalized band in a material that is partially filled with electrons is known as conduction band. These are highly mobile and responsible for electrical conductivity.

Semiconductors :-

The materials which have conductivity between conductors (metals) and insulators (ceramics)

Eg: Si, Ge, In, Ga etc.

As thermal Energy increases, the conductivity increases in case of Semiconductors.

EFFECTIVE MASS :

$$E = \frac{p^2}{2m}$$

E → Kinetic Energy of free Electron
p → momentum, v - velocity, m - mass

$p = mv$

$$K \cdot E = \frac{1}{2} m v^2 \Rightarrow \frac{1}{2m} m^2 \cdot v^2 \Rightarrow \frac{1}{2m} (mv)^2$$

$$= \frac{p^2}{2m}$$

m^* = Effective mass.

Insulator :- Insulator is a poor conductor of Electricity.

Resistivity ⇒ $\rho > 10^9 \Omega$-cm.

Free Electron concentration, $n \simeq 10^7$ Electrons/m³

$E_g >> 1eV$

Metal :- Metal is a Excellent conductor of Electricity

$\rho < 10^{-3} \Omega$-cm

Free Electron concentration, $n = 10^{28}$ Electrons/m³

$E_g = 0eV$.

Advantages of semiconductor devices :-

- Smaller in size
- Requires no cathode heating power (warm up time)
- operate on low DC power
- very long life.

Dis Advantages.

- Frequency range of operation is low.
- Smaller power output
- Low permissible temperature
- more noise

IONIC BOND :- complete transfer of valence Electrons between two atoms.. It is a type of chemical bond that produces two oppositely charged ions.

Covalent Bond :- The bond in which sharing of electrons takes place is known as covalent bond.

Types of semiconductors

- Intrinsic
- Extrinsic

Intrinsic semiconductor :-

~~[the semiconductor in which (privalent impurities are dop.)]~~

The semiconductor in its pure form is known as Intrinsic semiconductor.

In Intrinsic semiconductor $n_p = p$ (i.e) $(n = p = n_i)$
(i.e) no. of holes = no. of electrons.

conductivity

$$\sigma = (n\mu_n + p\mu_p)e = ne\mu_n + pe\mu_p$$

μ = mobility

n = Magnitude of Free Electron concentration.

p = magnitude of Hole concentration

current density (J) $= \sigma E = (n\mu_n + p\mu_p) \times e \times E$
$= \sigma \times E$

$$\boxed{n_i = A \times T^{3/2} e^{-E_{G0}/2KT}}$$

E_G = forbidden Energy gap

A = constant for semiconductor

T = Temp in K & K = Boltzmann const

Extrinsic semi conductor:

The semiconductor in its impure form is known as Extrinsic semi conductor.

Doping:- The process of inducing impurities into a material is termed as doping.

There are two types of Extrinsic semi conductor they are:-

(i) P-type semiconductor

(ii) N-type semiconductor.

P-TYPE SEMICONDUCTOR :-

-) An intrinsic semiconductor when doped with trivalent (3) impurity atoms like Boron, Gallium, Indium (or) Aluminium etc becomes p-type or Acceptor type

-) Because of the Energy supplied while doping, the impurity atom dislodges one Ge atom from the crystal lattice.

-) the doping level is low, (ie) there is one impurity atom for one million Ge atoms, the impurity atom is surrounded by Ge atom.

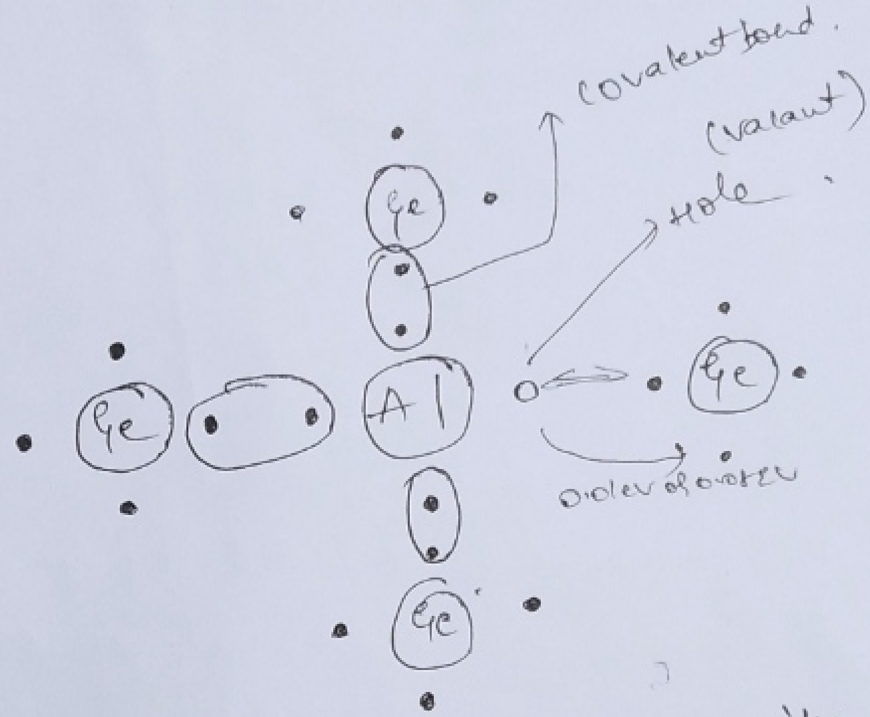
-) Now the three valence Electrons of impurity atom are shared by 3 Ge atoms. the fourth Ge atom has no Electron to share with the impurity atom, the covalent bond is not filled or a hole Exists.

-) The impurity atom tries to steal one Electron from the neighbouring Ge atoms and it does when sufficient Energy is supplied to it.

-) So hole moves, there will be a natural tendency in the crystal to form 4 covalent bonds.

-) The impurity atom since all the other Germanium atoms have four covalent bonds and the structure of Ge semiconductor is crystalline and symmetrical

-) The Energy required for the impurity atom to steal one Ge Electron is 0.01eV to 0.08eV. This hole is in excess to the hole created by thermal agitation.



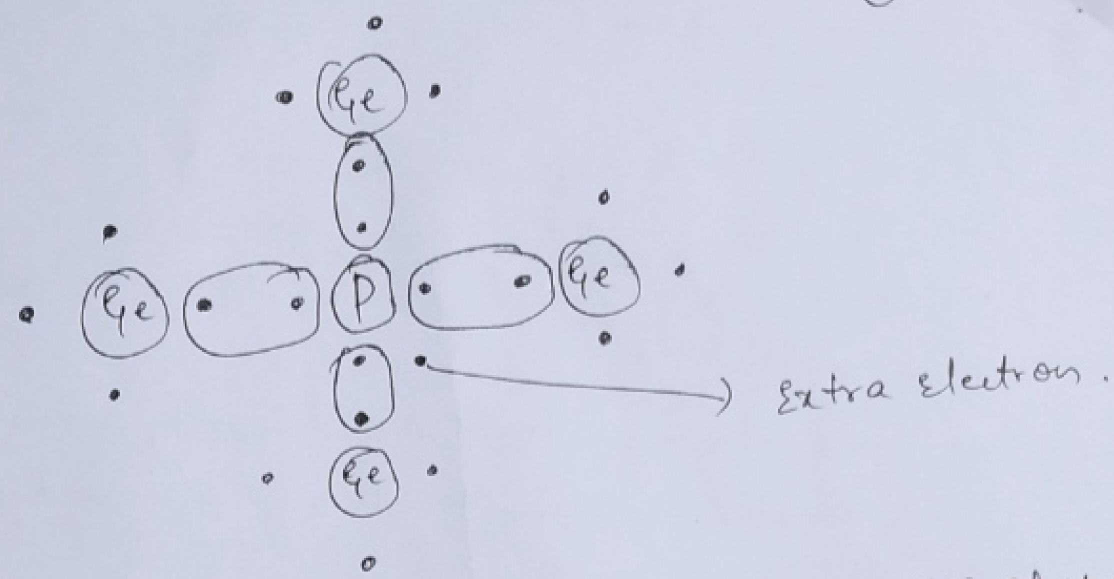
In P-type semiconductor $p >> n_i$ (ie) Majority charge carriers are holes & minority are Electrons

(ii) N-type semiconductor:-

-) Intrinsic semiconductor in which pentavalent impurities are doped is known as N-type semiconductor.

-) Ge is tetravalent (4), it becomes n-type when pentavalent impurity atoms such as Phosphorus (P), or Arsenic are added to it.

- The impurity atoms have size of the same order of that of Ge atoms
- Because of the Energy supplied while doping, the impurity atom dislodges one from its normal position in the crystal lattices takes up that position.
- But since the concentration of impurity atoms is very small, the impurity atom is surrounded by Ge atoms.
- The impurity atom is pentavalent. That is, it has 5 Electrons in its outermost orbital.
- Now four of these are shared by Ge atoms, surrounding the impurity atom and they form covalent bonds.
- So one Electron of the impurity atom is left free. The Energy required to dislodge this fifth Electron from its parent impurity atom is very little of the order of 0.01eV to 0.05eV
- This free Electron in excess to the free Electron that will be generated because of breaking of covalent bonds due to thermal agitation.
- Since an Excess Electron is available for Each impurity atom, or it can donate an Electron it is called n-type or donor-type semiconductor.



In n-type semiconductor $n >> n_i$, (i.e) Electrons are majority charge carriers and holes are minority charge carriers.

MASS ACTION LAW:-

In an intrinsic semiconductor (number of free electrons $n = n_i$) & (No. of holes $p = p_i$)

Since the crystal is Electrically neutral

$$n_i p_i = n_i^2$$

Regardless of individual magnitudes of n & p, the product is always constant

$$np = n_i^2$$

$$n_i = A T^{3/2} e^{-\frac{E_{g0}}{2KT}}$$

(A = constant for a semiconductor
T = Temperature in °K
E_g = Energy Gap in EV
K = Boltzman's const)

This is called Mass-Action law.

Law of Electrical Neutrality

- Let 'N_D' be concentration of donor atoms in a doped semiconductor. It donates an electron & becomes positively charged ion and the positive charged density contributed by them is N_D.
- If 'p' is the hole density, then total positive charge density is $N_D + p$.
- Similarly 'N_A' be concentration of acceptor atoms, it accepts an electron & becomes negatively charged & the negative charge density is denoted by N_A
- If 'n' is the electron density, then total negative charge density is $N_A + n$.

$\therefore$ Total positive charge = Total Negative charge

$$\boxed{N_D + p = N_A + n}$$

This is law of Electrical Neutrality

In n-type material, $N_A = 0$ ($\because n >> p$), p can be neglected

so $N_A = 0$, $p \cong 0$

$$N_D + 0 = 0 + n_n$$

$$N_D \simeq n_n$$

we know that $n_n \times p_n = n_i^2$

$$N_D \times p_n = n_i^2$$

$$p_n = \frac{n_i^2}{N_D}$$

$\therefore$ Hole density in n-type semiconductor $p_n = \frac{n_i^2}{N_D}$

Similarly ~~hole~~ Electron concentration in p-type semiconductor

$N_D = 0$ & $(p >> n)$

$\therefore n \cong 0$

$$N_A + 0 = 0 + p_p$$

$$N_A \simeq p_p$$

$$n_p \times p_p = n_i^2$$

$$\boxed{n_p = \frac{n_i^2}{N_A}}$$

FERMI LEVEL :

It is defined as the Energy state, with 50% probability of being filled if no forbidden Energy gap exists. In other words, it is the mass Energy level of the Electrons, at 0° K.

Fermi Dirac probability function is given by

$$f(E) = \frac{1}{1 + e^{\frac{(E - E_F)}{KT}}}$$

where E = Energy state

E_F = Fermi Energy level.

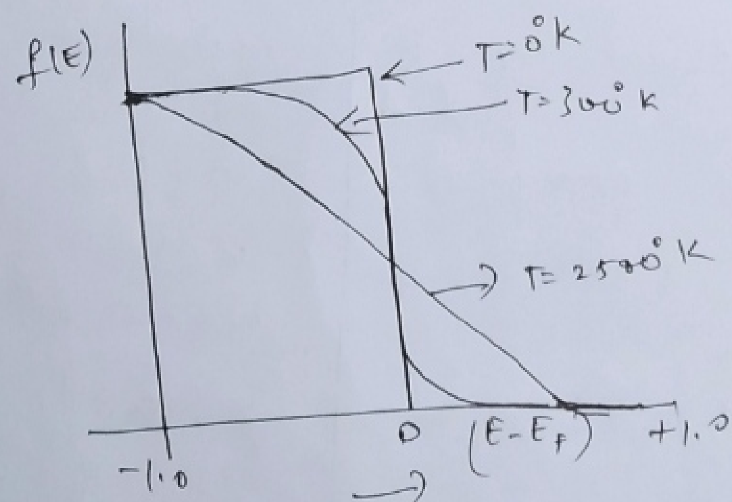
K = Boltzman constant & T = Temperature in °K.

when $E = E_F$

$$f(E) = \frac{1}{1 + e^{\frac{(E_F - E_F)}{KT}}} = \frac{1}{1 + e^{\left(\frac{0}{KT}\right)}} = \frac{1}{1 + e^0}$$

$$= \frac{1}{1+1} = \frac{1}{2} \quad (\because e^0 = 1)$$

$$f(E) = \frac{1}{2}.$$

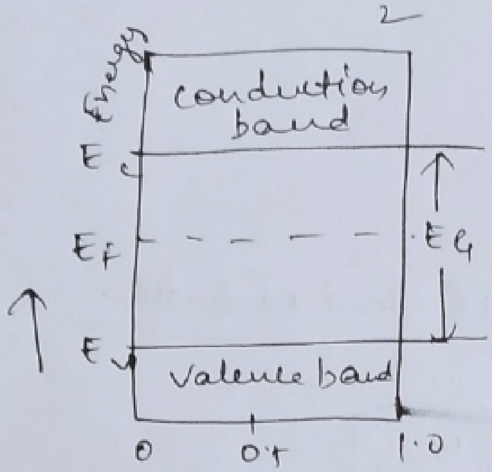


Fermi level is the maximum Energy level that can be occupied by the Electrons at 0°K. Fermi level or characteristic Energy represents the Energy state with 50% probability of being filled if no forbidden band Exists.

If $E = E_F$, then $f(E) = 1/2$ for an value of temperature.

FERMI LEVEL IN INTRINSIC SEMICONDUCTOR

$$E_F = \frac{E_C + E_V}{2}$$



In Intrinsic semiconductor, Fermi level lies in the middle of Energy Gap E_G.

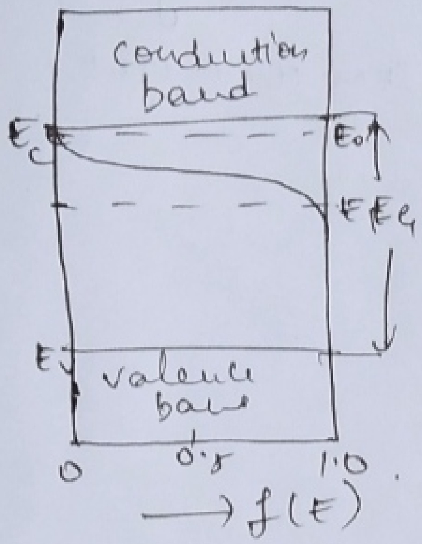
FERMILEVEL IN DOPED SEMICONDUCTOR.

$$E_G = KT \ln\left(\frac{N_C N_V}{n_i^2}\right)$$

In n-type semiconductor

$$E_F = E_C - KT\left[\ln\left[\frac{N_C}{N_D}\right]\right]$$

So, the Fermi level is close to conduction band E_C in n-type semiconductor.

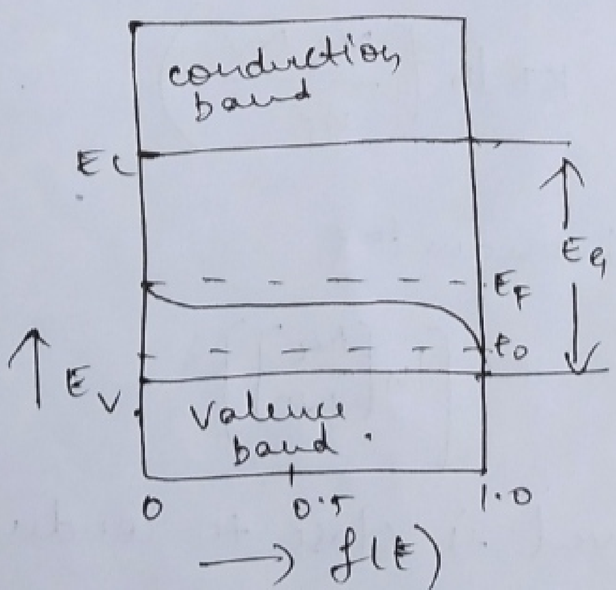


Fermi level in n-type semiconductor.

In p-type semi conductor,

$$E_F = E_V + KT\left[\ln\left(\frac{N_V}{N_A}\right)\right]$$

Fermi level is close to valence band E_V in p-type semiconductor ~~in case of~~



Principle and operation of Diode:

Diode is a semiconductor device that essentially acts as a one-way switch for current. It allows current to flow easily in one direction, but severely restricts current from flowing in the opposite direction

Anode cathode

The word Diode refers to 'Di' means two and 'Ode' means Electrode. As the newly formed component have two terminals (or) Electrodes

The arrow indicates the flow of current through it when the diode is in forward biased mode, the dash or the block at the tip of the arrow indicates the blockage of current from the opposite direction.

Cut-in voltage: The voltage at which forward bias current of the diode starts increasing rapidly is known as cut in voltage cut-off. It is higher than the threshold voltage

Cut-off voltage: The voltage between the threshold voltage and break down voltage is known as cut-off voltage.

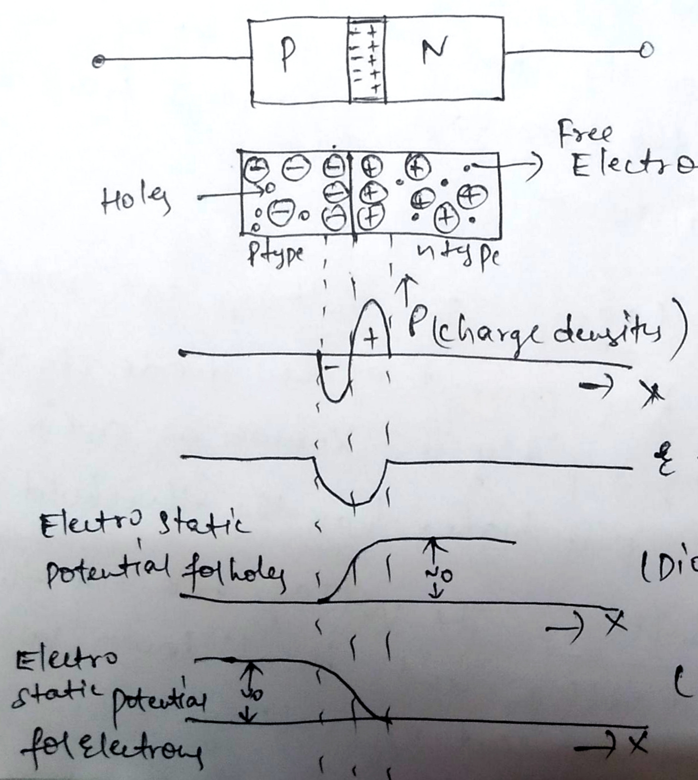
Breakdown voltage: The maximum reverse bias voltage that can be applied to a p-n diode is limited by breakdown. Breakdown is characterized by the rapid increase of the current under reverse bias. The corresponding voltage is referred to break down voltage.

Threshold voltage: The minimum voltage at which the diode conducts (starts) is known as Threshold voltage.

For Silicon $V_{th} = 0.7V$

For Germanium $V_{th} = 0.3V$

Theory of PN JUNCTION:



$$\mathcal{E} = -\int \frac{\rho}{\epsilon}\, dx = -\frac{dV}{dx}$$

(Diode is open circuited)

(Diode is short circu

Qualitative theory of PN Junction diode:-

In a piece of Semiconductor material, if one half is doped by p-type impurity and the other half is doped by N-type impurity, a PN junction is formed. The plane dividing the two halves and Zones is called PN junction. The N-type material has high concentration of free electrons, while p-type material has high concentration of holes. Therefore, at the junction there is a tendency for the free electrons to diffuse over the p-side and holes to the N-side. This process is called diffusion.

→ As the free electrons move across the junction from N-type to p-type, the donor ions becomes positively charged and from p-type to n-type, the acceptor ions becomes negatively charged.

PN Junction under Forward bias condition:-

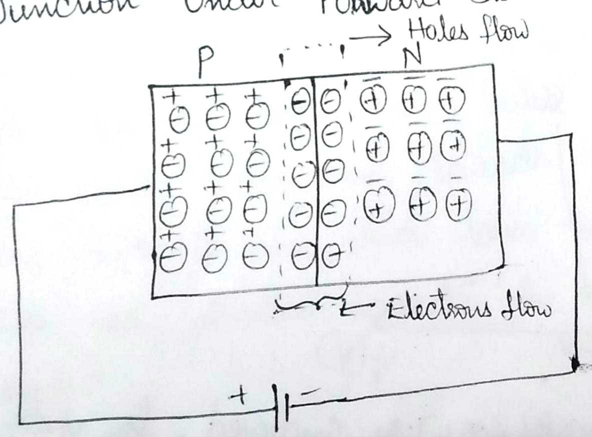


fig:- PN Junction Under Forward bias

When the positive terminal of the battery is connected to the p-type and negative terminal to the N-type of PN junction diode, the bias applied is known as forward bias.

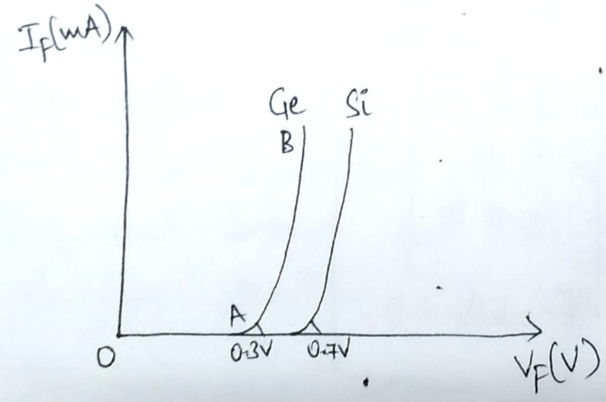
→ The applied potential with external battery acts in oppositio to the internal potential barrier and disturbs the equilibriu

→ As soon as equilibrium is disturbed by the application of an external voltage, the Fermi level is no longer continuous across the junction.

→ Under the forward bias condition, the applied positive potential repels the holes in P-type region so that the holes move towards the junction and the applied -ve potential repels the electrons in the N-type region and the electrons move towards the junction.

→ Eventually, when the applied potential is more than the internal barrier potential the depletion region and internal potential barrier disappear.

→ Ideal characteristics of PN junction under forward bias condition as follows:



→ As the forward voltage (V_F) is increased, for $V_F < V_0$, the forward current I_F is almost zero because the potential barrier prevents the holes from P-region and electrons from N-region to flow across the depletion region in the opposite direction

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→ For $V_F > V_0$, the potential barrier at the junction completely disappears and hence, the holes across the junction from P-type to N-type and the electrons cross the junction in the opposite direction, resulting in relatively large current flow in the external circuit.

PN Junction Under Reverse Bias condition:-

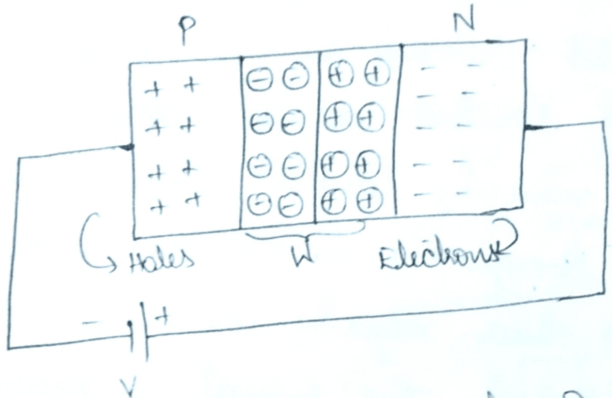


fig:- PN junction under Reverse bias

→ When the -ve terminal of the battery is connected to the P-type and +ve terminal of the battery is connected to the N-type of the PN junction, the bias applied is known as reverse bias.

→ Under applied reverse bias, holes which form the majority carriers of the p-side move towards the -ve terminal of the battery and electrons which form the majority carrier of the N-side are attracted towards the +ve terminal of the battery.

→ Hence, the width of the depletion region which is depleted of mobile charge carriers increases. Thus the electric field produced by applied reverse bias, is in the same direction as the electric field of the potential barrier. Hence, the potential barrier is increased which prevents the flow of majority carriers in both directions. therefore, theoretically no current Should flow in the Circuit. But in practice, a very Small current of the order of a few microamperes flows under reverse bias.

→ Under reverse bias condition, the thermally generated hole in the p-region are attracted towards the -ve terminal of the battery and electrons in the N-region are attracted towards the positive terminal of the battery.

→ Consequently, the minority carriers, electrons in the p-region and holes in the N-region, wander over to the junction and flow towards their majority carrier side giving rise to Small reverse current. this current is Known as reverse Saturation Current I_0. The magnitude of reverse Saturation current mainly depends upon junction temperature because the major Source of minority carriers is is thermally broken Covalent bonds.

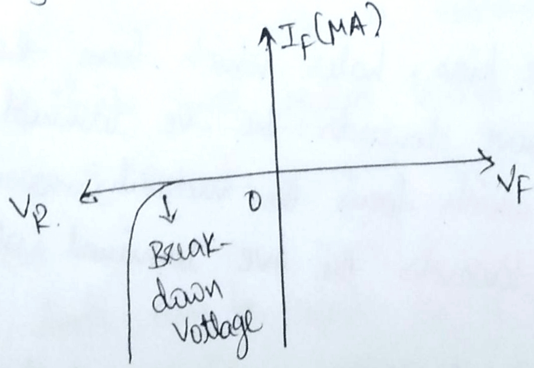
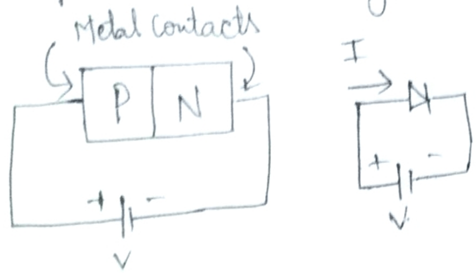


fig:- V-I characteristics Under Reverse bias

PN Junction as a diode :-

The characteristics of the PN junction vary and depends upon the polarity of the applied Voltage. For a forward-bias voltage, the current increases exponentially with the increase of voltage. A small change in the forward bias voltage increases the corresponding forward-bias current by orders of magnitude and hence the forward-bias PN junction will have a very small resistance. The level of current flowing across a forward-biased PN junction largely depends upon the junction area.

→ In the reverse-bias direction, the current remains small, i.e. almost zero, irrespective of magnitude of the applied voltage and hence the reverse bias PN junction will have a high resistance. The reverse bias current depends on the junction are temperature and type of semiconductor material.



fig(a):- Forward-bias ckt

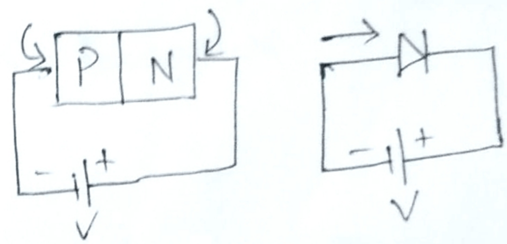
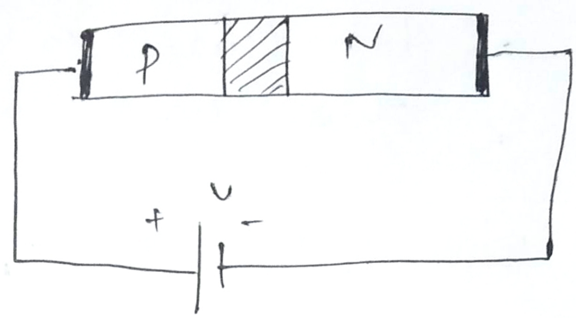


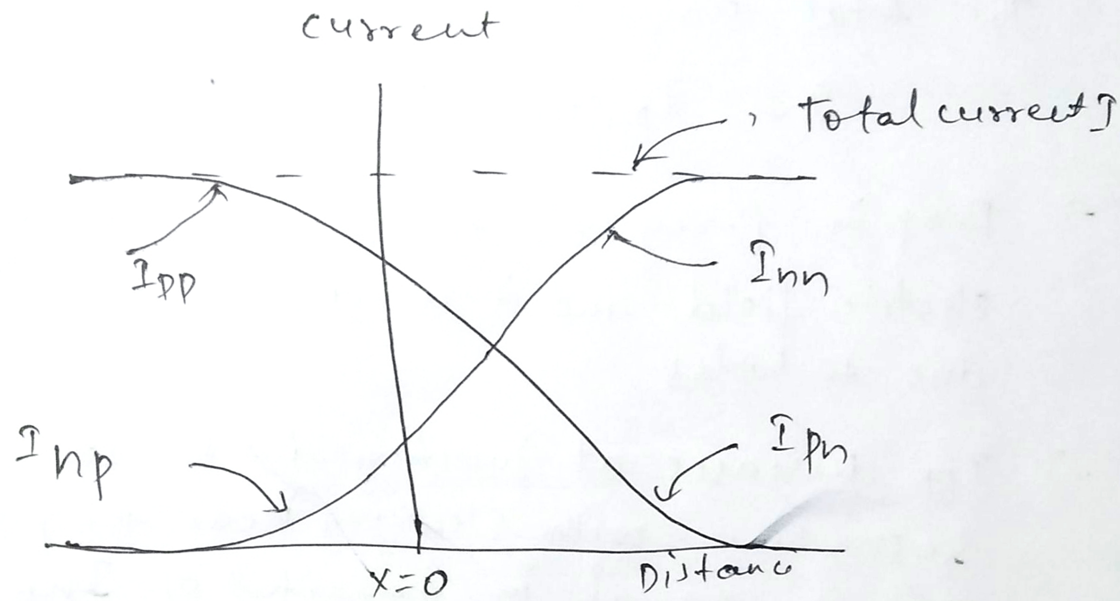
fig:-(b) Reverse bias ckt

→ In the forward-bias, a relatively large current is produced by a fairly small applied voltage. In the reverse bias, only a very small current, ranging from nanoamps to microamps is produced.

→ The diode can be used as a voltage controlled switch i.e OFF for a reverse-bias voltage and ON for a forward-bias voltage.

Current components in a P-N JUNCTION DIODE





ted

- when a forward bias is applied to the diode holes ar injected into n-side and Electrons to the p-side.
- the number of this injected carries decreases exponentially with distance from the junction.
- since the diffusion current of minority carriers is propostional to the number of carriers the minority carriers current decreases exponentialy

where I_{pp} = hole current in p-region

$(I_{np}) I_{np}$ = Electron current in p-region

$(I_{pn}) I_{pn}$ = hole current in n-region

I_{nn} = Electron current in n-region

There are two minority currents I_{np} & I_{pn}

The total current accross the junction is

$$I = I_{pn}(0) + I_{np}(0) \quad (x = 0)$$

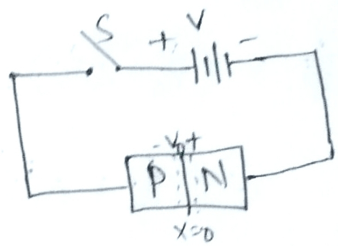
-) Deep in p-region the current is because of electric field and it is drift current (I_{pp}) due to holes.

-) I_{pp} decreases at junction due to some holes. Recombine with electrons near the junction and is equal in magnitud of I_{np}

-) So, in forward bias, the current is hole current as the majority charge carries are holes. Thus the current enters as hole current and leaves as electron current. in forward bias.

Diode Equation:-

Let us consider an open circuit P-N junction as shown in fig: with switch S open. Let hole and electron densities in p-region are P_p and n_p respectively. Similarly, electron and hole densities in N-region are n_n and P_n respectively.



The density of holes in p-region and density of holes in N-region are related by Boltzmann relation as

$$P_p = P_n e^{V_B/V_T}$$

where V_B is barrier potential across depletion layer

V_T is volt equivalent of temperature

$$V_T = \frac{KT}{e} = \frac{T}{11,600}$$

where K is Boltzmann Constant $= 1.381 \times 10^{-23}$ J/K

→ For open circuited P-N junction, $V_B = V_0$, hence

$$P_p = P_n e^{V_0/V_T} \quad \text{——— (1)}$$

Consider that the junction is biased in the forward direction by applying a voltage V i.e. by closing switch S. Now the barrier voltage V_B is decreased from its equilibrium value V_0 by an amount V or $V_B = V_0 - V$. With forward bias, the hole density in p-region remains constant upto depletion region while in N-region just at the junction it increases from P_n to $P_n + \Delta P_n$ due to diffusion of holes across the junction. As the holes diffuse further in

N-region, they combine with electrons and their density decreases with increase of distance from the junction. Ultimately at large distance it becomes the same as P_n. Now the hole density in N-region can be expressed by Boltzmann relation as

$$P_p = (P_n + \Delta P_n) . e^{(V_0 - V)/V_T}$$

$$= (P_n + \Delta P_n) e^{V_0/V_T} e^{-V/V_T} \quad \text{——— (2)}$$

Substituting the value of P_p in eqn (2) we get

$$P_n e^{V_0/V_T} = (P_n + \Delta P_n) . e^{V_0/V_T} e^{-V/V_T}$$

$$P_n = (P_n + \Delta P_n) e^{-V/V_T}$$

$$P_n e^{V/V_T} = (P_n + \Delta P_n)$$

$$\Delta P_n = P_n (e^{V/V_T} - 1) \quad \text{——— (3)}$$

From eqn (1) $\quad P_n = P_p e^{-V_0/V_T} \quad$ ——— (4)

Subst the value of P_n from eqn (4) in eqn (3) we get

$$\Delta P_n = P_p e^{-V_0/V_T} (e^{V/V_T} - 1) \quad \text{——— (5)}$$

The diffusion of holes constitute the hole current. The hole current I_p is proportional to ΔP_n. So

$I_p \propto \Delta P_n$ or $I_p \propto P_p e^{-V_0/V_T} (e^{V/V_T} - 1)$

$$I_p = I_{sp}(e^{V/V_T} - 1) \quad \text{——} \quad (6)$$

where I_{sp} represents the constant of proportionality.

→ In a similar way, an expression for electron current due to diffusion of electrons from N-region to p-region may be obtained. This is given by

$$I_n = I_{sn}(e^{V/V_T} - 1) \quad \text{——} \quad (7)$$

The total current I is given by

$$I = I_p + I_n$$

$$= I_{sp}(e^{V/V_T} - 1) + I_{sn}(e^{V/V_T} - 1)$$

$$\boxed{I = I_0(e^{V/V_T} - 1)} \quad \text{——} \quad (8)$$

where I_0 is called the saturation current.

Eqn (8) is called diode current equation

In general $\boxed{I = I_0\left(e^{V/\eta V_T} - 1\right)}$ —— (9)

where I = forward or reverse diode current

I_0 = Reverse saturation current

V = External voltage, which is +ve for forward bia[s] and -ve for reverse bias

η = constant, which depends upon the material property and have a value one for Ge and 2 for Si:

V_T = Volt equivalent of temperature.

For forward biased junction:

The value of V will be +ve. For large forward biased voltage $e^{V/nV_T} >> 1$. In this case.

$$I_f = I_0 e^{V/nV_T} \quad \text{—— (10)}$$

This eqn shows that for a given temperature the forward current increases exponentially with voltage V. except for a small value of V.

For reverse biased junction:

In this we have

$$I_r = I_0 (e^{-V/nV_T} - 1)$$

for a reverse bias whose magnitude is large compared with V_T, we have

$$(e^{-V/nV_T} \to 0)$$

$$\Rightarrow I_r \to -I_0$$

Hence I_0 is called reverse saturation current. This is constant independent of applied reverse bias.

Volt- Ampere characteristics of a P-N JUNCTION DIODE

The general Expression for current in the p-n junction diode is given by

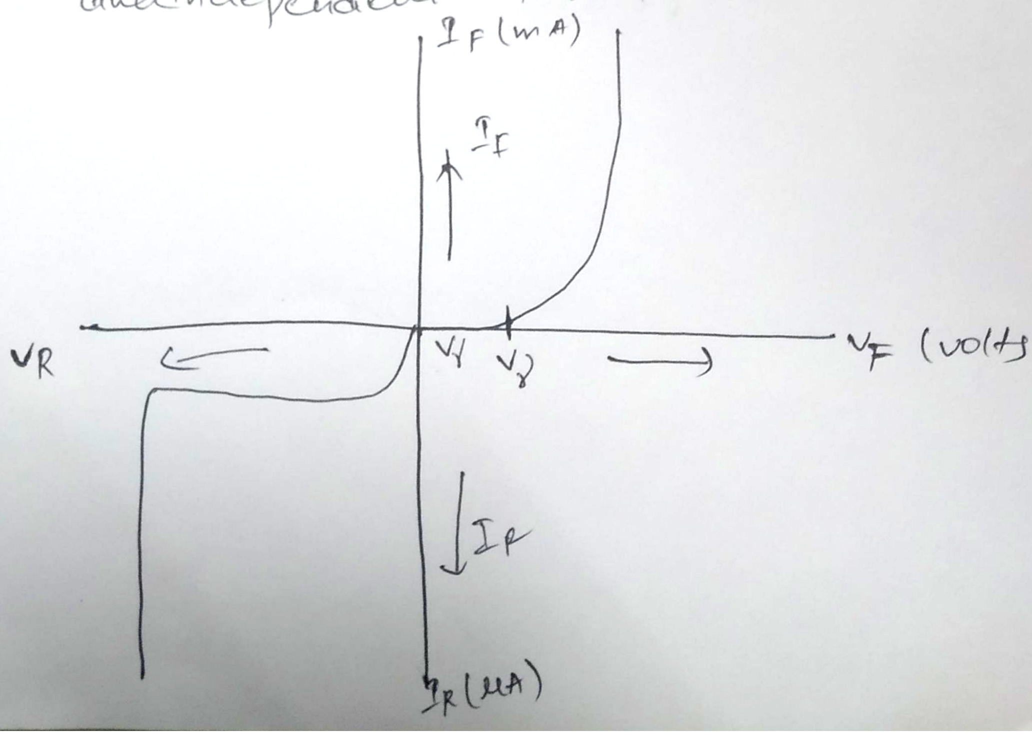
$$I = I_0 \left(e^{\frac{V}{\eta V_T}} - 1 \right)$$

$\eta = 1$ for Ge, $\eta = 1$ or 2 for Si. For silicon, I will be less than that for Germanium

$V_T = 26mV$

If $V >> V_T$, I_0 can be neglected. So I increases Exponentially with forward bias voltage

In case of reverse bias, if the reverse voltage $-V >> V_T$, then e^{-V/V_T} is neglected and so reverse current $-I_0$ remains constant and independent on V.



Temperature dependence of VI characteristics of diode:-

The reverse saturation current I_0, Voltage equivalent of temperature V_T are temperature dependent. Hence the diode current I is also temperature dependent.

→ The dependence of I_0 on temperature T is given by

$$I_0 = KT^m e^{-V_{G0}/\eta V_T} \quad \text{——— (1)}$$

where K = Constant independent of temperature

m = 2 for Ge and 1.5 for Si

V_{G0} = forbidden energy gap = 0.785V for Ge and 1.21V for Si

→ As temperature increases, I_0 increases and hence diode current increases. To keep diode current constant, it is necessary to reduce the applied voltage V.

→ For a constant diode current $\frac{dI}{dT} = 0$

Diode current equation is given by

$$I = I_0 (e^{V/\eta V_T} - 1)$$

for forward bias $I >> I_0$, then

$$I = I_0 e^{V/\eta V_T} \quad \text{——— (2)}$$

Subst eqn (1) in (2)

$$I = KT^m e^{-V_{G0}/\eta V_T} \cdot e^{V/\eta V_T}$$

$$I = KT^m e^{(V - V_{G0})/\eta V_T} \quad \text{——— (3)}$$

Since $V_T = KT$, where K = Boltzmann's Constant

$$I = KT^m e^{(V - V_{G0})/\eta KT} \quad \text{——— (4)}$$

differentiating the above eqn w.r.to T, we get

$$\frac{dI}{dT} = K\left[mT^{m-1} e^{(V-V_{G0})/\eta KT} + T^{m} e^{(V-V_{G0})/\eta KT} \cdot \frac{d}{dT}\left(\frac{V-V_{G0}}{\eta KT}\right)\right]$$

$$\frac{dI}{dT} = Ke^{(V-V_{G0})/\eta KT}\left[mT^{m-1} + \frac{T^{m}}{\eta K}\left(\frac{T\frac{dv}{dT} - (V-V_{G0})\times 1}{T^2}\right)\right]$$

$$= Ke^{(V-V_{G0})/\eta KT}\left[\frac{mT^{m}}{T} + \frac{T^{m}}{\eta KT^2}\left(T\frac{dv}{dT} - (V-V_{G0})\right)\right]$$

$$= Ke^{(V-V_{G0})/\eta KT} \times \frac{T^{m}}{\eta KT^2}\left[m\eta KT + \left(T\frac{dv}{dT} - (V-V_{G0})\right)\right]$$

replace KT with V_T, then

$$\frac{dI}{dT} = Ke^{(V-V_{G0})/\eta KT} \times \frac{T^{m-1}}{\eta V_T}\left[m\eta V_T + \left(T\frac{dv}{dT} - (V-V_{G0})\right)\right]$$

$$m\eta V_T + T\frac{dv}{dT} - (V-V_{G0}) = 0$$

$$T\frac{dv}{dT} = V-V_{G0} - m\eta V_T$$

$$\frac{dv}{dT} = \frac{V-(V_{G0}+m\eta V_T)}{T}$$

This is the required change in voltage necessary to keep diode current constant.

→ Hence, for Ge, at cut in voltage $V = V_0 = 0.2V$ and $m = 2$, $\eta = 1$, $T = 300K$ and $V_{G0} = 0.785V$ in above eqn, we get

$$\frac{dv}{dT} = \frac{0.2 - (0.785 + 2 \times 1 \times 26 \times 10^{-3})}{300} = -2.12 \, mV/^oC \text{ for Ge.}$$

→ The -ve sign indicates that the voltage must be reduced at a rate of 2.12mV per degree change in temperature to keep diode current constant.

Similarly, $\frac{dv}{dT} = -2.3 \, mV/^oC$, for Si

Effect of temperature on reverse saturation current:-

From eqn (1.), $I_0 = KT^m e^{-V_{G0}/\eta V_T}$

taking logarithm on both sides, we get

$$\ln(I_0) = \ln(KT^m e^{-V_{G0}/\eta V_T})$$

$$= \ln K + \ln T^m - \frac{V_{G0}}{\eta V_T}$$

$$= \ln K + m \ln T - \frac{V_{G0}}{\eta V_T}$$

Subst $V_T = KT$, we get

$$\ln(I_0) = \ln K + m \ln T - \frac{V_{G0}}{\eta KT}$$

diffn above eqn w.r.to T, we get

$$\frac{d \ln(I_0)}{dT} = 0 + \frac{m}{T} - \frac{V_{G0}}{\eta K}\left(-\frac{1}{T^2}\right) = \frac{m}{T} + \frac{V_{G0}}{\eta KT^2}$$

Replacing KT with "V_T" we have

$$\frac{d[\ln I_0]}{dT} = \frac{m}{T} + \frac{V_{G0}}{\eta T V_T}$$

→ For Germanium, Subst the values at room temperature

$$\frac{d[\ln I_0]}{dT} = \frac{2}{300} + \frac{0.785}{1 \times 300 \times 26 \times 10^{-3}} = 0.11 ^\circ C$$

This indicates that I_0 increases by 11% per degree rise in temperature.

for Silicon $\frac{d[\ln I_0]}{dT} = 0.08 ^\circ C$.

→ This indicates that I_0 increases by 8% per degree rise in temperature.

→ practically it is found that the reverse saturation current I_0 increases by 7% per °C change in temperature for both silicon and germanium diodes. If a T°C is 1MA then at (T+1)°C, it becomes 1.07MA and so on. It can be concluded that reverse saturation current approximately doubles i.e. 1.07^{10} for every 10°C rise in temperature.

→ The above result can be mathematically represented as,

$$I_{02} = \left(2^{\frac{T_2 - T_1}{10}}\right) I_{01} = \left(2^{\frac{\Delta T}{10}}\right) I_{01}$$

where I_{02} is the reverse saturation current at T_2 and

I_{01} is the " " " T_1

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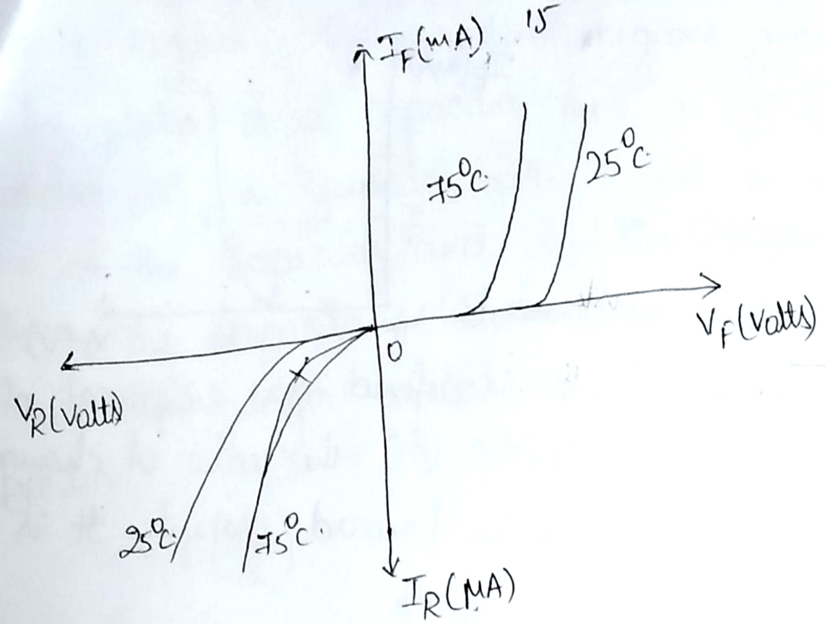


fig:- Effect of temperature on the diode characteristics

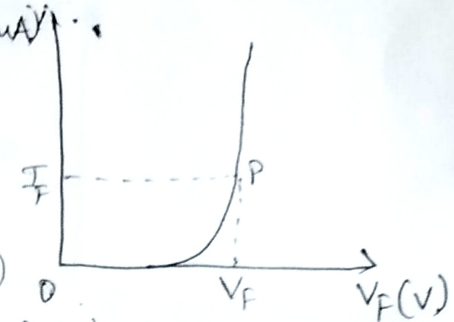
Ideal versus practical - Resistance levels (static and dynamic):-

Static Resistance:-

An ideal diode should offer zero resistance in forward bias and infinite resistance in the reverse bias. But in practice no diode can act as an ideal diode. So the real diode doesnot offer zero resistance when it is forward biased and an infinite resistance when reverse biased. This shows that when a real diode is forward biased has a definite resistance. This resistance is known as static or forward resistance of diode.

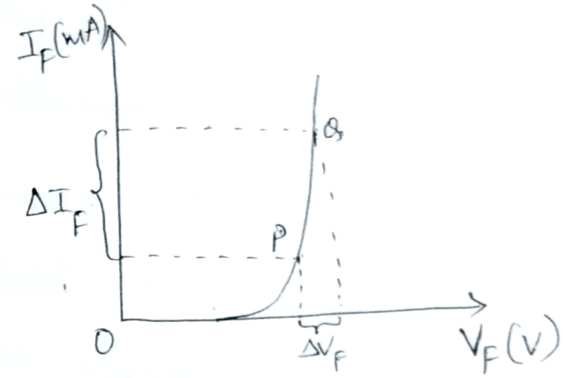
"Static resistance is defined as the ratio of d.c voltage across the diode to the d.c current flowing through it". If V_F and I_F be the d.c voltage across diode to the d.c current flowing through it respectively. then the static Resistance R_F is given by

$$R_F = \frac{V_F}{I_F}$$



Dynamic Resistance:-

The dynamic resistance (or) ac resistance of a diode is defined as reciprocal of the slope of forward characteristic (or) the ratio of change in forward voltage to change in forward current. It is denoted by r_{ac}.



$$r_{ac} = \frac{\Delta V_F}{\Delta I_F}$$

$$I = I_0 e^{V/\eta V_T} \quad ; \text{ for FB.}$$

$$\frac{dI}{dV} = \frac{d}{dV}\left(I_0 e^{V/\eta V_T}\right) = \frac{d}{dV}\left(I_0 e^{V/\eta KT}\right)$$

$$= I_0 e^{V/\eta KT} \times \frac{1}{\eta KT} = \frac{I}{\eta KT}$$

$$\Rightarrow \boxed{r_{ac} = \frac{dV}{dI} = \frac{\eta KT}{I}}$$

Capacitive effects in P-N Junction diode:-

The depletion layer width decreases when the P-N junction is forward biased while increases when P-N junction is reverse biased. The depletion layer acts as a dielectric medium (Non-conductive) between

P and N regions. Therefore these regions may be regarded as the plates of a capacitor. Thus a P-N junction may be regarded as a capacitor with P and N regions as the plates of the capacitor and depletion layer as dielectric medium. The capacitance formed in junction area is called as depletion layer capacitance. For a parallel plate capacitor

$$C = \epsilon\left(\frac{A}{d}\right)$$

where ϵ = permitivity of dielectric
A = area of plates
d = seperation between the plates

→ As the value of d increases in reverse bias, hence depletion layer capacitance decreases. Depletion layer capacitance increases in forward bias because d decreases

① Space charge (or) Transition capacitance (C_T):-

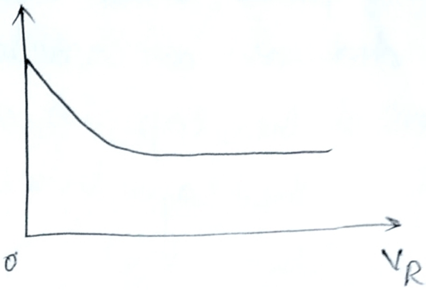
In reverse bias, the depletion layer capacitance is called as transition capacitance and dinoted by C_T. This capacitance is voltage dependent and is given by

$$C_T = \frac{K}{(V_0+V_R)^n}$$

where V_0 = cut in voltage
V_R = applied reverse voltage
K - constant depends on material (n)

$n = \frac{1}{2}$ for alloy junction and $\frac{1}{3}$ for diffused junction.

→ The space charge capacitance C_T decreases with increase in applied reverse voltage (V_R).



a) Step graded junction:-

In this case, there is an abrupt change from acceptor ion concentration on P-side to donor ion concentration on N-side. This type of junction is alloy junction. In this junction, usually the acceptor density N_a and donor density N_d are kept unequal.

$$C_T = \frac{\epsilon A}{x}$$

for alloyed junction, $x = \sqrt{\frac{2\epsilon V_B}{e N_d}}$

Subst x in C_T

$$\Rightarrow C_T = \epsilon A \left[\frac{e N_d}{2 \epsilon V_B}\right]^{1/2} = A\left[\left(\frac{e\epsilon}{2}\right)\left(\frac{N_d}{V_B}\right)\right]^{1/2}$$

(b) Linearly graded junction:-

In this type of junction, the charge densities varies linearly with distance. So $N_a = N_d$, hence x is given by

$$x = \left[\frac{6 \epsilon V_B}{e N_d}\right]^{1/2}$$

$$C_T = \epsilon A \left[\frac{e N_d}{6 \epsilon V_B}\right]^{1/2} = A\left[\left(\frac{e\epsilon}{6}\right)\left(\frac{N_d}{V_B}\right)\right]^{1/2}$$

② Diffusion capacitance (C_D):-

When the P-N junction is forward biased, the depletion layer capacitance is called as diffusion capacitance and denoted by C_D. The charge is stored on both sides of junction when forward bias is applied. Thus the amount of stored charge varies with applied voltage. hence this capacitance is also called as storage capacitance. and is given by

$$C_D = \frac{dq}{dV}$$

The current $I = \frac{q}{\tau}$

where q = charge.

τ = mean life time of carriers

$$I = I_0 \left[e^{V/\eta V_T} - 1 \right]$$

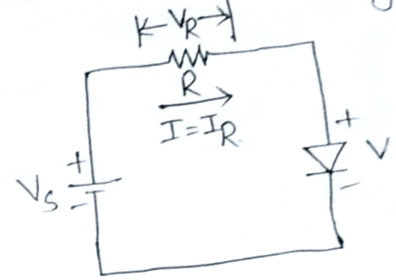
$$q = I_0 \tau \left[e^{V/\eta V_T} - 1 \right] = I_0 \tau e^{V/\eta V_T} \quad [\because \text{Forward bias}]$$

$$C_D = \frac{dq}{dV} = \frac{d}{dV}\left[\tau I_0 e^{V/\eta V_T} \right] = \frac{\tau I_0}{\eta V_T} e^{V/\eta V_T}$$

$$\boxed{C_D = \frac{\tau I}{\eta V_T}} \quad \left(\because I = I_0 e^{V/\eta V_T} \right)$$

Diode equivalent circuits:- 20

The basic diode circuit consists of a dc voltage V_s which is supplied across a resistor and a diode. In order to find the instantaneous diode voltage V and current I, the circuit can be analysed when the instantaneous source voltage is V_s. From KVL, ~~the~~



$$V_s = IR + V \quad \text{——— (1)}$$

The ideal diode current equation is

$$I = I_0\left[e^{V/\eta V_T} - 1\right] \quad \text{——— (2)}$$

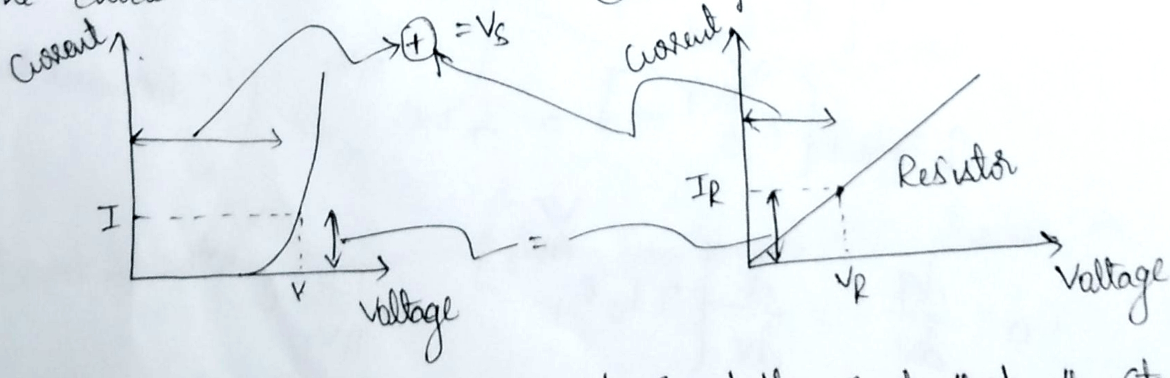
Subst eqn (2) in (1)

$$V_s = I_0 R\left[e^{V/\eta V_T} - 1\right] + V$$

Load Line Analysis:-

From KCL, $I = I_R$ and from KVL $\Rightarrow V + V_R = V_s$

(i) The diode characteristics are: (ii) Output across resistor



→ Flip the resistor curve horizontally such that the slope of the curve is $-1/R$ and push the 2 curves together untill the y-axis are V_s apart. The intersection point of the flipped resistor curve on the diode characteristics is called as operating point or quiescent point (Q).

To draw load line, I is determined when the device is short-circuited and V is determined when the device is open circuited, so that the point B ($V=0$; $I = V_S/R$) and A ($V=V_S$, $I=0$) lies somewhere on the y-axis and x-axis respectively of the diode characteristics. Thus a straight line drawn connecting the points A and B is called the load line. This load line intersects the diode characteristi at some point which is chosen as operating point for the device. The operating point provides the diode voltage V, appearing across the diode and current I, flowing through the diode.