

18/8/22

UNIT - IV

Bipolar Junction Transistors (BJT)

Transistor is a solid state who's operation depends upon flow of electric charge carriers within the solid

- * The transistor is a current control device
- * Transistor is small in size and it is light weighted
- * Transistor has three terminal and two junction semiconductor device
- * These are categorised into two types
 - 1. Unipolar and 2. Bipolar transistor

In bipolar transistor the electrical conduction is due to both holes and electrons whereas in unipolar transistor the electrical conduction is due to either holes or electrons.

Transistor was invented by John Bardeen f W.H. Brattain in 1948

Under normal working operation of transistor it has two junction, one junction is in forward bias and the other junction is in reverse bias

Forward biased junction offers low resistance and reverse biased junction offers high resistance path. So, by giving a weak single signal to a low resistance region and taking output from the high resistance region from this we get an amplified signal. Hence, transistor indicates transfer of signal from low resistance to high resistance

* Transfer + Resistor = Transistor

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A junction transistor is simply a sandwich of one type of semiconductor material between two layers of the other type.

There are two types of transistors

1. n-p-n transistor

2. p-n-p transistor

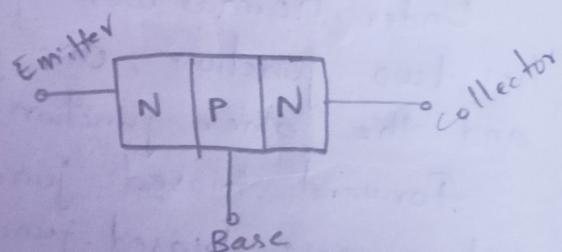
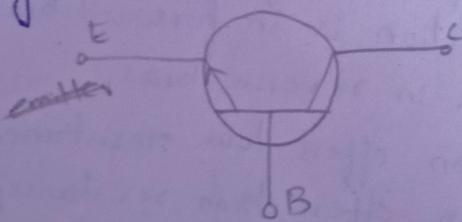
1. n-p-n transistor:-

When a layer of p-type material is sandwiched between two layers of n-type material then that transistor is known as n-p-n transistor. Similarly

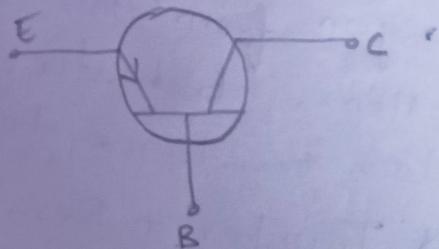
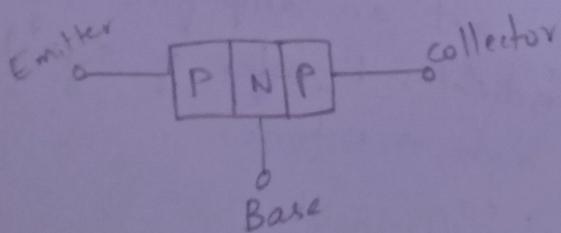
2. p-n-p transistor:-

When a layer of n-type material is sandwiched between two layers of p-type material then this transistor is known as p-n-p transistor

Transistors are made either Silicon or Germanium crystal.



Structure and Symbol of N-P-N Transistor



Structure and Symbol of P-N-P Transistor

→ Emitter :-

This forms the left hand section of the transistor. The main function of this region is to supply majority charge carriers (either holes or electrons) to the base and hence it is more heavily doped compared to other regions.

→ Base :-

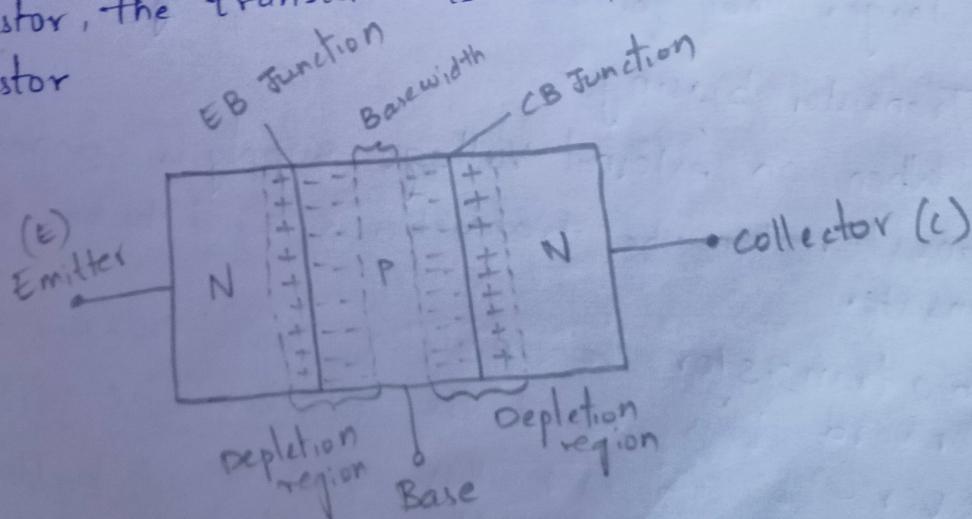
The middle section of the transistor is known as base. It is very light doped and thin as compared to either emitter or collector. So that it may pass most of the injected charge carriers to the collector.

→ Collector :-

The right hand section of the transistor is called as collector. The main function of the collector is to collect majority charge carriers from the base. This is moderately doped.

→ Unbiased transistor:-

When no external supply is connected to a transistor, the transistor is said to be unbiased transistor.



→ A transistor consist of two diodes.

The junction b/w emitter and base called as emib

base diode or emitter diode similarly the junction between base and collector is called as collector base diode or simply collector diode

When no battery is connected between different terminals the transistor is said to be unbaised or open circuit state.

There are two depletion regions at the two junctions of a transistor. The width of the depletion layers will be different because the regions are doped at different levels.

It is important to mention here that depletion region penetrates more deeply into lightly doped side. Therefore, the depletion region at emitter junction penetrates less in heavily doped emitter and extends more in base region.

Similarly the depletion region at collector junction penetrates less in heavily doped collector, and extends more in lightly doped base region.

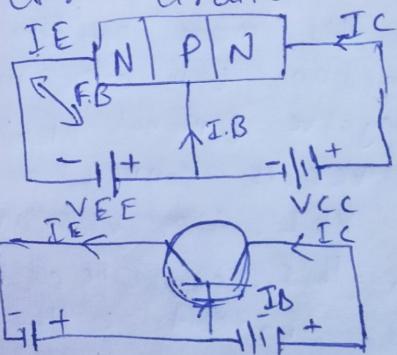
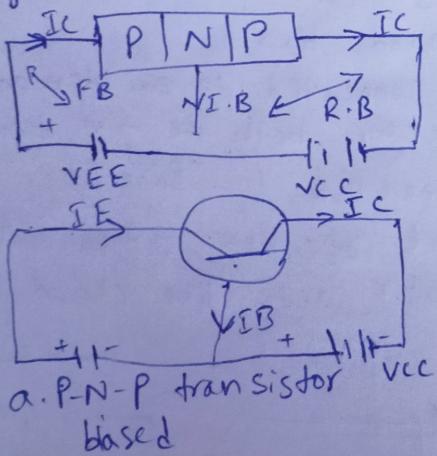
So, the depletion layer formed at collector junction is larger than formed at emitter junction.

→ Transistor biasing :-

When an external voltage supply is connected to transistor then the transistor is said to be biased transistor.

In a transistor the emitter base junction is always forward biased and the collector base junction always reverse biased, for these purpose a battery V_{EE} connected b/w emitter and base a battery V_{CC} connected b/w collector and base

- The emitter base junction of PNP transistor is forward biased by connecting the +ve terminal of VEE to emitter and -ve terminal to base.
- Similarly the emitter base junction of N-PN transistor is forward biased by connecting the -ve terminal of VEE of emitted +ve terminals to base.
- The collector base junction of P-N-P transistor is reverse biased by connecting the -ve terminal of VCC collector and +ve terminal to base.
- Similarly the called or base junction of N-P-N transistor is in reverse biased by connecting +ve terminal to VCC to collector and -ve terminal to base.
- The forward biasing of emitter base junction allows a low resistance for emitter circuit and reverse biasing of collector base junction provides high resistance in the collector circuit.



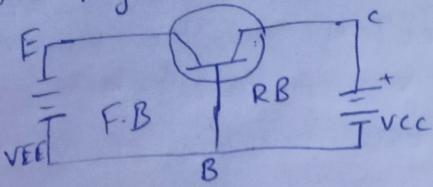
b) N-P-N transistor biased

Different modes of operation of transistor:

There are four possible ways of biasing a transistor these are called modes of operation of a transistor. These are listed below.

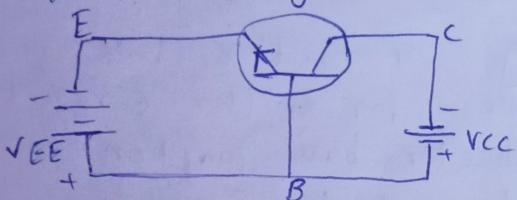
Cases	E-B junction	C-B junction	Region of operation
1.	Forward bias	Reverse bias	Active
2	Forward bias	Forward bias	Saturation
3	Reverse	Reverse	Cut-off
4	Reverse	forward	Inverted

Active Region:



- In this mode emitter base region is in forward bias
 collector base junction reverse bias. While considering N-P-N transistor. In the emitter base circuit a battery is connected emitter +ve is connected to base
 → similarly battery Vcc is connected to collector base circuit such that +ve is connected to collector and -ve is connected to base
 → In this region the transistor is used for amplification.

2. Saturation Region:



In this mode emitters base junction and collector base junction both are in forward bias.

→ Negative terminal of VEE is connected to emitter and -ve of Vcc is connected to collector both the +ve terminals of VEE and Vcc are connected to base.

→ In this case collector current becomes independent of base current so the transistor acts like closed switch.

3. Cut-off Region:

→ In this mode both the Junction are in Reverse biased + in this region the transistor has R.B. Partially zero current because the emitter does not emit charge carriers to base of course there is negligible current due to minority carriers. In these situations the transistor acts like open switch.

4) Inverted Region:-

\Rightarrow In this region emitter-base junction is in reverse bias and collector-base junction is in F.B
 \Rightarrow Here the collector can not inject V_{BE}

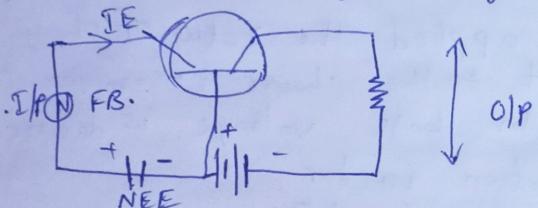
majority carriers into the base because the dropping level of emitter and collector is not same

\Rightarrow In this region the action of transistor is very poor.
Transistor circuit configuration:

The transistor configurations are classified into 3 types

1. Common Base (CB) Configuration.
2. common emitter (CE) Configuration.
3. Common collector (CC) Configuration.

1. Common Base (CB) Configuration.



Here the term common is used to denote the terminal which is common to the input and output circuit. This is because when a transistor is connected in a circuit four terminals are required two for input and two for output while a transistor has 3 terminals. This directly removes one terminal of the resistor common to both input and output terminal. A common terminal is generally grounded.

In common base configuration the input signal is applied between emitter and base while the output is taken from collector and base.

A base is common to input and output circuit hence the name is common base configuration.

DC current amplification factor (or) DC gain:

When no signal is applied then the ratio of the collector current to the emitter current is called

DC alpha of a transistor (α_{dc})

$$\alpha_{dc} = \frac{I_c}{I_E}$$

Negative sign indicates that I_E flows into transistor while I_c flows out of it

α_{dc} simply by α then

$$\alpha = -\frac{I_c}{I_E}$$

α of a transistor is a measure of quality of a transistor higher value of α gives the better transistor. By considering only magnitudes of the current.

$$I_c = \alpha I_E \text{ and } I_B = I_E - I_c$$

$$I_c = I_E - I_B$$

$$I_B = I_E - \alpha I_E \Rightarrow I_E (1 - \alpha)$$

Ac current:

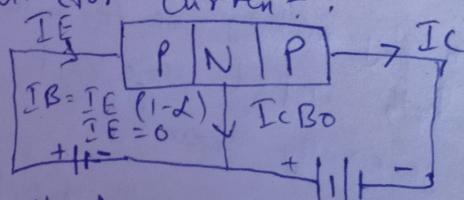
When signal is applied the ratio of change in collector's current to the change in emitter current of constant collector base voltage is defined as current amplification factor

$$\alpha_{ac} = \frac{\Delta I_c}{\Delta I_E}$$

$$\Rightarrow \alpha_{dc} = \alpha_{ac} = \alpha$$

The practical values of transistor range from 0.9 to 0.99

Total collector current.



The total collector current

1) Current produced by normal transistor action i.e., emitter current (I_E)

This is due to majority carriers and it's value is αI_E .

2) The leakage current I_{CBO} . This is due to minority carriers across collector base junction being reverse biased. Therefore.

Total Current = $I_E + I_{CBO}$
 Collector : Majority

or
 If $I_E = 0$

$$I_C = I_{CBO}$$

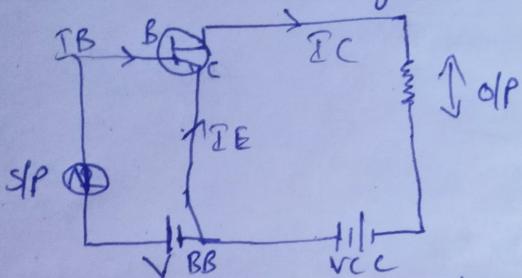
Total collector current also be expressed as

$$I_C = \beta [I_C + I_B] + I_{CBO}$$

$$I_C (1 - \beta) = I_B + I_{CBO}$$

$$I_C = \left(\frac{1}{1-\beta}\right) I_B + \left(\frac{1}{1-\beta}\right) I_{CBO}$$

Common emitter Configuration



In this configuration the input signal is applied between base and emitter of the output is taken from the collector and emitter.

→ As emitter is common to both input and output circuits hence the name as common emitter Configuration. The above circuit shows common emitter PNP transistor.

Base Current Amplification factor (or) DC Gain (β): When no signal is applied then the ratio of collector current to the base current Amplification factor $B_A = \beta = \frac{\Delta I_C}{\Delta I_B}$

From eqn ①

Almost in all transistors the base $I_C = \beta I_B$

Current is less than 5% of the emitters current Due to this β is generally greater than 20 and it reaches ~~from 100~~ 20 - 500

→ Hence common emitter configuration is frequently used when current gain as well as voltage gain is required

Total collector current: (I_{CC})

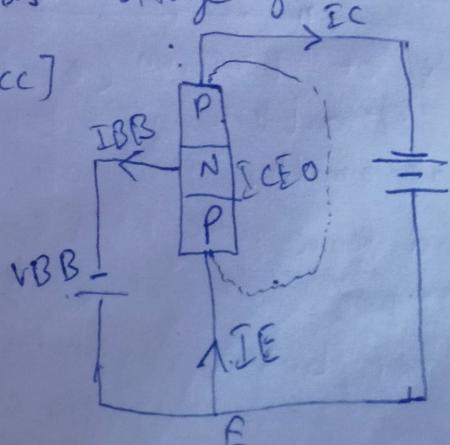
Total collector current

$$I_C = \beta I_B + I_{CEO} \rightarrow ③$$

If $I_B = 0$

$$\therefore I_C = I_{CEO}$$

We know that



$$I_E = I_B + I_C$$

$$I_C = \alpha I_E + I_{CBO}$$

$$I_C = \alpha (I_C + I_B) + I_{CBO}$$

$$I_C (1-\alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO} \rightarrow ④$$

from ② & ④

$$B = \frac{\alpha}{1-\alpha} + I_{CEO} \frac{1}{1-\alpha} I_{CBO} \rightarrow ⑤$$

Sub I_{CEO} in eqn ②

$$I_C = \beta I_B + \left(\frac{1}{1-\alpha}\right) I_{CBO}$$

$$\boxed{I_C = \beta I_B + (\beta + 1) I_{CEO}} \rightarrow ⑥$$

Relation between α and β

we know that

$$\alpha = \frac{I_C}{I_E} \text{ and } B = \frac{I_C}{I_B}$$

$$I_E = I_C + I_B \quad I_B = I_E - I_C$$

$$\text{Now } B = \frac{I_C}{I_E - I_C} = \frac{I_C / I_E}{1 - I_C / I_E}$$

$$\text{or } \boxed{B = \frac{\alpha}{1-\alpha}} \rightarrow ⑦$$

Cross multiply eqn 7

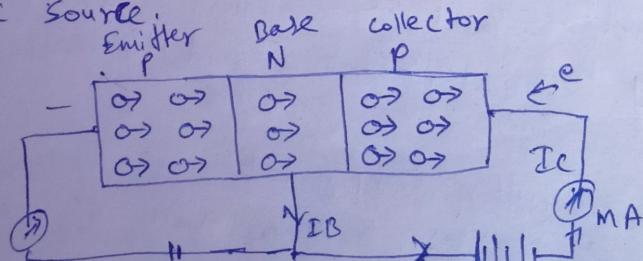
$$B(1-\alpha) = \alpha \text{ (or)}$$

$$B = \beta \alpha = \alpha$$

$$\beta = \alpha(1+\beta)$$

$$\therefore \boxed{\alpha = \frac{B}{1+B}}$$

Operation of PNP Transistor Below fig shows a PNP transistor with emitter base junction as forward biased by dc source.



1) The holes of P region (emitter) are repelled by the positive terminal of battery VEE towards the base. The potential barrier at emitter junction is reduced as it is forward bias and hence the holes cross the junction and penetrate into N-region. This constitute the emitter current I_E .

2) The width of base region is very thin and it is lightly doped and hence only two to five % of the holes recombine

with the free e^- of N-region. This constitute the base current I_B . Which of course is very small.

3. The remaining holes (95% to 98%) are able to drift across the base and enter the collector region. They are swept up by the negative collector voltage V_{CC} .

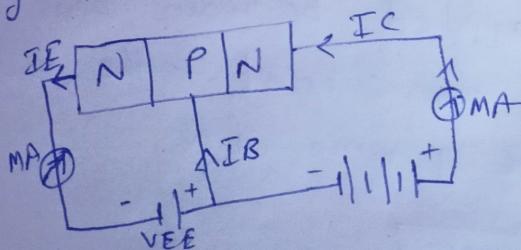
This constitutes the collector current I_C .

4) As each hole reaches the collector electrode, an electron is emitted from the +ve terminal of battery and neutralizes the hole. Now, a covalent bond near the emitter electrode breaks down. The liberated electron enters the +ve terminal of battery V_{EE} while the hole immediately of battery V_{EE} , while the hole immediately moves towards the emitter junction. This process is repeated again and again.

Operation of NPN transistor

The biasing of a NPN transistor is shown in below fig. The emitter junction is forward-biased because electrons are repelled from the -ve emitter.

battery terminal V_{EE} towards the junction. The collector junction is reverse biased because e^- are flowing away from the collector junction towards the +ve collector battery terminal V_{CC} .



The operation of NPN transistor is.

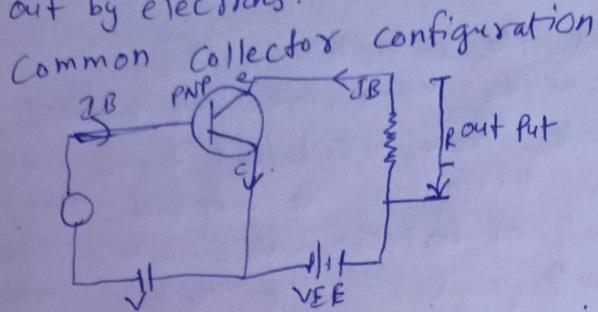
1) The electrons in the emitter region are repelled from the -ve terminal of battery towards the emitter junction since the potential barrier at the junction is reduced due to forward bias and base region is very thin and lightly doped, electrons cross the P-type base region.

2) A few electrons combine with the holes in P-region are lost as charge carriers.

3) Now the e^- in N-region (Collector region) readily swept up by the +ve Collector voltage V_{CC} .

4) For every electron flowing out the collector and entering the

+ve terminal of battery V_{CC} , an electron from the -ve emitter battery terminal enters the emitter region. In this way electron conduction takes place continuously so long as the two junctions are properly biased. So the current conducting in NPN transistor is carried out by electrons.



In this configuration the input signal is applied between base and collector and output is taken from the emitter.

→ As collector is common to input and output circuit hence the name as common collector configuration. The above circuit shows the common collector PNP transistor circuit.

Current Amplification factor (or) DC Current gain

(γ):

When no signal is applied between base and collector then the ratio of emitter current to the base current is called as DC gamma of a transistor

$$\gamma_{DC} = \gamma = \frac{I_E}{I_B} \rightarrow ①$$

AC current gain:

When signal is applied then the ratio of change in emitter current to the change in base current is known as AC current gain.

$$\gamma = \frac{\Delta I_E}{\Delta I_B} \rightarrow ②$$

Total emitter current:
we know that $I_E = I_B + I_C$
Also $I_C = \alpha I_E + I_{CBO}$

$$I_E = I_B + [\alpha I_E + I_{CBO}] \\ = I_B + \alpha I_E + I_{CBO}$$

$$I_E (1-\alpha) = I_B + I_{CBO}$$

$$I_E = \frac{I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha}$$

$$I_E = (1+\beta)I_B + (1+\beta)I_{CBO} \quad \left[\because \frac{1}{1-\alpha} = 1+\beta \right]$$

Relation between β and α

w. I_C . That

$$\beta = \frac{I_E}{I_B} \quad \& \quad \alpha = \frac{I_C}{I_E}$$

$$\text{Also } \beta = \frac{I_E}{I_E - I_C} : \frac{1}{1 - (I_C/I_E)} = \frac{1}{1-\alpha} \rightarrow \textcircled{4}$$

WE KNOW THE RELATION b/w β & α

$$\boxed{(1-\alpha) = \frac{1}{1+\beta}}$$

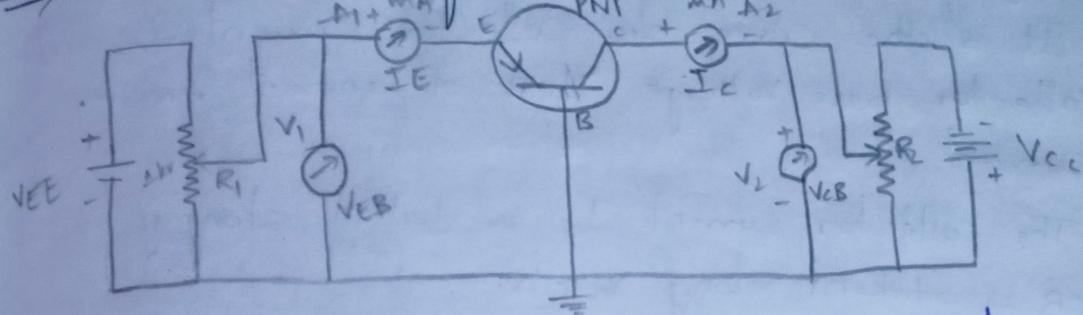
Substituting this value in eqn 4

$$\text{we have } \beta = \frac{1}{1-\alpha} = 1+\beta$$

$$\boxed{\frac{1}{1-\alpha} = 1+\beta}$$

Comparison of different characteristics in different configurations.

1/9/24 Characteristics of common base circuits:



If the base of the PNP or NPN transistor is connected to Ground then it is called as common base configuration.

→ Input characteristics:

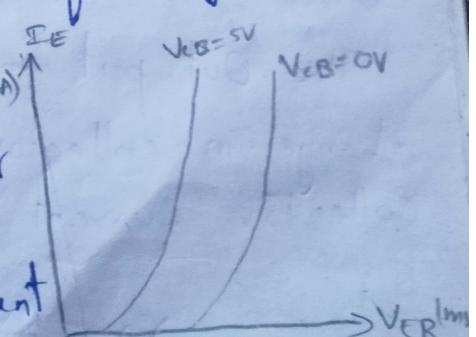
It is the curve b/w input voltage V_{EB} and input current I_E of constant collector base voltage.

The emitter current I_E is taken along y-axis and emitter base voltage along x-axis.

The junction b/w emitter and base is in forward bias and collector to base junction is in reverse bias.

The two terminals of BJT emitter and base acts as a PN junction diode. Then input characteristics of common base configuration is similar to forward bias of P-N junction diode.

Input resistance is defined (mA) as the ratio of change in emitter base voltage to the change in emitter base voltage at a constant collector base voltage.



i/p resistance

$$I_E = \text{const} = \frac{\Delta V_{EB}}{\Delta I_E} \quad | V_{CB} = \text{const}$$

It is the curve b/w collector current I_c and Collector base Voltage V_{CB} at constant emitter current

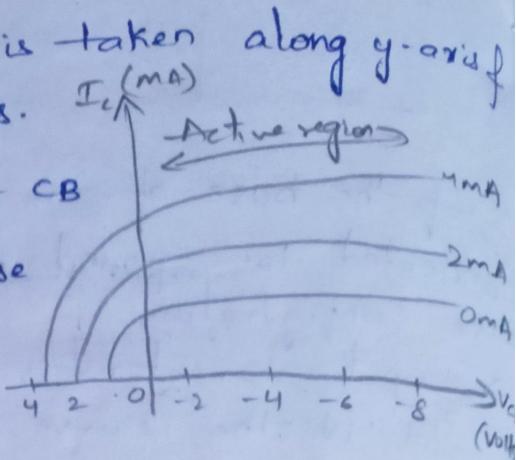
The collector current I_c is taken along y-axis if V_{CB} is taken along x-axis.

The output characteristics of CB configuration has three base regions.

1. Active region

2. Cut off region

3. Saturation region.



1. Active region :-

In the active region the emitter base junction is in forward bias while collector base junction is in reverse bias. In this region, collector current I_c is approximately equal to emitter current I_e so the transistor acts as an amplifier.

In the active region the collector current is almost constant, in output resistance.

The Out-put resistance is defined as the ratio of change in collector base Voltage to the change in collector current at a constant emitter current I_e .

$$r_o = \frac{\Delta V_{CB}}{\Delta I_c} \quad | I_e = \text{constant}$$

→ 2 Cutoff region:

The region below the curve $I_e = 0$ is known as Cutoff region, where I_c is nearly zero. and the

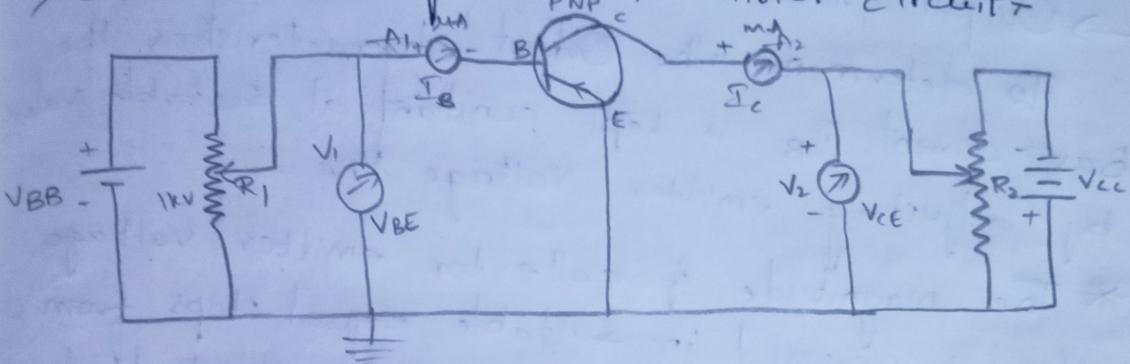
and
ex
ris f
1mA
2mA
0mA
 $\rightarrow V_{CB}$
(Volts)

Collector base junction and emitter base junction both are in reverse biased.

3. Saturation region:-

In this region emitter base junction and collector base junction both are in V_C decreases rapidly as V_{CB} becomes more negative.

→ Characteristics of common emitter circuit



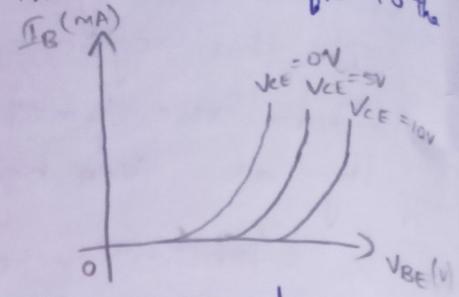
In CE configuration emitter is connected to ground, input is applied to base terminal and Output is taken across the collector terminal.

Input characteristics:

To determine the input characteristics the collector-to-emitter Voltage is kept constant and Base current is increased from '0' with equal steps by increasing V_{CE} the circuit diagram of CE configuration is shown in above fig.

The Value of V_{BE} and I_B are noted for fixed values of V_{CE} . When $V_{CE} = 0V$ the Base-emitter junction is forward Biased and junction behave as forward biased diode. Hence the input characteristic for $V_{CE} = 0$ is similar to that of forward Biased diode when V_{CE} is increased the width of the depletion region at the reverse biased collector base junction will increase.

Hence the effective width of Base will decrease
this effect causes decreases in the Base Current
 I_B therefore for $V_{CE} > 0V$ the curve shifts to the right as V_{CE} increases.



→ Output characteristics →

To determine the Output characteristics the Base current I_B is kept constant at suitable value by DC by adjusting emitter voltage V_{BE} .

* The magnitude of collector emitter voltage V_{CE} is increased in suitable equal steps from 0 and the Collector current (I_c) is noted for each settings of V_{CE} .

The output characteristics of CE configuration consist of 3 regions

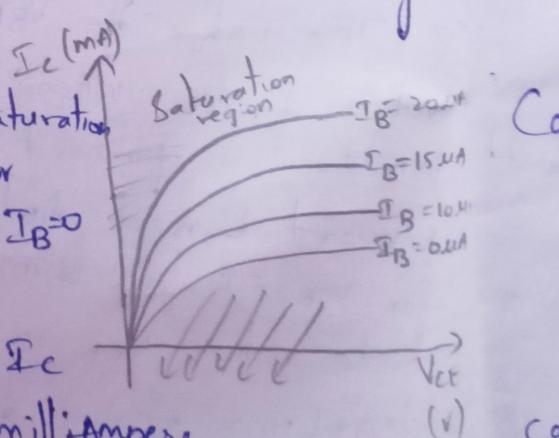
1) Active region 2) Saturation region 3) cut-off region.

* Under saturation region the collector current is almost constant with I_B but the current in milli ampere.

* Under saturation regions means both junctions are in forward bias that current I_c linearly increases with V_{CE}

* When $V_{CE} = 0$ small reverse saturation current flows between collector to emitter terminal even if $I_B = 0$ micro ampere

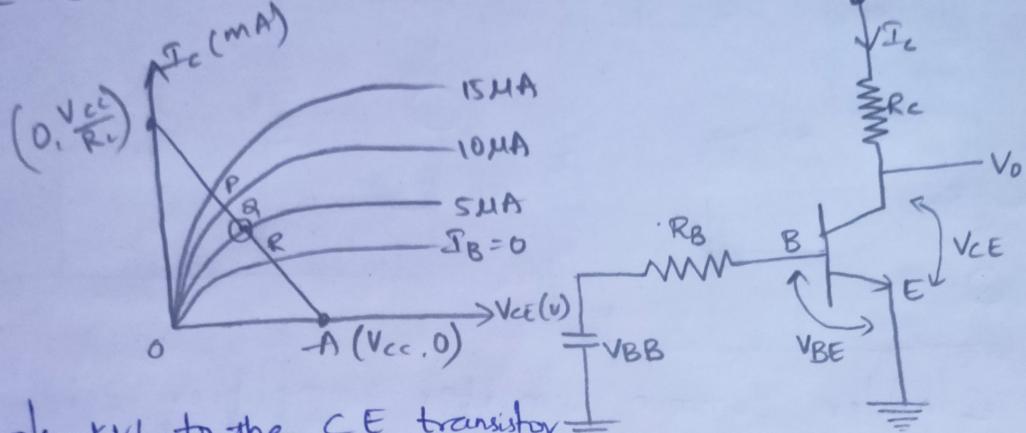
* At different values of I_B the I_c current shifts its level in milliAmpere



→ Biasing:-

In amplifier circuit - the Output Signal power is always greater than - the input Signal power. Here the dc Source supplies the power to the transistor circuit to get the Output Signal power greater than the input Signal power. The biasing is needed to operate the transistor in desired region and to work as an amplifier.

* DC Load line :-



- Apply KVL to the CE transistor

$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CC} - V_{CE} = I_C R_C$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C}$$

$$I_C = -\left(\frac{1}{R_C}\right)V_{CE} + \frac{V_{CC}}{R_C}$$

By comparing with $y = mx + c$

I_C Versus V_{CE} with slope $\left(-\frac{1}{R_C}\right)$

Case(i) :- When $I_C = 0$

$$\frac{V_{CC} - V_{CE}}{R_C} = 0 \Rightarrow V_{CC} - V_{CE} = 0$$

$$\Rightarrow V_{CC} = V_{CE}$$

Now coordinate can be represented as $A(V_{CC}, 0)$

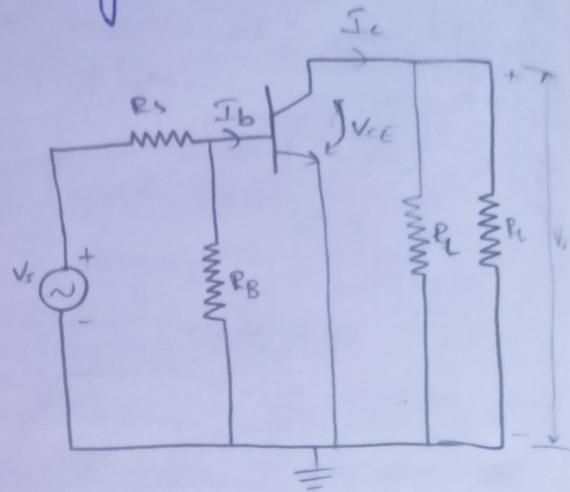
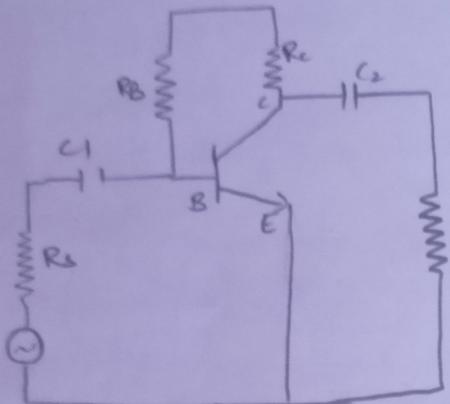
Case(ii) :- When $V_{CC} = 0 \Rightarrow I_C = \frac{V_{CC}}{R_C}$

Now coordinate can be represented as $B(0, \frac{V_{CC}}{R_C})$.

With the help of A & B coordinates a straight line can be drawn on output characteristics. If case attaches to the output current line is known as 'dc' load line.

The points are called as Q points (Operating points) and represented by PQR.

→ AC load line :-



Consider common emitter amplifier circuit with capacitors C_1 and C_2 and different resistors such as R_s , R_b and R_L shown in figure. For

-AC analysis the capacitors are short circuits and dc supply source is connected to ground

from the above circuit the equivalent resistance

$$R_{ac} = \frac{R_c R_L}{R_c + R_L}$$

$$\text{The Output Voltage } V_{CE} = I_c R_{ac}$$

$$P_c = \frac{V_{CE}}{R_{ac}}$$

From the characteristics the collector current should be lies in b/w Saturation and cutoff regions.

∴ with the help of transistor operating voltage of currents
The current can be written as

$$I_c = \frac{V_{CEO}}{R_{ac}} - \frac{V_{CE}}{R_{ac}} + I_{cq}$$

Case(i) : When $V_{CE} = 0$

$$I_C = \frac{V_{CEQ}}{R_{AC}} + I_{CQ}$$

Coordinate can be represented as $A(0, \frac{V_{CEQ}}{R_{AC}} + I_{CQ})$

Case(ii) : When $I_C = 0$

$$0 = \frac{V_{CEQ}}{R_{AC}} - \frac{V_{CE}}{R_{AC}} + I_{CQ}$$

$$\frac{V_{CE}}{R_{AC}} = \frac{V_{CEQ}}{R_{AC}} + I_{CQ}$$

$$V_{CE} = R_{AC} \left(\frac{V_{CEQ}}{R_{AC}} \right) + I_{CQ}$$

$$V_{CE} = V_{CEQ} + I_{CQ} R_{AC}$$

Now coordinate can be represented as

$$B(V_{CEQ} + I_{CQ} R_{AC}, 0)$$

With the help of above two coordinates A & B a straight can be drawn on CE output characteristics and it touches different points with the line which is called as ac load line

* The common point b/w dc & ac load line is called operating point or Q-point or ~~Q~~ point of the transistor.

* The Output power which is delivered with ac load line analysis is given by $P = V_{CEQ} I_{CQ}$

→ stability :

One more source of biasing is used in stability to be consider due to the variation of input voltage to establish the operating point in active region.

Their are two techniques.

1. Stabilization and 2. Compensation technique

1. Stabilization technique:

This technique consists of resistive components which permits the variation in input current I_B to maintain I_C almost constant.

2. Compensation technique:

In this technique sensitive devices such as diodes, transistors and thermistors are used. These devices produce compensating voltage or currents in such a way that the operating point should be maintained stable.

→ Stability factors:

There are three stability factors. Such as S, S' , S'' .

* Stability factor 'S':-

It is defined as the ratio of change in collector current to the change in reverse saturation current I_{CBO} or I_{CO} by keeping ' β ' and V_{BE} constant.

$$S = \frac{\Delta I_C}{\Delta I_{CO}} \quad | \text{ where } V_{BE}, \beta \text{ are constant}$$

* Stability factor "S'":

It is defined as the ratio of change in collector current to the change in base to emitter voltage by keeping I_{CO} and β constant.

$$S' = \frac{\Delta I_C}{\Delta V_{BE}} \quad | \text{ where } I_{CO} \text{ & } \beta \text{ constant}$$

* Stability factor "S'':

It is defined as the ratio of change in collector current to the change in ' β ' by keeping I_{CO} & V_{BE} constant.

$$S'' = \frac{\Delta I_C}{\Delta \beta} \quad | \text{ where } V_{BE} \text{ & } I_{CO} \text{ constant}$$

Q9/2 Advantages and disadvantages of fixed bias

Circuit: Advantages:-

1. It is a simple circuit
2. Maximum flexibility due to changes in operating point in the active region.

Disadvantages :-

1. Thermal stability is not provided by this circuit

$$\text{Since } I_c = \beta I_B + (1 + \beta) I_{Co}$$

2. Stability factor depends on ' β ' $\therefore S = 1 + \beta$

Therefore, β may change from one transistor to another transistor and $I_c = \beta I_B$ therefore, I_c changes this will shift the operating bias point hence stabilization of fixed bias circuits is

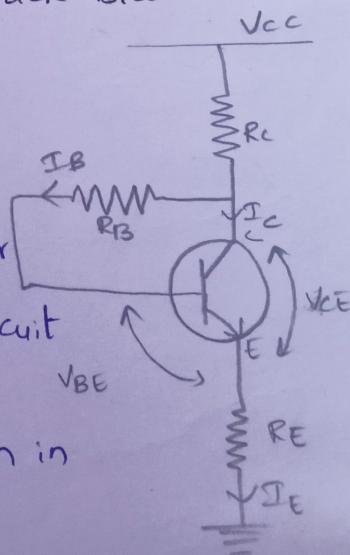
Very poor

→ Collector to emitter feedback bias.

$$S = \frac{1 + \beta}{1 - \beta \left(\frac{\partial I_B}{\partial I_c} \right)}$$

$S = 1$

It is also called as collector to base with emitter bias circuit and diagram of collector to emitter feedback bias is shown in above figure



→ Apply KVL to the base emitter loop.

$$Vcc - (I_B + I_c)R_c - I_B R_B - V_{BE} - I_E R_E = 0$$

$$Vcc - V_{BE} = I_B R_c + I_c R_c + I_B R_B + I_E R_E$$

$$Vcc - V_{BE} = I_B R_c + \beta I_B R_c + I_B R_B + (I_B + I_c) R_E$$

$$Vcc - V_{BE} = I_B (R_c + \beta R_c + R_B + R_E) + I_c R_E$$

$$V_{CC} - V_{BE} - I_c R_E = \frac{I_B}{\beta} (R_B + R_E + R_C(1+\beta))$$

$$\frac{V_{CC} - V_{BE} - I_c R_E}{R_B + R_E + R_C(1+\beta)} = \frac{I_B}{\beta}$$

$$V_{CC} - V_{BE} = \frac{I_B}{\beta} (R_C + \beta R_C + R_B + R_E) + \beta I_B R_E$$

$$V_{CC} - V_{BE} = I_B (R_C + \beta R_C + R_B + R_E + \beta R_E)$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_C(1+\beta) + R_E(1+\beta) + R_B}$$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B + (R_C + R_E)(1+\beta)}$$

Stability factor S for collector to Emitter bias circuit

- Apply KVL to collector to base emitter loop.

$$V_{CC} - (I_B + I_c) R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{CC} - V_{BE} = (I_B + I_c) R_C + I_B R_B + I_E R_E$$

$$V_{CC} - V_{BE} = I_B R_C + I_c R_C + I_B R_B + (I_B + I_c) R_E$$

$$V_{CC} - V_{BE} = I_B R_C + I_c R_C + I_B R_B + I_B R_E + I_c R_C$$

$$V_{CC} - V_{BE} = I_B [R_E + R_B + R_C] + I_c [R_E + R_B + R_C]$$

$$V_{CC} - V_{BE} - I_c (R_E + R_C) = I_B (R_E + R_B + R_C)$$

$$I_B = \frac{V_{CC} - V_{BE} - I_c (R_E + R_C)}{R_E + R_B + R_C}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_E + R_B + R_C} - \frac{I_c (R_E + R_C)}{R_E + R_B + R_C}$$

Differentiate w.r.t I_c .

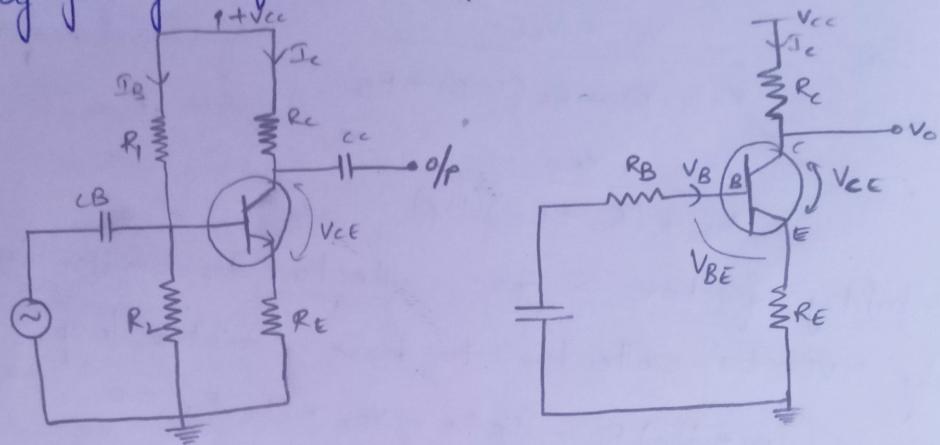
$$\frac{\partial I_B}{\partial I_c} = \frac{\partial}{\partial I_c} \left(\frac{V_{CC} - V_{BE}}{R_E + R_B + R_C} \right) - \frac{\partial}{\partial I_c} \left(\frac{I_c (R_E + R_C)}{R_E + R_B + R_C} \right)$$

$$\frac{\partial I_B}{\partial I_c} = 0 - \frac{\partial}{\partial I_c} \left(\frac{R_E + R_C}{R_E + R_B + R_C} \right) = - \left[\frac{R_E + R_C}{(R_E + R_B + R_C)^2} \right]$$

$$S = \frac{1+\beta}{1-\beta \left(\frac{\partial I_B}{\partial I_c} \right)} \Rightarrow S = \frac{1+\beta}{1+\beta \left(\frac{R_E + R_C}{R_E + R_B + R_C} \right)} //$$

→ Voltage divider bias:-

It is also called as self bias, in this circuit the biasing is provided by three resistors R_1 , R_2 & R_E . The R_1 , R_2 resistors are providing potential divider by giving a fixed voltage with its base.



From the circuit, base resistance R_B is the parallel combination of R_1 & R_2 . Therefore $R_B = \frac{R_1 R_2}{R_1 + R_2}$

The base voltage of the above circuit is equal to the Thévenin's voltage. $V_B = V_{th} = \frac{R_2}{R_1 + R_2} \times V_{cc}$

Apply KVL to collector to emitter loop.

$$V_{cc} - I_c R_C - V_{CE} - I_E R_E = 0$$

$$V_{cc} - I_c R_C - V_{CE} - (I_c - I_B) R_E = 0$$

$$V_{cc} - I_c R_C - V_{CE} - I_B R_E - I_c R_E = 0$$

$$V_{cc} = I_B R_E + I_c (R_C + R_E) + V_{CE}$$

Apply KVL to the base emitter loop.

$$V_{th} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{th} - I_B R_B - V_{BE} - (I_B + I_c) R_E = 0$$

$$V_{th} - I_B R_B - V_{BE} - I_B R_E - I_c R_E = 0$$

$$V_{th} - V_{BE} - I_c R_E = I_B (R_E + R_B)$$

$$I_B = \frac{V_{th} - V_{BE} - I_c R_E}{R_B + R_E}$$

Stability factor (s) for self bias:-

Apply KVL to the Base emitter loop.

$$V_{th} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{th} = I_B R_B + V_{BE} + I_E R_E$$

$$V_{th} = I_B R_B + V_{BE} + I_E R_E$$

$$V_{th} = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$$V_{th} = I_B R_B + V_{BE} + I_B R_E + I_C R_E$$

Diffr w.r.t to I_C

$$\frac{\partial}{\partial I_C} V_{th} = \frac{\partial}{\partial I_C} I_B R_B + \frac{\partial}{\partial I_C} V_{BE} + \frac{\partial}{\partial I_C} I_B R_E + \frac{\partial}{\partial I_C} I_C R_E$$

$$0 = \frac{\partial I_B}{\partial I_C} R_B + 0 + \frac{\partial I_B}{\partial I_C} R_E + R_E$$

$$0 = \frac{\partial I_B}{\partial I_C} (R_B + R_E) + R_E$$

$$-R_E = \frac{\partial I_B}{\partial I_C} (R_B + R_E) \Rightarrow \frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_B + R_E}$$

$$\Rightarrow s = \frac{1+\beta}{1-\beta \left(\frac{\partial I_B}{\partial I_C} \right)} = \frac{1+\beta}{1-\beta \left(\frac{-R_E}{R_B + R_E} \right)} = \frac{1+\beta}{1+\beta \left(\frac{R_E}{R_B + R_E} \right)}$$

$$= \frac{1+\beta}{1+\beta \left(\frac{R_E}{R_B + R_E} \right)} \Rightarrow \frac{1+\beta}{1+\beta \left(\frac{R_E}{R_E / (1 + \frac{R_E}{R_B})} \right)} = \frac{1+\beta}{1+\beta(1)} \frac{R_B}{R_E} \quad \text{cancel } 1+\beta$$