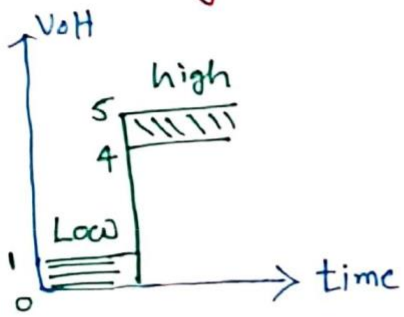
Digital Logic Families

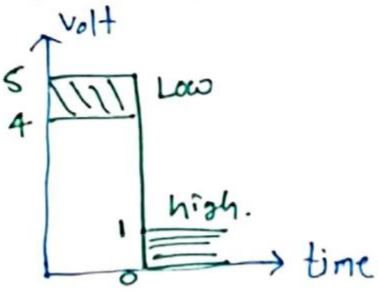
→ A group of compatible IC's with same logic levels and supply voltages fabricated for performing varies logical functions referred as a logic family.

- two types of logic levels

Positive logic

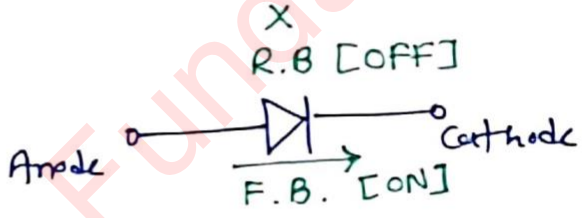


Negative logic

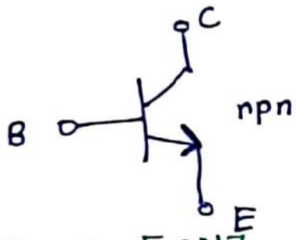


Logical functions
- NOT, OR, NOR, AND, NAND, XOR and XNOR.

- Semiconductor devices



- Bipolar [Charge Carriers are e^- & holes]
- Unipolar [One type of charge carrier e^- or holes.]



B = V_{cc} [ON]
B = 0 [OFF]

Digital Logic Families

Bipolar Logic Families
[It uses e^- & holes as Charge Carrier.]
- [Resistor, transistor & Diodes]

Saturated [devices will be ON or OFF.]
- ON → Saturation region
- OFF → Cut OFF region

eg, RTL, DTL, DCTL, I^2L, HTL, TTL.

Non-Saturated [devices will be used in active region.]
e.g. Schottky TTL, ECL.

Unipolar Logic Families
[It uses one type charge carrier e^- or holes.]
- [MOS]
  - pMOS, nMOS, CMOS

Bi CMOS Logic Families.
MOS → Bipolar
BiCMOS
- → I/p & logical Oper.n [CMOS]
- → O/p [Bipolar] [MOS]

Merits, Demerits and characteristics of digital IC.

Merits

- It reduces overall size of the system.
- It reduces overall cost of the system.
- It improves reliability of the system, by reducing interconnection of wiring.
- It reduces power consuption of the system.

Demerits

- It can not handle large power.
- Electrical device like resistors, inductors, transformer & large capacitor can not be implemented with great precision on chip.
- They are suitable for low power applications.

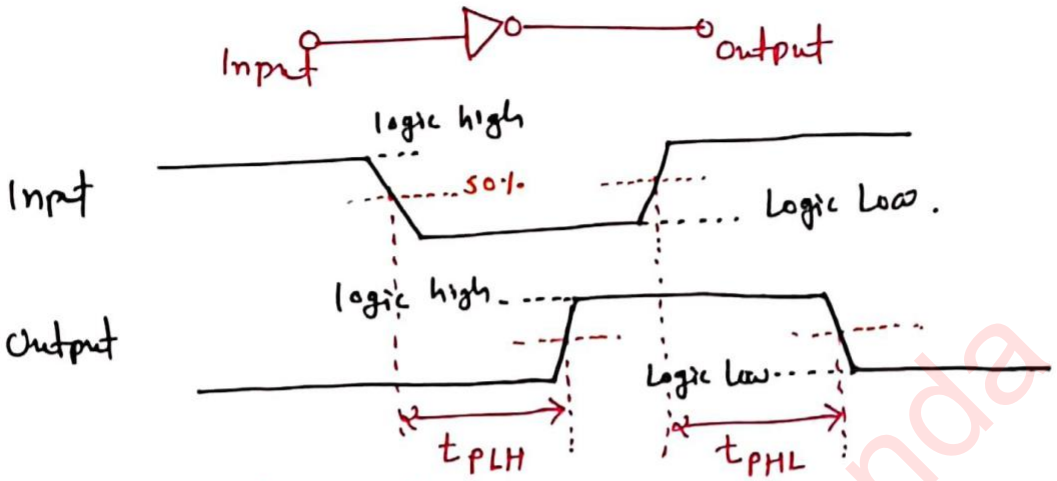
Characteristics

1. Propagation delay
2. Threshold Voltage.
3. Power dissipation
4. Figure of merit
5. Fan out and Fan in
6. Noise immunity
7. Operating Temp.
8. Voltage and current parameters.

Characteristics of digital IC

1] Propagation Delay & Threshold Voltage

- It is average transition time of signal from I/p to O/p.
- It defines operating speed of IC.
- It is measured in terms of nsec.



$$\rightarrow t_p = \frac{t_{PLH} + t_{PHL}}{2}$$

where, t_{PLH} = delay with O/p goes from Low to high

t_{PHL} = delay with O/p goes from high to low

ex ⇒ $t_{PLH} = 5$ nsec

$t_{PHL} = 7$ nsec

$t_p = \frac{5+7}{2} = 6$ nsec

2] Power dissipation of IC

- It is the amount of power dissipated in an IC in form of heat.
- Total power dissipation

$$P_d = V_{cc} \times I_{cc(avg)}$$

- where, $I_{cc} = \frac{I_{ccH} + I_{ccL}}{2}$
- Power dissipation per logic gates

$$P_{dn} = \frac{V_{cc} \times I_{cc(avg)}}{n}$$

- Supply Voltage
  - V_{cc} → TTL
  - V_{DD} → CMOS

eg: $V_{cc} = 5$ V, $I_{ccH} = 0.5$ mA, $I_{ccL} = 1$ mA, $P_d = ?$

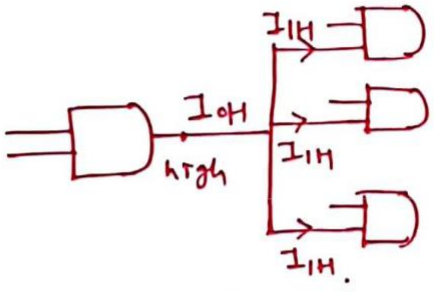
- $I_{cc} = \frac{I_{ccH} + I_{ccL}}{2} = \frac{1.5}{2} = 0.75$ mA
- $P_d = I_{cc} V_{cc} = 5 \times 0.75 = 3.75$ mW

3] Figure of Merit

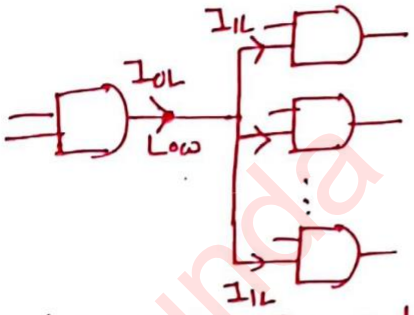
Figure of Merit = propagation delay x power dissipation.

Characteristics of digital IC

- **Fan Out**
  - No of similar gates can be driven by a gate without imparing normal operation of given circuit is **Fan Out**
  - It should be as high as possible, so that we can drive Large number of gates by single gate.
  - It defines current supply by given gate.

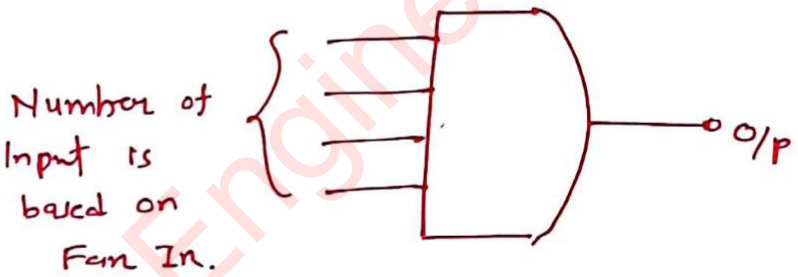


- high state Fan out $= \frac{I_{OH}(max)}{I_{IH}}$



- Low state Fan out $= \frac{I_{OL}(max)}{I_{IL}}$

- **Fan In**
  - Fan In of Logic gate is defined as the number of inputs that the gate is designed to handle.

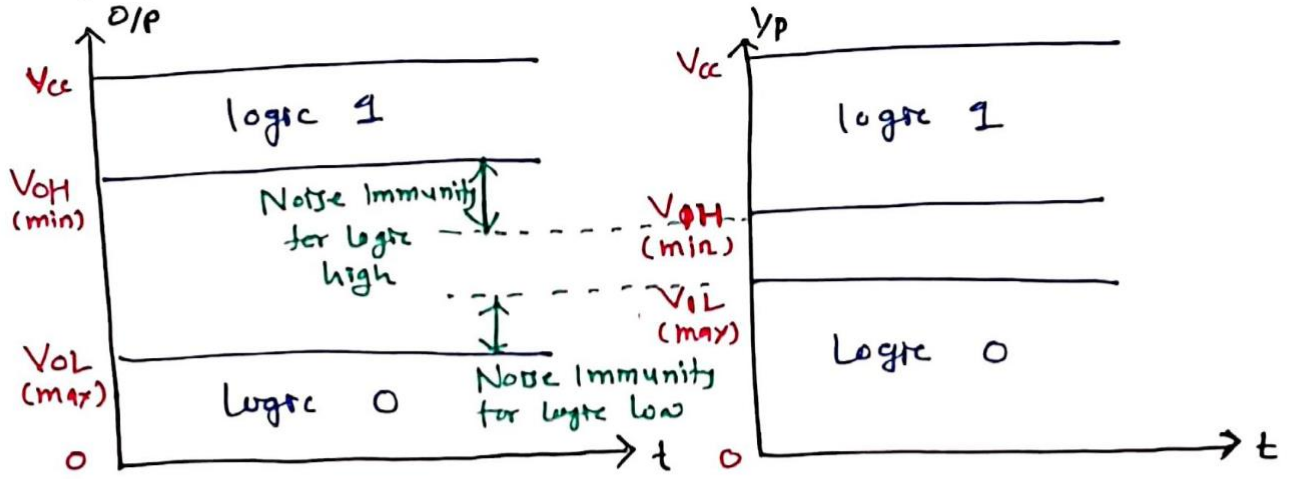


Operating Temp.

- For Commercial applications [0 to 70°C]
- For Industrial applications [0 to 85°C]
- For Military applications [-55°C to 125°C].

Characteristics of digital IC

Voltage and Current Parameters



$V_{OH(min)}$ — It is min o/p volt for logic 1

$V_{OL(max)}$ — It is max o/p volt for logic 0

$V_{IH(min)}$ — It is min Vp volt for logic 1

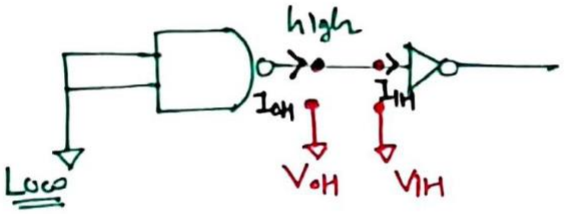
$V_{IL(max)}$ — It is max Vp volt for logic 0

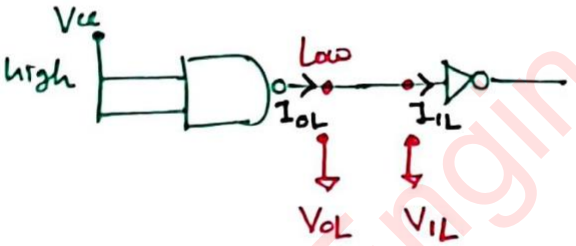
I_{OH} → high Level o/p current

I_{OL} → Low Level o/p current

I_{IH} → high Level Vp current

I_{IL} → Low Level Vp current





→ Noise margin

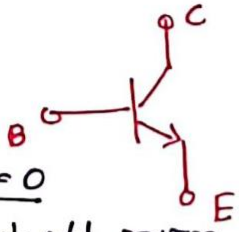
$NM_H = V_{OH} - V_{IH}$

$NM_L = V_{IL} - V_{OL}$

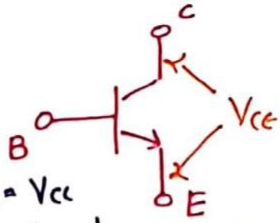
Resistor Transistor Logic [RTL]

→ This logic family includes resistors and transistors in it's Integrated Circuit. so, it is refferred as RTL family.

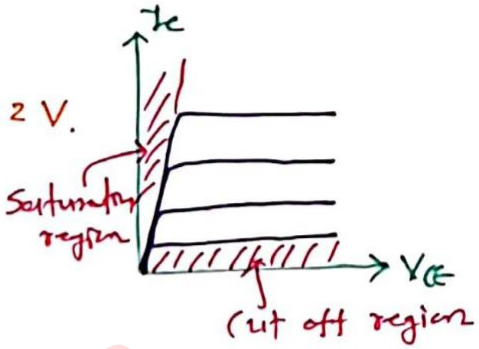
→ Here we use transistor in saturation and cut off region. so, speed of this logic family is low.

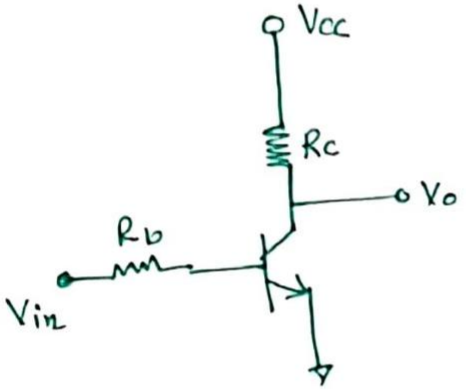


- B = 0
- Cut off region
- C to E terminal act like Open Circuit.

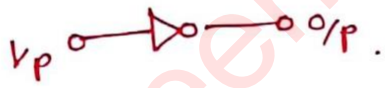


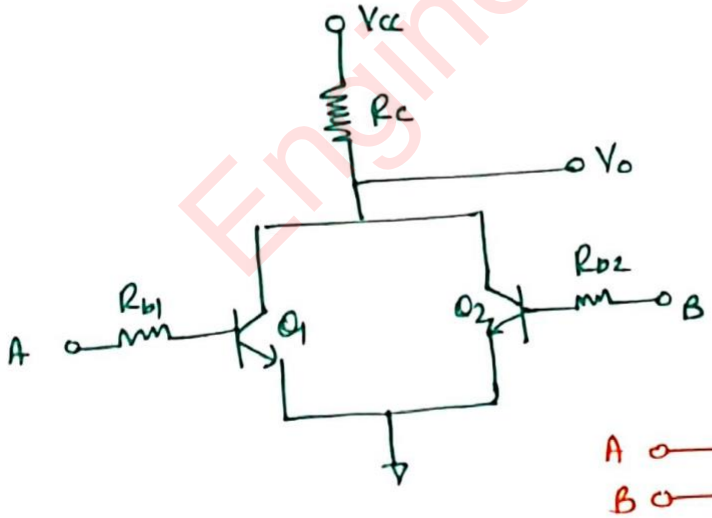
- B = Vcc
- Saturation region
- C to E current will flow.



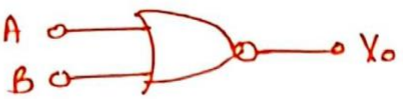


I/p	O/p	Transistor region
Low	high	Cut off [0.C]
high	Low	Sat. [V_{CE} = 0.2 V]





A	B	Vo
Low	Low	high
Low	high	Low
high	Low	Low
high	high	Low

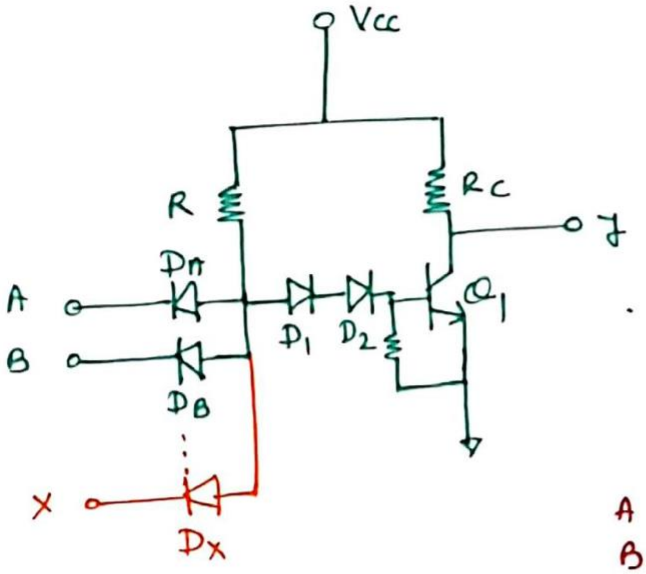


Disadvantages

- Low Noise margin
- Low fan out
- Low speed
- high power dissipation

Diode Transistor Logic [DTL]

- RTL families has low NM, low fan out, slow speed & higher power dissipation. so, we don't use RTL in recent IC's.
- DTL has improved NM and fan out compared to RTL.



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Disadvantage
- Low Speed
- power dissipation.

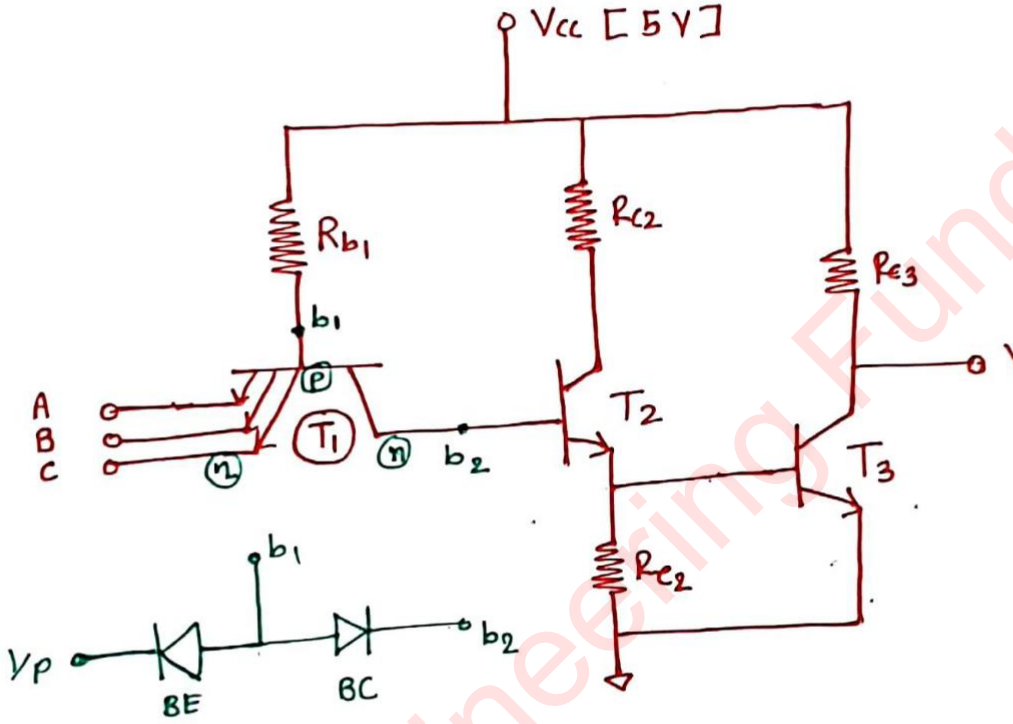
Transistor Transistor Logic (TTL)

TTL Classifications

- Standard TTL
- TTL totempole Output
- TTL Open Collector Output
- TTL Tristate.

- TTL offers higher speed compared to RTL and DTL

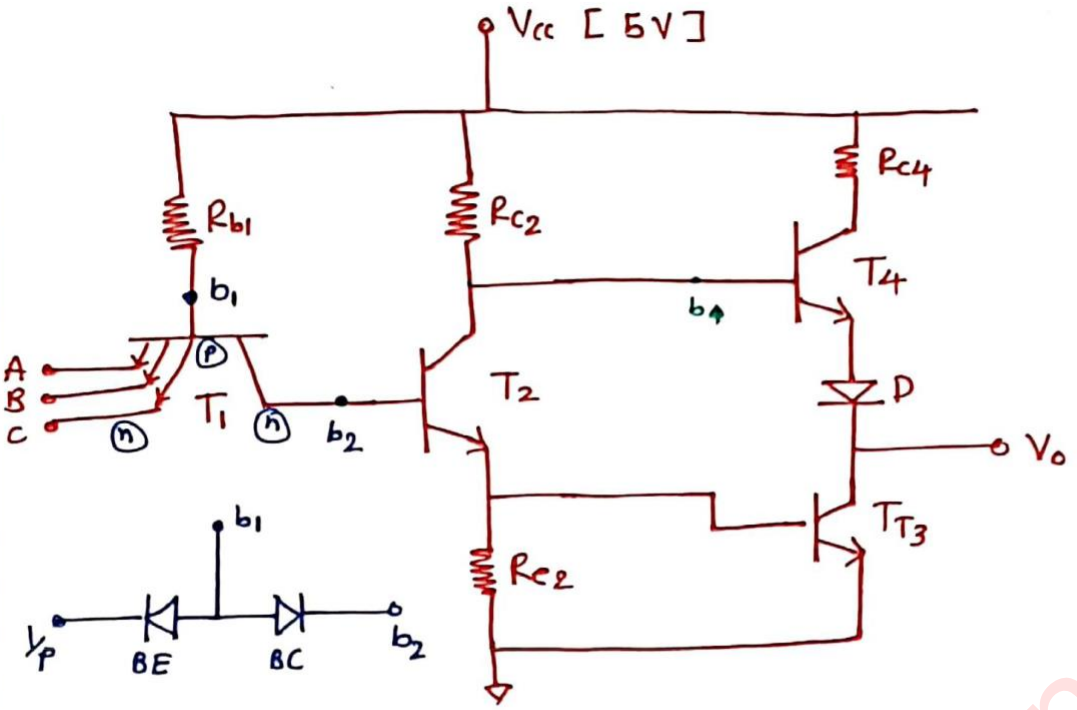
TTL NAND Circuit



A	B	C	Vo
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

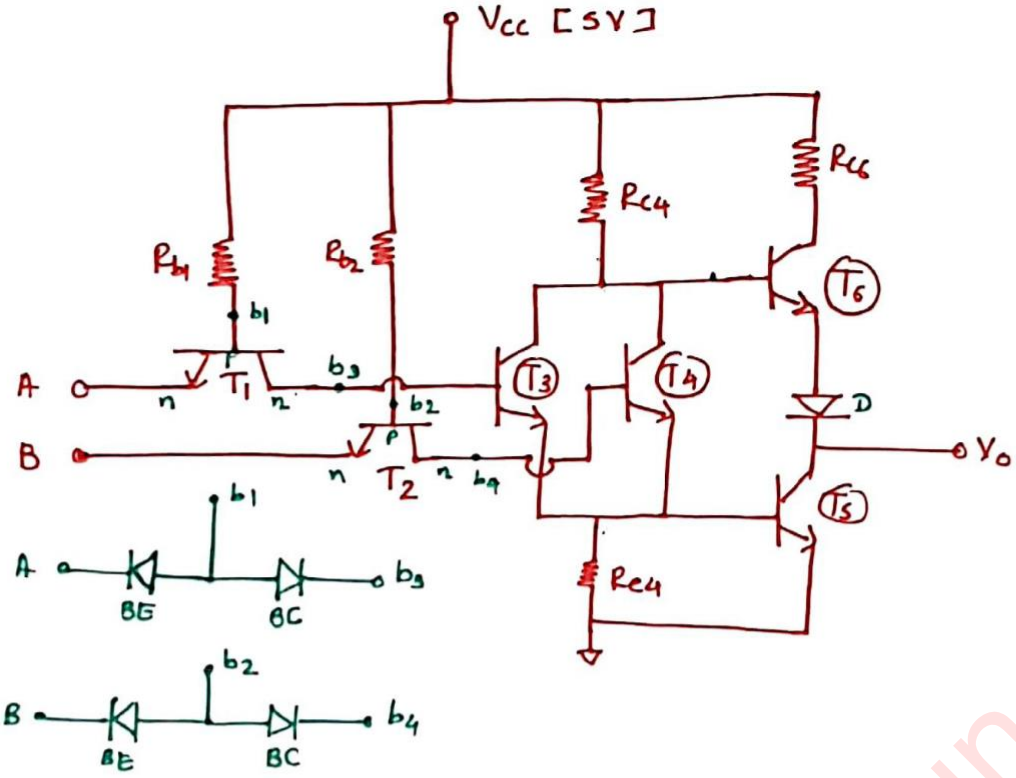
TTL NAND gate

TTL NAND gate with Totem pole Output



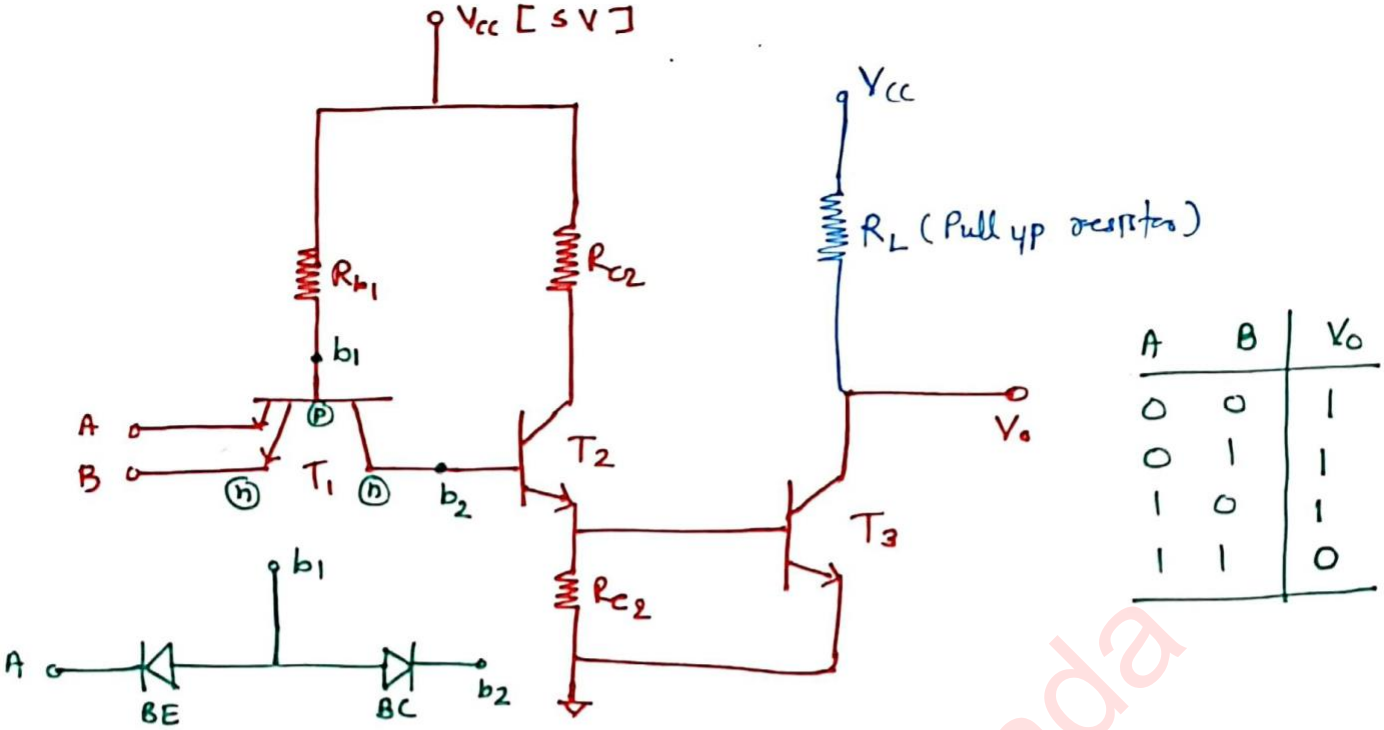
A	B	C	V_o
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

TTL NOR gate using Totempole.



A	B	Y_0
0	0	1
0	1	0
1	0	0
1	1	0

TTL Oprn Collector NAND gate



A	B	V_o
0	0	1
0	1	1
1	0	1
1	1	0

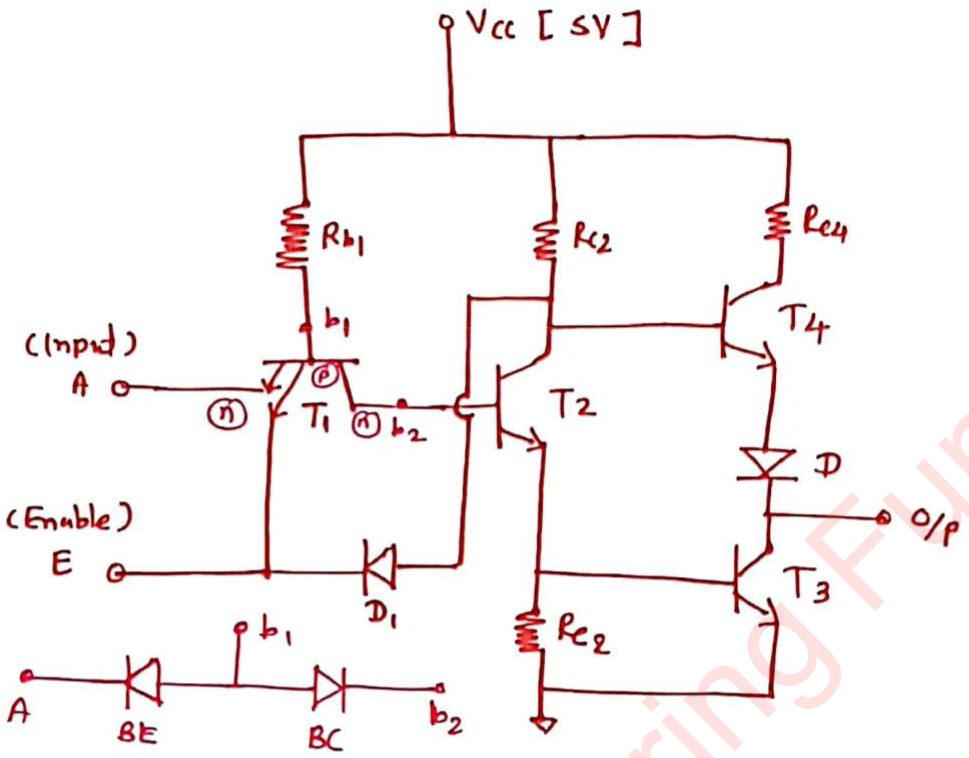
TTL tristate Logic

- In tristate at o/p we have three state

1] Logic high

2] Logic Low

3] High Impedance state.



→ E = 0 , high Impedance

→ E = 1, A = 0 } o/p = logic 1

→ E = 1, A = 1 } o/p = logic 0