Combinational & Sequential Circuit

Digital Electronics

Combinational Circuit

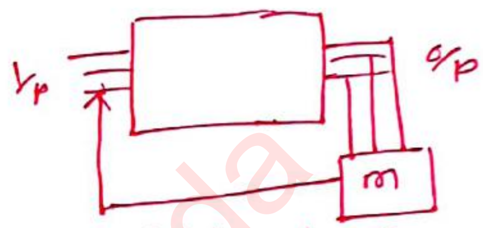
→ O/p is only depending on present I/p.

- No Feedback
- No memory

Eg - HA / FA
- HS / FS
- mux / Demux
- Encoder / Decoder
- Code Converter.

Sequential Circuit

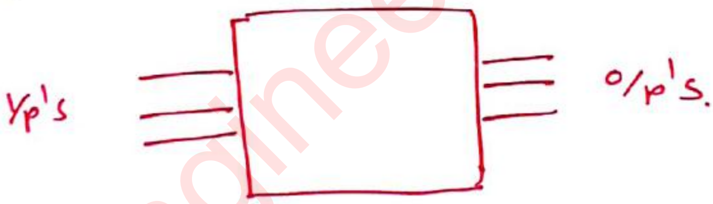
→ O/p is depending on present I/p and past O/p.



Posibility of memory & feedback.

Eg. - Counter
- Shift register
- Flip Flop.

- Designing of combinational Circuits.



Step-1 - Determine & Define total I/p's and total O/p's of the circuit.

Step-2 - Make truth table that defines relationship in bet.^{n} I/p's and O/p's.

Step-3 - Determine boolean eq.^{n} using K-map.

Step-4 - Based on boolean eq.^{n}, we can form circuit.

Combinational Circuit designing example

The minimal function that can detect "divisible by 2" with 8421 BCD [$D_8 D_4 D_2 D_1$] is given by $\boxed{\overline{D_1}}$

	D_8	D_4	D_2	D_1	Y
0 –	0	0	0	0	1
1 –	0	0	0	1	0
2 –	0	0	1	0	1
3 –	0	0	1	1	0
4 –	0	1	0	0	1
5 –	0	1	0	1	0
6 –	0	1	1	0	1
7 –	0	1	1	1	0
8 –	1	0	0	0	1
9 –	1	0	0	1	0
10 –	1	0	1	0	X
⋮			⋮		⋮
15 –	1	1	1	1	X

Y

D_2D_1 \ D_8D_4	00	01	11	10
00	1_0	1_4	X_{12}	1_8
01	0_1	0_5	X_{13}	0_9
11	0_3	0_7	X_{15}	X_{11}
10	1_2	1_6	X_{14}	X_{10}

$\boxed{\overline{D_1}}$

The minimal function that can detect "divisible by 3" with 8421 BCD [$D_8 D_4 D_2 D_1$] is given by ______

$$\boxed{Y = D_1 D_8 + \overline{D_1} D_2 D_4 + D_1 D_2 \overline{D_4} + \overline{D_1}\,\overline{D_2}\,\overline{D_4}\,\overline{D_8}}$$

	D_8	D_4	D_2	D_1	Y
0 –	0	0	0	0	1
1 –	0	0	0	1	0
2 –	0	0	1	0	0
3 –	0	0	1	1	1
4 –	0	1	0	0	0
5 –	0	1	0	1	0
6 –	0	1	1	0	1
7 –	0	1	1	1	0
8 –	1	0	0	0	0
9 –	1	0	0	1	1
10 –	1	0	1	0	X
⋮			⋮		⋮
15 –	1	1	1	1	X

Y

D_2D_1 \ D_8D_4	00	01	11	10
00	1_0	0_4	X_{12}	0_8
01	0_1	0_5	X_{13}	1_9
11	1_3	0_7	X_{15}	X_{11}
10	0_2	1_6	X_{14}	X_{10}

IV ($\overline{D_1}\,\overline{D_2}\,\overline{D_4}\,\overline{D_8}$)

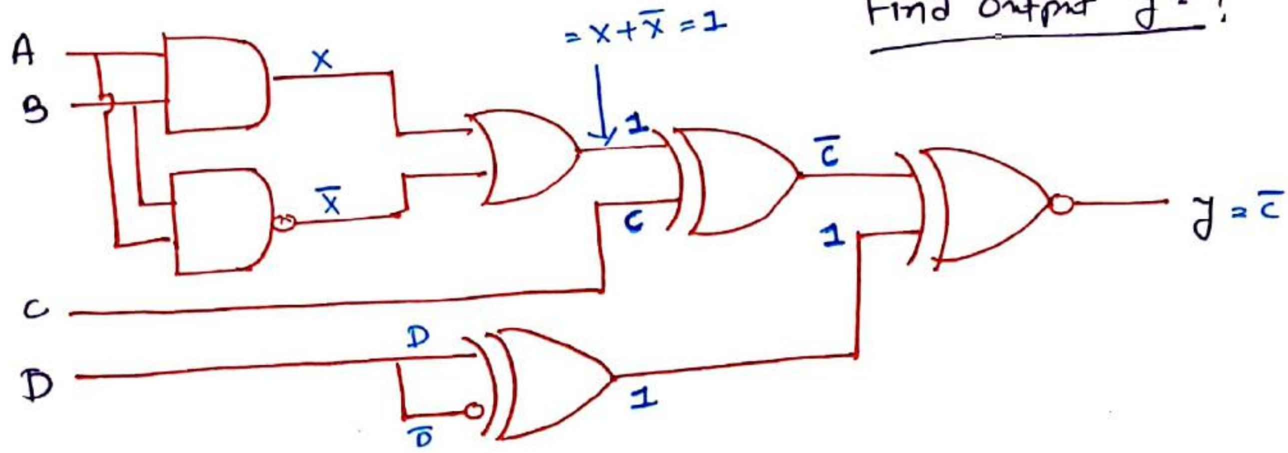
I ($D_8 D_1$)

III ($D_1 D_2 \overline{D_4}$)

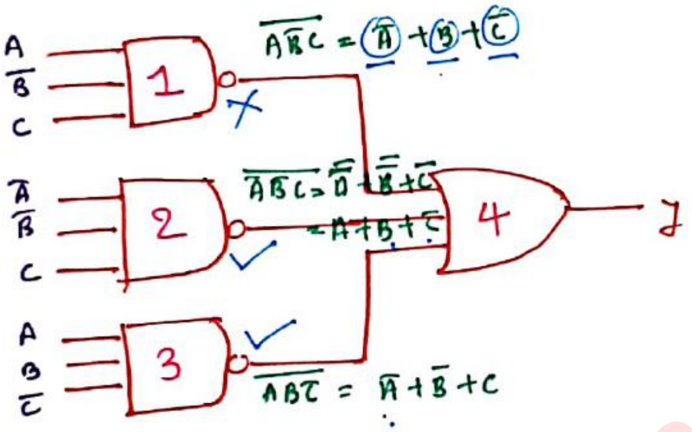
II ($D_2 \overline{D_1} D_4$)

Combinational Circuit Examples. 85

1) Find output y = ?

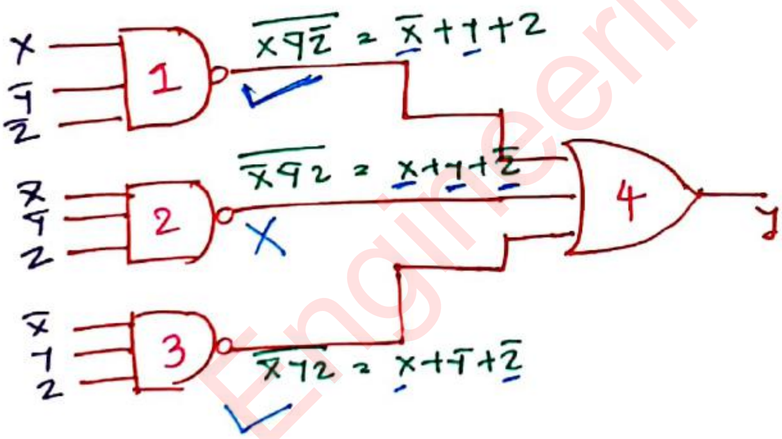


2)



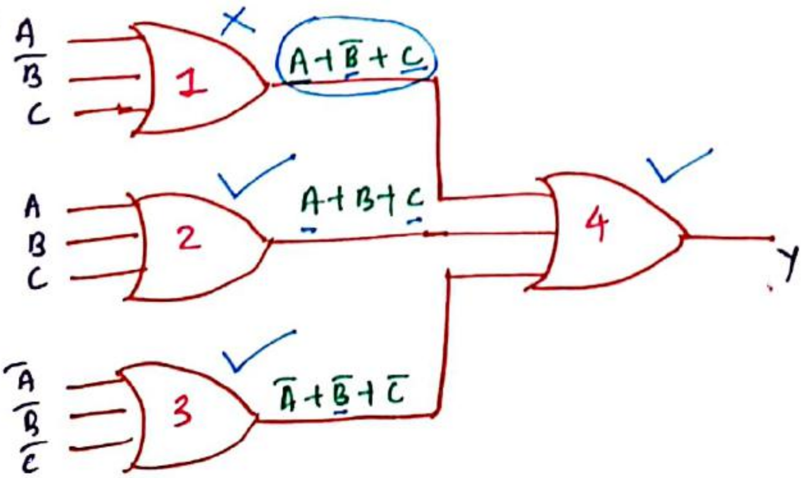
what is redundant gate in given combinational circuit ?

3)



what is redundant gate in given combinational circuit ?

4)



what is redundant gate in given combinational circuit ?

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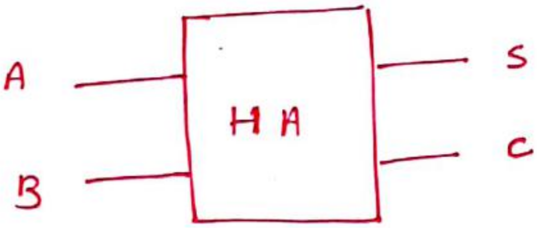
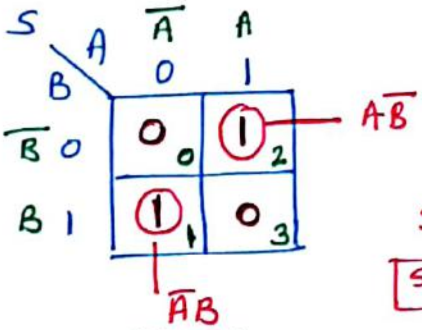
HALF ADDER 86

→ Half Adder we perform two bit addition.

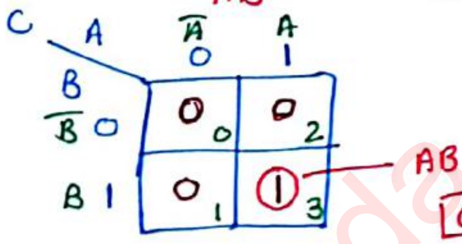




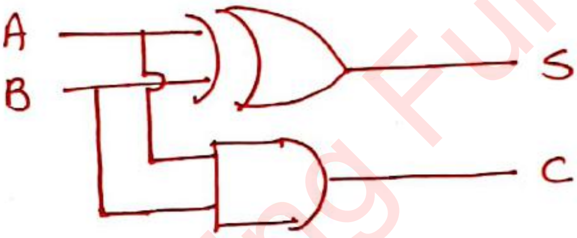
$S = A\bar{B} + \bar{A}B$

$\boxed{S = A \oplus B}$

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



$\boxed{C = A.B}$



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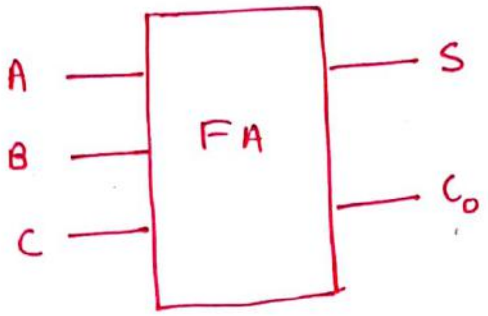
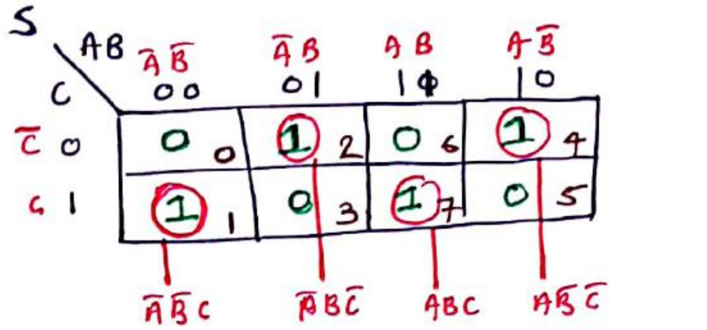
Full Adder 87

- Full Adder Circuit is used to perform 3 bits addition.



A	B	C	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



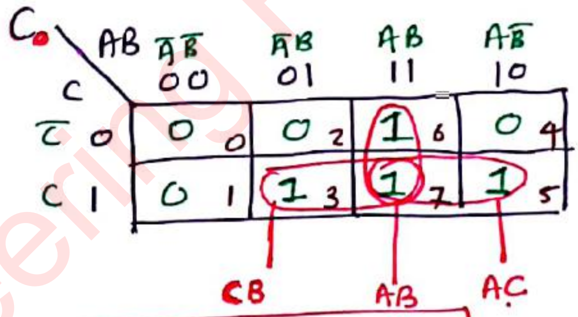
$$\rightarrow S = \bar{A}\bar{B}C + \bar{A}B\bar{C} + ABC + A\bar{B}\bar{C}$$

$$= \bar{A}(\bar{B}C + B\bar{C}) + A(BC + \bar{B}\bar{C})$$

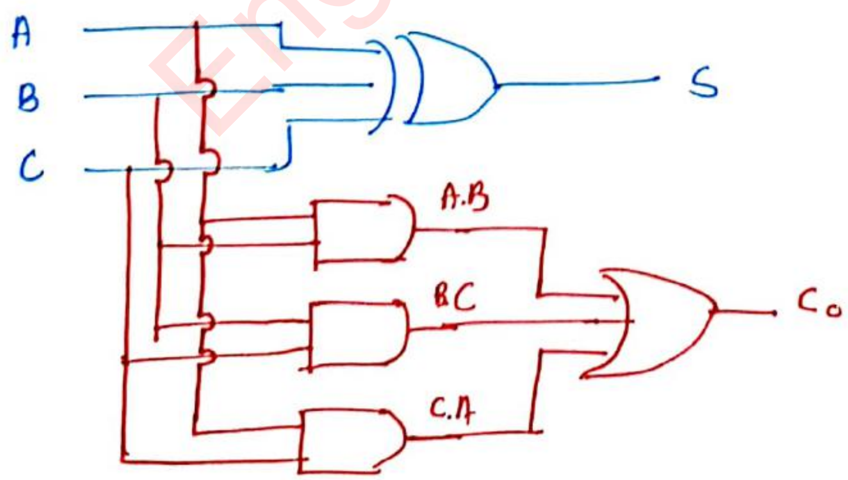
$$= \bar{A}(B \oplus C) + A(B \odot C)$$

$$= \bar{A}(B \oplus C) + A(\overline{B \oplus C})$$

$$\boxed{S = A \oplus B \oplus C}$$



$$\boxed{C_o = AB + B.C + A.C}$$



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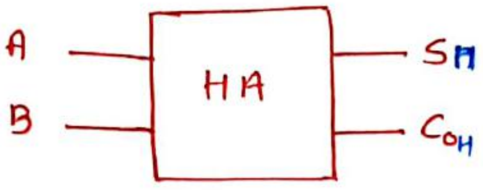
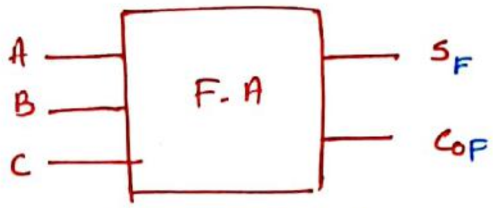
Full Adder circuit using Half Adder.



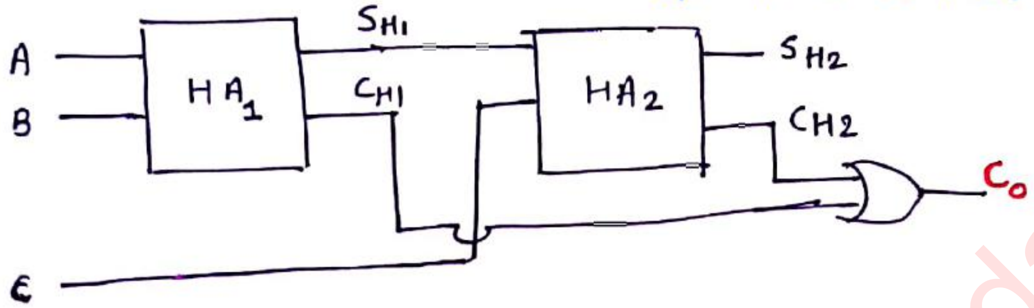
$S_H = A \oplus B$

$C_{OH} = A.B$



$S_F = A \oplus B \oplus C$

$C_{OF} = AB + BC + CA$



- $S_{H_1} = A \oplus B = A\bar{B} + \bar{A}B$

  $C_{H1} = A.B$

$S_{H_2} = S_{H_1} \oplus C = A \oplus B \oplus C$

$C_{H2} = S_{H_1} . C$

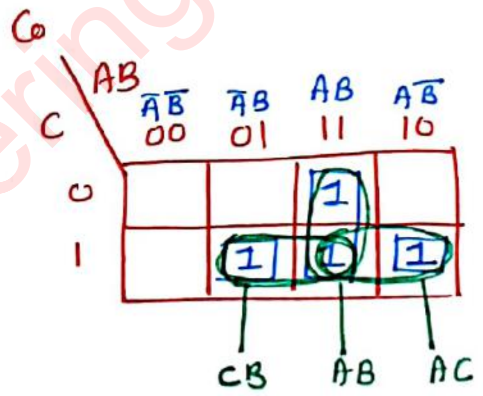
$= (A\bar{B} + \bar{A}B).C$

$= A\bar{B}C + \bar{A}B.C$

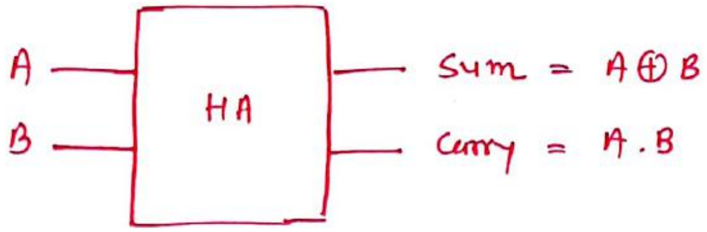
- $C_0 = C_{H_2} + C_{H1}$

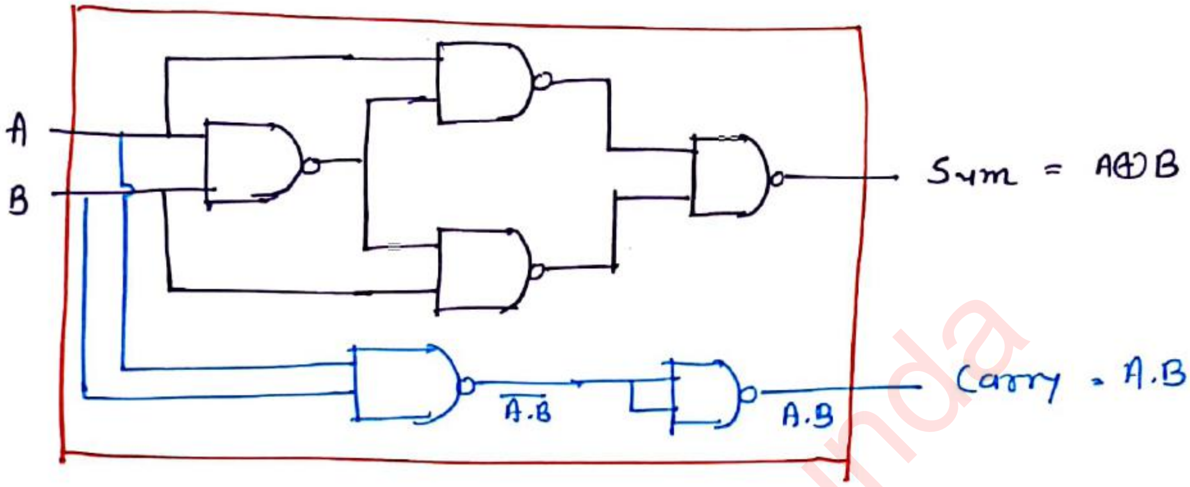
  $= A.B + A\bar{B}C + \bar{A}BC$

  $= A.B + BC + AC$



HALF ADDER BY NAND GATES





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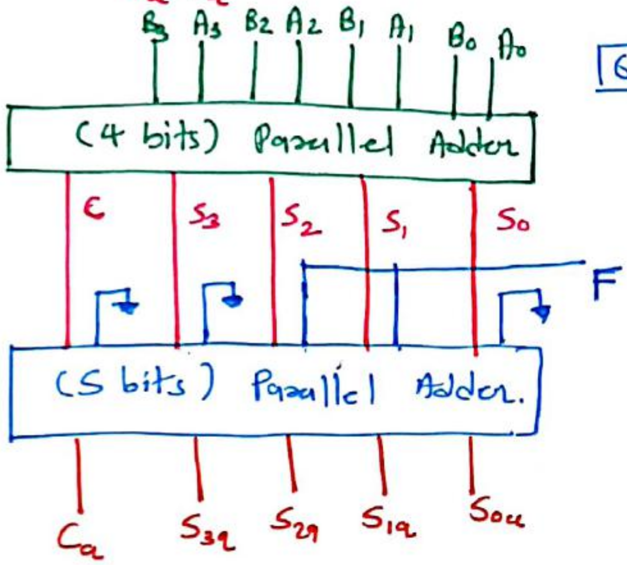
BCD Adder.

91

$A \leftarrow$ BCD data
$+\ B \leftarrow$ BCD data

C S [If $S < 9$]
$+6$ [If $S > 9$]
$C_a\ S_a$



$\boxed{6 \rightarrow 00110}$

C	S_3	S_2	S_1	S_0		
0	0	0	0	0	$\rightarrow$	0
0	0	0	0	1	$\rightarrow$	1
0	0	0	1	0	$\rightarrow$	2
0	0	0	1	1	$\rightarrow$	3
0	0	1	0	0	$\rightarrow$	4
0	0	1	0	1	$\rightarrow$	5
0	0	1	1	0	$\rightarrow$	6
0	0	1	1	1	$\rightarrow$	7
0	1	0	0	0	$\rightarrow$	8
0	1	0	0	1	$\rightarrow$	9
0	1	0	1	0	$\rightarrow$	10
0	1	0	1	1	$\rightarrow$	11
0	1	1	0	0	$\rightarrow$	12
0	1	1	0	1	$\rightarrow$	13
0	1	1	1	0	$\rightarrow$	14
0	1	1	1	1	$\rightarrow$	15
1	0	0	0	0	$\rightarrow$	16
1	0	0	0	1	$\rightarrow$	17
1	0	0	1	0	$\rightarrow$	18

[$S<9$] (rows 0–9)

($S>9$) ($C=0$) (rows 10–15)

($S>9$) ($C=1$) (rows 16–18)

$\rightarrow$ Cond.^{n} 1 $\rightarrow$ $C = 1$

$\rightarrow$ Cond.^{n} 2 $\rightarrow$ find Kmap

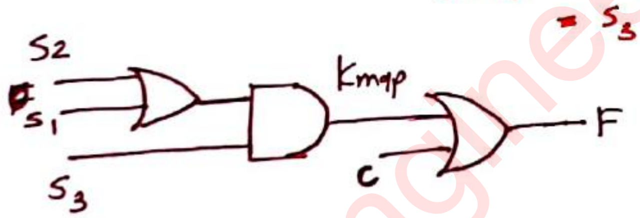
Kmap $= S_2S_3 + S_1S_3$
$= S_3(S_2 + S_1)$

Kmap

$S_1S_0 \backslash S_3S_2$	00	01	11	10
00	0	4	1 (12)	8
01	1	5	1 (13)	9
11	3	7	1 (15)	1 (11)
10	2	6	1 (14)	1 (10)

S_2S_3

S_1S_3



$S < 9$	$15 < S < 9$	$S > 9$ ($C=1$)
$A = 4$	$A = 5$	
$B = 4$	$B = 6$	
8	11	
01000	01011	
C S_3 S_2 S_1 S_0	C S_3 S_2 S_1 S_0	

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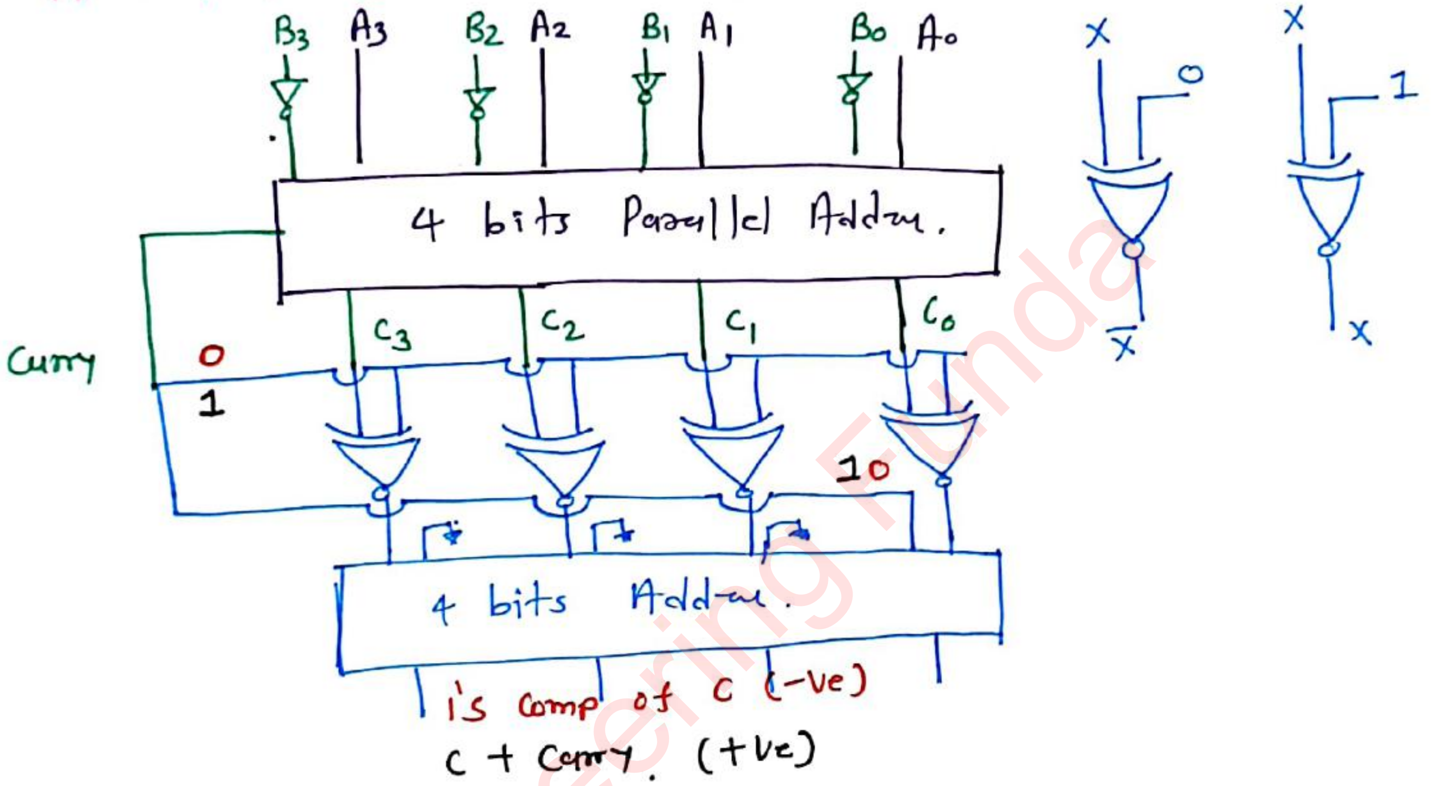
1's compliment subtraction using parallel Adder

$$\begin{array}{c} A \\ -B \\ \hline R \end{array} \quad \xrightarrow[\text{1's Comp}]{\text{Binary}} \quad \begin{array}{c} A \\ (-B) \\ \hline \text{Carry } C \end{array}$$

Step 1

Step-2

- If carry = 1 [Result is +ve] ⇒ R = C + carry
- If carry = 0 [Result is −ve] ⇒ R = 1's comp. of C.



2's Compliment Substruction using Parallel Adder

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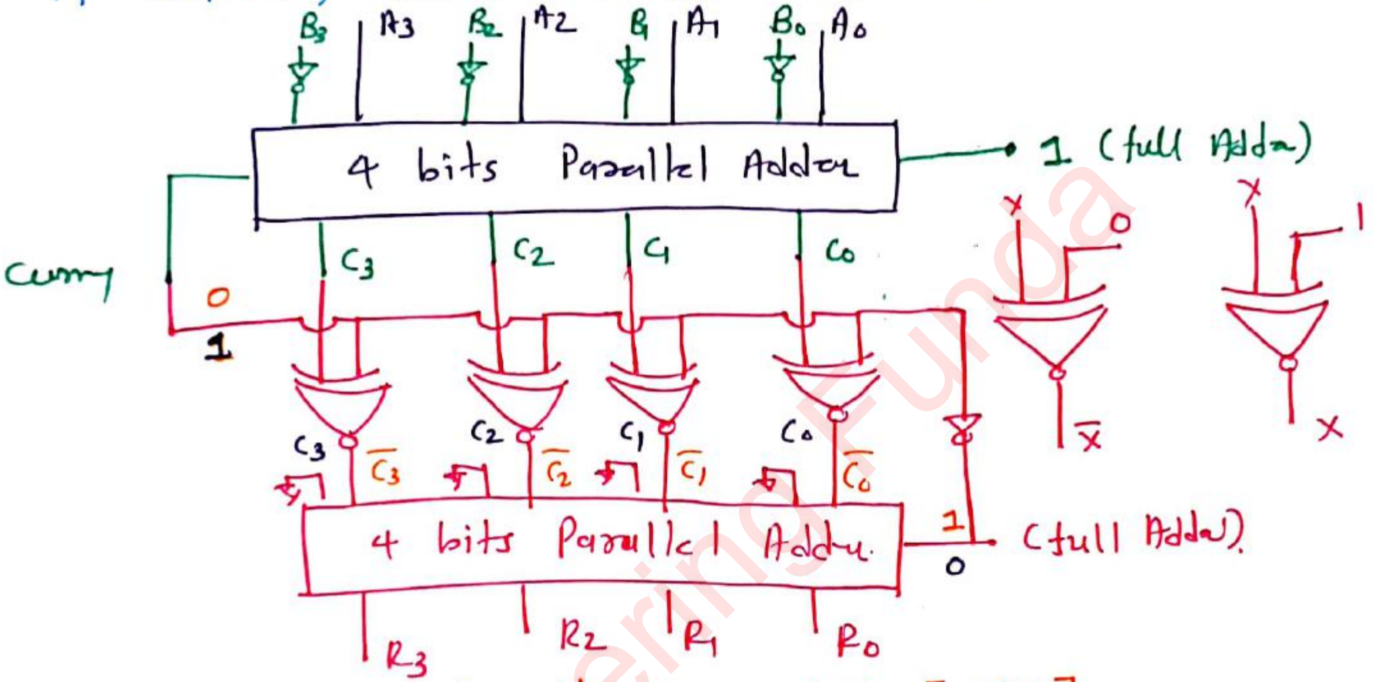
A $\xrightarrow{\text{Binary}}$ A
−B $\xrightarrow{\text{2's Comp.}}$ −B
R .... Carry C

Step-1

→ If Carry = 0, Result is (−Ve), ⇒ R = 2's Comp. of C
If Carry = 1, Result is (+Ve), ⇒ R = S

Step 2



R = 2's Comp of C [−Ve].
R = C [+Ve].

Half Subtractor 94

→ Half Subtractor is performing two bits subtraction.

$$\begin{array}{r} X \\ -\ Y \\ \hline B\ D \end{array}$$

(X−Y)

X	Y	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

D

Y \ X	$\bar{X}$ 0	X 1
$\bar{Y}$ 0	0	1
Y 1	1	0

$$D = X\bar{Y} + \bar{X}Y$$
$$= X \oplus Y$$

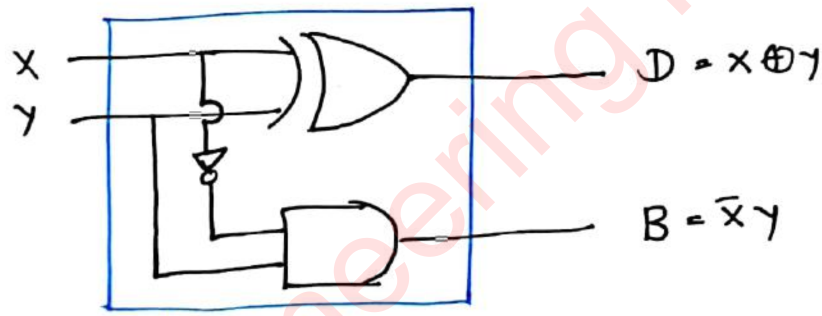
B

Y \ X	$\bar{X}$ 0	X 1
$\bar{Y}$ 0	0	0
Y 1	1	0

$$B = \bar{X}Y$$

→ for Y − X

$$B = X\bar{Y}$$

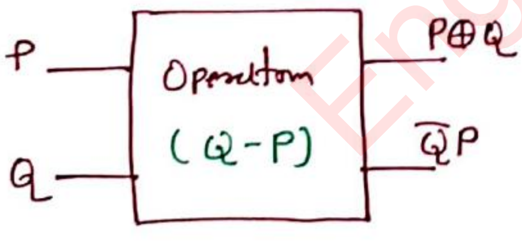


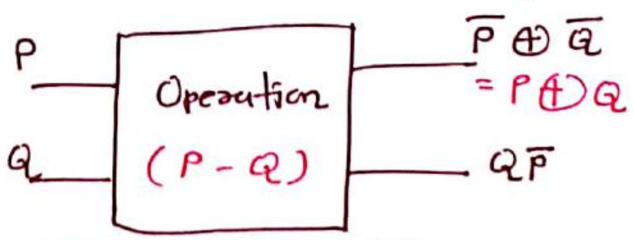
Half Sub.

Half Adder

$S = X \oplus Y$

$C = XY$

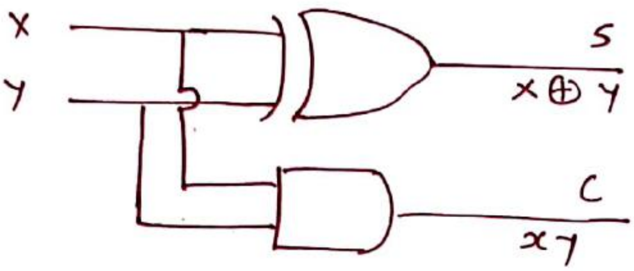




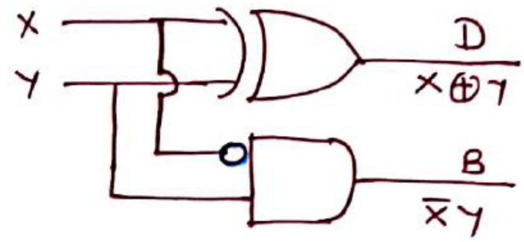
$$\bar{P} \oplus \bar{Q} = \bar{P}\bar{\bar{Q}} + \bar{\bar{P}}\bar{Q}$$
$$= \bar{P}Q + P\bar{Q}$$
$$= P \oplus Q$$

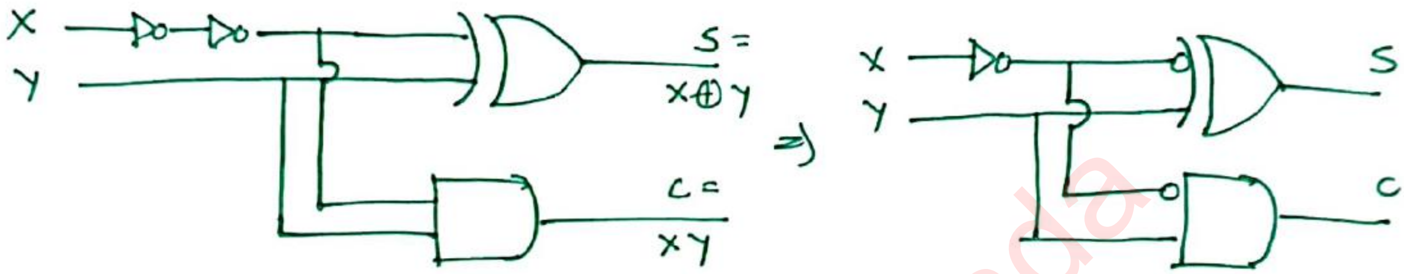
Half Adder using Half Subtractor 95

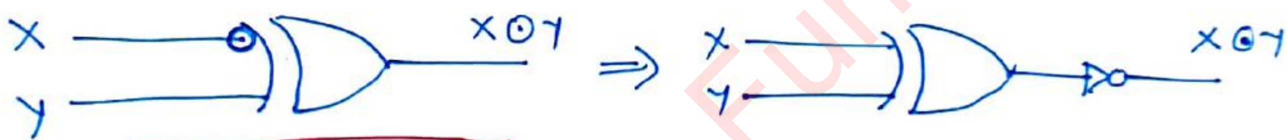
→ Half Adder

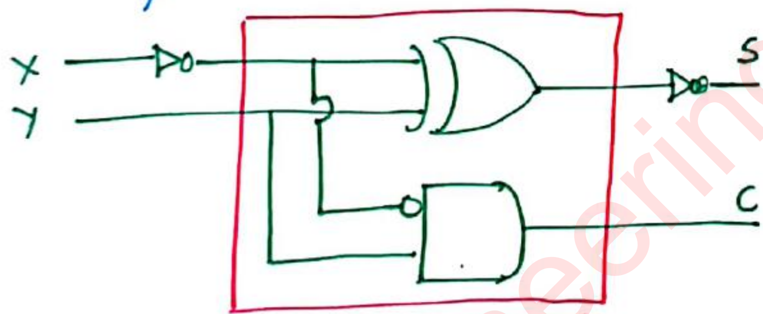


→ Half Subtractor

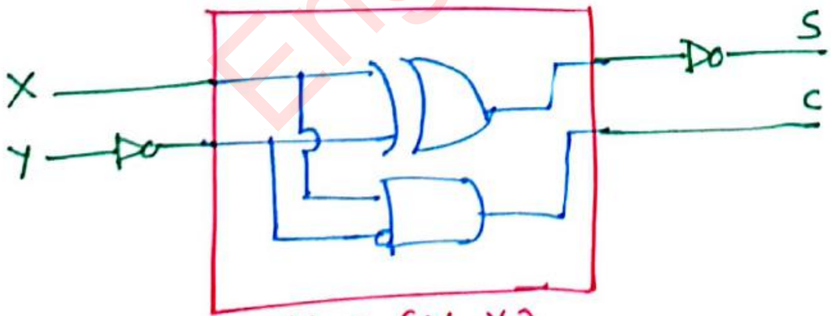








H.S (X-Y)



H.S (Y-X)

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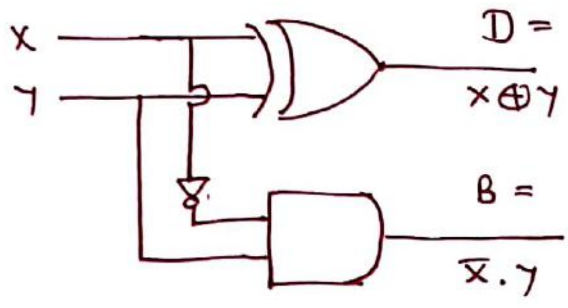
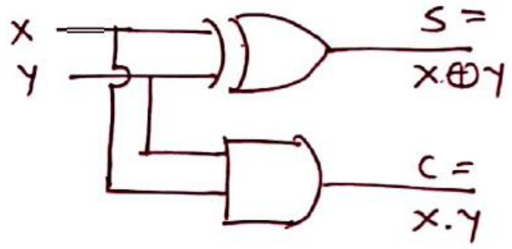
Half Subtractor using Half Adder. 96

→ Half subtractor

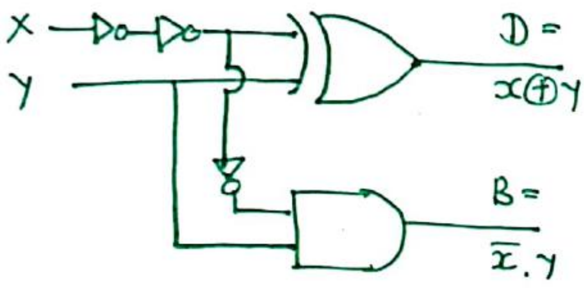


(x − y)

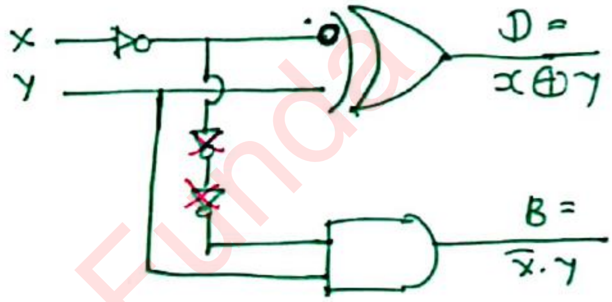
→ Half Adder



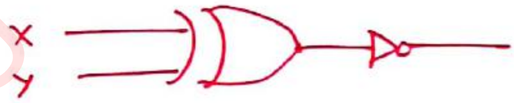
(x + y)

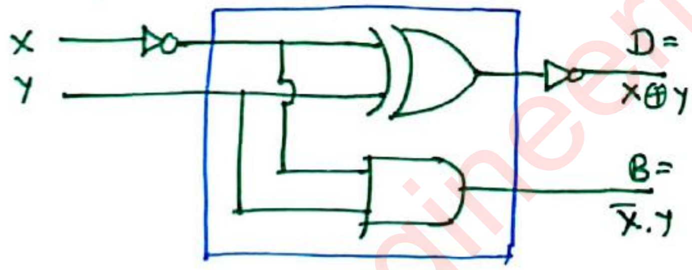


⇒

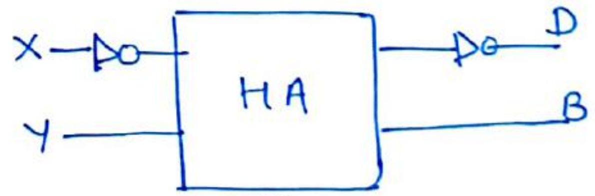


⇒

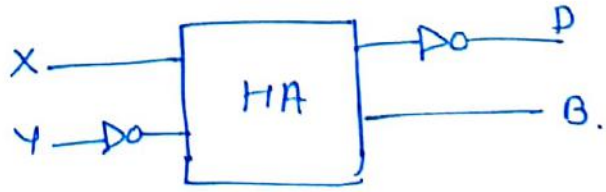




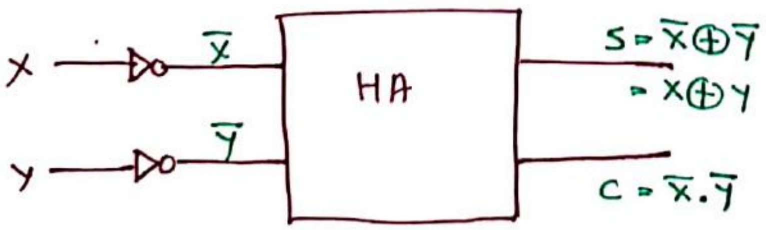
Half Adder.



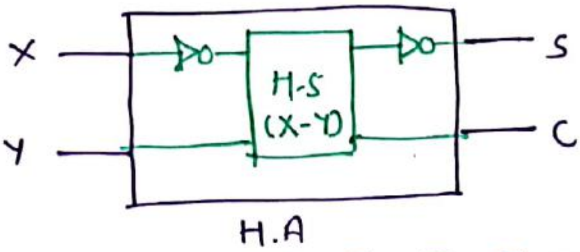
(X − Y)

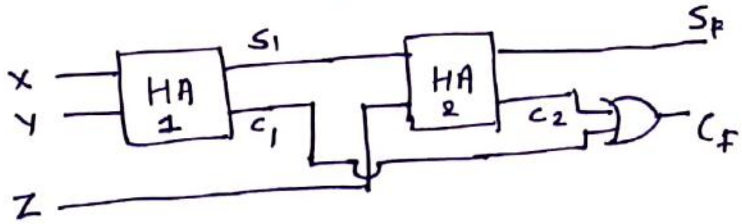


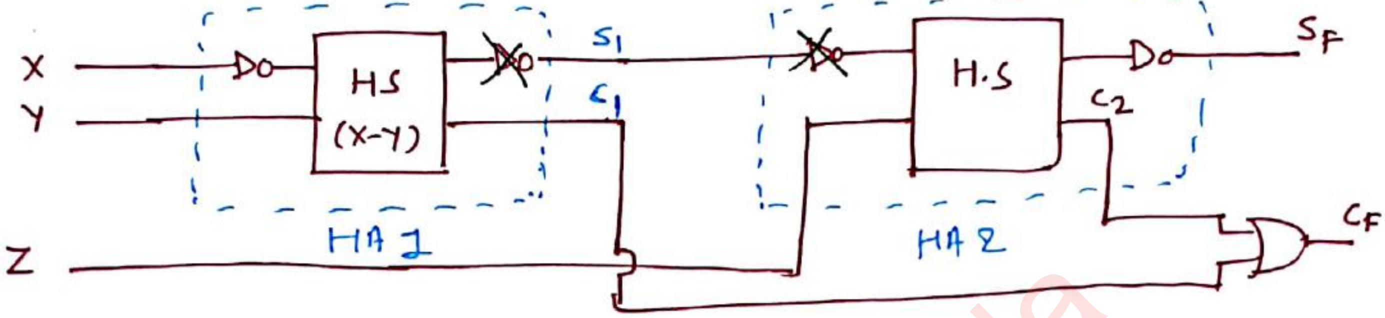
(Y − X).

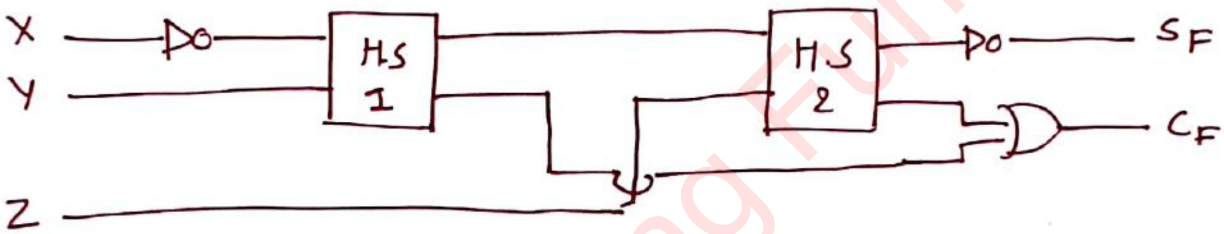


Full Adder using Half Subtractor 97









Full Subtractor 98

→ Full Subtractor performs 3 bits Subtraction.

$(A - B - C)$ or $A - (B + C)$

A	B	C	D	B_o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

D

C \ AB	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$D = \bar{A}\bar{B}C + \bar{A}B\bar{C} + ABC + A\bar{B}\bar{C}$

$= \bar{A}(\bar{B}C + B\bar{C}) + A(BC + \bar{B}\bar{C})$

$= \bar{A}(B \oplus C) + A(B \odot C)$

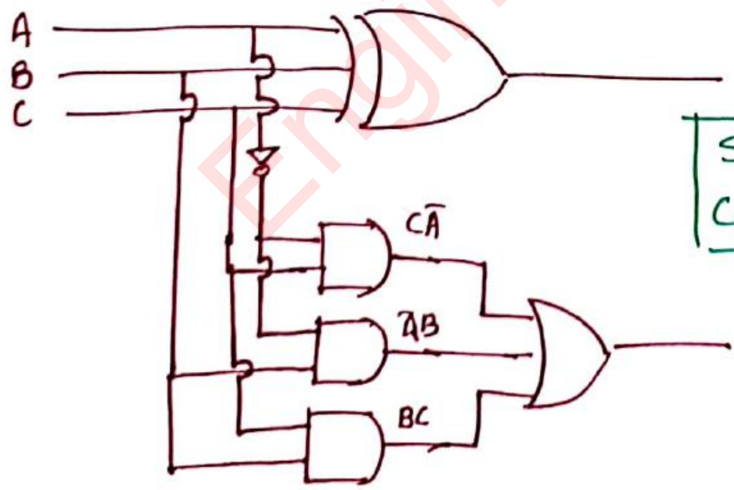
$= A \oplus B \oplus C$

B_o

C \ AB	00	01	11	10
0	0	1	0	0
1	1	1	1	0

$C\bar{A}$ $\bar{A}B$ BC

$B_o = C\bar{A} + \bar{A}B + BC$



$D = A \oplus B \oplus C$

$\boxed{\begin{array}{l} \text{Sum} = A \oplus B \oplus C \\ \text{Carry} = AB + BC + CA \end{array}}$ Full Adder.

$B_o = C\bar{A} + \bar{A}B + BC$

$(\underline{A} - B - C)$

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Full Adder using Full Subtractor 199

→ Full Adder.

$[A + B + C]$

$S = A \oplus B \oplus C$

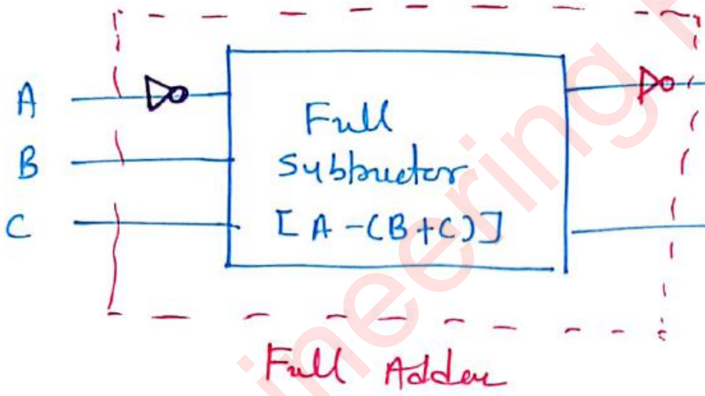
$C_0 = AB + BC + CA$

→ Full Subtractor

$[A - (B + C)]$

$D = A \oplus B \oplus C$

$B_0 = \bar{A}B + \bar{A}C + BC$



$D = A \oplus B \oplus C$

$D = \bar{A} \oplus B \oplus C$

$D = A \oplus B \oplus C$

$B_0 = \bar{A}B + \bar{A}C + BC$

$C_0 = AB + AC + BC$

Full subtractor using Half Subtractor

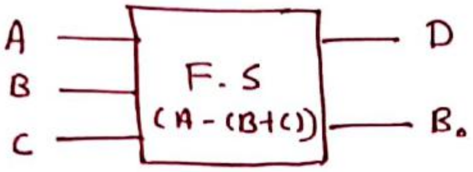
→ Full subtractor

[A, B, C]

[A − (B + C)]

→ $D = A \oplus B \oplus C$

$B_o = \bar{A}B + \bar{A}C + BC$



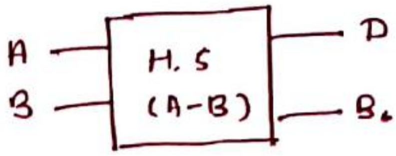
→ Half subtractor

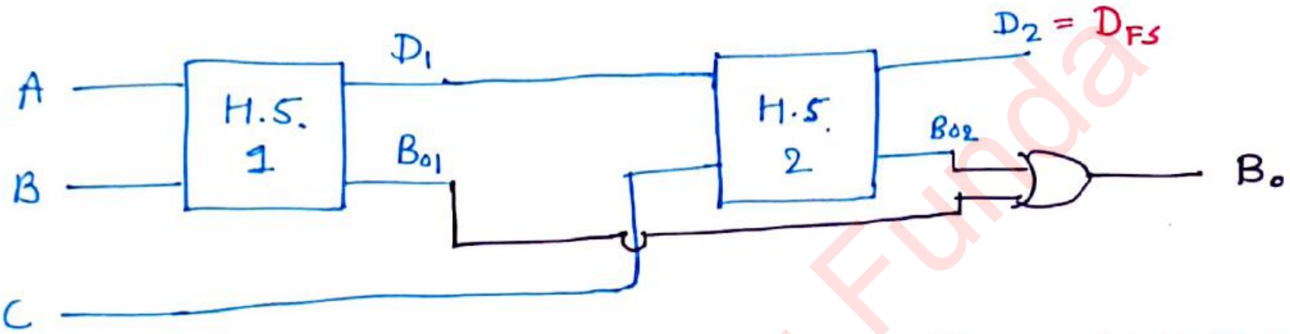
[A, B]

[A − B]

→ $D = A \oplus B$

$B_o = \bar{A}B$





<u>H.S.1</u> $D_1 = A \oplus B$

$B_{01} = \bar{A}B$

<u>H.S.2</u> $D_2 = D_1 \oplus C = A \oplus B \oplus C$

$B_{02} = \overline{D_1} \cdot C$

$$\begin{aligned}
\rightarrow B_o &= B_{01} + B_{02} \\
&= \bar{A}B + \overline{D_1} \cdot C \\
&= \bar{A}B + (\overline{A \oplus B}) \cdot C \\
&= \bar{A}B + (AB + \bar{A}\bar{B}) \cdot C \\
&= \bar{A}B + ABC + \bar{A}\bar{B}C \\
&= \bar{A}B + \bar{A}C + BC
\end{aligned}$$

B_o

C \ AB	00	01	11	10
0		1		
1	1	1	1	

$\bar{A}C$ $\bar{A}B$ BC

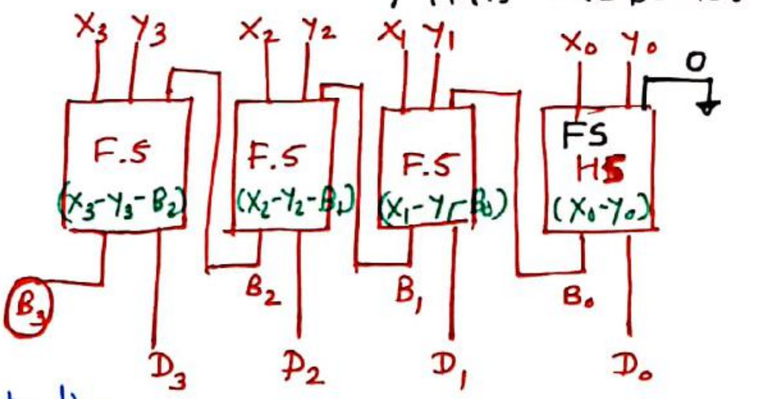
Parallel Subtractor using Full Subtractor / Half subtractor.

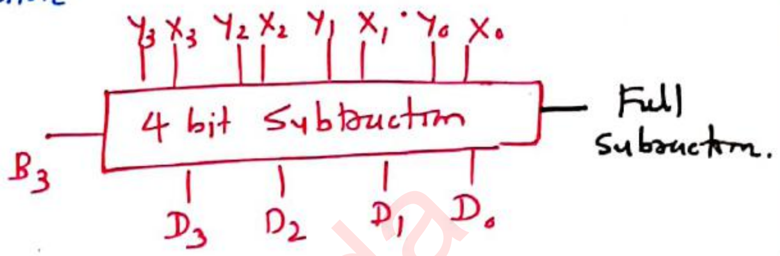
$$\begin{array}{r} X \\ -\ Y \\ \hline B_0\ D \end{array}$$

B_3	B_2	B_1	B_0	0
	X_3	X_2	X_1	X_0
	Y_3	Y_2	Y_1	Y_0
B_3	D_3	D_2	D_1	D_0

$(X-Y-B)$ Full Subtraction.

(X_0-Y_0) Half Subtraction





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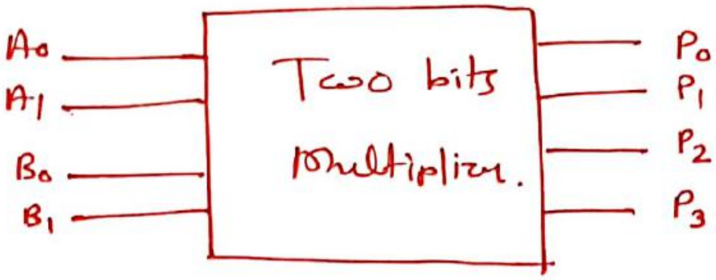
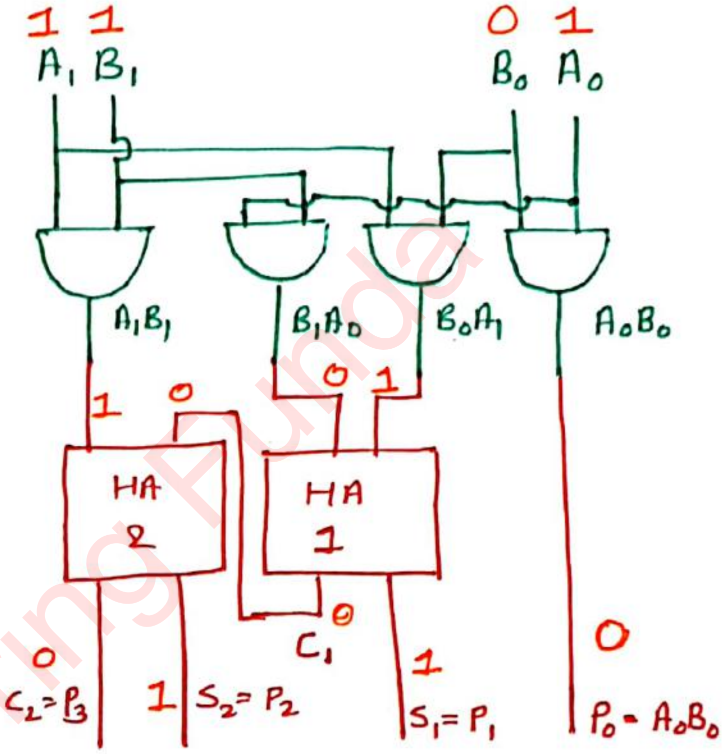
2 Bits Multiplier using Half Adder 1.03



$$\begin{array}{r} 11 \\ 10 \\ \hline 0110 \end{array}$$

		A_1	A_0
		B_1	B_0
	C_1	B_0A_1	B_0A_0
C_2	A_1B_1	B_1A_0	X
P_3	P_2	P_1	P_0



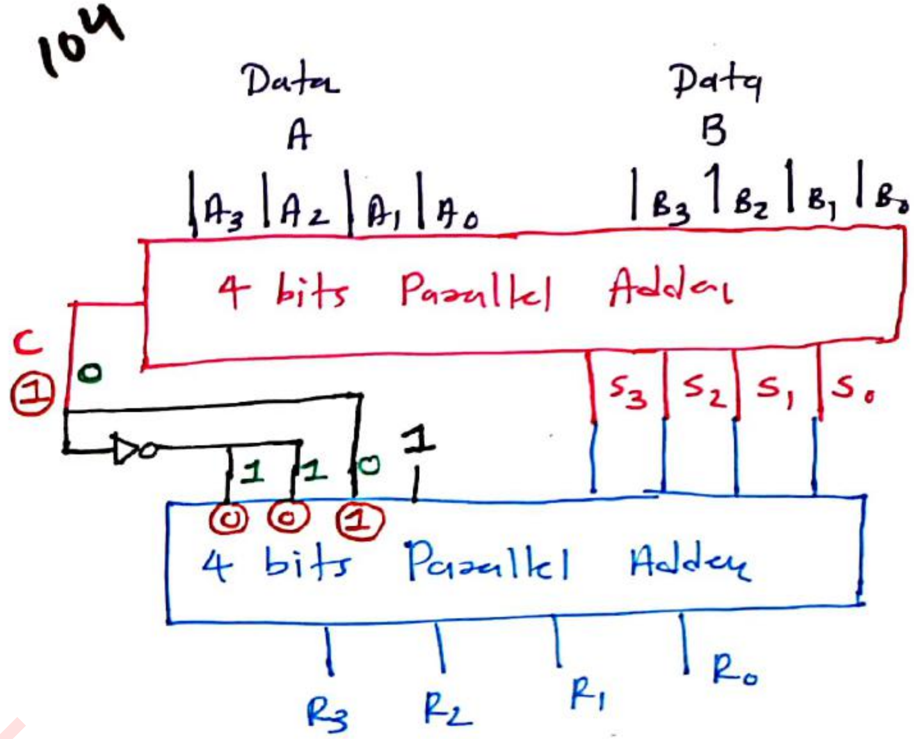
→ $P_0 = B_0A_0$

$P_1 = HA_1[B_0A_1, B_1A_0]$

$P_2 = HA_2[C_1, A_1B_1]$

$P_3 = C_2$

Excess-3 Addition by Parallel Adder



Step-1 – take two Excess-3 data A, B

Step-2 – Add Two data A & B

$A + B = S$ (carry C)

Step-3 – Check

If $C = 0$

Ans = $S - 3$

$-3 \rightarrow -0011$

$\downarrow$ 1's Comp

1100

+1 $\downarrow$ 2's Comp

$\boxed{1101}$

If $C = 1$

Ans = $S + 3$

$+3 \rightarrow 0011$

2 bits Comparator 105

A_1	A_0	B_1	B_0		A>B	A=B	A<B
0	0	0	0	→	0	1	0
0	0	0	1	→	0	0	1
0	0	1	0	→	0	0	1
0	0	1	1	→	0	0	1
0	1	0	0	→	1	0	0
0	1	0	1	→	0	1	0
0	1	1	0	→	0	0	1
0	1	1	1	→	0	0	1
1	0	0	0	→	1	0	0
1	0	0	1	→	1	0	0
1	0	1	0	→	0	1	0
1	0	1	1	→	0	0	1
1	1	0	0	→	1	0	0
1	1	0	1	→	1	0	0
1	1	1	0	→	1	0	0
1	1	1	1	→	0	1	0

A>B

B_1B_0 \ A_1A_0	00	01	11	10
00		1	1	1
01			1	1
11				
10			1	

$A_0\overline{B_1}\,\overline{B_0}$

$A_1A_0\overline{B_0}$

$A_1\overline{B_1}$

$(A>B) = A_1\overline{B_1} + A_0\overline{B_1}\,\overline{B_0} + A_1A_0\overline{B_0}$

A=B

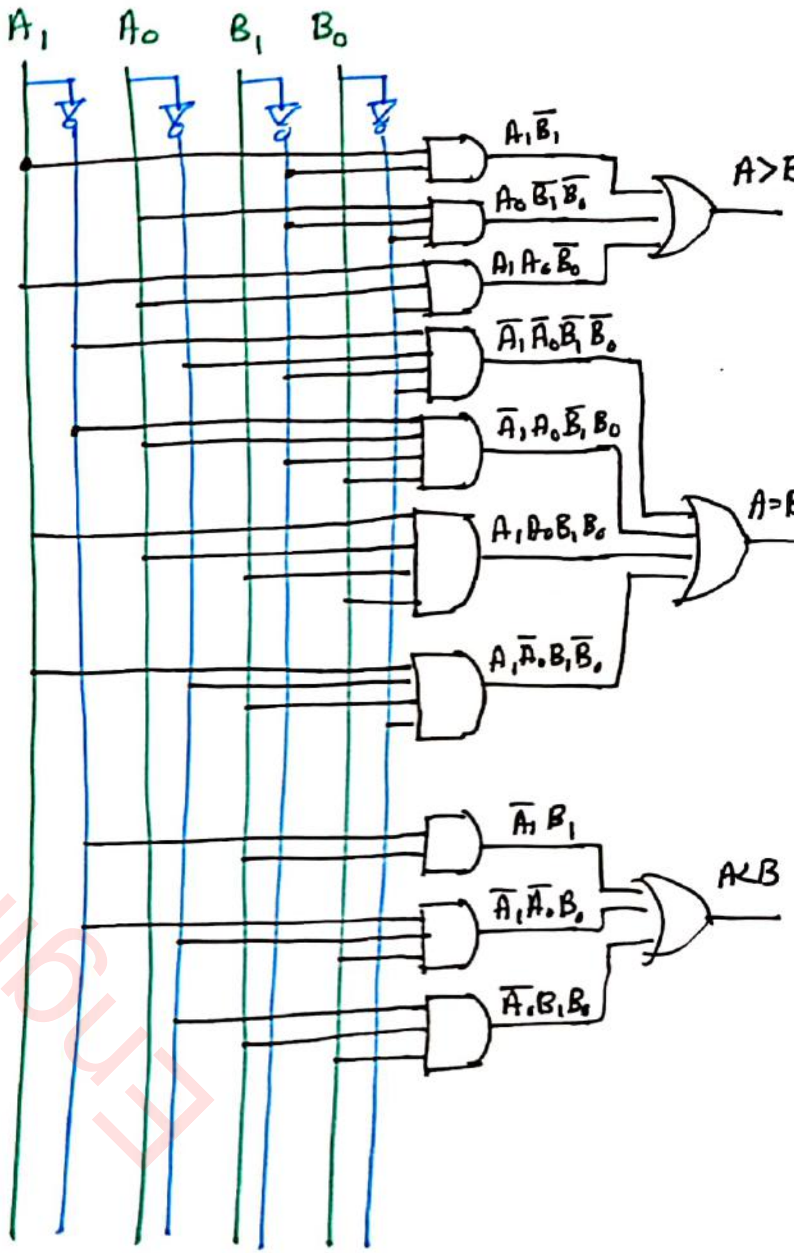
B_1B_0 \ A_1A_0	00	01	11	10
00	1			
01		1		
11			1	
10				1

$(A=B) = \overline{A_1}\,\overline{A_0}\,\overline{B_1}\,\overline{B_0} + \overline{A_1}A_0\overline{B_1}B_0 +$
$A_1A_0B_1B_0 + A_1\overline{A_0}B_1\overline{B_0}$

A<B

B_1B_0 \ A_1A_0	00	01	11	10
00				
01	1			
11	1	1		1
10	1	1		

$(A<B) = \overline{A_1}B_1 + \overline{A_1}\,\overline{A_0}B_0 + \overline{A_0}B_1B_0$



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Seven Segment Display Decoder

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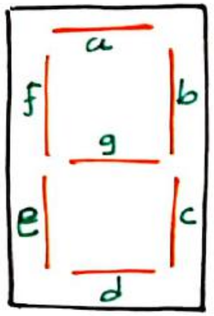

Digit	b_3	b_2	b_1	b_0	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1
other	1	0	1	0	x	x	x	x	x	x	x
	1	1	1	1	x	x	x	x	x	x	x

a

b_1b_0 \ b_3b_2	00	01	11	10
00	1_0	0_4	X_{12}	1_8
01	0_1	1_5	X_{13}	1_9
11	1_3	1_7	X_{15}	X_{11}
10	1_2	1_6	X_{14}	X_{10}

$a = b_1 + b_3 + b_0b_2 + \overline{b_0}\,\overline{b_2}$

b

b_1b_0 \ b_3b_2	00	01	11	10
00	1_0	1_4	X_{12}	1_8
01	1_1	0_5	X_{13}	1_9
11	1_3	1_7	X_{15}	X_{11}
10	1_2	0_6	X_{14}	X_{10}

$b = \overline{b_2} + \overline{b_1}\,\overline{b_0} + b_1b_0$

c

b_1b_0 \ b_3b_2	00	01	11	10
00	1_0	1_4	X_{12}	1_8
01	1_1	1_5	X_{13}	1_9
11	1_3	1_7	X_{15}	X_{11}
10	0_2	1_6	X_{14}	X_{10}

$c = \overline{b_1} + b_0 + b_2$

D

b_1b_0 \ b_3b_2	00	01	11	10
00	1_0	0_4	X_{12}	1_8
01	0_1	1_5	X_{13}	1_9
11	1_3	0_7	X_{15}	X_{11}
10	1_2	1_6	X_{14}	X_{10}

$d = b_3 + b_1\overline{b_0} + b_1\overline{b_2} + \overline{b_0}\,\overline{b_2} + \overline{b_1}b_0b_2$

e

b_1b_0 \ b_3b_2	00	01	11	10
00	1_0	0_4	X_{12}	1_8
01	0_1	0_5	X_{13}	0_9
11	0_3	0_7	X_{15}	X_{11}
10	1_2	1_6	X_{14}	X_{10}

$e = b_1\overline{b_0} + \overline{b_0}\,\overline{b_2}$

f

b_1b_0 \ b_3b_2	00	01	11	10
00	1_0	1_4	X_{12}	1_8
01	0_1	1_5	X_{13}	1_9
11	0_3	0_7	X_{15}	X_{11}
10	0_2	1_6	X_{14}	X_{10}

$f = b_3 + \overline{b_0}b_2 + \overline{b_0}\,\overline{b_1} + \overline{b_1}\,\overline{b_2}$

g

b_1b_0 \ b_3b_2	00	01	11	10
00	0_0	1_4	X_{12}	1_8
01	0_1	1_5	X_{13}	1_9
11	1_3	0_7	X_{15}	X_{11}
10	1_2	1_6	X_{14}	X_{10}

$g = b_3 + \overline{b_1}b_2 + b_1\overline{b_0} + b_1\overline{b_2}$

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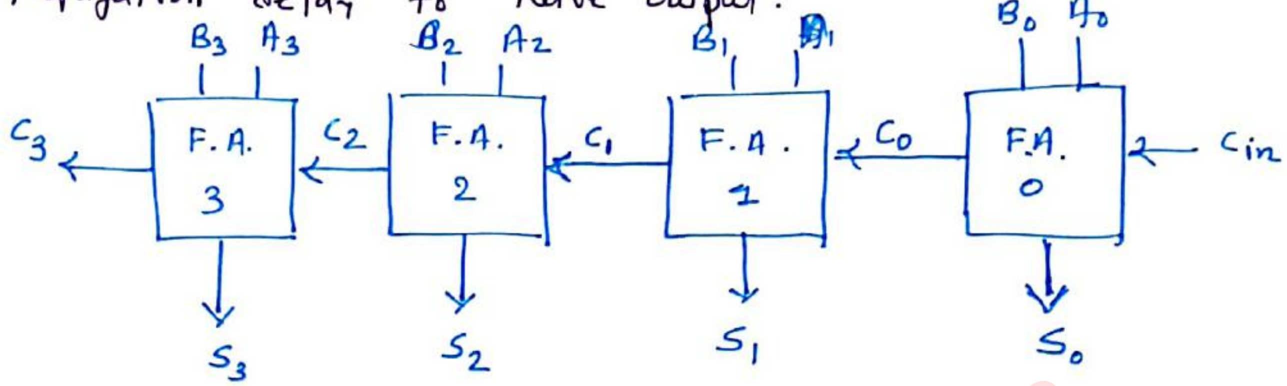
Carry Look Ahead Adder [CLA Adder]

- CLA Adder is batter then Full Adder in teams of Speed.
- By Full Adder when we have parallel Adder, it takes Propagation delay to have output.



A_0	B_0	C_{in}	C_0	
0	0	0	0	
0	0	1	0	
0	1	0	0	
0	1	1	1	–
1	0	0	0	
1	0	1	1	– $A_0\bar{B}_0C_{in}$
1	1	0	1	A_0B_0
1	1	1	1	

$$\rightarrow C_0 = A_0B_0 + A_0\bar{B}_0C_{in} + \bar{A}_0B_0C_{in}$$
$$= A_0B_0 + C_{in}(A_0\bar{B}_0 + \bar{A}_0B_0)$$
$$= A_0B_0 + C_{in}(A_0 \oplus B_0)$$

$$\rightarrow C_i = \underbrace{A_iB_i}_{\text{Carry generator } G_i} + C_{i-1}\underbrace{(A_i \oplus B_i)}_{\text{Carry Propagator } P_i}$$

$$\rightarrow \boxed{C_i = [G_i + C_{i-1}P_i]}$$

$\rightarrow$ $i=0$

$$C_0 = G_0 + C_{-1}P_0$$

$\rightarrow$ $i=1$

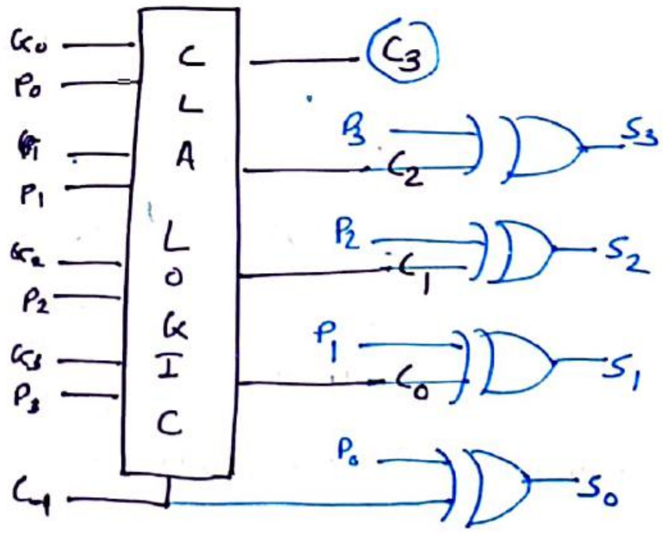
$$C_1 = G_1 + C_0P_1 = G_1 + [G_0 + C_{-1}P_0]P_1$$
$$= G_1 + P_1G_0 + P_1P_0C_{-1}$$

$\rightarrow$ $i=2$

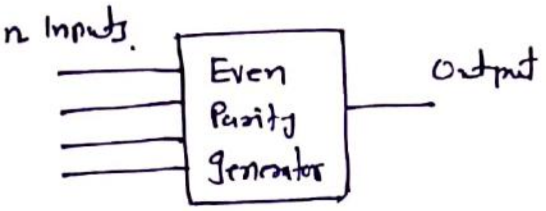
$$C_2 = G_2 + C_1P_2$$
$$= G_2 + P_2[G_1 + P_1G_0 + P_1P_0C_{-1}]$$
$$= G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_{-1}$$

$\rightarrow$ $i=3$

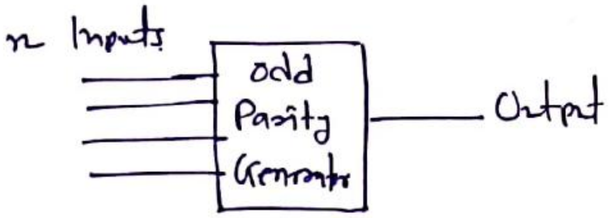
$$C_3 = G_3 + C_2P_3$$
$$= G_3 + P_3[G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_{-1}]$$
$$= G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_{-1}$$



Even Parity Generator / Odd Parity Generator



— For even parity generator output = 1 when number of 1's at I/p is Odd.



— For odd parity generator output = 1, when number of 1's at o/p is even.

b_3	b_2	b_1	b_0	O/p (Even parity) P	
0	0	0	0	0	(0)
0	0	0	1	1	(1)
0	0	1	0	1	(2)
0	0	1	1	0	(3)
0	1	0	0	1	(4)
0	1	0	1	0	(5)
0	1	1	0	0	(6)
0	1	1	1	1	(7)
1	0	0	0	1	(8)
1	0	0	1	0	(9)
1	0	1	0	0	(10)
1	0	1	1	1	(11)
1	1	0	0	0	(12)
1	1	0	1	1	(13)
1	1	1	0	1	(14)
1	1	1	1	0	(15)

$$Q_{odd} = \overline{b_3 \oplus b_2 \oplus b_1 \oplus b_0}$$

P

b_1b_0 \ b_3b_2	00	01	11	10
00	0_0	1_4	0_{12}	1_8
01	1_1	0_5	1_{13}	0_9
11	0_3	1_7	0_{15}	1_{11}
10	1_2	0_6	1_{14}	0_{10}

$$P(b_0 b_1 b_2 b_3) = b_0 \oplus b_1 \oplus b_2 \oplus b_3$$

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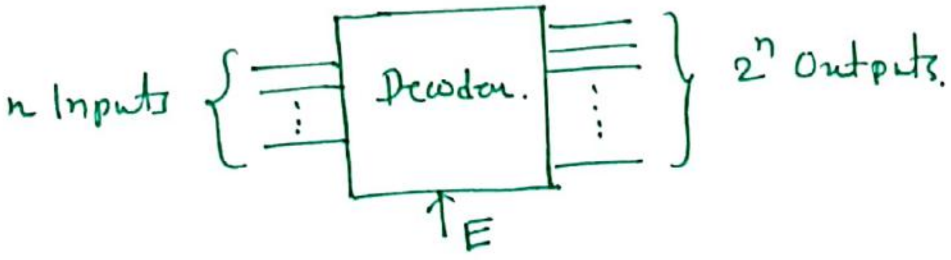
Decoder Basics and 2 X 4 Decoder

- Decoder decodes n Inputs to 2^n Outputs.

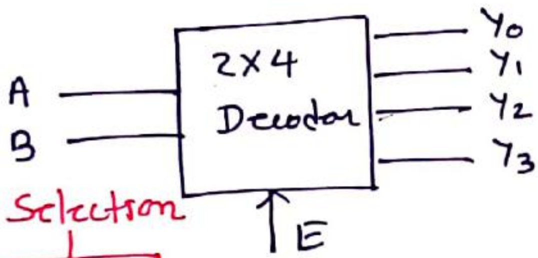


E = Enable.

If E = 0, Decoder is desabled.

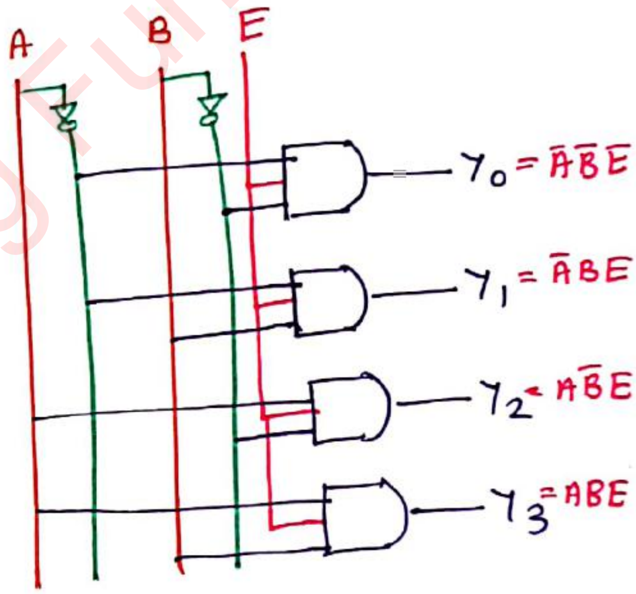
If E = 1, Decoder is Enabled.

- 2 X 4 Decoder.

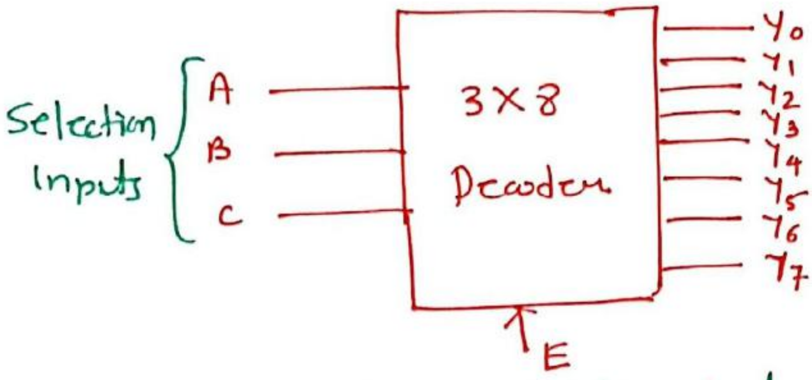


Selection

E	A	B	Y_0	Y_1	Y_2	Y_3
0	X	X	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1



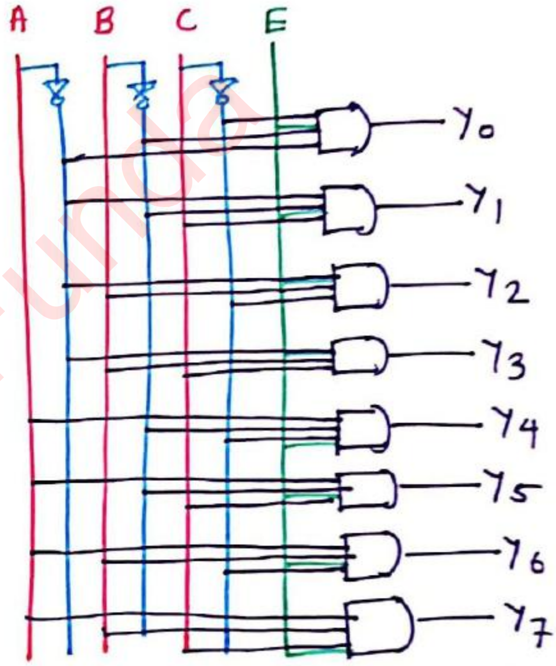
3 X 8 Decoder 110



E is enable terminal
E = 0 , Decoder is desabled.
E = 1 , Decoder is Enabled.

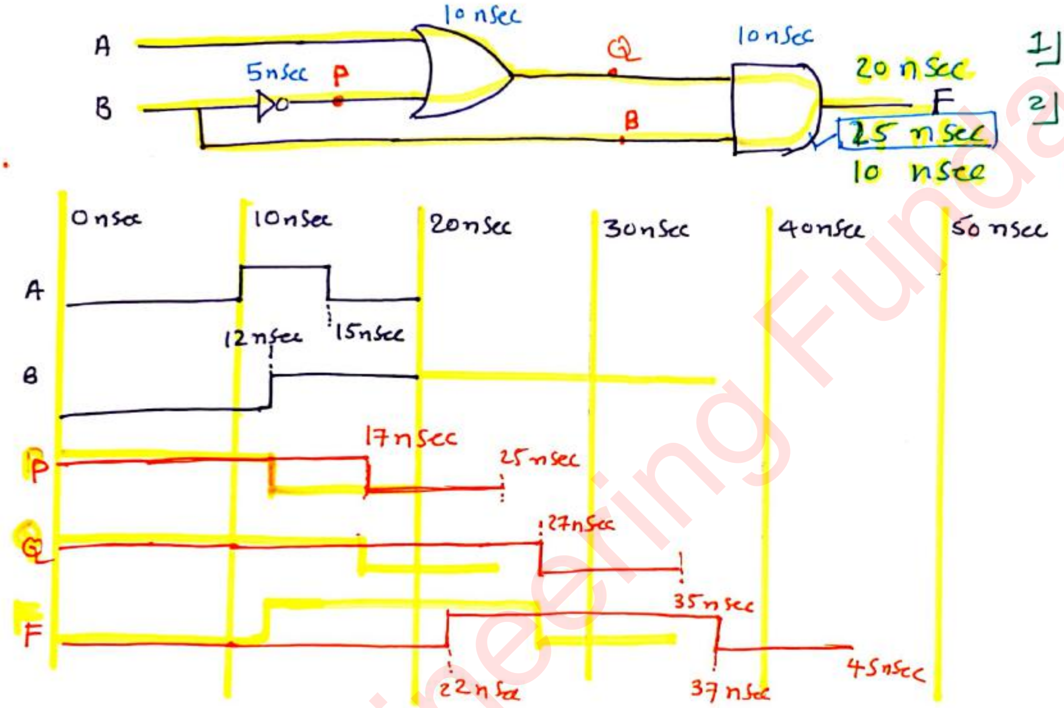
E	A	B	C	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
0	X	X	X	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	0	0	0
1	0	1	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1

Selection Inputs — Outputs.



$Y_7 = ABCE$

Combinational Circuit Output waveform with delay of gates. [Part 1]

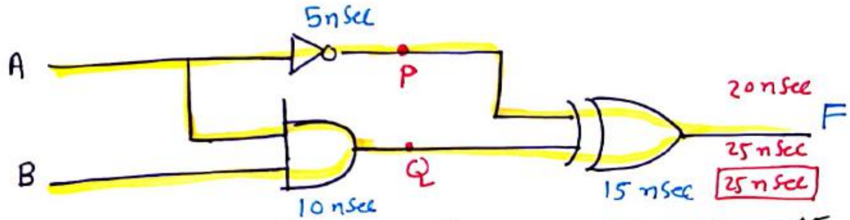


F.

1] Find output waveform

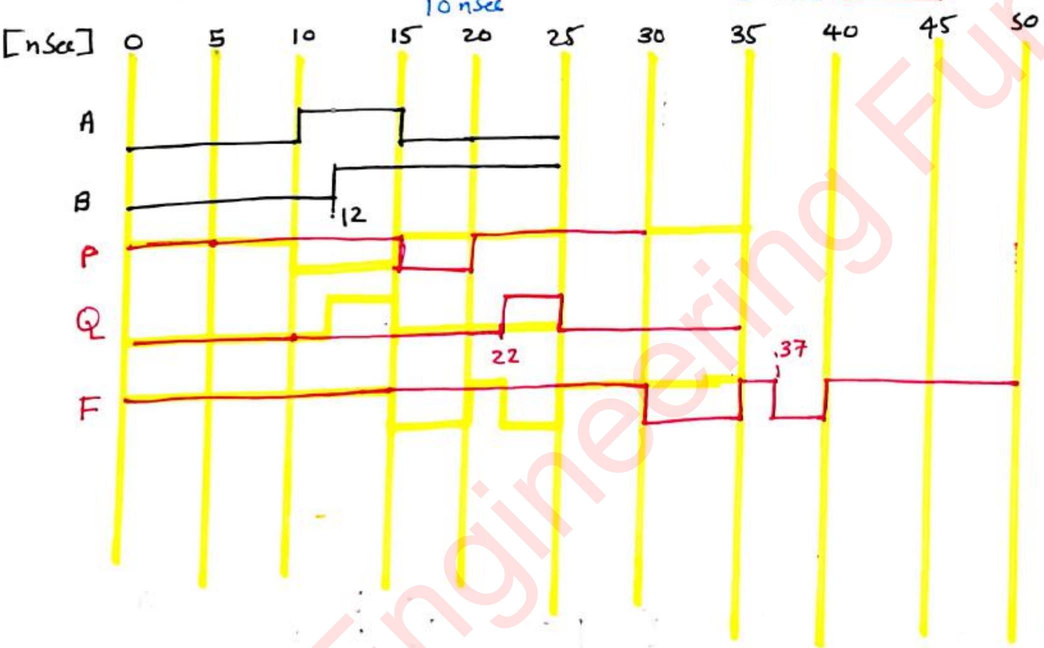
2] Find total delay of given Combinational circuit.

Combinational Circuit Output waveform with delay at gates [Part 2]. 112

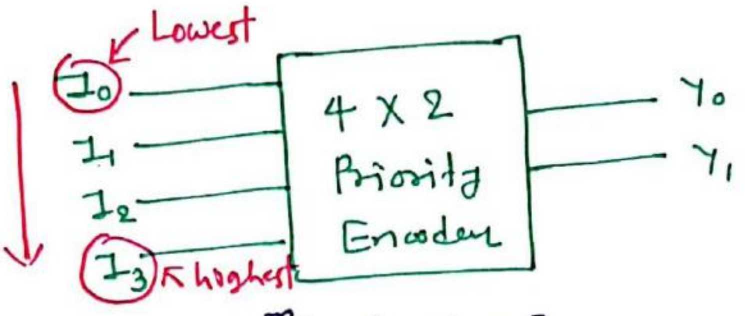


1] Find output waveform F.

2] Find total delay of given Combinational circuit.



Priority Encoder



$\rightarrow n = 4 = 2^m \Rightarrow m = 2$

I_3	I_2	I_1	I_0	Y_1	Y_0
0	0	0	0	X	X
0	0	0	1	0	0
0	0	1	X	0	1
0	1	X	X	1	0
1	X	X	X	1	1

Y_1 (I_1I_0 rows, I_3I_2 columns)

I_1I_0 \ I_3I_2	00	01	11	10
00	X	1	1	1
01	0	1	1	1
11	0	1	1	1
10	0	1	1	1

I_2 I_3

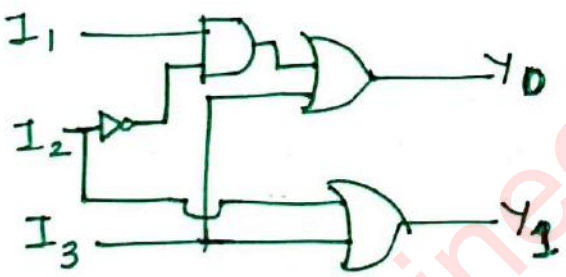
$$\boxed{Y_1 = I_3 + I_2}$$

Y_0 (I_1I_0 rows, I_3I_2 columns)

I_1I_0 \ I_3I_2	00	01	11	10
00	X	0	1	1
01	0	0	1	1
11	1	0	1	1
10	1	0	1	1

$I_1\overline{I_2}$ I_3

$$\boxed{Y_0 = I_3 + I_1\overline{I_2}}$$



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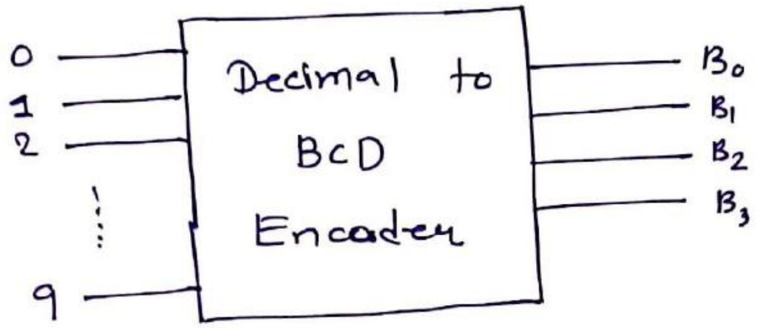
Decimal to BCD Encoder 114

→ Decimal [0 to 9] to BCD [0000 to 1001] Encoder.



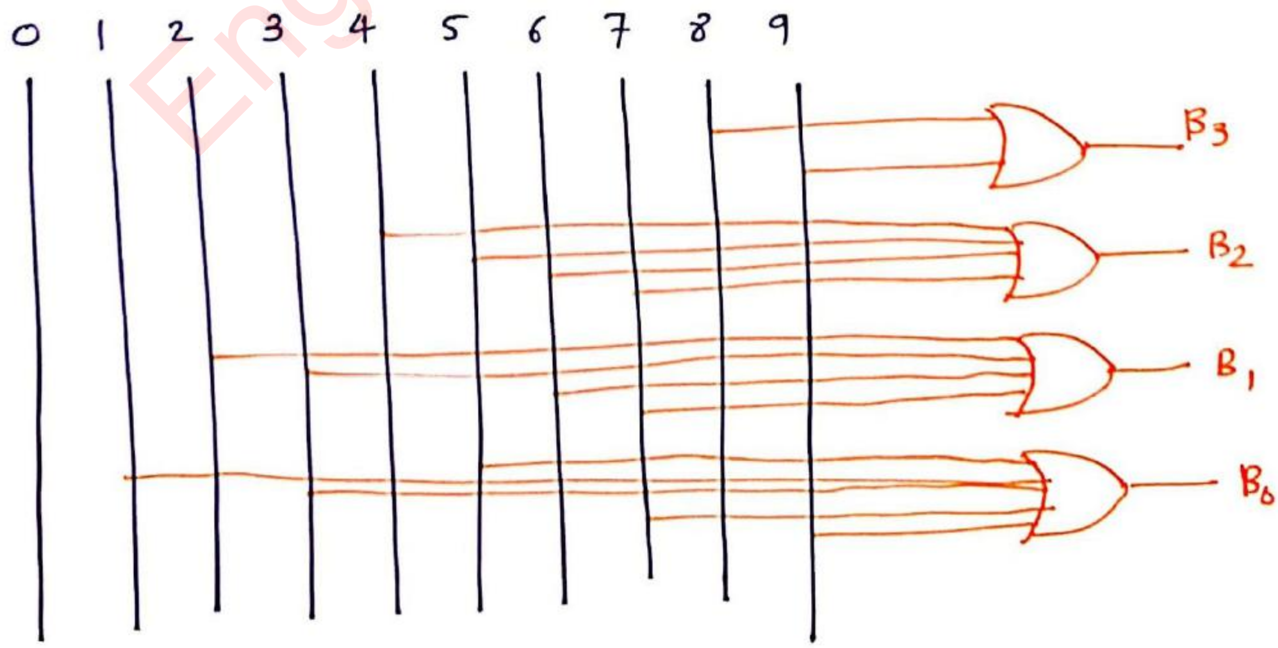
Input Decimal Number	O/P B_3	B_2	B_1	B_0
0 →	0	0	0	0
1 →	0	0	0	1
2 →	0	0	1	0
3 →	0	0	1	1
4 →	0	1	0	0
5 →	0	1	0	1
6 →	0	1	1	0
7 →	0	1	1	1
8 →	1	0	0	0
9 →	1	0	0	1

$B_3 = 8 + 9$

$B_2 = 4 + 5 + 6 + 7$

$B_1 = 2 + 3 + 6 + 7$

$B_0 = 1 + 3 + 5 + 7 + 9$



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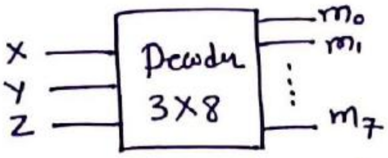
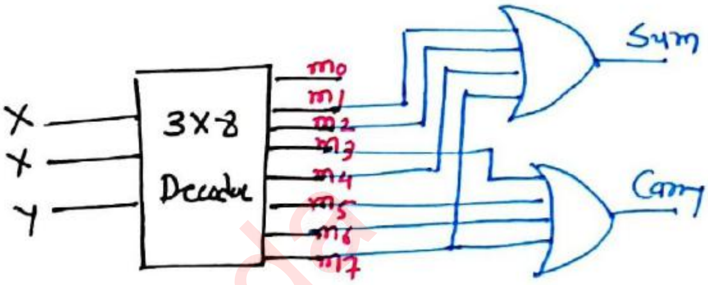
Full Adder using Decoder 115



$m = 2^n = 2^3 = 8$

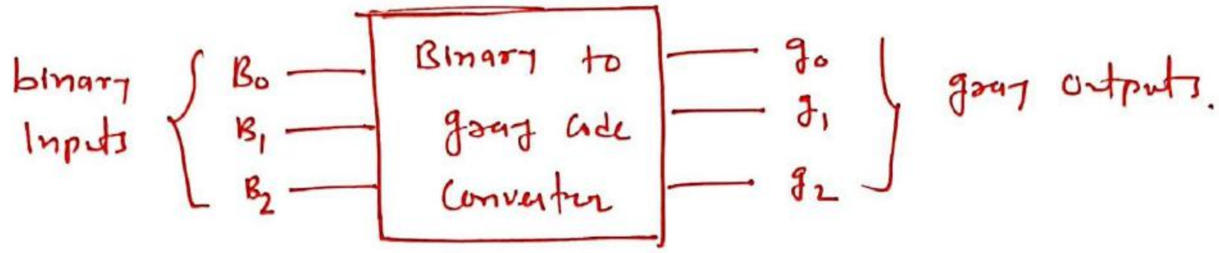
X	Y	Z	S	C	O/P
0	0	0	0	0	m_0
0	0	1	1	0	m_1
0	1	0	1	0	m_2
0	1	1	0	1	m_3
1	0	0	1	0	m_4
1	0	1	0	1	m_5
1	1	0	0	1	m_6
1	1	1	1	1	m_7



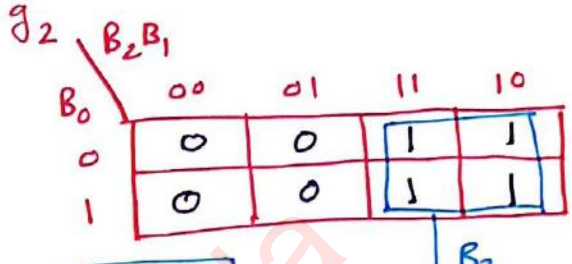
$S = m_1 + m_2 + m_4 + m_7$

$C = m_3 + m_5 + m_6 + m_7$

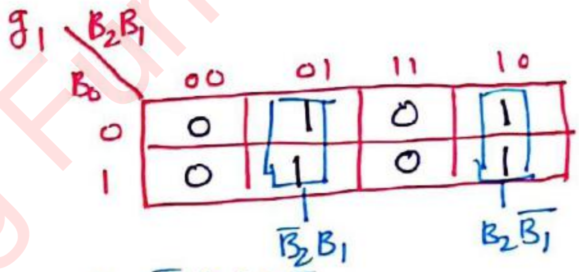
Binary to Gray Code Converter



Inputs			Outputs		
B_2	B_1	B_0	g_2	g_1	g_0
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

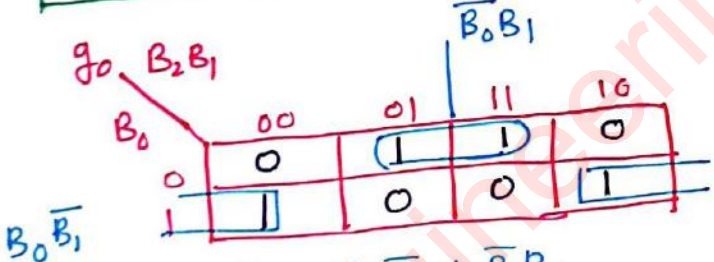


$\boxed{g_2 = B_2}$



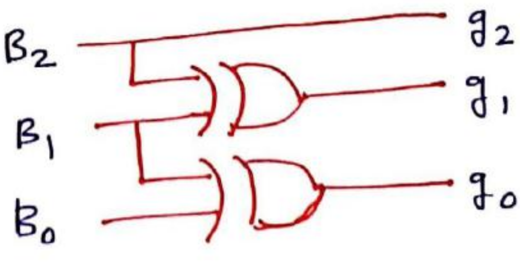
$g_1 = \overline{B_2}B_1 + B_2\overline{B_1}$

$\boxed{g_1 = B_2 \oplus B_1}$



$g_0 = B_0\overline{B_1} + \overline{B_0}B_1$

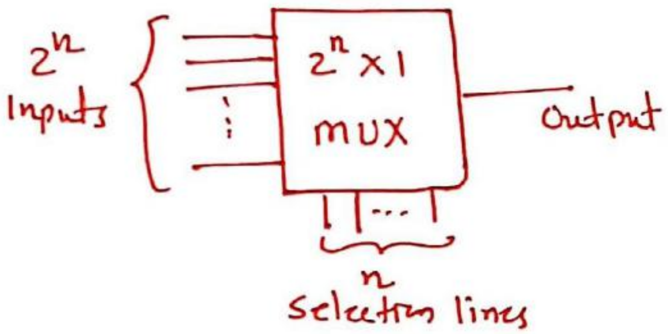
$\boxed{g_0 = B_0 \oplus B_1}$

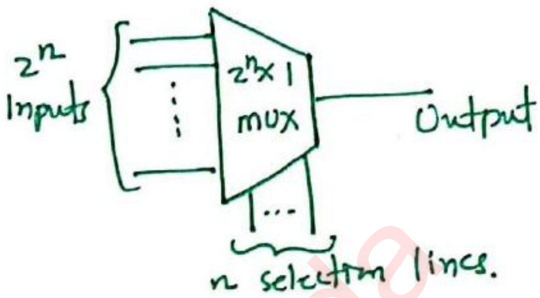


Multiplexer [MUX]

→ $[2^n \times 1]$ MUX
(2^n ↑ Inputs, 1 ↑ Output)

→ n is number of selection lines.





→ MUX IC's ⇝ MSI scale IC's.

Advantages

1] Complexity is less
2] Cost is less
3] less wiring.

Applications

1] Data Selector
2] Switch
3] combinational circuits.

Types → $[2^n \times 1]$ MUX

$[2 \times 1]$ MUX	$[4 \times 1]$ MUX	$[8 \times 1]$ MUX	$[16 \times 1]$ MUX
$n=1$	$n=2$	$n=3$	$n=4$

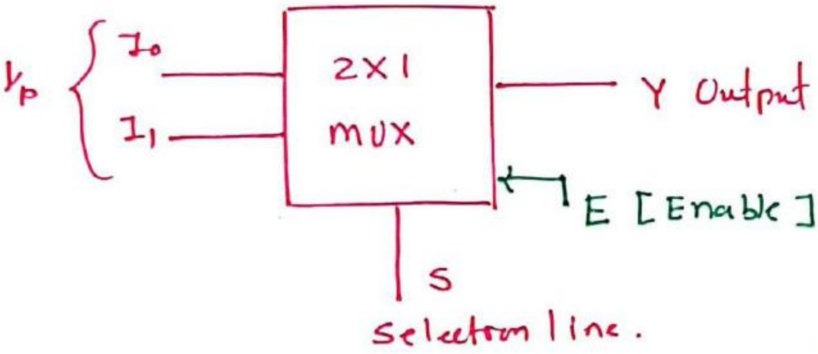
$[32 \times 1]$ MUX
$n=5$

2 x 1 Multiplexer 118

→ [2^n x 1] MUX

→ n = 1, 1 selection line

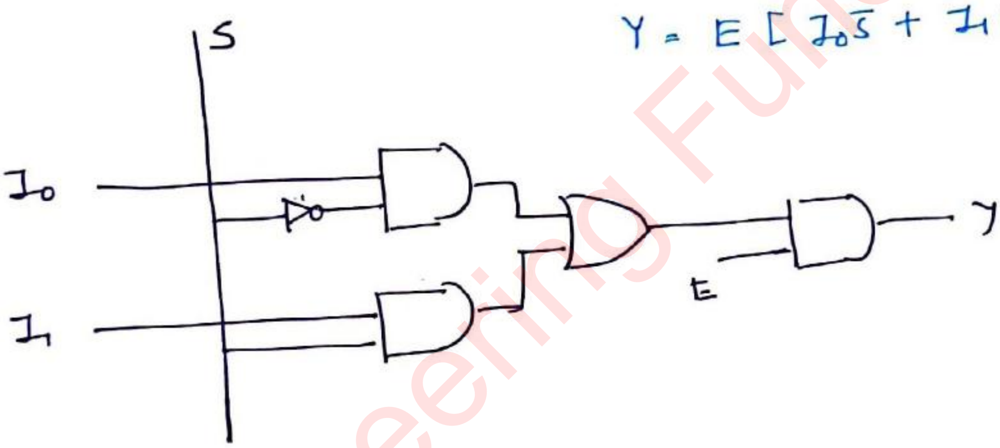
→ 2 Inputs, 1 Output.



E	S	Y
0	X	0
1	0	I_0
1	1	I_1

$$Y = I_0 \bar{S} E + I_1 S E$$

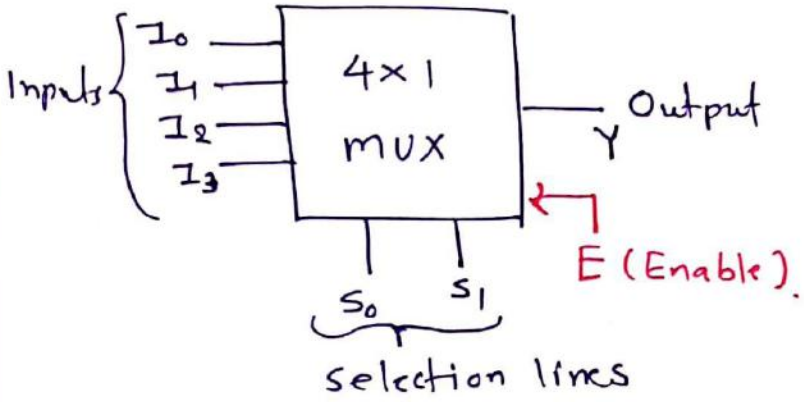
$$Y = E [I_0 \bar{S} + I_1 S]$$



4x1 MUX 119

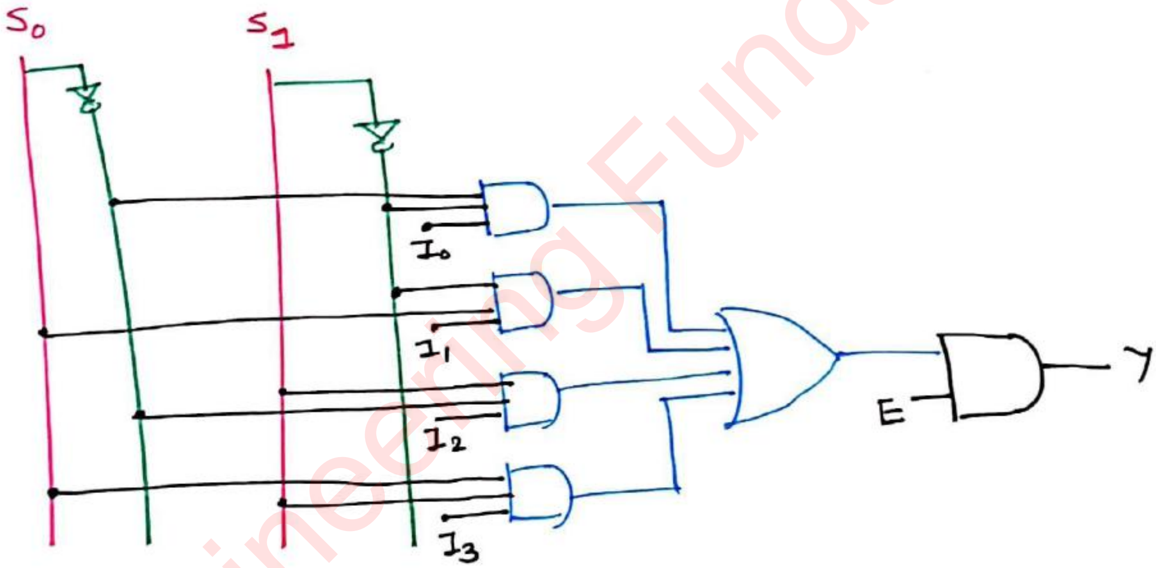
→ [$2^n \times 1$] MUX

⇒ $n = 2$, 2 Selection lines.



E	S_1	S_0	Y
0	X	X	0
1	0	0	I_0
1	0	1	I_1
1	1	0	I_2
1	1	1	I_3

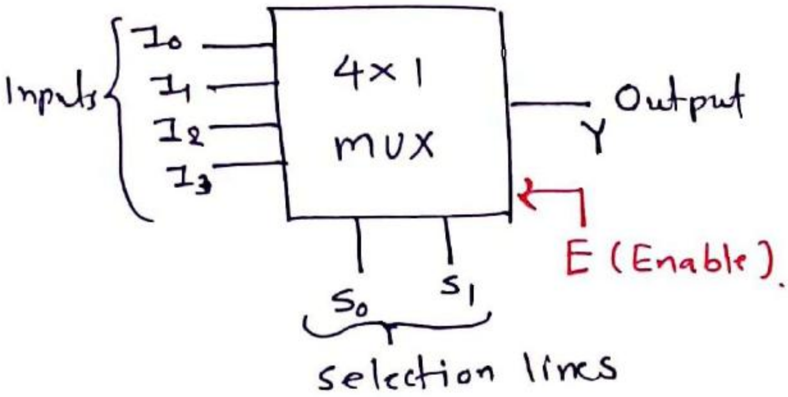
$$Y = E.[\,\bar{S_1}\bar{S_0} I_0 + \bar{S_1} S_0 I_1 + S_1 \bar{S_0} I_2 + S_1 S_0 I_3\,]$$



4x1 MUX

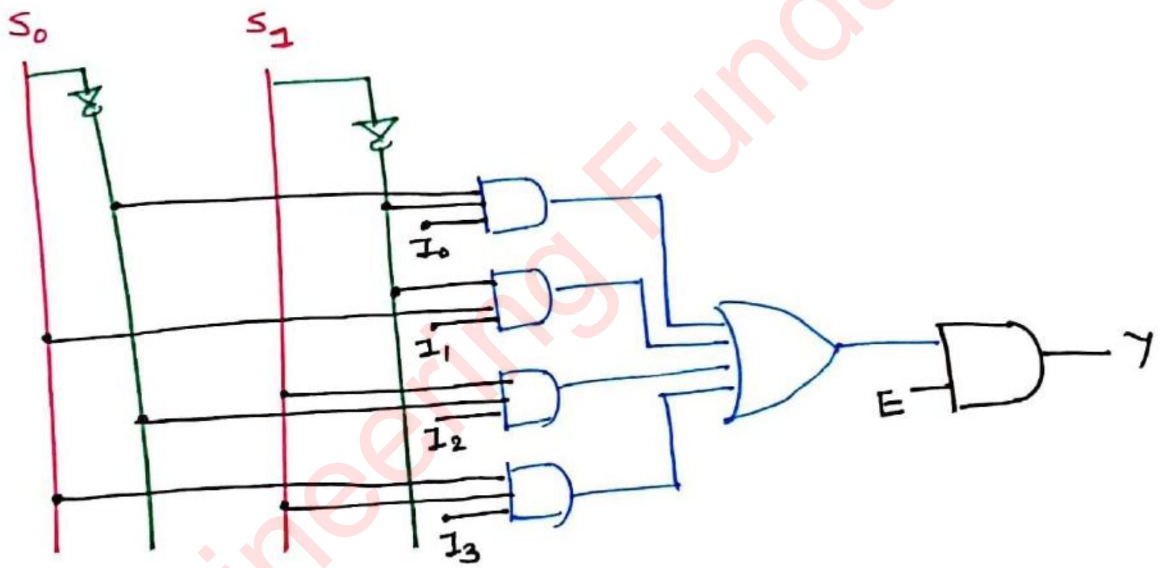
→ [$2^n \times 1$] MUX

⇒ $n = 2$, 2 Selection lines.



E	S_1	S_0	Y
0	X	X	0
1	0	0	I_0
1	0	1	I_1
1	1	0	I_2
1	1	1	I_3

$$Y = E.[\,\bar{S_1}\bar{S_0}I_0 + \bar{S_1}S_0I_1 + S_1\bar{S_0}I_2 + S_1S_0I_3\,]$$



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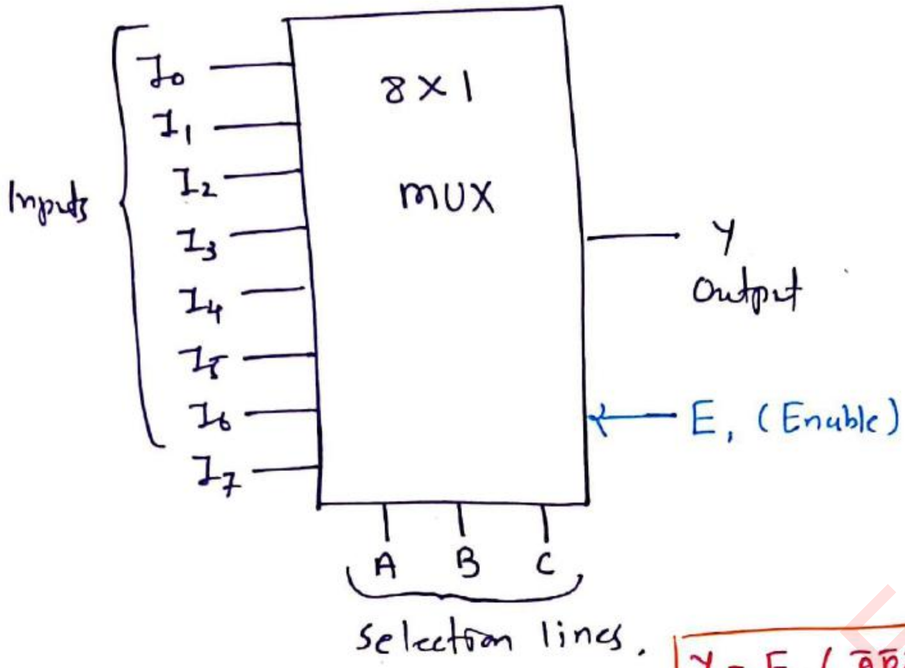
8 X 1 MUX 120

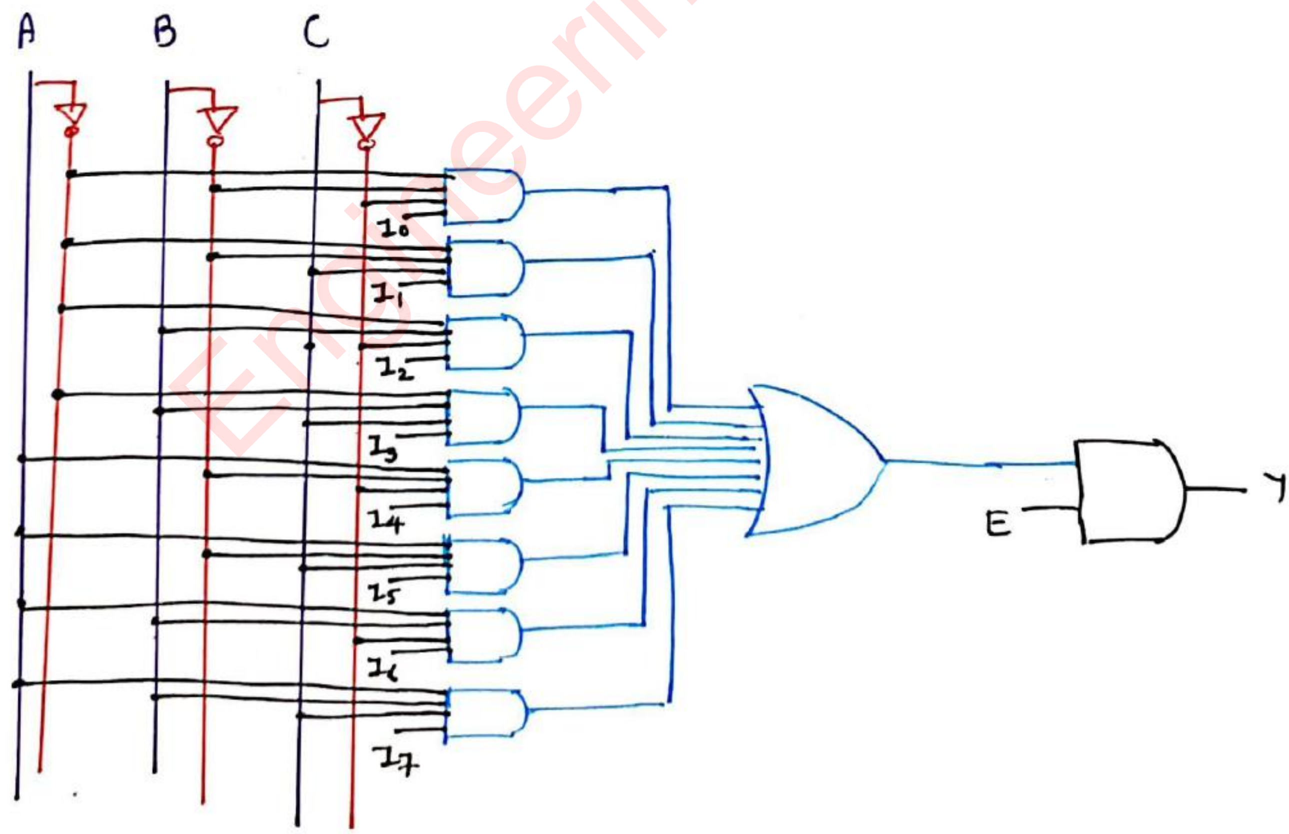
→ $[2^n \times 1]$ MUX

→ $n=3$, 3 selection lines



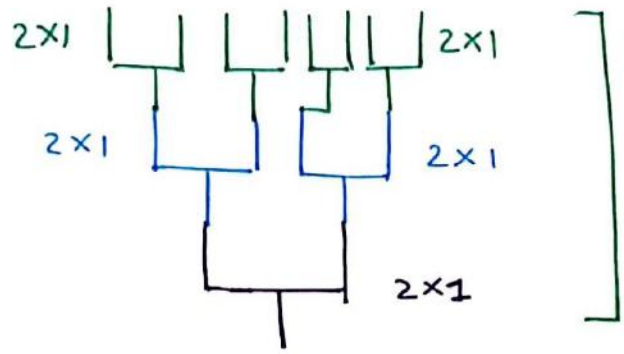
E	A	B	C	Y
0	X	X	X	0
1	0	0	0	I_0
1	0	0	1	I_1
1	0	1	0	I_2
1	0	1	1	I_3
1	1	0	0	I_4
1	1	0	1	I_5
1	1	1	0	I_6
1	1	1	1	I_7

$$\boxed{Y = E.(\bar{A}\bar{B}\bar{C}I_0 + \bar{A}\bar{B}CI_1 + \bar{A}B\bar{C}I_2 + \bar{A}BCI_3 + A\bar{B}\bar{C}I_4 + A\bar{B}CI_5 + AB\bar{C}I_6 + ABCI_7)}$$



MUX Tree 121

→ MUX Tree is used to obtain higher order MUX using Lower Order MUX.



8X1 MUX By 2X1 MUX

MUX Tree

1] How many 4X1 MUX is req^ed to make 32X1 MUX.

$\frac{32}{4} = 8$

$\frac{8}{4} = 2$

$\frac{2}{4} = 0.5 < 1$

$= 8 + 2 + 1$
$= 11$

2] How many 2X1 MUX is req^ed to get 64X1 MUX.

$\frac{64}{2} = 32$

$\frac{32}{2} = 16$

$\frac{16}{2} = 8$

$\frac{8}{2} = 4$

$\frac{4}{2} = 2$

$\frac{2}{2} = 1$

$= 32 + 16 + 8 + 4 + 2 + 1$
$= 63$

3] How many 8X1 MUX req^ed to get 64X1 MUX.

$\frac{64}{8} = 8$

$\frac{8}{8} = 1$

$= 8 + 1$
$= 9$

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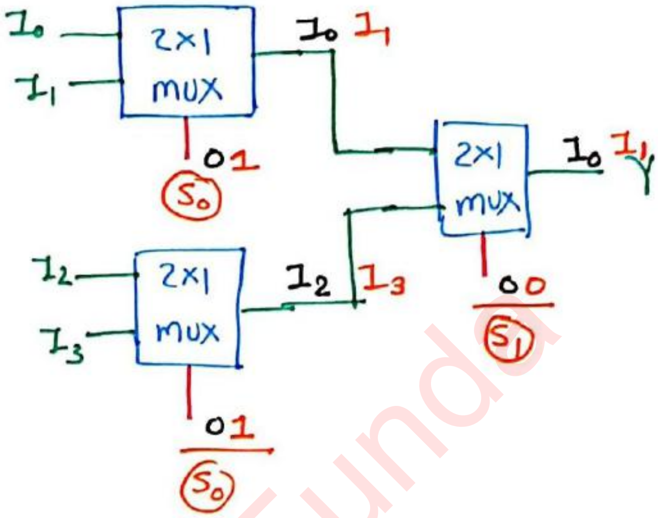
Design 4X1 MUX using 2X1 MUX. 122

→ 1st find, How many 2X1 MUX req.ed to get 4X1 MUX.

$\frac{4}{2} = 2 \qquad = 2 + 1$

$\frac{2}{2} = 1 \qquad = 3$

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3



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Design 8X1 MUX using 2X1 MUX 123

→ 1st Find, How many 2X1 MUX is req.cd to get 8X1 MUX

$\frac{8}{2} = 4$

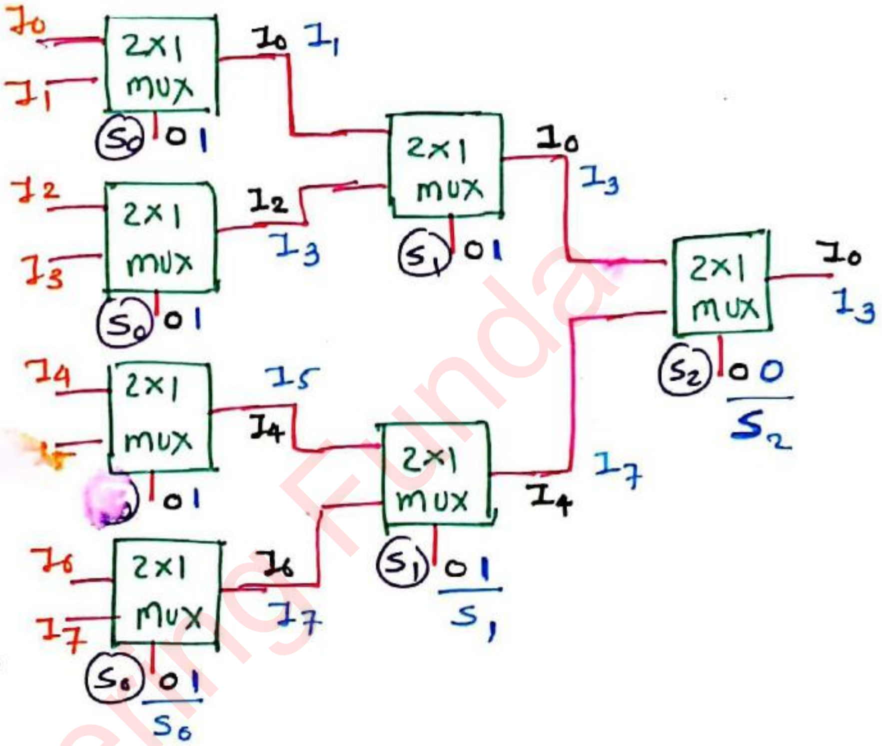
$\frac{4}{2} = 2$

$\frac{2}{2} = 1$

$= 4 + 2 + 1$

$= 7$

S_2	S_1	S_0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7



8x1 MUX using 4x1 MUX 12h

→ 1^{st} step is to find, How many 4x1 MUX is req.^{ed} to get 8x1 MUX

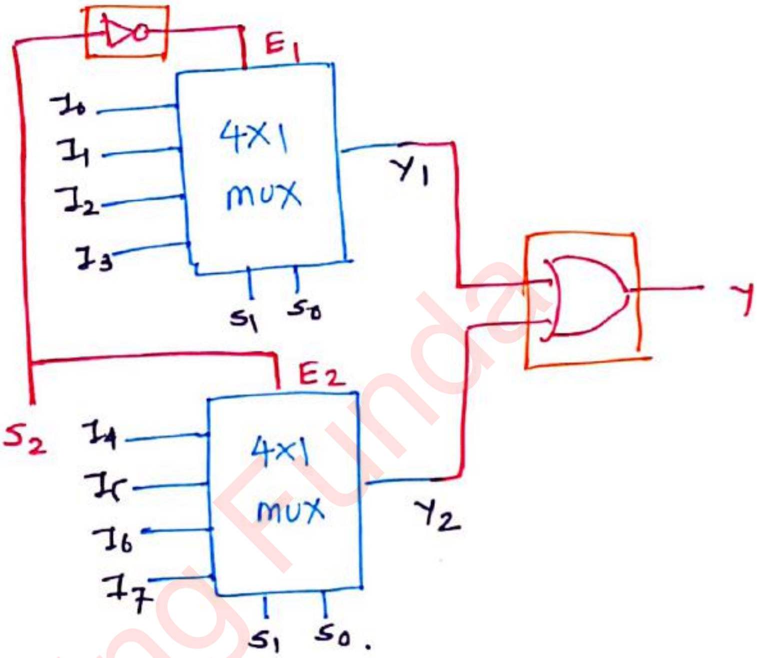
$\frac{8}{4} = 2$ $\quad = 2 + 0.5$

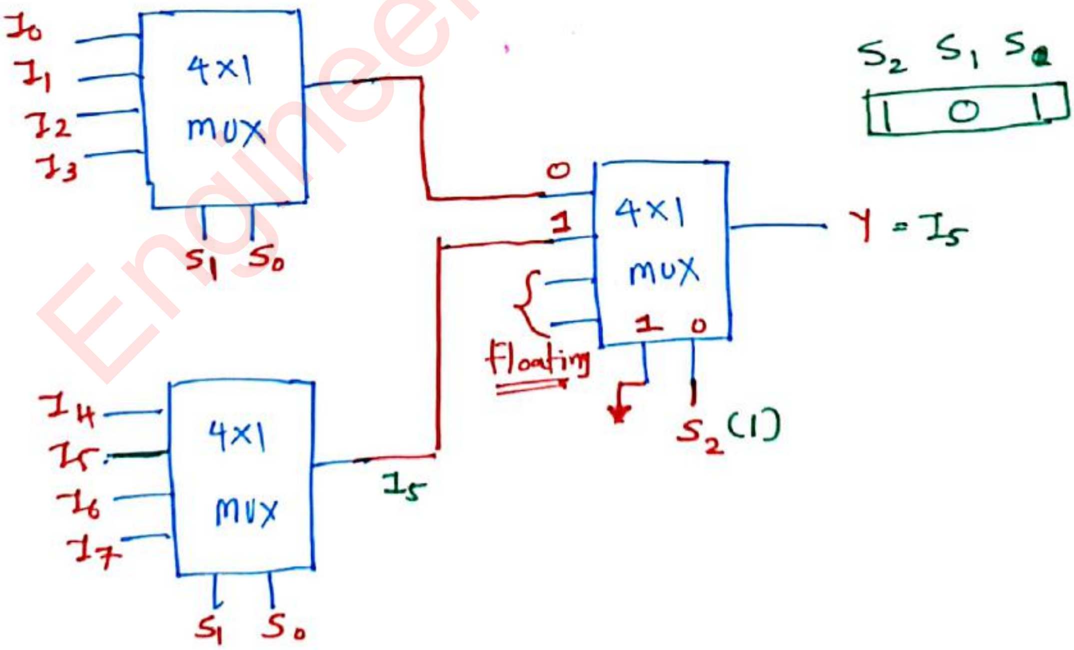
$\frac{2}{4} = 0.5 < 1$ $\quad = 2.5$

$= 3$ [without Additional gates]

→

S_2	S_1	S_0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7





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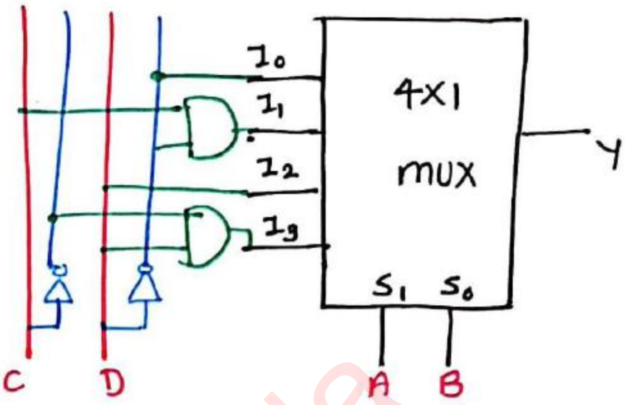
SOP Implementation by MUX 125

Function $F(A,B,C,D) = \Sigma_m(0,2,6,9,11,13)$ make it by 4X1 MUX.

F

CD \ AB	00	01	11	10
00	1 ₀	4	12	8
01	1	5	1 (13)	1 (9)
11	3	7	15	1 (11)
10	1 (2)	1 (6)	14	10

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3



$I_0 = \bar{D}$ | $I_2 = D$

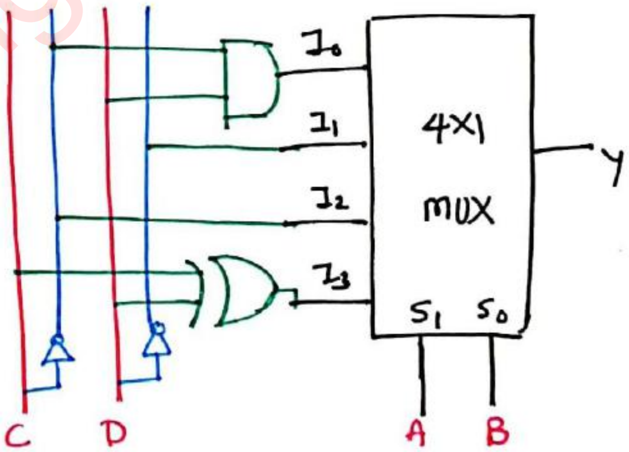
$I_1 = C\bar{D}$ | $I_3 = \bar{C}D$

Function $F(A,B,C,D) = \Sigma_m(1,4,6,8,9,13,14)$ make it by 4X1 MUX.

F

CD \ AB	00	01	11	10
00	0	1 (4)	12	1 (8)
01	1 (1)	5	1 (13)	1 (9)
11	3	7	15	11
10	2	1 (6)	1 (14)	10

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3



$I_0 = \bar{C}D$ | $I_2 = \bar{C}$

$I_1 = \bar{D}$ | $I_3 = \bar{C}D + C\bar{D}$

$= C \oplus D$

Full Adder by 2X1 MUX

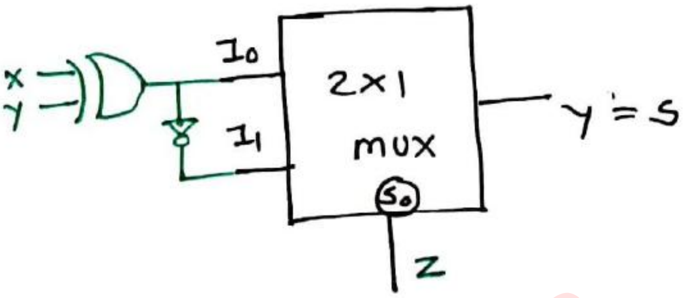
127

X	Y	Z	S	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

S

z \ xy	00	01	11	10
0		1		1
1	1		1	

S_0	Y $= x \oplus y$
0	$I_0 = \bar{x}y + x\bar{y}$
1	$I_1 = \bar{x}\bar{y} + xy = \overline{x \oplus y}$



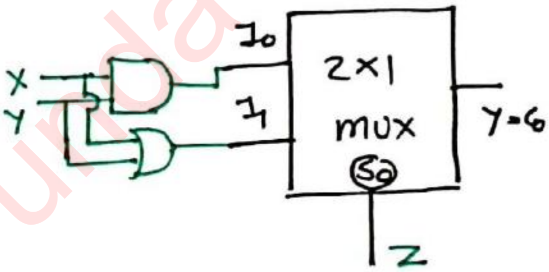
Co

z \ xy	00	01	11	10
0			1	
1		1	1	1

$I_0 = x.y$

$I_1 = y + x$

S_0	$Y = C_0$
0	I_0
1	I_1



Full Adder by 2X1 MUX

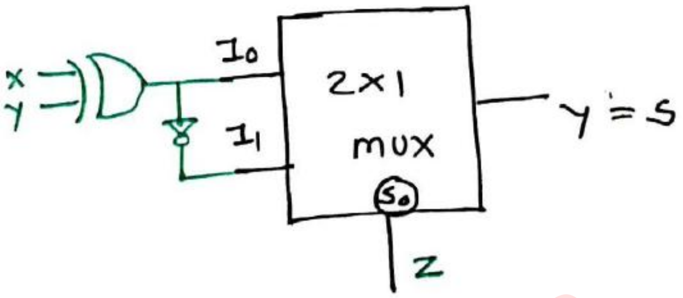
127

X	Y	Z	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

S

Z \ XY	00	01	11	10
0		1		1
1	1		1	

S_0	Y
	$= X \oplus Y$
0	$I_0 = \bar{x}y + x\bar{y}$
1	$I_1 = \bar{x}\bar{y} + xy$
	$= \overline{x \oplus y}$



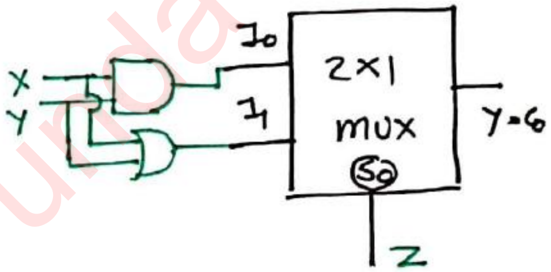
C_o

Z \ XY	00	01	11	10
0			1	
1		1	1	1

$I_0 = x \cdot y$

$I_1 = y + x$

S_0	$Y = C_o$
0	I_0
1	I_1



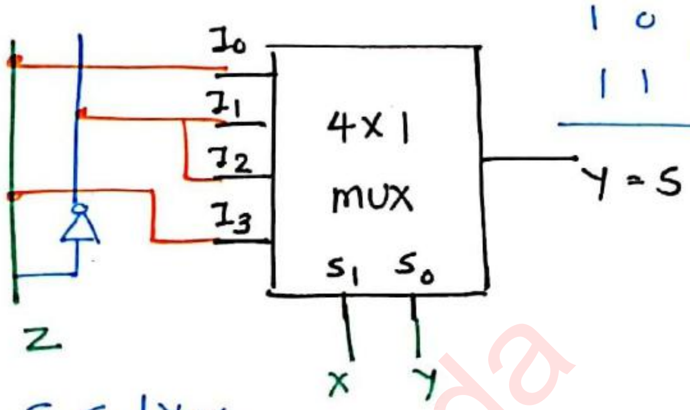
Full Adder using 4X1 MUX

X	Y	Z	S	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

S

Z \ XY	00	01	11	10
0		1		1
1	1		1	

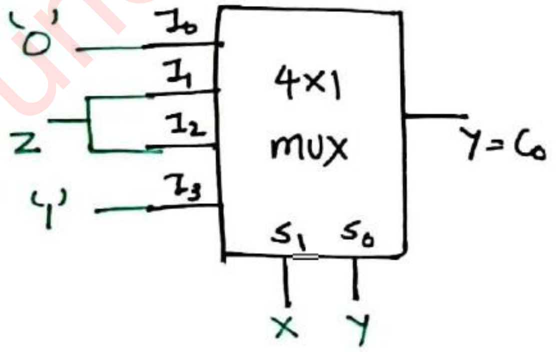
S_1	S_0	$Y = S$
0	0	$I_0 = Z$
0	1	$I_1 = \overline{Z}$
1	0	$I_2 = \overline{Z}$
1	1	$I_3 = Z$



C

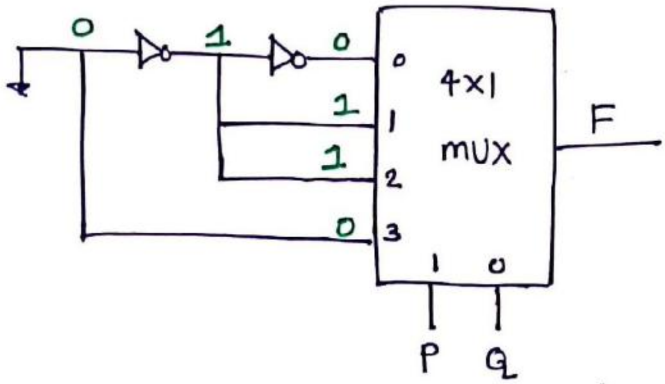
Z \ XY	00	01	11	10
0			1	
1		1	1	1

S_1	S_0	$Y = C_0$
0	0	$I_0 = 0$
0	1	$I_1 = Z$
1	0	$I_2 = Z$
1	1	$I_3 = 1$



Boolean function from Multiplexer Circuit 128

1)

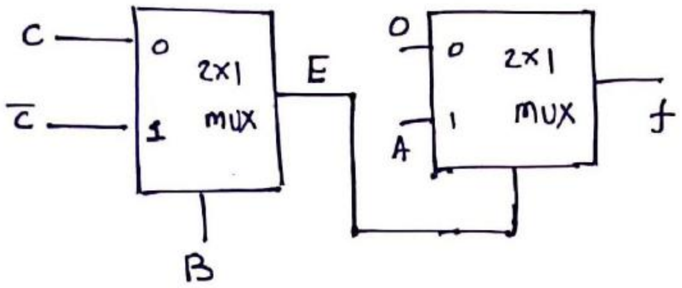


$$F = \bar{P}\bar{Q}.0 + \bar{P}Q.1 + P\bar{Q}.1 + PQ.0$$

$$F = \bar{P}Q + P\bar{Q}$$

$$\boxed{F = P \oplus Q}$$

2)



$$\rightarrow E = \bar{B}C + B\bar{C}$$

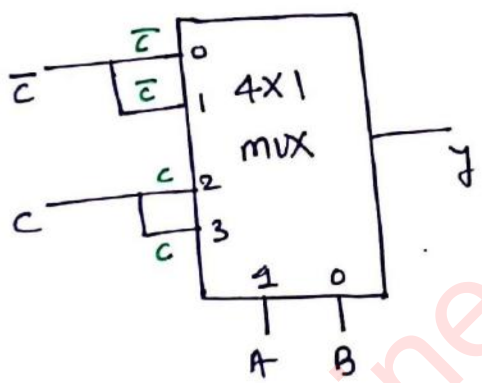
$$= B \oplus C$$

$$\rightarrow f = \bar{E}.0 + EA$$

$$= A.E$$

$$= A.(B \oplus C)$$

3)



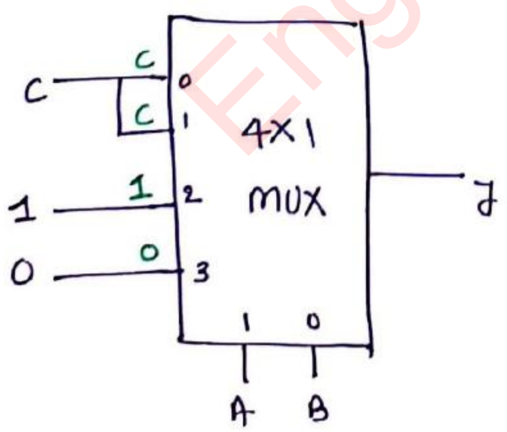
$$\rightarrow Y = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}C + ABC$$

$$= \bar{A}\bar{C}(\bar{B}+B) + AC(\bar{B}+B)$$

$$= \bar{A}\bar{C} + AC$$

$$= \overline{A \oplus C} \quad \text{or} \quad A \odot C$$

4)



$$\rightarrow Y = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}.1 + AB.0$$

$$= \bar{A}C(\bar{B}+B) + A\bar{B}$$

$$Y = \bar{A}C + A\bar{B}$$

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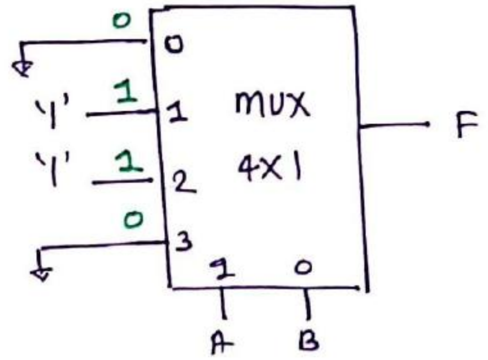
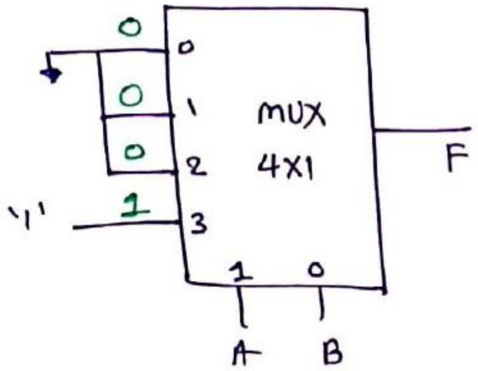
Identification of logic gate from multiplexer Circuit

1)



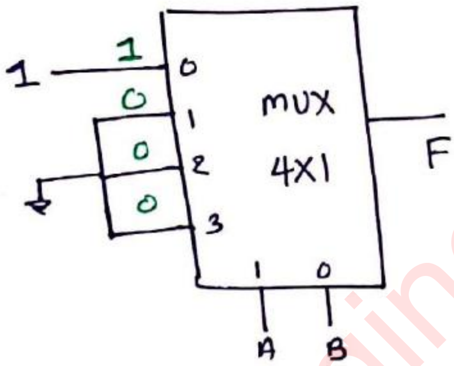
$$F = \bar{A}\bar{B}.0 + \bar{A}B.1 + A\bar{B}.1 + AB.0$$
$$= \bar{A}B + A\bar{B}$$
$$= A \oplus B$$ [XOR gate]

2)



$$F = \bar{A}\bar{B}.0 + \bar{A}B.0 + A\bar{B}.0 + AB.1$$
$$= A.B$$
[AND gate].

3)



$$F = \bar{A}\bar{B}.1 + \bar{A}B.0 + A.\bar{B}.0 + AB.0$$
$$= \bar{A}\bar{B}$$
$$= \overline{(A+B)}$$ [NOR gate]

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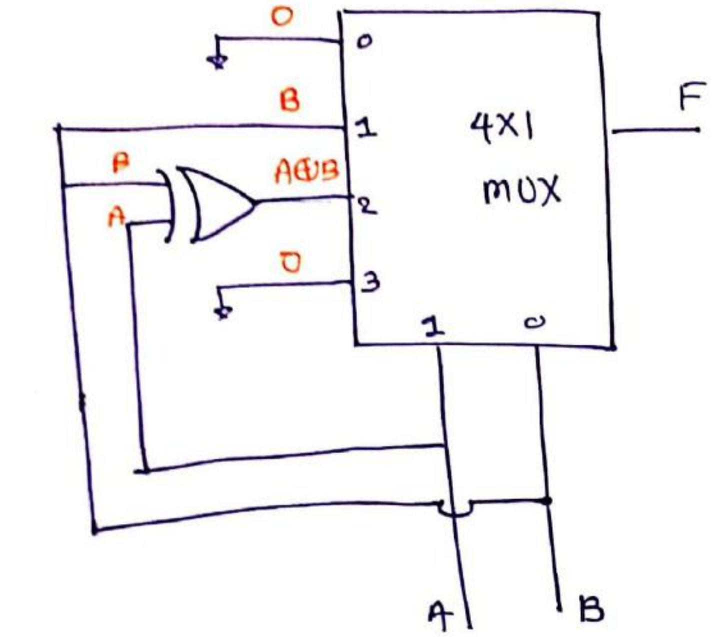
Examples based on Multiplexer



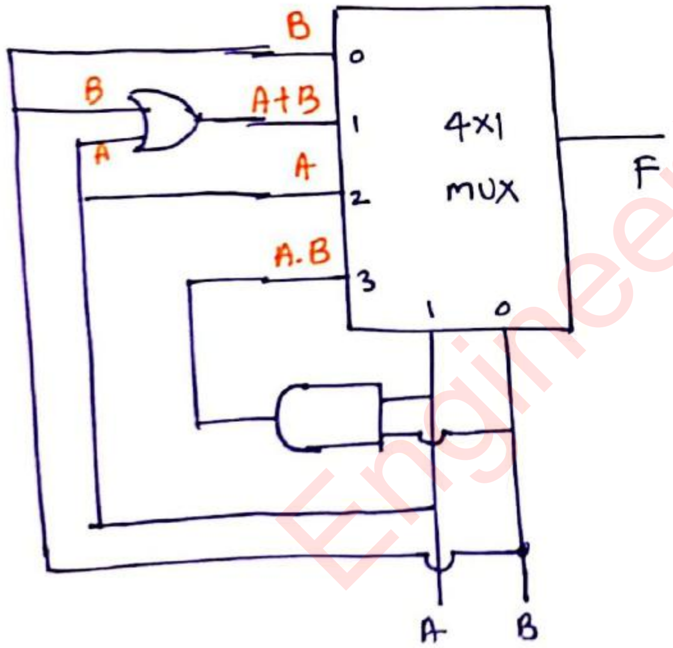
$$F = \bar{A}\bar{B}.0 + \bar{A}B.B + A\bar{B}(A\bar{B}+\bar{A}B) + AB.0$$

$$= \bar{A}B + A\bar{B}A\bar{B} + A\bar{B}\bar{A}B$$

$$= \bar{A}B + A\bar{B} + 0$$

$$= \bar{A}B + A\bar{B}$$

$$= A \oplus B$$



$$F = \bar{A}\bar{B}.B + \bar{A}B.(A+B) + A\bar{B}.A + AB.AB$$

$$= 0 + \bar{A}BA + \bar{A}BB + A\bar{B} + AB$$

$$= \underset{1}{\bar{A}B} + \underset{2}{A\bar{B}} + \underset{3}{AB}$$

$$= \sum_m (1,2,3)$$

$$- [0,1,2,3]$$

$$= \prod_m [0]$$

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GATE / ISRO Examples based on Multiplexer

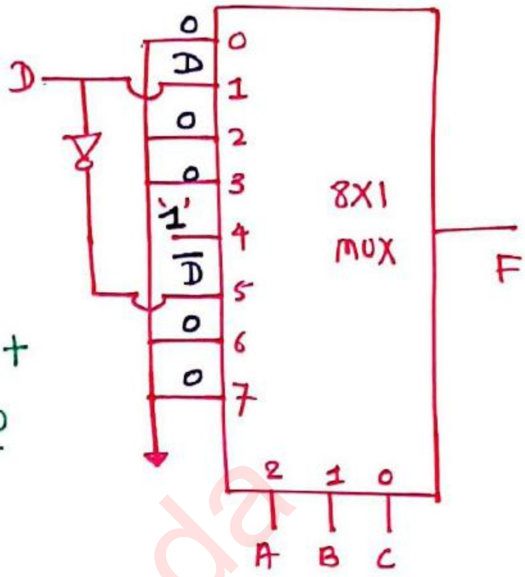
1] Function $F(A,B,C,D)$ can be expressed as

✓ a] $\Sigma_m(3,8,9,10)$

b] $\Sigma_m(3,8,10,14)$

c] $\Pi(0,1,2,4,5,6,7,11,12,13,15)$

d] $\Pi(0,1,2,4,5,6,7,10,12,13,15)$



$\rightarrow F = \underline{\bar{A}\bar{B}\bar{C}.0} + \bar{A}\bar{B}C.D + \underline{\bar{A}B\bar{C}.0} + \underline{\bar{A}BC.0} +$

$\quad A\bar{B}\bar{C}.1 + A\bar{B}C.\bar{D} + \underline{AB\bar{C}.0} + \underline{ABC.0}$

$= \bar{A}\bar{B}CD + A\bar{B}\bar{C} + A\bar{B}C\bar{D}$

$\quad \underline{0011}\quad \underline{1000,\ 1001}\quad \underline{1010}$

$\quad 3 \quad 8,9 \quad 10$

$= \Sigma_m(3,8,9,10)$

2] Find the correct statements.

A Multiplexer.

✓ a] Selects one of many inputs and transmits on single output.

✗ b] Routs the data from single input to many of outputs.

✓ c] It converts parallel data to serial data

✓ d] is a combinational circuit.

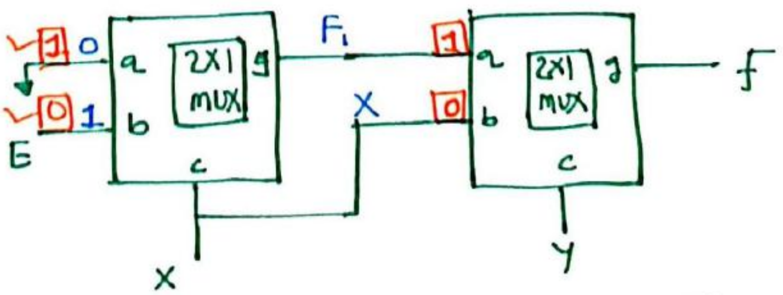
3] If function $g = ac + b\bar{c}$ then find the output f

(a) $X \oplus Y$

(b) $XE + X\bar{Y}$

✓ (c) $X\bar{Y} + E\bar{X}Y$

(d) None of these



$- \ g = \bar{c}a + cb$ ✗

$- \ g = \bar{c}b + ca$ ✓

$F_1 = \bar{X}E + X.0$

$\quad = \bar{X}E$

$\rightarrow f = \bar{Y}X + YF_1$

$\quad = \bar{Y}X + Y\bar{X}E$

Coincidence Logic 132

- To get Coincidence logic following Condⁿ should get satisfied.

Cond.ⁿ ① Inputs terminals ≥ 2, Output terminal $= 1$

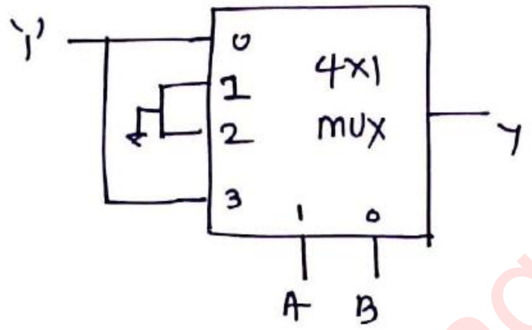
Cond.ⁿ ② If all I/p's $= 0$, O/p $= 1$

If all I/p's $= 1$, O/p $= 1$

e.g. Two terminal XNOR gate.

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

e.g.



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Demultiplexer and 1 to 2 Demultiplexer | 33

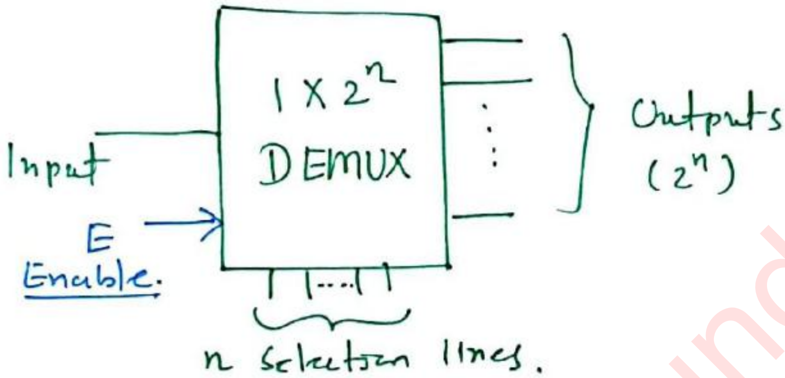
→ It is having reverse operation to that of multiplexer.

→ Basic form of Demultiplexer is $[\underline{1} \times \underline{2^n}]$ DeMUX.

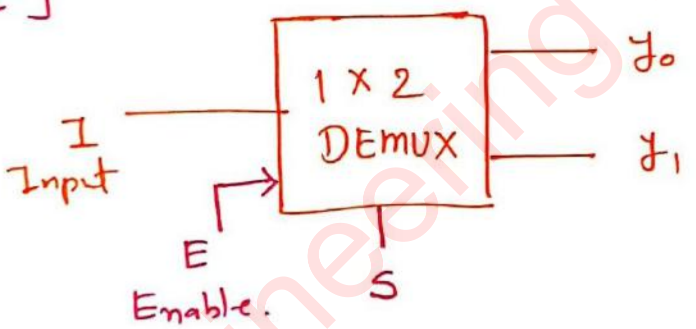
→ Demultiplexer is serial to parallel converter.

Input ↗ 1, Outputs = 2^n ↖ 2^n

[n = No of selection lines].



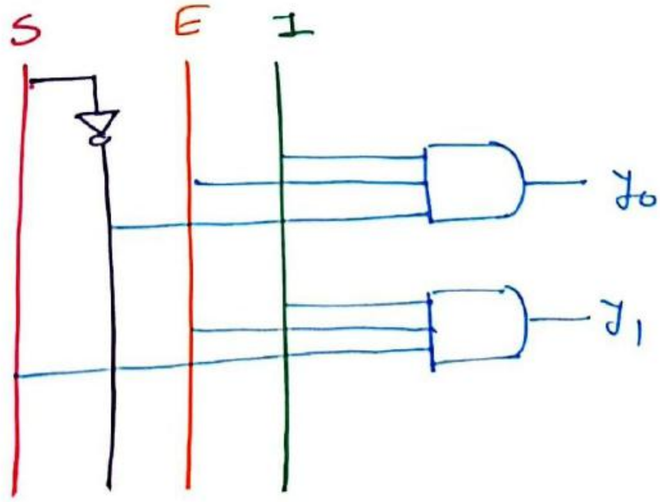
- 1 to 2 Demultiplexer
- $[1 \text{ to } 2^n]$
- $n = 1$



E	S	Y_0	Y_1
0	X	0	0
1	0	I	0
1	1	0	I

- $y_0 = I E \bar{S}$

  $y_1 = I E S$



Applications

- Data Distribution
- Serial to parallel Converter.
- One to many Circuit.

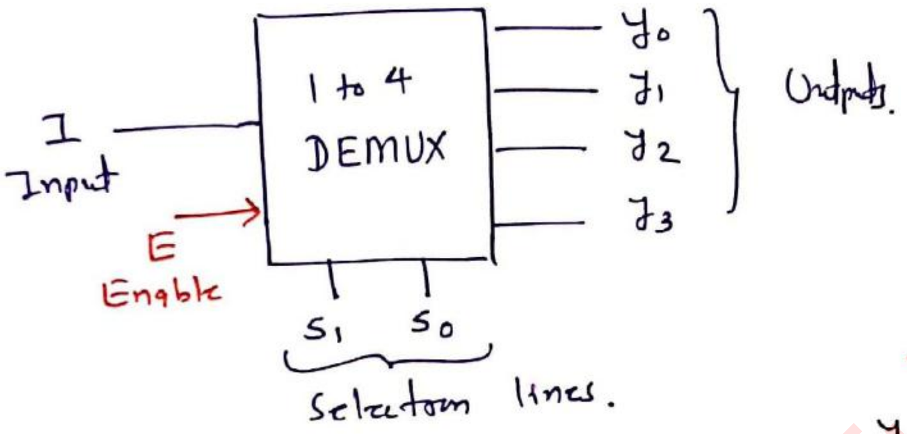
1 to 4 Demultiplexer

1 → 1 Input

4 → 4 Outputs.

→ [1 x 2^n] DeMux

→ n = 2, Selection lines.



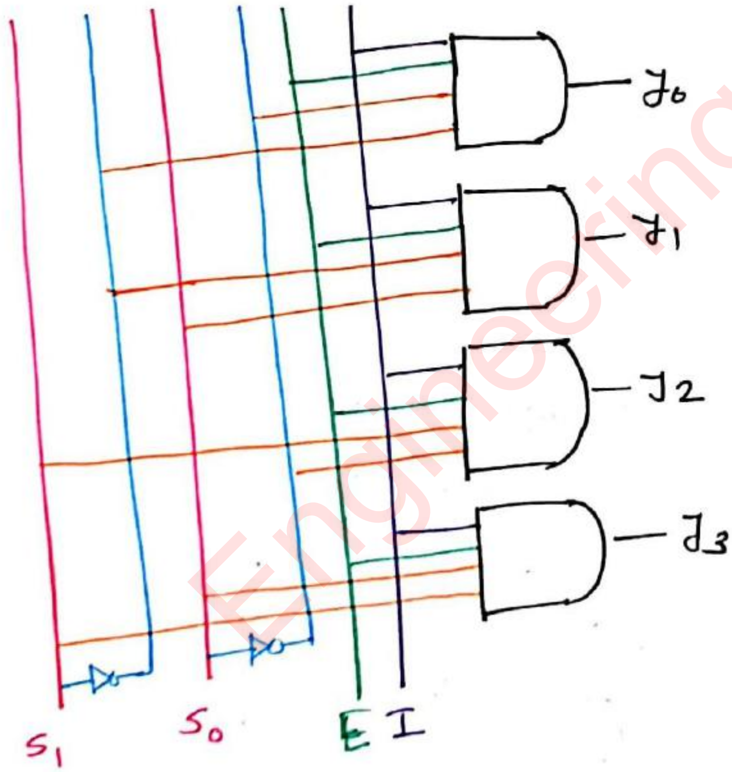
E	S_1	S_0	Y_0	Y_1	Y_2	Y_3
0	X	X	0	0	0	0
1	0	0	I	0	0	0
1	0	1	0	I	0	0
1	1	0	0	0	I	0
1	1	1	0	0	0	I

$y_0 = I E \bar{S_1} \bar{S_0}$

$y_1 = I E \bar{S_1} S_0$

$y_2 = I E S_1 \bar{S_0}$

$y_3 = I E S_1 S_0$

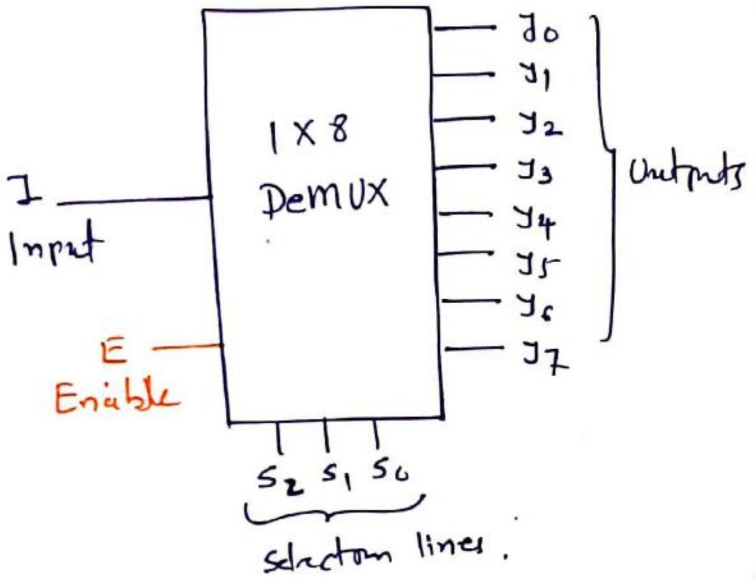


1 to 8 Demultiplexer

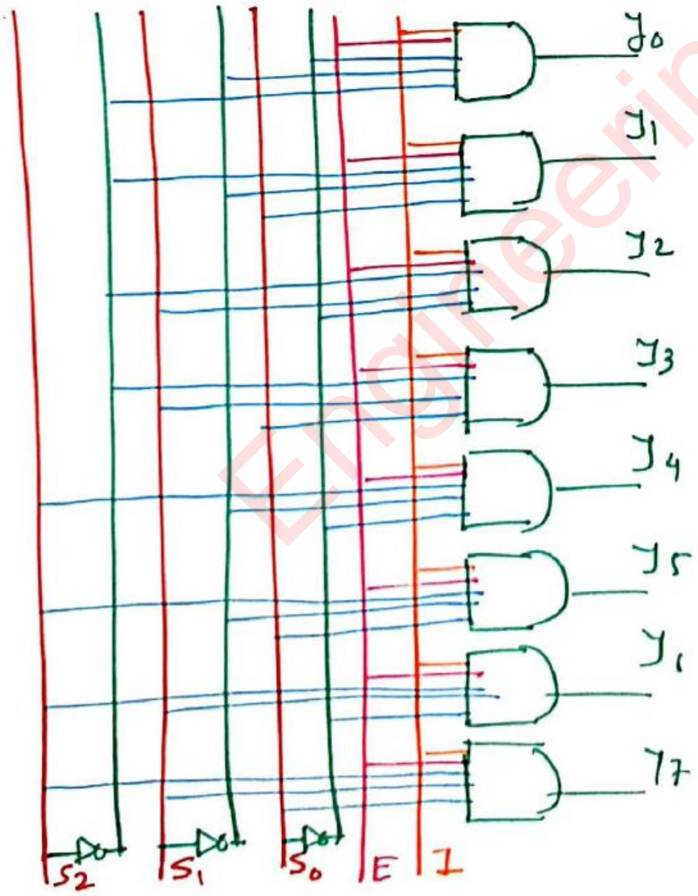
1 Input → 1   8 ← 8 Outputs.

→ $[1 \times 2^n]$ DeMUX

→ $n = 3$, Selection lines.



E	S_2	S_1	S_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
0	X	X	X	0	0	0	0	0	0	0	0
1	0	0	0	I	0	0	0	0	0	0	0
1	0	0	1	0	I	0	0	0	0	0	0
1	0	1	0	0	0	I	0	0	0	0	0
1	0	1	1	0	0	0	I	0	0	0	0
1	1	0	0	0	0	0	0	I	0	0	0
1	1	0	1	0	0	0	0	0	I	0	0
1	1	1	0	0	0	0	0	0	0	I	0
1	1	1	1	0	0	0	0	0	0	0	I



$y_0 = I E \overline{S_2}\,\overline{S_1}\,\overline{S_0}$

$y_1 = I E \overline{S_2}\,\overline{S_1}\,S_0$

$y_2 = I E \overline{S_2}\,S_1\,\overline{S_0}$

$y_3 = I E \overline{S_2}\,S_1\,S_0$

$y_4 = I E S_2\,\overline{S_1}\,\overline{S_0}$

$y_5 = I E S_2\,\overline{S_1}\,S_0$

$y_6 = I E S_2\,S_1\,\overline{S_0}$

$y_7 = I E S_2\,S_1\,S_0$

Full Subtractor using 1:8 DeMUX. 136

(A − B − Bin)

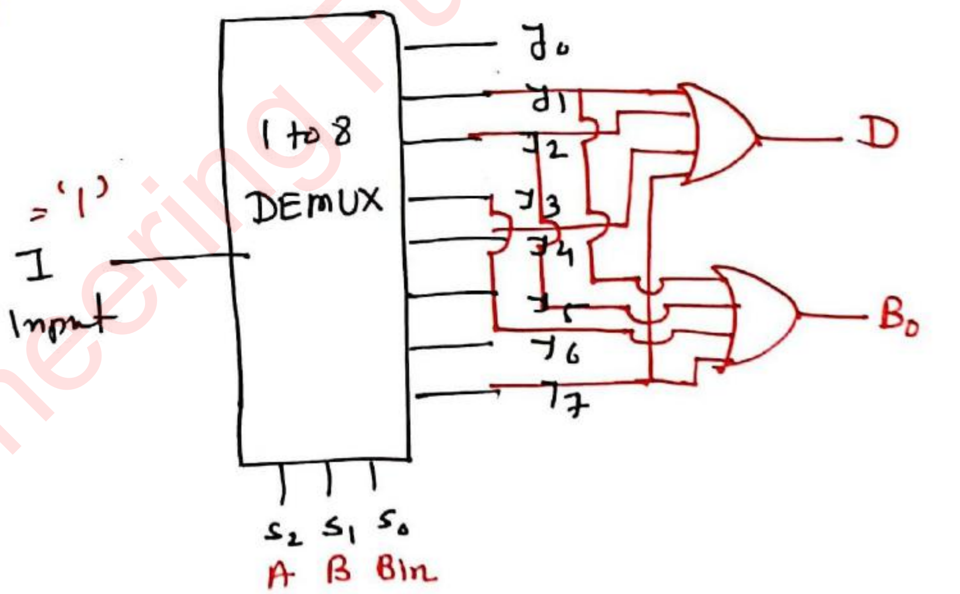
1 Input, 8 outputs → [1 × 2^n] Demux.
→ n = 3, Selection lines.

	A	B	Bin	D	Bo
m_0	0	0	0	0	0
m_1	0	0	1	1	1
m_2	0	1	0	1	1
m_3	0	1	1	0	1
m_4	1	0	0	1	0
m_5	1	0	1	0	0
m_6	1	1	0	0	0
m_7	1	1	1	1	1

S_2	S_1	S_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
0	0	0	I	0	0	0	0	0	0	0
0	0	1	0	I	0	0	0	0	0	0
0	1	0	0	0	I	0	0	0	0	0
0	1	1	0	0	0	I	0	0	0	0
1	0	0	0	0	0	0	I	0	0	0
1	0	1	0	0	0	0	0	I	0	0
1	1	0	0	0	0	0	0	0	I	0
1	1	1	0	0	0	0	0	0	0	I

→ $D = \Sigma m(1, 2, 4, 7)$

$B_o = \Sigma m(1, 2, 3, 7)$



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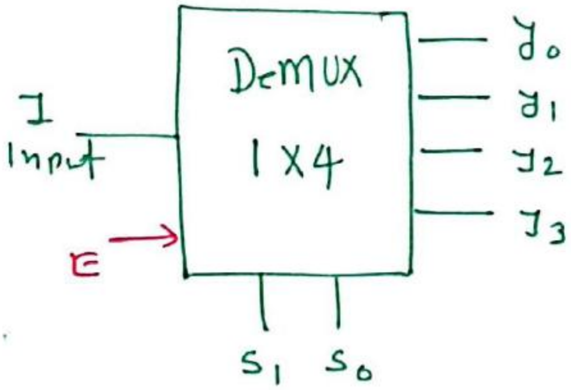
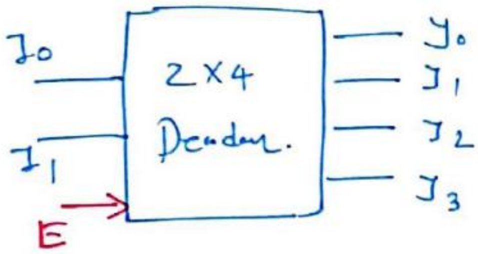
DeMUX as Decoder 137





→ If $I = '1'$

→ $S_1 S_0 = I_0 I_1$

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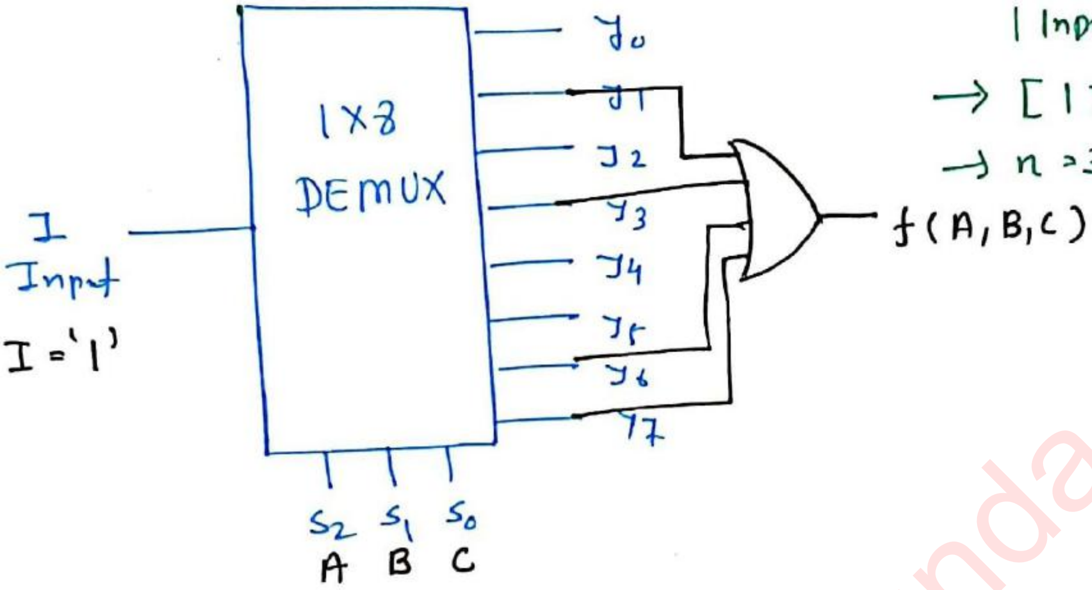
Implementation of boolean expression using DeMUX.

Implement $F(A, B, C) = \Sigma m(1, 3, 6, 7)$ using $\underline{1} \times \underline{8}$ DeMUX.

1 Input, 8 Outputs.

→ $[1 \times 2^n]$ DeMUX

→ $n = 3$, selection lines.



→ I = '1'

- Implement $f(A, B, C) = AB + B\bar{A} + C$ using $\underline{1} \times \underline{8}$ DeMUX

1 Input, 8 Outputs.

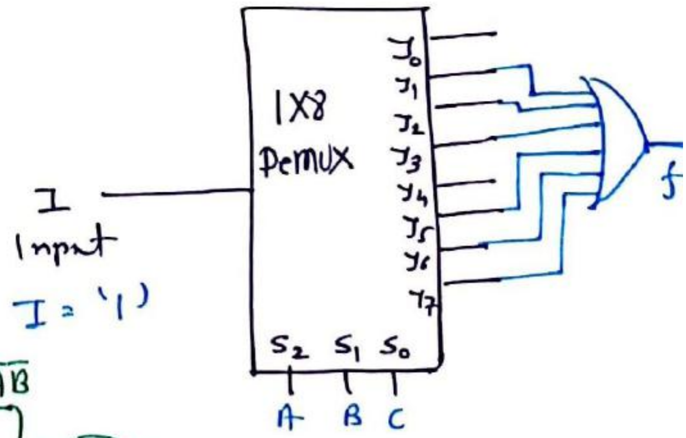
→ $[1 \times 2^n]$ DeMUX

→ $n = 3$ Selection lines

f

C \ AB	00	01	11	10
0	$_0$	1 $_2$	1 $_6$	$_4$
1	1 $_1$	1 $_3$	1 $_7$	1 $_5$

$f(A, B, C) = \Sigma m(1, 2, 3, 5, 6, 7)$



- If $y = \underset{3}{AB} + \underset{0}{\bar{A}\bar{B}}$, Implement using 1×4 DeMUX

→ $y = \Sigma m(0, 3)$