**A) HALF ADDER Code:-**

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-- Company:

-- Engineer:

-- Create Date: 20.09.2023 17:00:16

-- Design Name:

-- Module Name: HA - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

-- Dependencies:

-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity HA is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

sum : out STD\_LOGIC;

carry : out STD\_LOGIC);

end HA;

architecture Behavioral of HA is

begin

sun<= a xor b;

carry<= a and b;

end Behavioral;

**HALF ADDER Test Bench:-**

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-- Company:

-- Engineer:

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-- Create Date: 20.09.2023 17:05:37

-- Design Name:

-- Module Name: HA\_tb - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

--

----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity HA\_tb is

-- Port ( );

end HA\_tb;

architecture Behavioral of HA\_tb is

component HA is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

sum : out STD\_LOGIC;

carry : out STD\_LOGIC);

end component;

signal a,b,sum,carry:STD\_LOGIC;

begin

U1: HA port map(a,b,sum,carry);

process

begin

a<='0';

b<='0';

wait for 100ns;

a<='0';

b<='1';

wait for 100ns;

a<='1';

b<='0';

wait for 100ns;

a<='1';

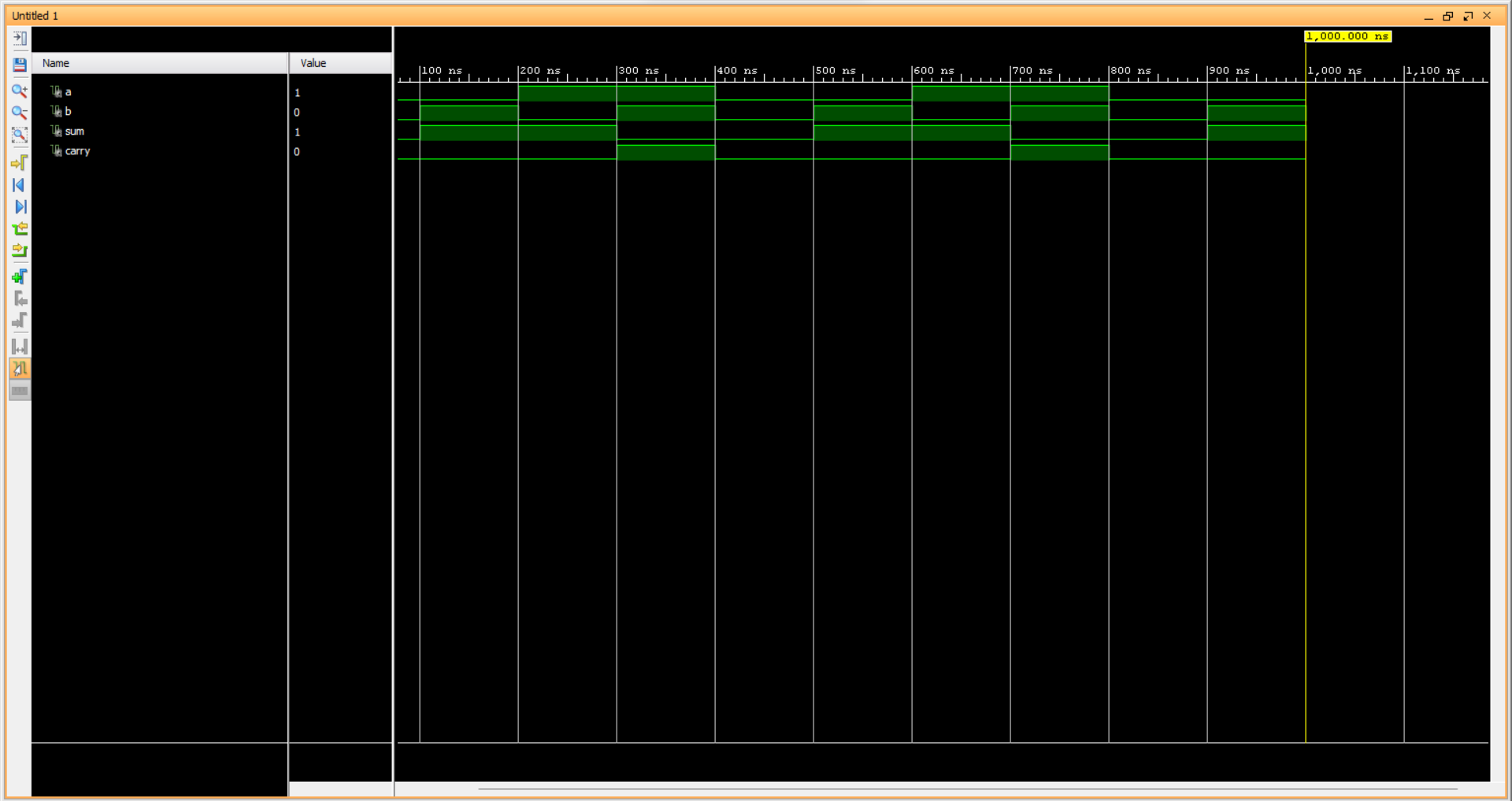
b<='1';

wait for 100ns;

end process;

end Behavioral;

**HALF ADDER O/P :-**

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**B) FULL ADDER Using Half Adders :-**

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-- Company:

-- Engineer:

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-- Create Date: 14.08.2023 15:20:44

-- Design Name:

-- Module Name: full\_adderst - Structural

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

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-- Dependencies:

--

-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

--

----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity full\_adderst is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

cin : in STD\_LOGIC;

s : out STD\_LOGIC;

cout : out STD\_LOGIC);

end full\_adderst;

architecture Structural of full\_adderst is

component half\_adder is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

s : out STD\_LOGIC;

c : out STD\_LOGIC);

end component;

component or\_gate is

Port ( p : in STD\_LOGIC;

q : in STD\_LOGIC;

r : out STD\_LOGIC);

end component;

signal temp1,temp2,temp3 : std\_logic;

begin

u1: half\_adder port map(a,b,temp1,temp2);

u2: half\_adder port map(temp1,cin,s,temp3);

u3: or\_gate port map(temp2,temp3,cout);

end Structural;

**Test Bench-**

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-- Company:

-- Engineer:

-- Create Date: 14.08.2023 15:35:08

-- Design Name:

-- Module Name: full\_addertb - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

-- Dependencies:

-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity full\_addertb is

-- Port ( );

end full\_addertb;

architecture Behavioral of full\_addertb is

component full\_adderst is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

cin : in STD\_LOGIC;

s : out STD\_LOGIC;

cout : out STD\_LOGIC);

end component;

signal a,b,cin,s,cout : std\_logic;

begin

u1 : full\_adderst port map(a,b,cin,s,cout);

process

begin

--stimuli generation

a<='0';

b<='0';

cin<='0';

wait for 100ns;

a<='0';

b<='0';

cin<='1';

wait for 100ns;

a<='0';

b<='1';

cin<='0';

wait for 100ns;

a<='0';

b<='1';

cin<='1';

wait for 100ns;

a<='1';

b<='0';

cin<='0';

wait for 100ns;

a<='1';

b<='0';

cin<='1';

wait for 100ns;

a<='1';

b<='1';

cin<='0';

wait for 100ns;

a<='1';

b<='1';

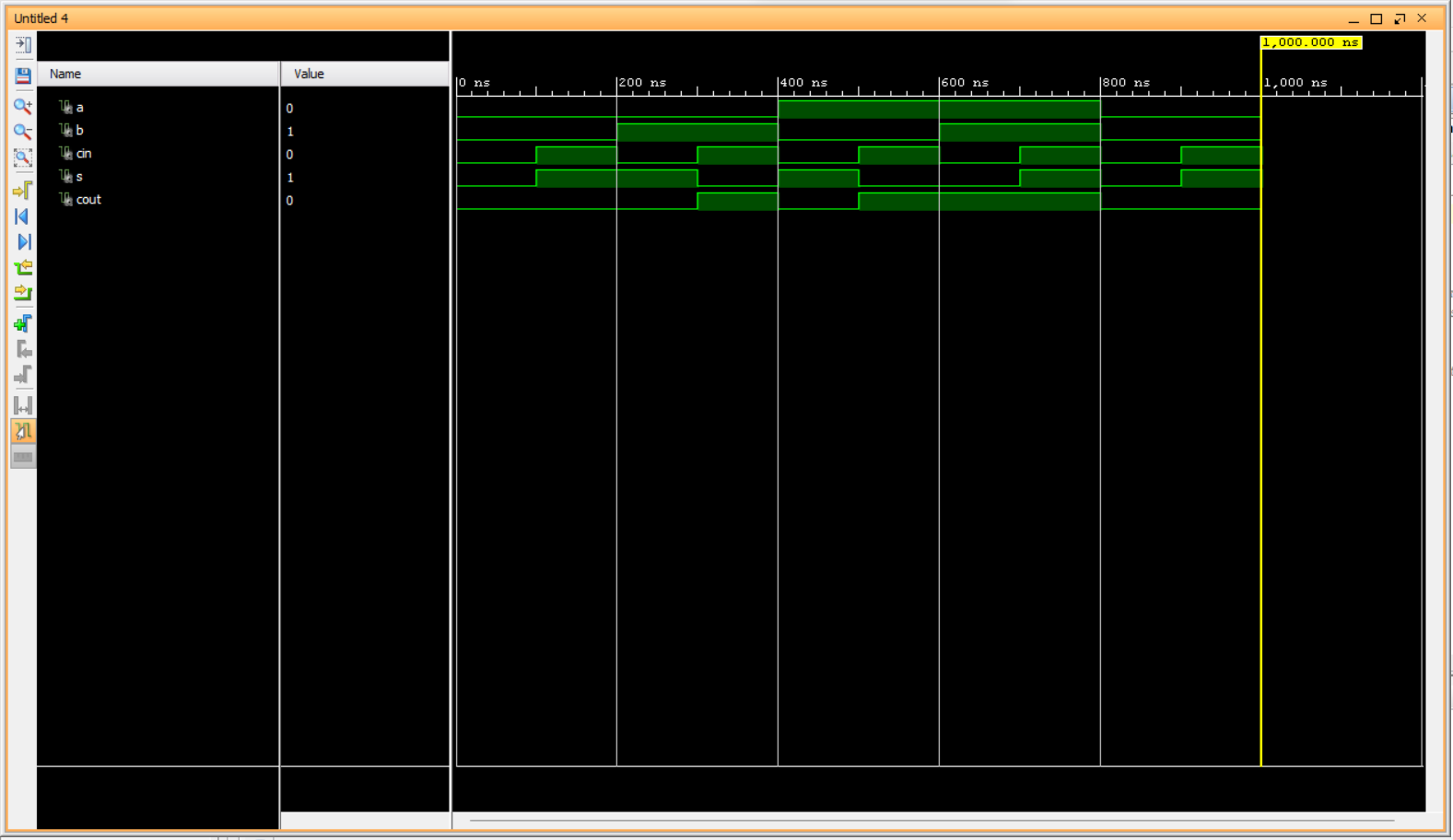
cin<='1';

wait for 100ns;

end process;

end Behavioral;

**FULL ADDER Using Half Adders O/P :-**

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**C) RCA Code :-**

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-- Company:

-- Engineer:

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-- Create Date: 21.08.2023 15:29:27

-- Design Name:

-- Module Name: RCA - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

--

----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity RCA is

Port ( a : in STD\_LOGIC\_VECTOR (3 downto 0);

b : in STD\_LOGIC\_VECTOR (3 downto 0);

Sum : out STD\_LOGIC\_VECTOR (3 downto 0);

Cout : out STD\_LOGIC;

Cin : in STD\_LOGIC);

end RCA;

architecture Behavioral of RCA is

COMPONENT full\_adder is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

cin : in STD\_LOGIC;

s : out STD\_LOGIC;

cout : out STD\_LOGIC);

end COMPONENT;

signal temp:std\_logic\_vector(3 downto 0);

begin

u1: full\_adder port map(a(0),b(0),cin,sum(0),temp(0));

u2: full\_adder port map(a(1),b(1),temp(0),sum(1),temp(1));

u3: full\_adder port map(a(2),b(2),temp(1),sum(2),temp(2));

u4: full\_adder port map(a(3),b(3),temp(2),sum(3),cout);

end Behavioral;

**RCA Test Bench:-**

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-- Company:

-- Engineer:

--

-- Create Date: 21.08.2023 15:56:54

-- Design Name:

-- Module Name: RCA\_tb - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

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-- Dependencies:

--

-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

--

----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity RCA\_tb is

-- Port ( );

end RCA\_tb;

architecture Behavioral of RCA\_tb is

component RCA is

Port ( a : in STD\_LOGIC\_VECTOR (3 downto 0);

b : in STD\_LOGIC\_VECTOR (3 downto 0);

Sum : out STD\_LOGIC\_VECTOR (3 downto 0);

Cout : out STD\_LOGIC;

Cin : in STD\_LOGIC);

end component;

signal a,b,sum : std\_logic\_vector(3 downto 0);

signal cout,cin : std\_logic;

begin

u1: RCA port map(a,b,sum,cout,cin);

process

begin

a<="0101";

b<="1010";

cin<='1';

wait for 200 ns;

a<="1101";

b<="1000";

cin<='0';

wait for 200 ns;

end process;

end Behavioral;

**RCA O/P:-**

