**Siso Main Code**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.std\_logic\_unsigned.ALL;

entity siso is

Port ( in1 : in STD\_LOGIC;

clk : in STD\_LOGIC;

slow\_clk : inout STD\_LOGIC;

out1 : out STD\_LOGIC);

end siso;

architecture Behavioral of siso is

signal q:std\_logic\_vector(3 downto 0);

signal counter: std\_logic\_vector(1 downto 0):=(others =>'0');

begin

process(slow\_clk,in1)

begin

if(slow\_clk'event and slow\_clk='1')then

q(3 downto 1) <= q(2 downto 0);

q(0)<= in1;

out1 <= q(3);

end if;

end process;

process(clk)

begin

if (clk'event and clk='1')then

counter <=counter+'1';

end if;

end process;

slow\_clk <= counter(1);

end Behavioral;

**Siso Tb**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.std\_logic\_unsigned.ALL;

entity siso is

Port ( in1 : in STD\_LOGIC;

clk : in STD\_LOGIC;

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if(slow\_clk'event and slow\_clk='1')then

q(3 downto 1) <= q(2 downto 0);

q(0)<= in1;

out1 <= q(3);

end if;

end process;

process(clk)

begin

if (clk'event and clk='1')then

counter <=counter+'1';

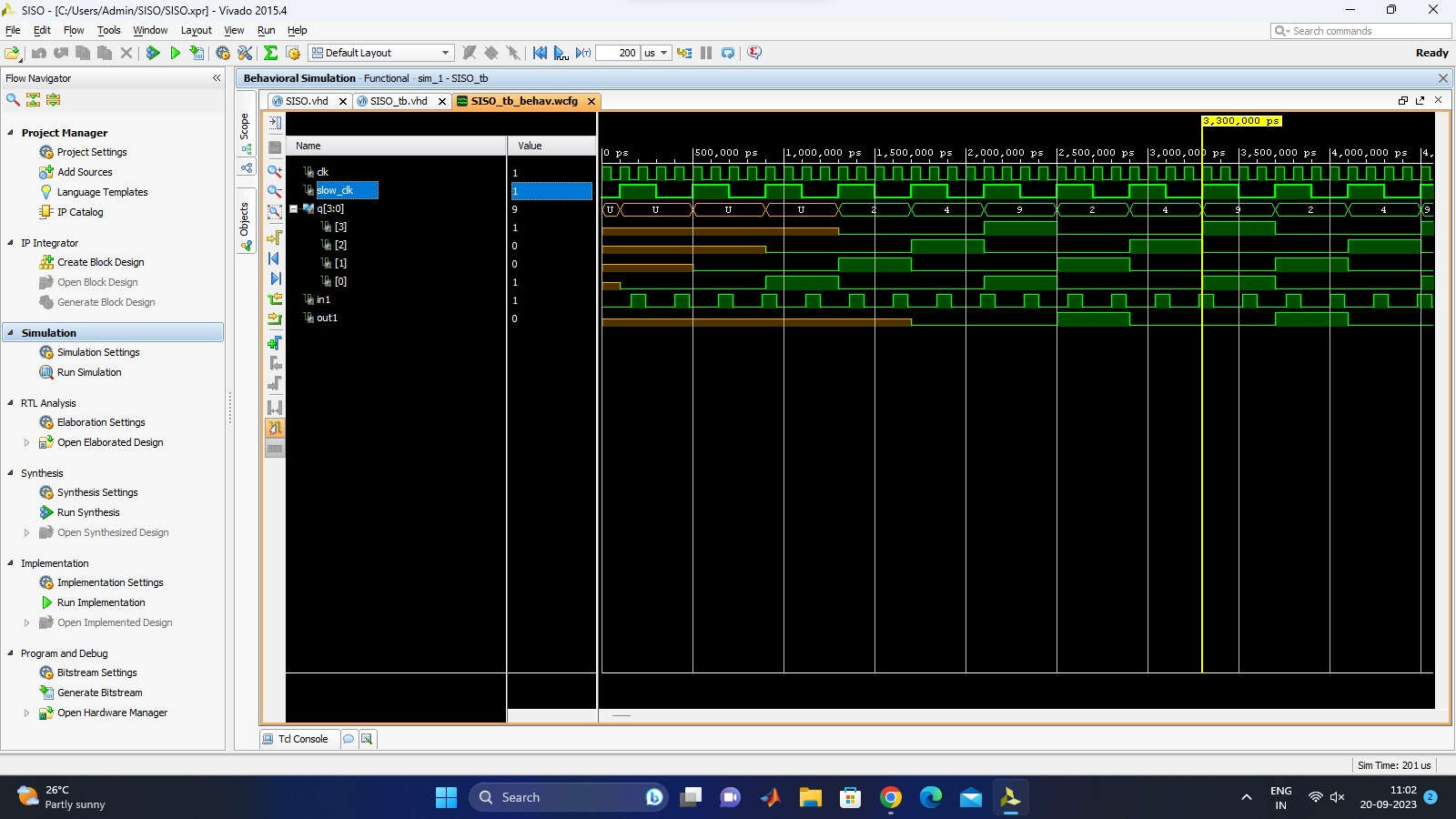
end if;

end process;

slow\_clk <= counter(1);

end Behavioral;

**OUTPUT:**

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