Problem 1:
Objective: Understand the behavior of MOSFETs.

(a) A certain MOSFET should have a threshold voltage of 0.8V; however, the experimentally measured threshold voltage is 0.6V. If we attribute this difference purely to interface charges, what is the areal density of interface charges, N_{oc} (in cm^{-2}), if $C_{ox} = 10^{-6}$ F/cm^2?

We know $V_{FB} = \phi_{ms} - \frac{qN_{OC}}{C_{ox}}$, so for a shift of -0.2V $\frac{qN_{OC}}{C_{ox}} = 0.2V$, and $N_{OC} = 1.2 \times 10^{12} cm^{-2}$. Note the units are per unit area (thus, "areal density"). The charges are assumed to be located entirely at the interface.

(b) One of the few helpful phenomena in short channel devices is velocity overshoot. If the geometry of a short-channel MOSFET leads to a 20% increase in the average saturation velocity, by how much will the cutoff frequency increase compared to results of the standard long-channel analysis? (Note: this is a very simple question, do not make it any more difficult than it initially appears).

We know that the cutoff frequency is proportional to $\frac{v_s}{L}$, so a 20% increase in v_s will result in a 20% increase in cutoff.

Problem 2:
Objective: Understand the behavior of MOSFETs.

Consider an ideal MOSFET with $V_T = 0.5V, \beta = 0.004\frac{A}{V^2}$ and $L = 50nm$.

(a) Use the level 1 model to calculate the transconductance and output resistance for $V_{GS} = 2V$, $V_{DS} = 0.5V$ and for $V_{GS} = 2V$, $V_{DS} = 2V$.

For $V_{GS} = 2V$, $V_{DS} = 0.5V$ we are below saturation ($V_{DS} < V_{GS} - V_T$) and

$$g_m = \beta V_{DS} = .004\frac{A}{V^2} \cdot 0.5V = 0.002\ S$$
$$r_0 = [\beta(V_{GS} - V_T - V_{DS})]^{-1} = 250\Omega$$

For $V_{GS} = 2V$, $V_{DS} = 2V$ we are in saturation ($V_{DS} > V_{GS} - V_T$) and

$$g_m = \beta(V_{GS} - V_T) = .004\frac{A}{V^2} \cdot 1.5V = 0.006\ S$$
$$r_0 \to \infty$$

(b) What is the ideal cutoff frequency when $V_{GS} = 2V$ and $V_{DS} = 2V$? Note that for this channel length you need to use the saturation drift velocity $v_s \approx 10^7$cm/s. This represents the intrinsic analog speed of the MOSFET, but we have neglected all parasitic circuit elements.

With the given voltages the devices is in saturation, so we can estimate the cutoff frequency using

$$f_m = \frac{3v_s}{4\pi L} = 477\ GHz$$

(c) What is the most effective device design parameter one could change to increase the cutoff frequency?

Shorten the channel.

Problem 3:
Objective: Understand the behavior of MOSFETs.

Consider a MOSFET operating in saturation, with the carrier velocity saturated, and with
$V_{DS} = 2$ V
$I_D = 2$ mA
Channel transit time, $\tau = 10^{-12}\ s$
Maximum theoretical cutoff frequency, $\frac{1}{2\pi\tau} = 160\ GHz$
Gate/input capacitance, $C_{gs} = C_{in} = 10^{-15}F$
Power dissipation, $I_D V_{DS} = 4\ mW$.

(a) How do these parameters change if we implement constant field scaling (slides 74 and 75 of section 8) with a scale factor of $S = 2$?

The scaled parameters are
$V_{DS} = 2$ V / S = 1 V
$I_D = 2$ mA / S = 1 mA
Channel transit time, $\tau = 10^{-12}\ s$ /S $= 5 \times 10^{-13}s$
Maximum theoretical cutoff frequency, $\frac{1}{2\pi\tau} = 160\ GHz$ * S =320 GHz
Gate/input capacitance, $C_{gs} = C_{in} = 10^{-15}F$ /S $= 5 \times 10^{-16}F$
Power dissipation, $I_D V_{DS} = 4\ mW/S^2 = 1\ mW$

(b) How do these parameters change if we implement the flexible scaling rules of Table 8.1 in Dimitrijev (slide 77 of section 8 in the notes) with the same scaling factor? (Assume V_{DS} does not change).

The scaled parameters are
$V_{DS} = 2$ V
$I_D = 2\ mA \cdot S = 4\ mA$
Channel transit time, $\tau = 10^{-12}\ s$ /S $= 5 \times 10^{-13}s$
Maximum theoretical cutoff frequency, $\frac{1}{2\pi\tau} = 160\ GHz$ * S =320 GHz
Gate/input capacitance, $C_{gs} = C_{in} = 10^{-15}F$ /S $= 5 \times 10^{-16}F$
Power dissipation, $I_D V_{DS} = 4\ mW * S = 8\ mW$

Note, the theoretical cutoff frequency increases by the scaling factor because the channel length, and thus the transit time, is reduced by S. However, your book notes that the switching frequency for a digital system increases by S^2 because the gate capacitance for the next device is reduced by S.