Problem 1:

(a) Do problem 8.6 in Dimitrijev. This problem allows you to review the simple model of the MOSFET channel as a resistor connecting source and drain. The way the problem is written you will solve for the width to length ratio (W/L) and have a valid answer, but if you want exact dimensions you can use $L = 0.2\mu m$ (the minimum channel dimension) to determine W.

8.6 Design an N-channel MOSFET, used as a voltage-controlled switch, so that the resistance in *on* mode is $R = 100\ \Omega$. The technological and circuit parameters are as follows: the threshold voltage is $V_T = 0.2$ V, the gate-oxide thickness is $t_{ox} = 3$ nm, the electron mobility in the channel is $\mu_n = 350\ \text{cm}^2/\text{V}\cdot\text{s}$, the gate voltage in *on* mode is $V_{GS} = 1.0$ V, and the minimum channel dimension is $0.2\ \mu$m.

The channel resistance is given by

$$R = \frac{1}{\mu_n C_{ox}\left(V_{gs} - V_T\right)}\frac{L}{W}$$

$$\text{so, } \frac{W}{L} = \frac{1}{R\mu_n C_{ox}\left(V_{gs} - V_T\right)} = \frac{1}{100\Omega \cdot 350\text{cm}^2/\text{V}\cdot\text{s} \cdot \frac{3.9\cdot 8.85\times 10^{-14}\text{F/cm}}{3\times 10^{-7}\text{cm}}(1\text{V} - 0.2\text{V})} = 31$$

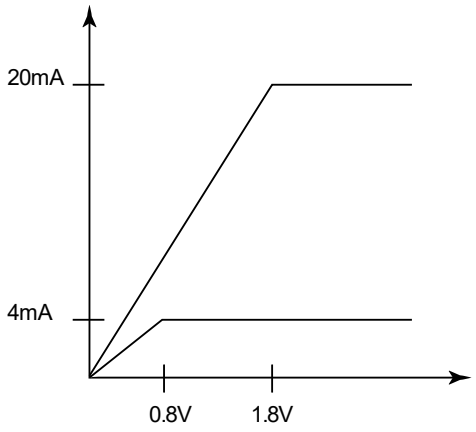
If we use the minimum channel dimension of L=0.2μm, then we have W = 6.2μm.

(b) Based on your answer to part (a), use the level 1 model to sketch I_D vs. V_{DS} for $V_{GS} = 1V$ and $V_{GS} = 2V$. You should calculate V_{Dsat} and I_{Dsat} for both gate voltages.

For $V_{GS} = 1V, V_{Dsat} = V_{GS} - V_T = 1V - 0.2V = 0.8V$ and
$I_{Dsat} = \frac{\mu_n C_{ox} W}{2L}(V_{GS} - V_T)^2 = 0.004A.$

For $V_{GS} = 2V, V_{Dsat} = V_{GS} - V_T = 2V - 0.2V = 1.8V$ and
$I_{Dsat} = \frac{\mu_n C_{ox} W}{2L}(V_{GS} - V_T)^2 = 0.02A.$

Here is a quick sketch:



Problem 2:
Objective**:** Understanding the MOSFET.

Consider a silicon MOSFET with a TiAlN gate ($\phi_m = 4.5\ V$), SiO_2 (t_{ox} = 3 nm) as the oxide, and doped such that $N_A = 5x10^{17}$ cm^{-3}. The width to length ratio (W/L) is 20. Also assume $\mu_0 = 350$ $cm^2\ V^{-1}\ S^{-1}$.

(a) What is the threshold voltage for this MOSFET? (this is the same as a MOS capacitor)
The threshold voltage is the sum of the flatband voltage, V_{FB}, the voltage required to invert the semiconductor, $2\phi_F$ and the voltage drop across the oxide, $\gamma\sqrt{2\phi_F}$.

$$V_{FB} = \phi_m - \phi_s = 4.5V - \left[4.03V + \frac{E_g}{2} + kT \cdot \ln\left(\frac{N_A}{n_i}\right)\right] = \text{-0.55V}$$

$$\phi_F = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) = 0.46\ V$$

$$\gamma = \frac{\sqrt{2\epsilon_s q N_A}}{C_{ox}} = 0.36V^{1/2}$$

$$V_T = V_{FB} + 2\phi_f + \gamma\sqrt{2\phi_F} = 0.71V$$

(b) Which of the following describes this MOSFET?

- n-channel depletion mode
- **n-channel enhancement mode**
- p-channel depletion mode
- p-channel enhancement mode

(c) What could you change about the device that would cause it to operate in depletion mode?

We need to lower the threshold voltage below zero volts; thus, one could alter the gate material to make the gate-semiconductor work function difference sufficiently negative. Alternatively, one could intentionally introduce charge in the oxide. You might have to do both for this structure.

(d) For a gate voltage of 3V, calculate V_{Dsat} using both the level 1 and the level 3 expressions. Note the difference between the two results.

Level 1: $V_{Dsat} = V_G - V_T = 2.3V$

Level 3: $F_B = \frac{\gamma}{2\sqrt{2\phi_F}} = 0.19$, $V_{Dsat} = \frac{V_G - V_T}{1+F_B} = 1.93V$

(e) Now calculate I_{Dsat} using both the level 1 and the level 3 expressions.

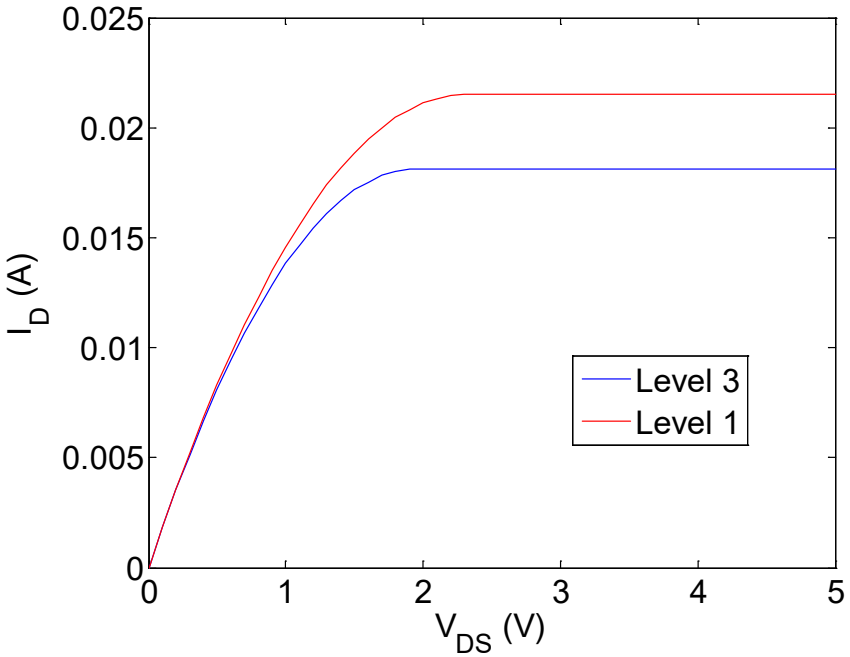
$\beta = \mu_0 C_{ox} \frac{W}{L} = 0.0081\ AV^{-2}$

Level 1: $I_{dsat} = \frac{\beta}{2}(V_G - V_T)^2 = 21\ mA$

Level 3: $I_{dsat} = \beta[(V_G - V_T)V_{dsat} - \frac{1}{2}(1 + F_B)V_{dsat}^2 = 18\ mA$

(f) Sketch a plot of I_D vs. V_{DS} for the MOSFET (when V_{GS} = 3V) that compares the results of the level 1 and level 3 models.

Here is a "sketch" (actually, I went ahead and plotted the results in Matlab)



For the following questions use the level 1 model for simplicity.

(g) What would the saturation current be for an otherwise identical device with N_A=2x10^{18} cm^{-3} and V_{GS} = 3V? Neglect the effect of changing the doping level on μ_0.

$V_{FB} = \phi_m - \phi_s = 4.5V - \left[4.03V + \frac{E_g}{2} + kT \cdot \ln\left(\frac{N_A}{n_i}\right)\right]$ = -0.59V

$$\phi_F = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) = 0.50\,V$$
$$\gamma = \frac{\sqrt{2\epsilon_s q N_A}}{C_{ox}} = 0.72V^{1/2}$$
$$V_T = V_{FB} + 2\phi_f + \gamma\sqrt{2\phi_F} = 1.1V$$

Level 1: $I_{dsat} = \frac{\beta}{2}(V_{GS} - V_T)^2 = 14\,mA$

(h) From part (g) we see that increasing the doping level increases the threshold voltage, and thus reduces the saturation current, for a given V_{GS}. We will learn that increasing the doping level is important for preventing punch-through in short channel devices. Thus we need a way to offset the increase in threshold voltage. The best way to do this is to reduce the oxide thickness. What would the saturation current be for the device when N_A=2x10^{18} cm^{-3}, t_{ox} = 2 nm and V_{GS} = 3V?
We first need to calculate the new threshold voltage, but only the oxide voltage drop changes:
$$\gamma = \frac{\sqrt{2\epsilon_s q N_A}}{C_{ox}} = 0.48V^{1/2}$$
$$V_T = V_{FB} + 2\phi_f + \gamma\sqrt{2\phi_F} = 0.88V$$

Level 1: $I_{dsat} = \frac{\beta}{2}(V_{GS} - V_T)^2 = 27mA$

Note that we have restored (and even exceeded) the saturation current of the device with the lower doping level.

(i) We also know that in a real MOSFET mobility is related to gate voltage. What would the saturation current be for the device in (h) if the mobility modulation constant is $\theta = 0.15\,V^{-1/2}$.

We need to adjust the mobility based on gate voltage. Thus,
$$\mu_{eff} = \frac{\mu_n}{1 + \theta(V_{GS} - V_T)} = 270\frac{cm^2}{V \cdot s}$$
and, $\beta = 0.009\,AV^{-2}$, $I_{Dsat} = 21mA$
So we see that there is a significant reduction in saturation current because of mobility degradation.

(j) We also know that in a real MOSFET the lateral field can saturate the electron velocity. Calculate the saturation current for the device in part (h), but assume the length of the channel is L = 30 nm (thus the width is W = 600 nm), and that the velocity is saturated at $v_{max} = 10^7 cm/s$.

$$I_{Dsat} = \frac{W v_{max} C_{ox}(V_{GS} - V_T)}{2} = 1.1mA$$

Problem 3:
Objective: Understand the behavior of short-channel MOSFETs.

(a) One sign of short-channel behavior is an increase in I_D with V_{DS} even in saturation. Explain at least two reasons why this effect is observed.

As V_{DS} increases beyond pinch-off the depletion region around the drain grows. As a result the channel length is reduced and the channel conductance increases. Thus, I_D increases with V_{DS} even in saturation.

(b) How would you change the doping level in the device to minimize the effect described in part (a). Explain your answer in two or three sentences.

In order to reduce channel length modulation one could increase the doping level in the device. This results in a smaller change in depletion region width with a change in drain bias.

(c) We know that the magnitude of the threshold voltage is reduced for a short channel device. Explain the origin of this reduction in two or three sentences.

In a short channel device the depletion regions associated with the source and drain partially deplete the region under the gate. As a result a smaller gate voltage (magnitude) is required to form the depletion region and reach inversion.

(d) How could you change a short-channel MOSFET device design to minimize threshold voltage shift resulting from part (c) (other than lengthening the channel)?

To minimize the threshold voltage shift one would increase doping levels, reduce junction depths, and decrease oxide thickness.

Problem 4:
Objective: Understand the behavior of MOSFETs.
(a) If a MOSFET has a subthreshold ideality factor of $n_s = 1.2$, what is the sub-threshold swing?

From the notes we can directly calculate $S = n_s \frac{kT}{q} \ln(10) = 72 \frac{mV}{decade}$.
Or, working it out explicitly as in Dimitrijev Example 8.4, we find

$$\frac{I_{D2}}{I_{D1}} = \exp\left[\frac{q(V_{GS2} - V_{GS1})}{n_s kT}\right] = \exp\left[\frac{qS}{n_s kT}\right] = 10$$

$$S = \frac{n_s kT}{q} \frac{\log(10)}{\log(e)} = 72 \frac{mV}{decade}$$

(b) Assuming $V_{GS} \ll V_T \; and \; V_{DS} \gg kT/q$, by how much do we have to reduce V_{GS} to reduce the sub-threshold current by a factor of 100?

If we want to reduce the sub-threshold current by 100, or two decades, we need to reduce V_{GS} by 144mV.

(c) Name one design change you could make to the device that would make n_s closer to 1.

To reduce the sub-threshold swing we need to increase the control of the gate over the channel. This is accomplished by reducing the oxide thickness, or increasing its dielectric constant. Alternatively, we could reduce the doping level to reduce the depletion capacitance and thus minimize the change in the depletion region with gate voltage.