# Sairam Sri Vatsavai

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## EDUCATION

### UNIVERSITY OF KENTUCKY
Doctoral candidate in Electrical Engineering
Aug 2019 - Till Date | Lexington, KY
GPA: 4.0/4.0 Till Date

### VARDHAMAN COLLEGE OF ENGINEERING
B.Tech in Electronics and Communication Engineering
May 2016 | Hyderabad, Telangana
CGPA: 8.52 / 9.0

## LINKS

Github:// **sairam954**
LinkedIn:// **sairam_sri_vatsavai**
HackerRank:// **sairamvgraju**

## COURSEWORK

### GRADUATE
Machine Learning (ML)
Deep Learning with Math
Bayesian Machine Learning
Advanced Computer Architecture
Digital Computer Structure
Solid State Electronics
Electromagnetic Fields
Photonics Integrated Circuits*
Large Scale Datascience*

## SKILLS

### PROGRAMMING
•Python •Java •C++ •C
Familiar:
•Javascript •Groovy •AngularJS
•Matlab •SystemC

### ML FRAMEWORK
•PyTorch •Keras •Numpy •Pandas

### DATABASE
• MySQL • MongoDB • Posgresql

### SYSTEM SIMULATORS
•Lumerical FDTD, MODE •Noxim •
Cacti • NVMain

### RPA
•Workfusion• Selenium
Familiar:
• UiPath

## AWARDS

•Fearless Problem Solver, EPAM
•Best L&D Mentor, EPAM

## SUMMARY


- Currently pursuing PhD in Electrical Engineering with research interests as design of accelerators for Neural Networks and Reservoir Computing.
- 3 year experienced Software Engineer with good implementation knowledge on Java, Python, Deep Learning, Workfusion Machine Learning
- Well aware of Clean Code principles, CI/CD practices and Agile methodology.


## EXPERIENCE

### UCAT LAB | Research Assistant
Jan 2020 - Till Date | Lexington, KY

- Working with **Dr. Ishan Thakkar** group to design accelerators for Deep Learning to reduce inference time, and addressing challenges in PNoCs with Silicon Photonics
- Implemented Delay feedback Reservoir computing with Silicon Microring [4] involving modeling of Silicon Microring, analyzing its performance on temporal and sequential ML tasks using PyTorch
- Developed a loss aware self adaptive PNoC PROTEUS [3] involving design space exploration of configuration parameters like Q, bit rate and supported wavelengths. Modelled losses using Python and Lumerical. Performed trace driven system level simulation with PARSEC benchmarks using SystemC, C++ with NOXIM
- Assisted in performing system level simulations for PNoCs with Silicon on Sapphire as device platform [2] and calculating the overhead associated with novel schemes to secure PNoCs from snooping attacks [1] using Cacti and NVMain

### EPAM |Software Engineer
July 2016 - July 2019 | Hyderabad, India

- As ML Engineer performed data analysis of documents, trained SME on tagging data,prepared training set, trained Information Extraction NER and document classification models, and deployed model on Worksfusion Control Tower
- To improve performance used OCR tuning, developed feature extractors, carried out Hyper-parameter tuning and post-processing
- As Workfusion SPA specialist provided solutions to automate the manual business process using Java for Web Automation, Surface Automation and Desktop Automation
- Mentored and trained teammates by designing training plan,creating tasks and evaluating progress to complete certification required for project

## PUBLICATIONS


[1] S. V. R. Chittamuru, I. Thakkar, S. Pasricha, S. S. Vatsavai, and V. Bhat. Exploiting process variations to secure photonic noc architectures from snooping attacks. *TCAD*, July 2020.

[2] V. S. P. Karempudi, S. S. Vatsavai, and I. Thakkar. Redesigning photonic interconnects with silicon-on-sapphire device platform for ultra-low-energy on-chip communication. *GLSVLSI 2020*, September 2020.

[3] S. S. Vatsavai, V. S. P. Karempudi, and I. Thakkar. Proteus: Rule-based self-adaptation in photonic nocs for loss-aware co-management of laser power and performance. *NOCS 2020*, September 2020.

[4] S. S. Vatsavai and I. Thakkar. Silicon photonic microring based chip-scale accelerator for delayed feedback reservoir computing. *VLSID 2021*, preprint.