

# INTER-INTEGRATED CIRCUIT (I2C) PROTOCOL

## I2C- *Other Names*

- Inter-Integrated Circuit
- I2C
- I<sup>2</sup>C
- Two Wire Interface
- TWI

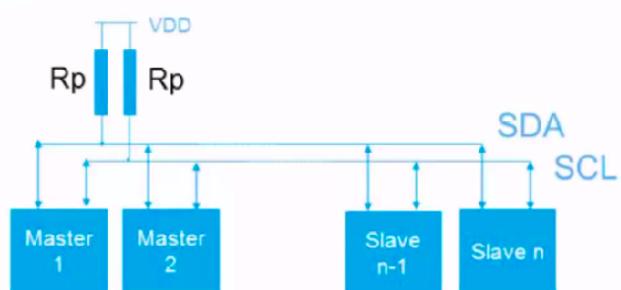
## I2C Lines

- SCL : Serial Clock

For synchronizing data transfer between the master and the slave.

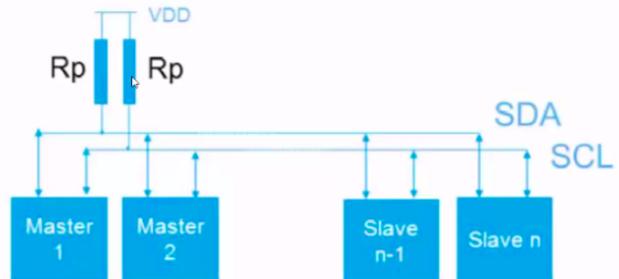
- SDA : Serial Data

The data line



## Operation Modes

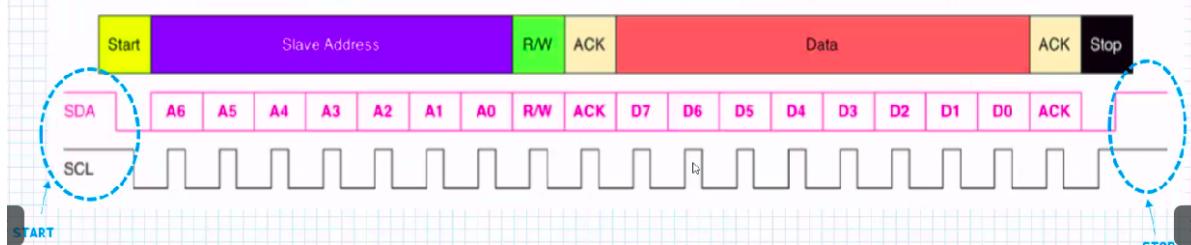
- Master Transmitter
- Master Receiver
- Slave Transmitter
- Slave Receiver



## The Protocol

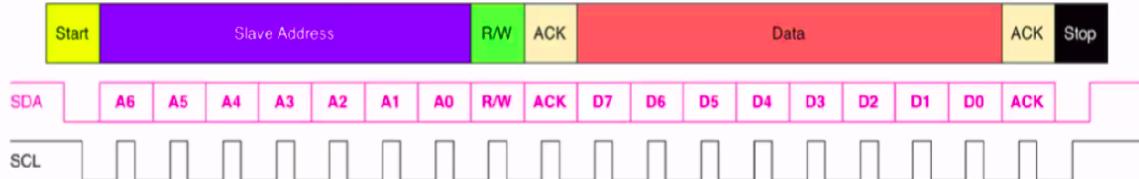
- Transactions are initiated and completed by the master.
- All messages have an address frame and a data frame.
- Data is placed on the SDA line after SCL goes low, and it is sampled after the SCL line goes high.

## The Protocol- START an STOP Condition



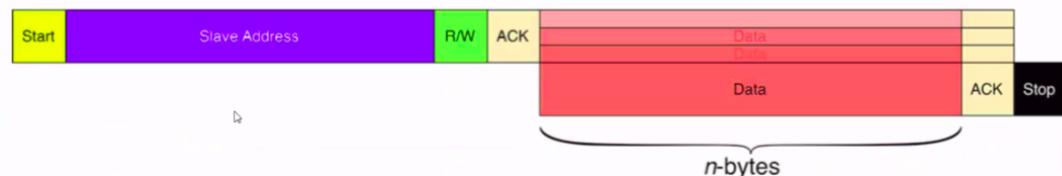
- All transactions begin with START and are terminated by STOP
- A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition
- A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.
- START and STOP conditions are always generated by the master
- The bus is considered to be free again a certain time after the STOP condition
- The bus stays busy if a repeated START is generated instead of a STOP condition

## The Protocol- Byte Format



- Any information transmitted on the SDA line must be eight bits long.
- The number of bytes that can be transmitted per transfer is unrestricted
- Each byte must be followed by an Acknowledge (ACK) bit
- Data is transferred with the Most Significant Bit (MSB) first

## The Protocol- Data Frame



- The data frame begins transmission after the address frame is sent.
- The master will simply continue generating clock pulses on SCL at a regular interval, and the data will be placed on SDA by either the master or the slave, depending on whether the R/W bit indicated a read or write operation.

## I2C Clock Speed

- This is the speed of the I2C interface and should correspond with the bus speeds defined in the I2C specification

***The specification defines the following modes :***

|                 |               |
|-----------------|---------------|
| Standard-mode   | : 100 KHz max |
| Fast-mode       | : 400 KHz max |
| Fast-mode Plus  | : 1 MHz       |
| High-speed mode | : 3.4 MHz     |

## I2C Duty Cycle

- Specifies the ratio between  $t_{LOW}$  and  $t_{HIGH}$  of the I2C SCL line
- *Possible values :*

`I2C_DUTYCYCLE_2 = 2:1`  
`I2C_DUTYCYCLE_16_9 = 16:9`

- By choosing the appropriate duty cycle we can pre-scale the peripheral clock to achieve the desired I2C speed.