Sait Sarper Özaslan

EEE-313 Electronic Circuit Design

Lab-3 nMOS Common Source Amplifier

22002861

Introduction

1. Finding V_{TN}

The first aim of this lab is to observe an NMOS FET's characteristic. Especially its threshold voltage and saturation currents. In this part we expect to see current occurrences in the MOSFET given in figure 1.

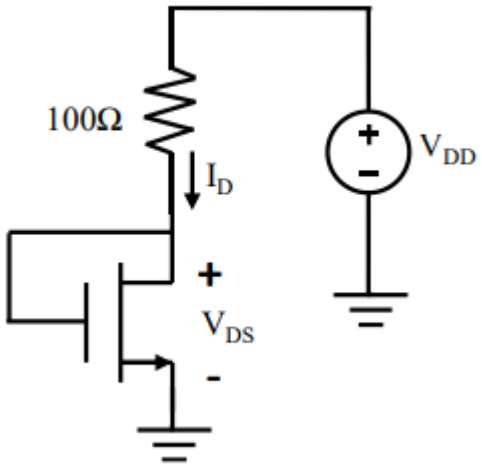

Figure 1: Test Circuit for finding in Vth

As $V_{DS} = V_{GS}$ we expect the circuit to be on saturation the moment it turns on since,

$$V_{DS} > V_{GS} - V_{TN}$$

The point it will turn on will be when,

$$V_{GS} - V_{TN} > 0$$

Therefore, we expect to see current when gate to source voltage is higher than the threshold voltage.

2. $I_{DS} - V_{DS}$ Curves

In this part what we are trying to observe is currents behavior when we change the V_{DD}. Moreover, we also change the gate voltage to see how it affects the drain current and see where the saturation occurs.

As the V_{DS} value will be lower than $V_{GS} - V_{TN}$ in the beginning the circuit will be at triode until V$V_{DS} \geq V_{GS} - V_{TN}$.

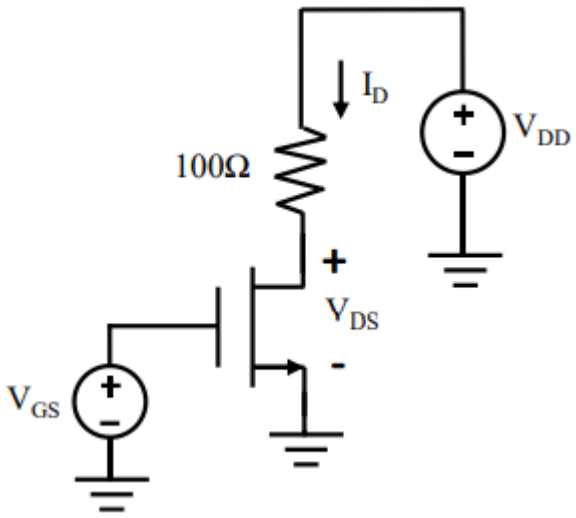

Figure 2: Test Circuit for I_{DS} – V_{DS} Curves

As we increase V_{GS} we expect to see a higher saturation current. This is due to 2 reasons:

- It takes longer for V_{DS} to be bigger than $V_{GS} - V_{TN}$ causing the need for a higher V_{DD} value.
- The current formula,

$$I_{DS} = K_N(V_{GS} - V_{TN})^2 \cdot (1 + \lambda V_{DS})$$

As V_{GS} and V_{DS} get higher, the saturation current will naturally get higher. We can get the values of Kn and λ by dividing the 2 current equations by each other and placing the found λ value to find K_N.

3. Common Source Amplifier.

In this part we apply a small signal and DC voltage to the circuit within the given specifications and report the gain of the circuit. In this part we first make the DC design of the circuit within these specifications and then add the small signal and observe the gain at output.

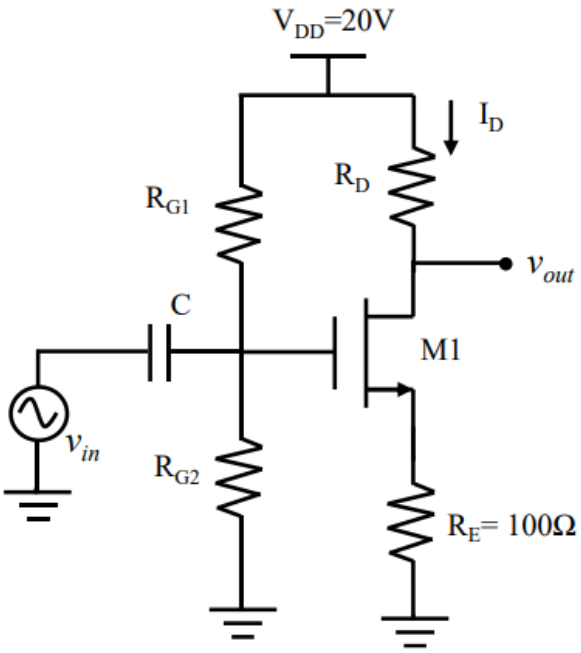

Figure 3: Common Source Amplifier to be Designed

Here are the specifications of the circuit:

- Rin > 30kΩ
- Rout < 2kΩ
- 10mA< ID < 15mA
- |AV|=|Vout / Vin|> 9 when Vin=100mVpp sine wave @ 10kHz

This part's theoretical and hardware analysis can only be done after the first two parts.

4. Addition of a Capacitor

Finally, we will add a capacitor that will short circuit the R_E from the rest of the circuit. We expect gain to increase in such case. This will be explained later with small signal model of the circuit

Implementation and Analysis

1. Finding V_{TN}

As explained in the intro we expect to see current change as soon as V_{GS} is bigger than threshold voltage. Using multimeter on the current path current =1mA was observed when V_{DD} =1.61Volts

From ohm's law we can calculate V_{GS} as 1.51V then it is safe to say that threshold voltage V_{TN} = 1.51Volts.

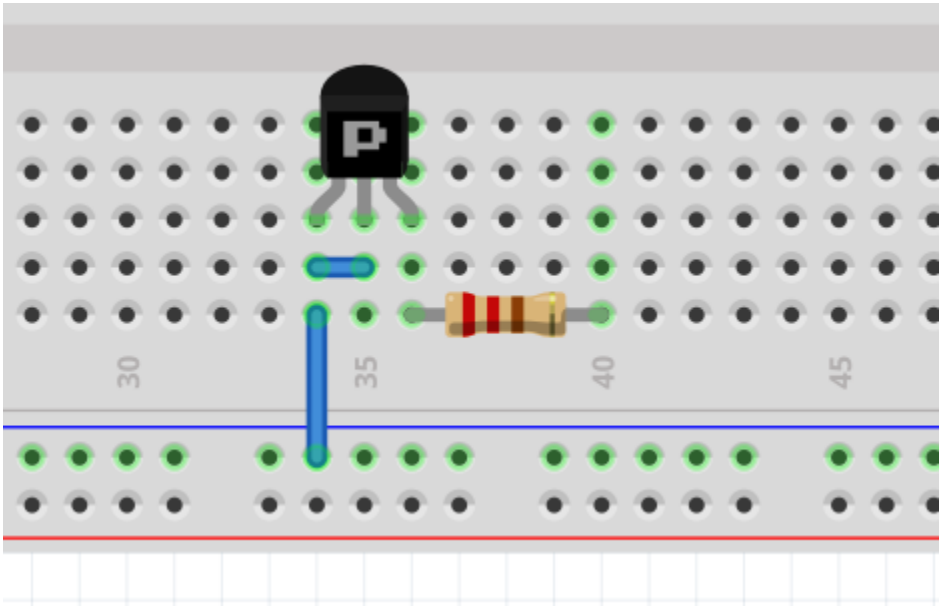

Figure 4: The circuit for the First Part

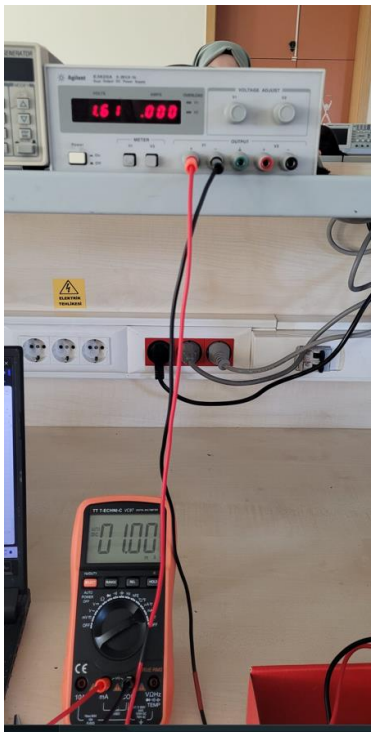

Figure 5: Occurrence of 1mA

Here is another example measurement, and all the V_{DD} and I_D Datas taken in this part can be seen in appendix A from the Matlab code.

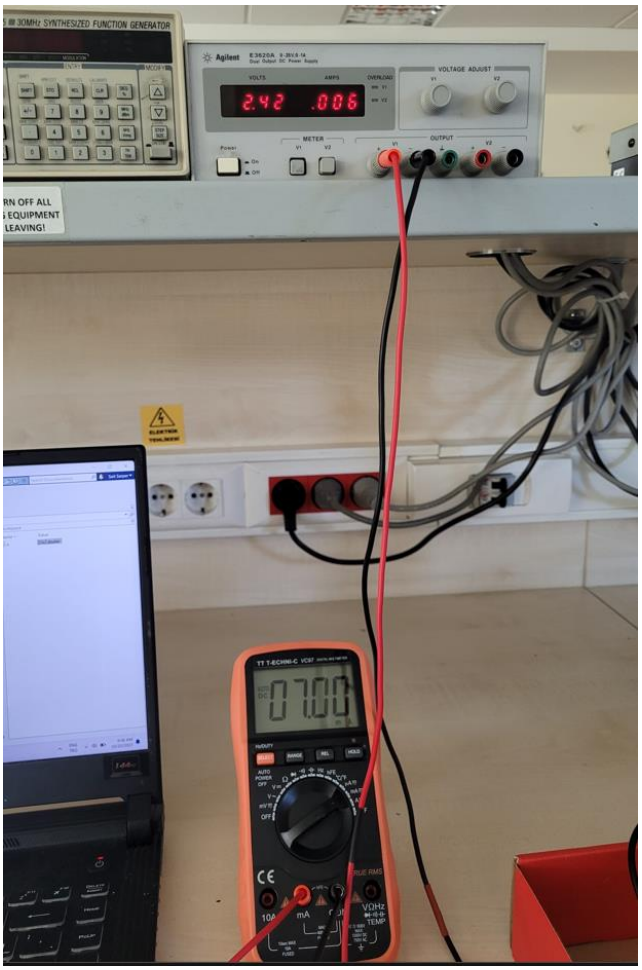

Figure 6: Occurrence of 7mA

The plot I_D vs V_{DS} was recorded as:

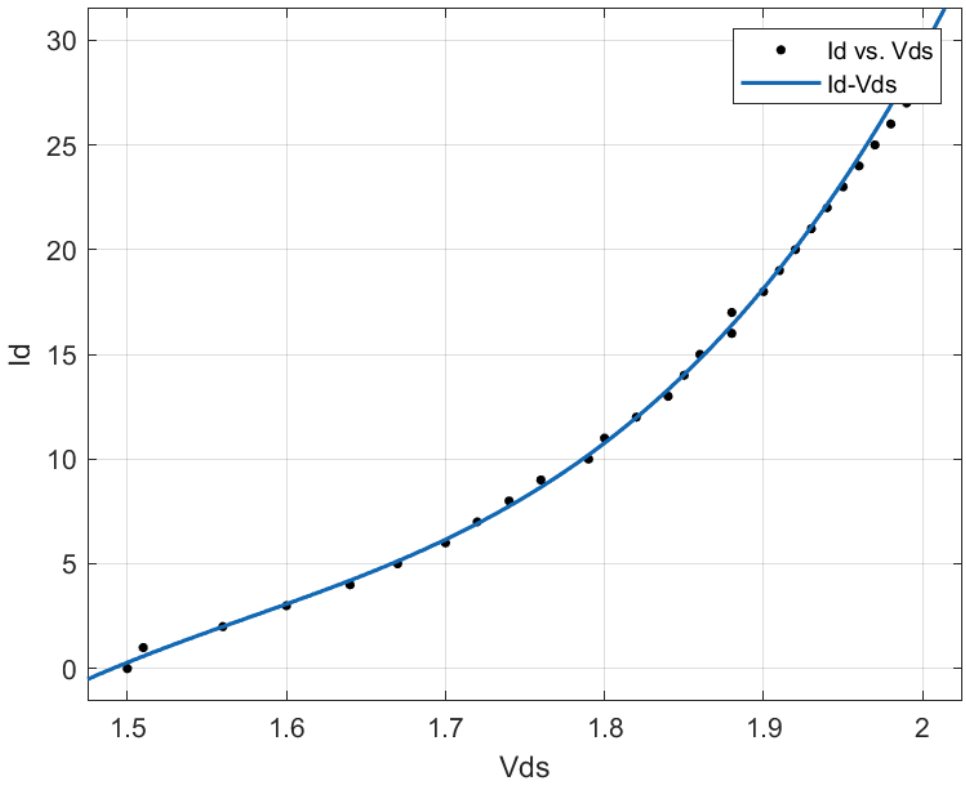

Figure 7: Vds-Id Plot with Third Degree Approximation

Though the relation between V_{DS} can be written as $V_{DD} - I_D * R$ where $R = 100\Omega$, which is a linear relation. However using curve fitter in MATLAB we have found it is not linear. This happens probably because increase in V_{DD} also results in increase in I_D. Therefore, it is better to use the relation

$$I_D = K_N(V_{GS} - V_{TN})^2(1 + \lambda V_{DS})$$

We also know that $V_{DS} = V_{GS}$. Hence, we can write the relation as,

$$I_D = K_N(V_{DS} - V_{TN})^2(1 + \lambda V_{DS})$$

Now we can see the relation more clearly as all the other values are constants apart from V_{DS} and I_D. That means I_D is in relation to the third power of V_{DS} and the curve fitter which uses third degree polynomial fitting confirms the mathematical relation.

Now we can move onto part 2 with the knowledge of $V_{TN} = 1.51V$.

2. $I_D - V_{DS}$ Curves

In this part we need to consider channel length modulation this means the current will not fully stabilize after it reaches saturation and there will be minimal but noticeable increases in I_D after the MOSFET reaches saturation. Essentially what is used is the equation below for saturation where I_D depends on V_{DS} only as the other values are constant.

$$I_D = K_N(V_{GS} - V_{TN})^2(1 + \lambda V_{DS})$$

Here are three different V_{GS} values and their plots:

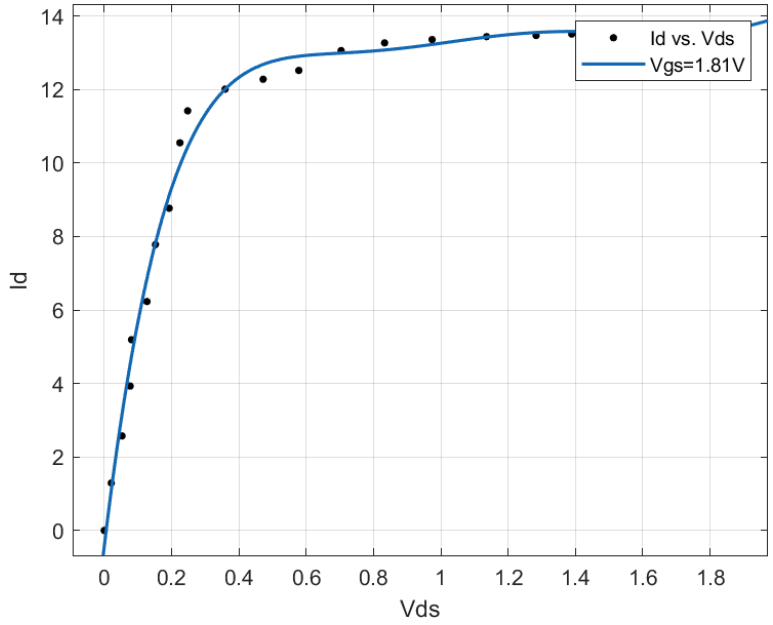

Figure 8: $V_{GS} = 0.3 + V_{TN} = 1.81V$

We expect to see current to start stabilizing after V_{DS} surpasses 0.3V as that is when the circuit will start behaving in the saturation state. From figure 7 we can more or less see that the increase in I_D slows down after V_{DS} value reaches 0.3V.

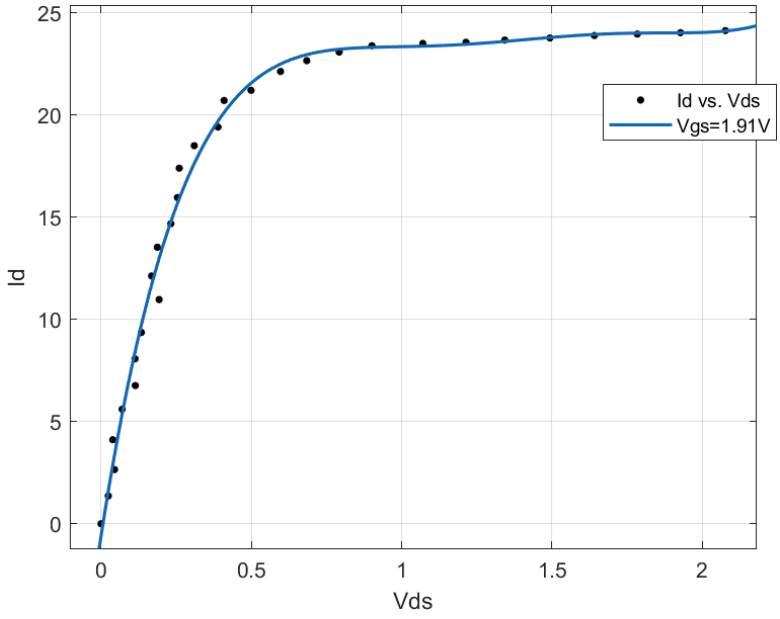

Figure 9: $V_{GS} = 0.4 + V_{TN} = 1.91V$

The same case can be observed in this part as well as current starts stabilizing after V_{DS}=0.4V.

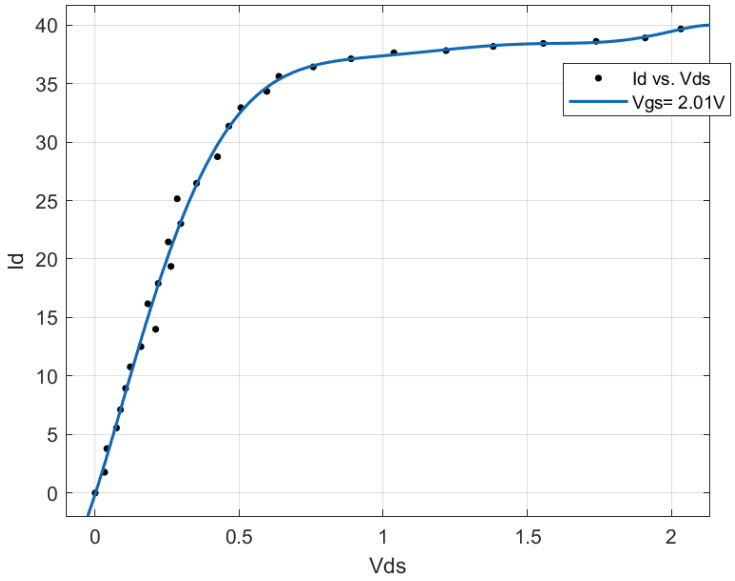

Figure 10: $V_{GS} = 0.5 + V_{TN} = 2.01$

Though stabilizing starts a bit later than $V_{DS} = 0.5V$, it can be considered the same spot.

Now we need to calculate K_N and λ. To do this we can pick 2 specific current values from all the Datas we have obtained and divide them by each other to find λ, then we can put λ into that equation and find K_N.

For this calculation I have picked the saturated points $V_{DS} = 1.078V \; and \; I_D = 23.42mA$ with$V_{DS} = 1.34V \; and \; I_D = 23.7mA$. Here is the derivation of $K_N \; and \; \lambda$:

$V_{GS} = V_{TH} + 0.4$

I_D	V_{DS}
23.42	1.078
23.7	1.34

$I_D = K_N (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$

$I_D = K_N (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$

Dividing them by each other:

$$\frac{23.42}{23.7} = \frac{1 + \lambda \, 1.078}{1 + \lambda \, 1.34} \Rightarrow \lambda = 0.048 \, V^{-1}$$

$$23.42 = K_N (0.4)^2 (1 + 0.048 \cdot 1.078) \Rightarrow K_N = 139.17 \, mA/V^2$$

Figure 11: Derivation of $K_N \; and \; \lambda$

- Now that we have found $K_N = 139.17 mA/V^2 \; and \; \lambda = \; 0.048 \; V^{-1}$. Let's move on to next part.

3. Finding the Gain of a Common Source Amplifier

3.1 Theoretical Analysis

To be able to have an appropriate design within the specifications we need to first find R_{in} and $R_{out.}$ After finding these values we can safely do the DC analysis of the circuit. For DC analysis we need MOSFET to be on saturation to have a working circuit. For small signal model to be valid, we need to pick a capacitor value who will behave almost like a short circuit given the small signal,

- $v_{in} = 100 mV_{pp} \sin e \; wave \; @ \; 10 kHz$

Capacitor's impedance can be calculated as,

$$|Z_C| = \frac{1}{2\pi \cdot f \cdot C_C}$$

If we pick, $C_C = \; 10 \mu F$ we get $Z_C = 1.59 \Omega$ which is a value small enough to be considered short during small signal analysis. Then we can now observe the small signal analysis for $R_{in} \; and \; R_{out}$.

Here is the small signal model:

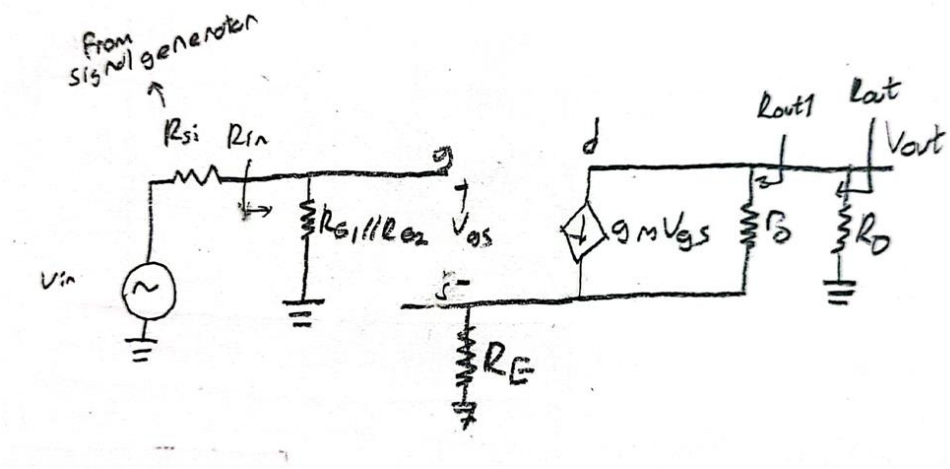

Figure 12: Small Signal Model

- ForR_{in}, it is obvious as the resistors who have effect on input resistance are $R_{G1} \; and \; R_{G2}$ which are in parallel. Hence, $R_{in} = \; R_{G1} // R_{G2}$.
- ForR_{out}, the explanation is a bit more complex. If we define the left part of R_D as R_{out1}. The final output resistance will be whatever value found in value found in R_{out1} paralleled with R_D. Then as long as$R_D \; < 2k\Omega$, we will have $R_{out} \; < 2k\Omega$.

With these in mind one can engage in the DC analysis of the circuit after specifying an I_D current between 10-15mA. For this lab $I_D = 12mA$ has been picked and DC analysis has been done accordingly. Here are the wholes list of chosen values:

- $R_D = 1.5k\Omega$
- $R_{G1} = 330k\Omega \; and \; R_{G2} = 68k\Omega$, aim in here is to have a low gate voltage that is higher than the threshold voltage but not too high that the circuit can't go into saturation state. Hence, the result of voltage divider should be within these specifications.
- $I_D = 12mA$

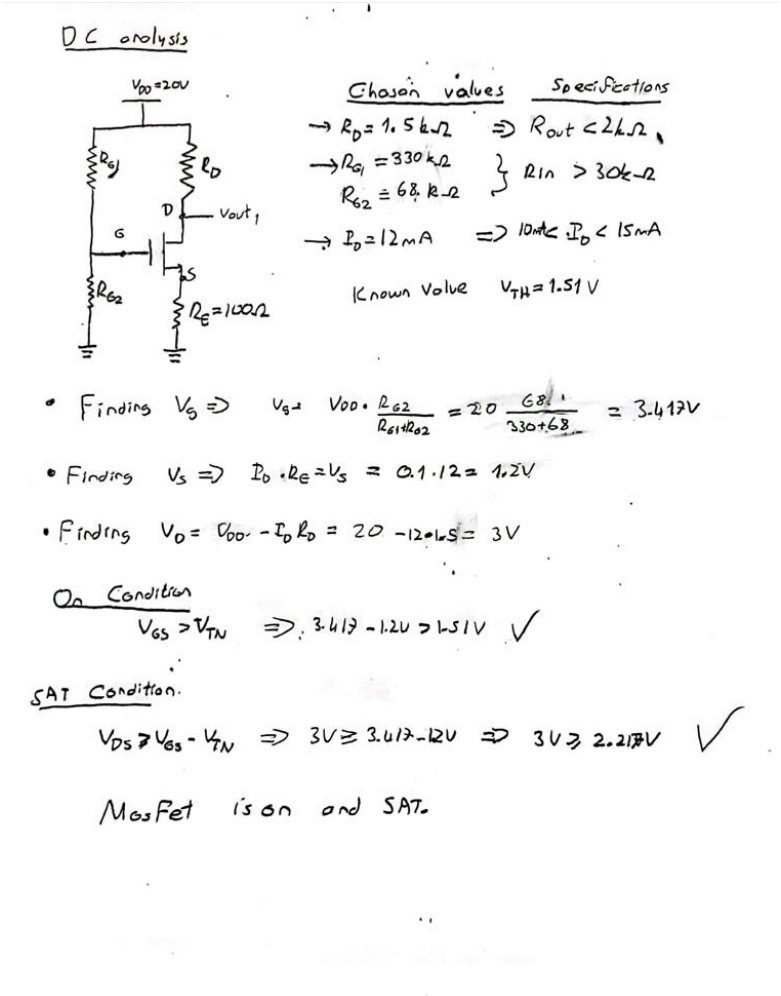

Figure 13: DC Analysis after Chosen Values

As can be seen in figure 13, the chosen values satisfy the Saturation and ON conditions. Hence, we can safely use this circuit for our small signal model. The chosen resistor values satisfy the conditions:

- $R_{in} = R_{G1}//R_{G2} = 56.3k > 30k\Omega$
- $R_{out} \cong R_D = 1.5k < 2k\Omega$

Looking back at figure 3, we can see the decoupling capacitor which allows us to disconnect the small signal from the analysis as capacitors are treated as open circuits.

Now we can look at the small signal gain:

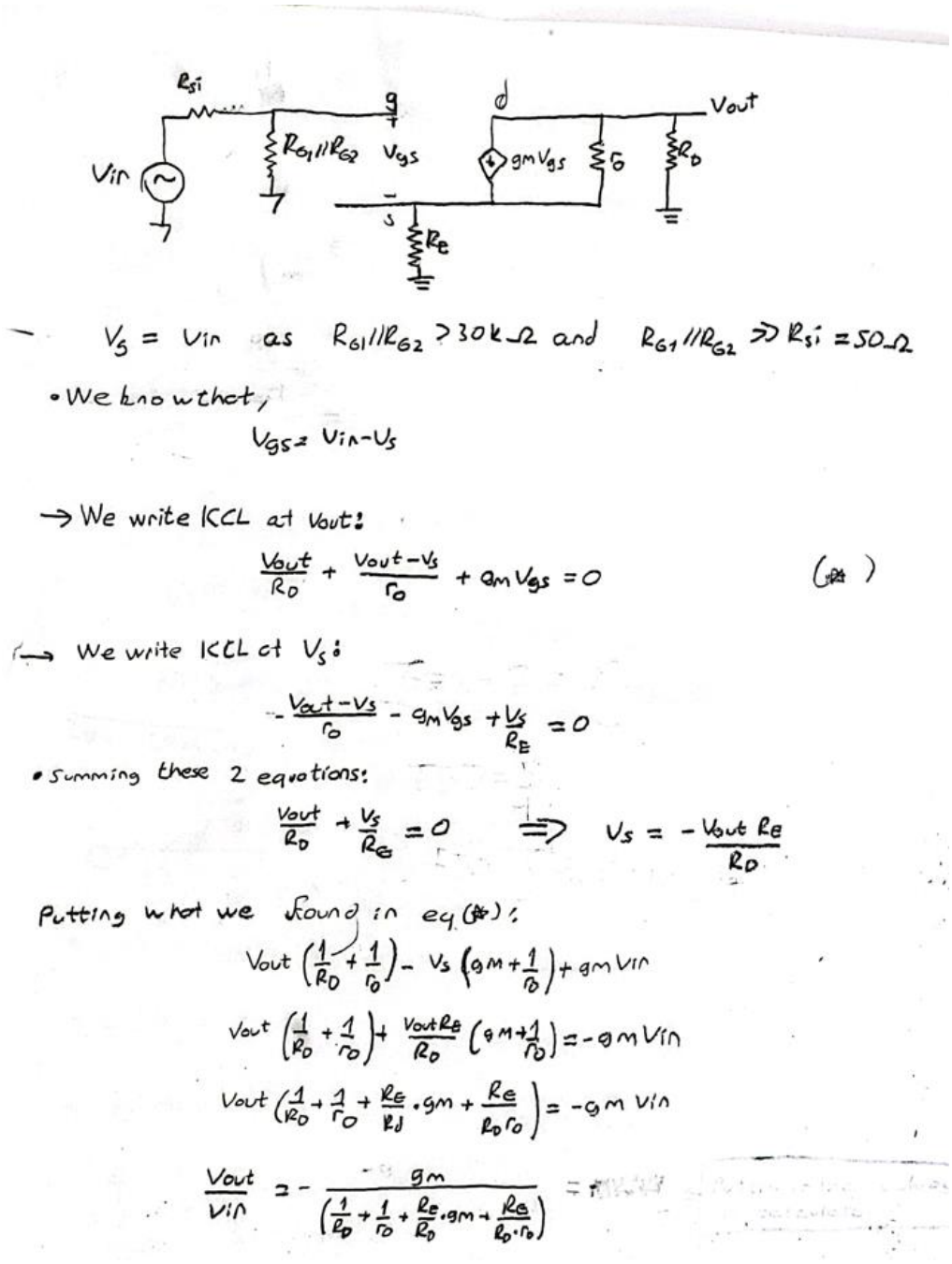

Figure 14: Calculation of Gain

The gain was found to be:

$$\left|\frac{V_{out}}{V_{in}}\right| = \frac{gm}{\left(\frac{1}{R_D} + \frac{1}{r_o} + \frac{R_E}{R_D} g_m + \frac{R_E}{R_D \cdot r_o}\right)} \quad (1)$$

3.2 Hardware and Expected Results

Here is the circuit to be used in this part:

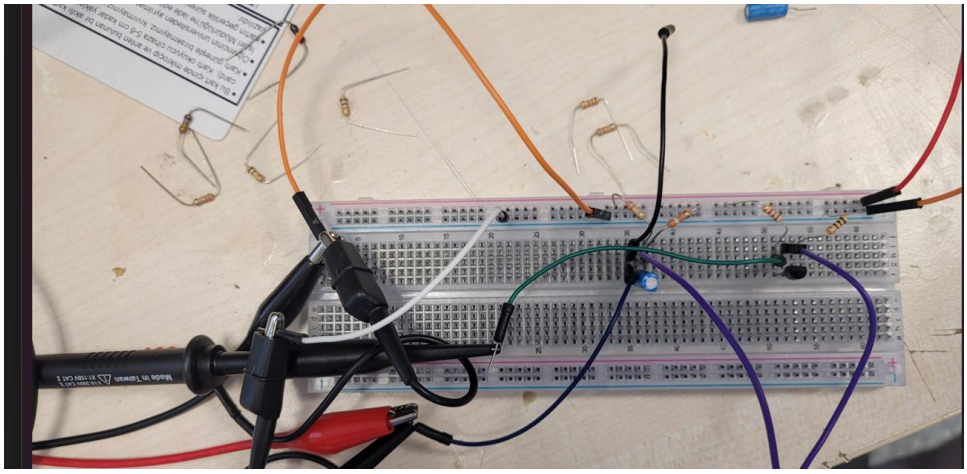

Figure 15: Reference Circuit to be used in Part 3

Before analyzing the gain, I wanted to check whether circuit is sending the chosen current value, $I_D = 12mA$. To check this, I measured the voltage across R_D, which was found as,

Figure 16: 17.36 V Across the Resistor

From this value, 17.36V, we calculate the current from Ohm's Law as $I_D = 11.57mA$

Before moving on to the small signal gain let's calculate $gm\ and\ r_o$ of the circuit:

- $gm = 2\sqrt{K_N I_D} = 80.25mA/V$
- $r_o = \frac{1}{\lambda I_D} = 1.8k\Omega$

$$\left| \frac{80.25k^{-1}}{\left(\frac{1}{1.5k} + \frac{1}{1.8k} + \frac{0.1k}{1.5k} 80.25k^{-1} + \frac{0.1k}{1.5k \cdot 1.8k} \right)} \right| = 12.1420566$$

$$k = 10^3 = 1\,000$$

Figure 17: Calculation of the Gain

With these values in mind, we expect the gain to be $A\left|\frac{V_{out}}{V_{in}}\right| = 12.14$. We found the gain to be larger than 9. As we have satisfied our last condition for the circuit, we can now move on to the gain test of this circuit.

Applying $V_{in} = 50mV_{pp}\sin(2\pi \cdot 10kHz)$ to this circuit the value will be doubled due to properties of wave generator where input is doubled if the resistive load the generator sees is much higher than the

input resistance of 50Ω . Then we will observe input voltage as $V_{in} = 100mV_{pp}\sin(2\pi \cdot 10kHz)$ from the probes.

Looking at the result we obtain:

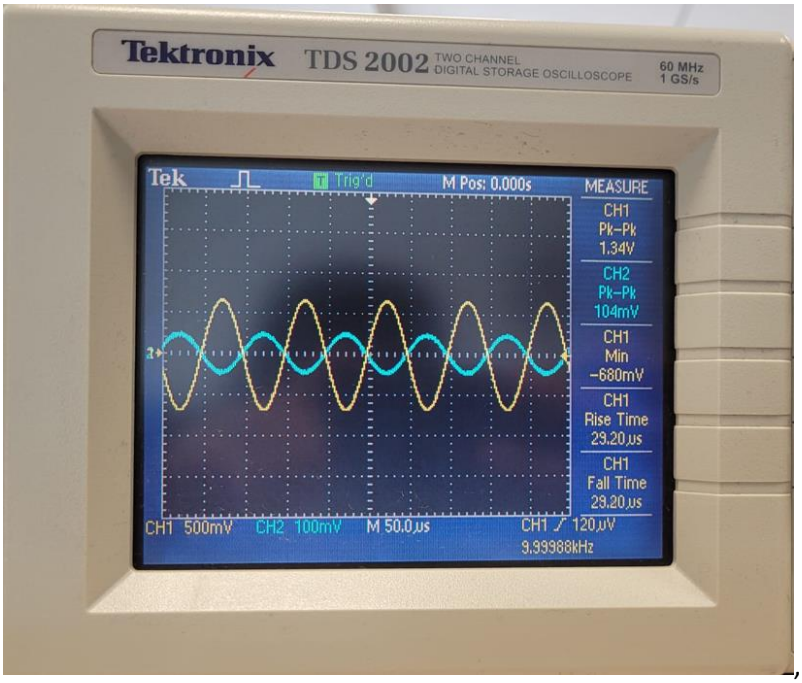

Figure 18: Gain of the Common Source Amplifier

From the values in figure 18, we found the gain as $A\left|\frac{V_{out}}{V_{in}}\right| = 12.88$which is higher than 9. This value is also close to the expected value, which increases the accuracy of our result. Therefore, we can say that we have obtained the necessary gain for the circuit and the circuit is working properly.

Next part is to increase the small signal to the point where distortion starts occurring in the output. After increasing the small signal input to $V_{in} = 700mVpp$, which is doubled to $V_{in} = 1.4Vpp$ in the signal generator, distortions started occurring at the sinusoidal output of the circuit.

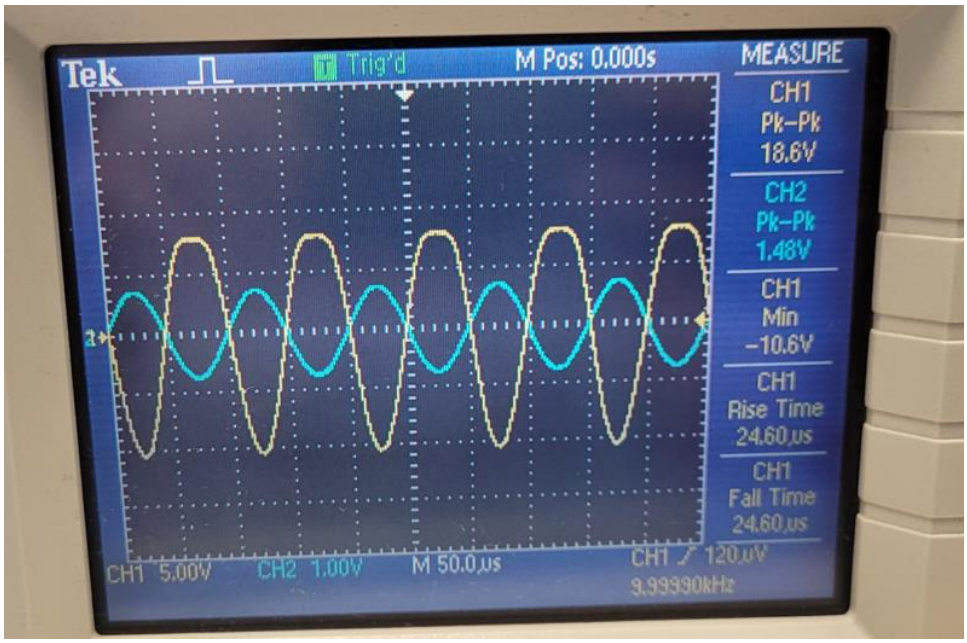

Figure 19: Occurrence of Distortion at Output

When we apply sinusoidal signals to the input of an amplifier, we will obtain sinusoidal signals at the output as long as the MOSFET operation remains linear. If the input starts getting too high such that MOSFET can't behave linear, a portion of the output signal will be cut off and we will observe a distorted signal at the output.

4. Impact of Adding a Capacitor Parallel to R_E

When we add a capacitor, $10\mu F$, to the amplifier to the circuit which is parallel with the R_E, the capacitor will allow us to short circuit the $R_E = 100\Omega$. Then we can easily take $R_E = 0\Omega$ and calculate the gain from the equation (1) from part 3. Hence, we found the relation as:

$$\left|\frac{V_{out}}{V_{in}}\right| = \frac{gm}{\left(\frac{1}{R_D} + \frac{1}{r_o}\right)}$$

Then the expected gain after putting in the values would be

$$A\left|\frac{V_{out}}{V_{in}}\right| = 65.66$$

Essentially, we want a high increase in the gain as to

Now looking at the hardware result we will see:

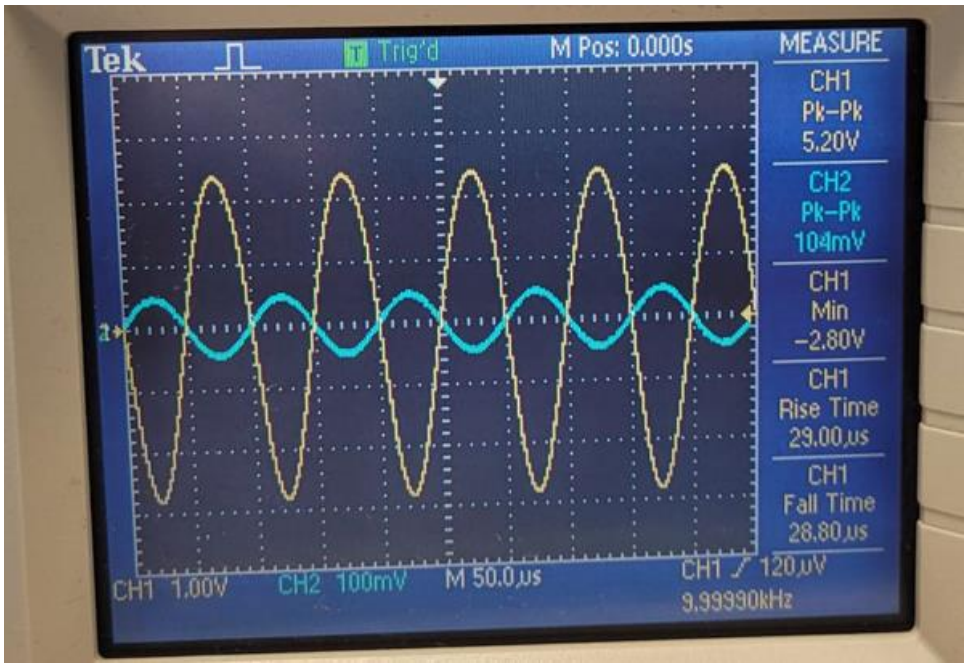

Figure 20: Gain with the Capacitor

Then the gain comes out as,

$$A\left|\frac{V_{out}}{V_{in}}\right| = 50$$

Though the result found is lower than the expected value, it is still within expectations as we expected to gain to increase to a high degree. The error essentially indicates that λ values is higher. As λ value increases r_o value goes down which will lower the gain as a result.

Conclusion

This lab's goal was to find out characteristics of NMOS FET and design a common source amplifier according to given characteristics. Essentially the first two parts of the lab allowed us to figure out threshold voltage, $\lambda \; and \; K_N$. One important thing I had struggled in this part was to pick two specific data points to be able to calculate $\lambda \; and \; K_N$ though the variation was minimal wherever I picked, I had to make sure that the data points I have acquired were correct which caused me to repeat part 2 several times. Otherwise, the expected gains I calculated in part 3 and 4 could have been extremely far off than its' actual values. Even then, I still acquired quite a bit of gain error in part 4. That means the final data point that I have chosen to calculate $\lambda \; and \; K_N$ from was still not accurate enough. This lab taught me the relations between λ, K_N and gain more comprehensively. I have realized that with one error in earlier steps could carry off to the next, which could have forced me to go back and do that part of the lab again.

Examining part 3 and part 4 of the lab, the importance of source resistance can be easily understood. It is a smart way to lower the gain and even with change input the gain was quite stable. One important detail to follow was the specifications of the circuit. With these specifications, I learnt how I can develop the small signal model first and see how my choice of values impact the circuit from both the small signal analysis and DC analysis point. In other words, I had to make sure that MOSFET was in saturation state while following the specifications that were made for the small signal representation of the circuit.

During part 3, it was also important to observe the distortion point as it gives an idea about why we want the MOSFET to be on saturation. I have learnt to be able to safely amplify the input signal without affecting its behavior, we need MOSFET to be always on saturation otherwise some parts of the signals get clipped.

One last can be said about the parallel capacitor to source resistance. Though the inclusion of this capacitor allowed extremely high gains, this could be an unwanted result as small changes in current will directly affect the output through g_m. It is important to have a stable circuit that doesn't instantly change its gain a lot depending on the current changes, eq (1) is a great example.

Appendixes

Appendix A- Code and Data from Part 1

```
a= [1.50000000000000    0;  %VDD vs ID
1.61000000000000    1;
1.76000000000000    2;
1.90000000000000    3;
2.04000000000000    4;
2.17000000000000    5;
2.30000000000000    6;
2.42000000000000    7;
2.54000000000000    8;
2.66000000000000    9;
2.79000000000000    10;
2.90000000000000    11;
3.02000000000000    12;
3.14000000000000    13;
3.25000000000000    14;
3.36000000000000    15;
3.48000000000000    16;
3.58000000000000    17;
3.70000000000000    18;
3.81000000000000    19;
3.92000000000000    20;
4.03000000000000    21;
4.14000000000000    22;
4.25000000000000    23;
4.36000000000000    24;
4.47000000000000    25;
4.58000000000000    26;
4.69000000000000    27;
4.77000000000000    28;
4.89000000000000    29;
5 30];

for x = 1:31
    a(x,1)= a(x,1)-0.1*a(x,2);
end
plot(a(:,1),a(:,2),"*");
Vds= a(:,1);
Id=a(:,2);
```

Figure 21: V_{DD} and $I_{D,}$ Matlab Code

Appendix B – Datas for V_{GS} = 1.81, 1.91 and 2.01V

```
n= [0   0; %VDD vs ID
0.150000000000000   1.29000000000000;
0.310000000000000   2.57000000000000;
0.470000000000000   3.93000000000000;
0.600000000000000   5.19000000000000;
0.780000000000000   6.53000000000000;
0.930000000000000   7.78000000000000;
1.07000000000000    8.77000000000000;
1.24000000000000    10.1500000000000;
1.39000000000000    11.4200000000000;
1.56000000000000    12.0100000000000;
1.70000000000000    12.2800000000000;
1.83000000000000    12.5200000000000;
2.01000000000000    13.0600000000000;
2.16000000000000    13.2700000000000;
2.31000000000000    13.3600000000000;
2.48000000000000    13.4400000000000;
2.63000000000000    13.4700000000000;
2.74000000000000    13.5100000000000;
2.87000000000000    13.5300000000000;
2.95000000000000    13.5500000000000;
3.07000000000000    13.5800000000000;
3.17000000000000    13.6100000000000;
3.24000000000000    13.6200000000000];
u= zeros(24,2);
u(:,1)=n(:,1)- 0.1*n(:,2);
u(:,2)=n(:,2);
figure
plot(u(:,1),u(:,2),".");
Vds= u(:,1);
Id=u(:,2);
```

Figure 22: V_{GS} = 1.81V

```
%1.91V
o=[0    0; %VDD vs ID
0.160000000000000   1.36000000000000;
0.310000000000000   2.65000000000000;
0.450000000000000   4.11000000000000;
0.630000000000000   5.60000000000000;
0.790000000000000   6.76000000000000;
0.920000000000000   8.07000000000000;
1.07000000000000    9.36000000000000;
1.29000000000000    10.9700000000000;
1.38000000000000    12.1200000000000;
1.54000000000000    13.5300000000000;
1.70000000000000    14.6800000000000;
1.85000000000000    15.9600000000000;
2   17.4000000000000;
2.16000000000000    18.5000000000000;
2.33000000000000    19.4100000000000;
2.48000000000000    20.7100000000000;
2.62000000000000    21.2100000000000;
2.81000000000000    22.1300000000000;
2.95000000000000    22.6600000000000;
3.10000000000000    23.0800000000000;
3.24000000000000    23.3900000000000;
3.42000000000000    23.4200000000000;
3.57000000000000    23.5600000000000;
3.71000000000000    23.7000000000000;
3.87000000000000    23.7700000000000;
4.03000000000000    23.8900000000000;
4.18000000000000    23.9600000000000;
4.33000000000000    24.0300000000000;
4.49000000000000    24.1300000000000];
o(:,1)=o(:,1)- 0.1*o(:,2);
o(:,2)=o(:,2);
plot(o(:,1),o(:,2),".");
Vds= o(:,1);
Id=o(:,2);
```

Figure 23: Datas and Code for V_{GS} = 1.91V

```
c=[0    0 %VDD vs ID
0.210000000000000   1.77000000000000;
0.420000000000000   3.79000000000000;
0.630000000000000   5.56000000000000;
0.800000000000000   7.12000000000000;
1   8.94000000000000;
1.20000000000000    10.7800000000000;
1.41000000000000    12.5100000000000;
1.61000000000000    14;
1.80000000000000    16.1700000000000;
2.01000000000000    17.9100000000000;
2.20000000000000    19.3700000000000;
2.40000000000000    21.4600000000000;
2.60000000000000    23.0300000000000;
2.80000000000000    25.1500000000000;
3   26.4800000000000;
3.30000000000000    28.7500000000000;
3.60000000000000    31.3600000000000;
3.80000000000000    32.9400000000000;
4.03000000000000    34.3400000000000;
4.20000000000000    35.6200000000000;
4.40000000000000    36.4300000000000;
4.60000000000000    37.1200000000000;
4.80000000000000    37.6300000000000;
5   37.8700000000000;
5.20000000000000    38.1800000000000;
5.40000000000000    38.4400000000000;
5.60000000000000    38.6100000000000;
5.80000000000000    38.9100000000000;
6   39.6700000000000];
c(:,1)=c(:,1)- 0.1*c(:,2);
c(:,2)=c(:,2);
figure
plot(c(:,1),c(:,2),".");
Vds= c(:,1);
Id=c(:,2);
```

Figure 24: Datas and Code for V_{GS} = 2.01V