Name: _____ **Section: _____**

Signature: _____ **EEE 313 Fall 2014-2015**

Bilkent University
Department of Electrical and Electronics Engineering
EEE 313 Electronic Circuit Design
Midterm 1
25 October 2014, 10:00
(4 questions, 120 minutes)

- This is a **closed book**, closed notes exam. No cheat sheet allowed.
- All cell-phones should be completely **turned off**.
- Use a calculator for numerical computations. Carry at least **4 significant digits** during calculations. Your final answer should be at least **3 significant digits**.
- Be sure to write the **units** of all numerical results.
- **Show** all work clearly.
- Please put your **final answer** for each part inside a box for easy identification. Do not give multiple answers, they will not be graded.
- Do not remove the **staple** from the exam sheets or separate pages of the exam. All extra pages must be stamped to your exam.
- You may leave the exam room when you are done. However, please do not leave during the **last five minutes** of the exam.
- At the end of the exam, please stay seated unitl **all** exam papers are collected.

FET equations:

n-channel MOSFET

$i_D = K_n(v_{GS} - V_{Tn})^2$ SAT

$i_D = K_n\left[2(v_{GS} - V_{Tn})v_{DS} - v_{DS}^2\right]$ NON-SAT

p-channel MOSFET

$i_D = K_p(v_{SG} + V_{Tp})^2$ SAT

$i_D = K_p\left[2(v_{SG} + V_{Tp})v_{SD} - v_{SD}^2\right]$ NON-SAT

n-channel JFET

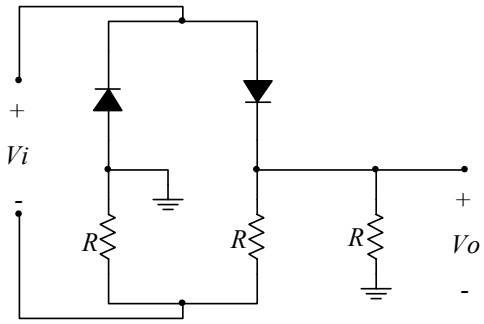
$i_D = \frac{I_{DSS}}{V_p^2}(v_{GS} - V_P)^2$ SAT

$i_D = \frac{I_{DSS}}{V_p^2}\left[2(v_{GS} - V_P)v_{DS} - v_{DS}^2\right]$ NON-SAT

Please do not write below this line

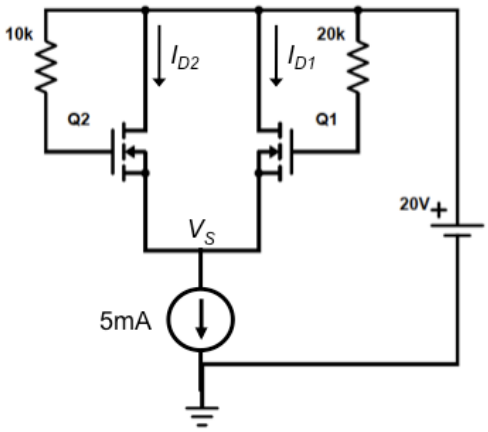
1. 25 pts.	
2. 20 pts.	
3. 25 pts.	
4. 30 pts.	
Total 100 pts.	

1. (20 points) The input signal V_i is a sinusoid with an amplitude of 20 V. For the diode assume V_g=0 V (i.e., V_{on} voltage) and that the diodes are ideal. All resistors are equal to 10 kΩ. Determine the output signal V_o.

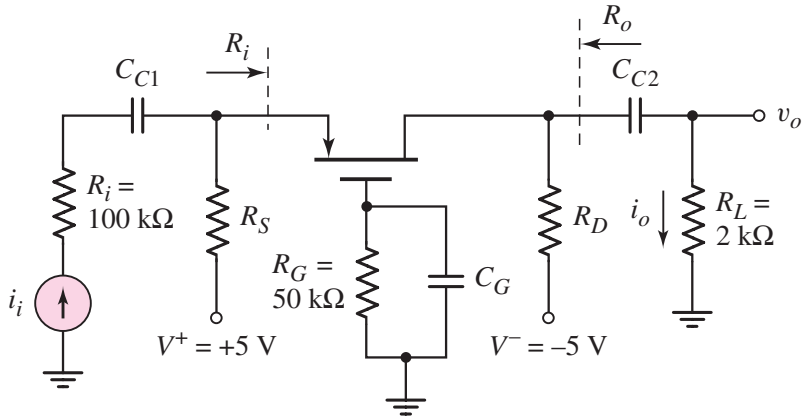


2. (20 points) For the following circuit, find the states of the n-channel MOS enhancement mode transistors Q1 and Q2, assuming that $V_{Tn1}= V_{Tn2}=2.5V$, and $K_{n1}=4$ $K_{n2}=1mA/V^2$.

Q_1 state	Q_2 state	I_{D1}	I_{D1}	V_S



3. (30 points) Consider the p-channel MOS common-gate circuit in the figure. The transistor parameters are: $V_{TP} = -1$ V, $K_p = 0.5$ mA/V^2, and $\lambda = 0$. (a) Determine R_S and R_D such that $I_{DQ} = 0.75$ mA and $V_{SDQ} = 6$ V. (b) Determine the input impedance R_i and the output impedance R_o. (c) Determine the load current i_o and the output voltage v_o, if $i_i = 5\sin(\omega t)$ μA. Assume all capacitors are very large. V^+ and V^- are applied DC voltages.



4. (30 points) Design the common source circuit below using an n-channel enhancement-mode MOSFET. The quiescent values are to be I_{DQ}= 5mA and V_{GSQ}= 4V. The transconductance is g_m=10mA/V. Let R_L=1kΩ, $A_v = v_{out}/v_{in} = -5$, R_{in}= 48kΩ. Find:

a) (10 points) R_1 and R_2
b) (10 points) R_D
c) (5 points) K_n
d) (5 points) V_{tn}