21-10-2017

BILKENT UNIVERSITY

Department of Electrical and Electronics Engineering

EEE313 Electronic Circuit Design

Midterm Exam I

SOLUTION

Surname: ______________________________

Name: ______________________________

ID-Number: ______________________________

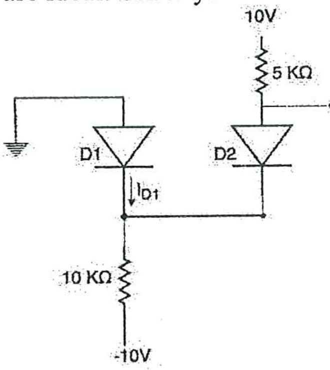
Signature: ______________________________

Duration is 110 minutes. Solve all 6 questions. Show all your work.
No books or notes.

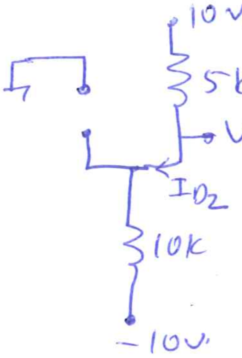
Q1 (20 points)	
Q2 (20 points)	
Q3 (10 points)	
Q4 (20 points)	
Q5 (20 points)	
Q6 (10 points)	
Total (100 points)	

Q1.

(a) Find V_O and I_{D1} in the circuit below. Justify the states of the diodes. Diodes in this circuit are ideal. Show your work.



Assume D_1 is OFF and D_2 is ON:



$I_{D_2} = \frac{10-(-10)}{5+10} = \frac{20}{15} = 1.33\,mA.$

$I_{D_2} > 0$ ∴ D_2 is ON. (2 p)

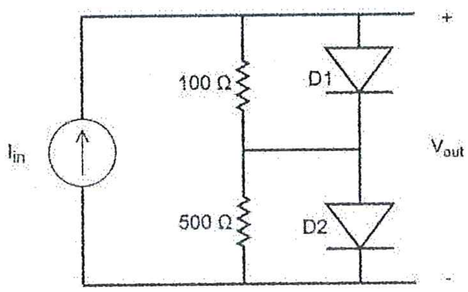
$V_O = 10 - I_{D_2} \times r = 10 - 5 \times 1.33 = 3.33\,V.$ (3 p)

$V_{D_1} = 0 - 3.33 = -3.33 < 0$ ✓ D_1 is OFF (3 p)

If another assumption is made and contradiction found, then +1 points.

⇒ Result $V_O = 3.33\,V.$
$I_{D_1} = 0$. (2 p)

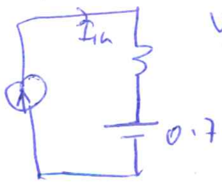
(b) Find and plot V_{out} versus I_{in} tranfer characteristics for the circuit below (Horizontal axis is I_{in} and the vertical axis is V_{out}). The cutin voltage for the diodes is $V_\gamma = 0.7$ V. Justify the states of the diodes. Show your work.



For low current both diodes are OFF and $V_{out} = I_{in} \times 600$

This ends when D_2 turn ON at $I_{in} \times 0.5 = 0.7$

$I_{in} = \frac{7}{5} = 1.4\,mA$

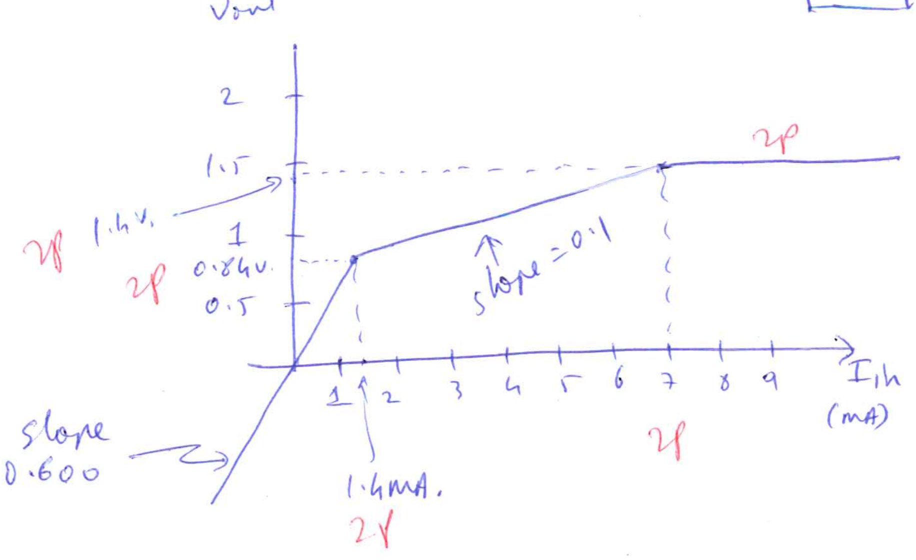


$V_{out} = 0.7 + 0.1\,I_{in}$

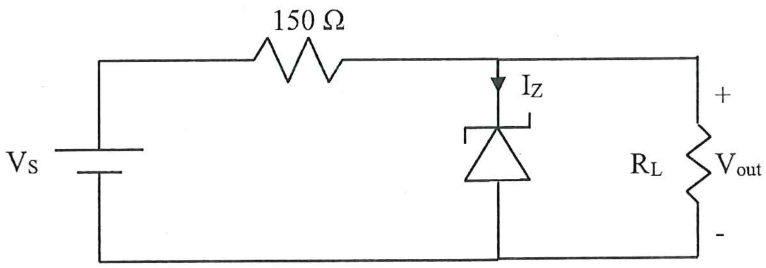
This continues until $I_{in} \times 0.1 = 0.7$

⇒ $I_{in} = 7\,mA.$

After which both diodes are ON and $V_{out} = 1.4\,V.$



Q2. For the circuit below, $V_S = 60$ V, the Zener diode has a Zener voltage of 15 V and an incremental resistance of 0 Ω. The Zener current I_Z needs to be more than 15 mA and the power rating of the Zener is 4 W. Show your work.



a) Determine the range of I_Z for proper operation of the Zener.
b) Find the range of the DC voltage source V_S such that the current limitations of the Zener diode are not violated, for $R_L = 150$ Ω.
c) Determine the range of the load resistor, R_L, for when $V_S = 60$ V, such that the current limitations of the Zener diode are not violated.

Solution:

a) $15\,mA < I_Z < \frac{4000}{15} = 267\,mA.$ (4P)

b) $R_L = 150\,\Omega = 0.15\,k\Omega.$

$$I_Z = \frac{V_S - 15}{0.15} - \frac{15}{0.15} = \frac{V_S - 30}{0.15}\ mA.$$

$$15 < I_Z < 267$$

$$15 < \frac{V_S - 30}{0.15} < 267$$

$$2.25 < V_S - 30 < 40$$

4P 4P

$$\boxed{32.25 < V_S < 70\ V.}$$

c) $V_S = 60$

$$I_Z = \frac{60-15}{0.15} - \frac{15}{R} = \frac{45}{0.15} - \frac{15}{R} = 300 - \frac{15}{R}$$

$$15 < I_Z < 267$$

$$15 < 300 - \frac{15}{R} < 267$$

$$-285 < -\frac{15}{R} < -33.33$$

$$285 > \frac{15}{R} > 33.33$$

$$285^{-1} < \frac{R}{15} < 33.33^{-1}$$

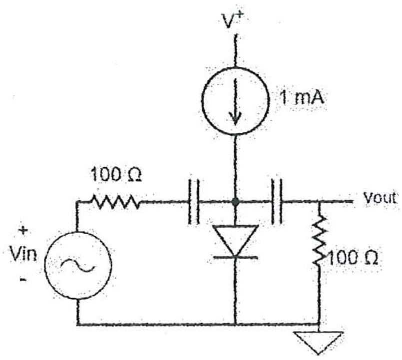
4P 4P

$$\frac{15}{285} < R < \frac{15}{33.33} \Rightarrow \boxed{52.6\,\Omega < R < 450}$$

Q3. In the circuit below, v_{in} = 10sinwt mV. Capacitors are very large.

a) Derive the formula for the incremental (small signal) resistance of the diode $r_d = V_T/I_{DQ}$.

b) Find the small signal component of the output voltage at 300°K (V_T = 26 mV). Show your work.



Solution

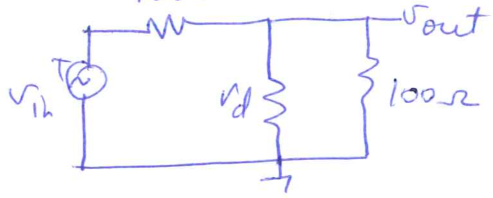
a) $$i_D = I_S\left(e^{\frac{v_D}{V_T}} - 1\right) \approx I_S e^{\frac{v_D}{V_T}} = I_S e^{\frac{(V_{DQ}+v_d)}{V_T}} = \underbrace{I_S e^{\frac{V_{DQ}}{V_T}}}_{I_{DQ}} e^{v_d/V_T}$$

$$\cong I_{DQ}\left(1 + \frac{v_d}{V_T}\right) = I_{DQ} + \underbrace{\frac{I_{DQ}}{V_T} v_d}_{i_d}$$

$$i_d = \frac{I_{DQ}}{V_T} v_d$$

$$v_d = \frac{V_T}{I_{DQ}} i_d = r_d i_D \quad \text{where } r_d = \frac{V_T}{I_{DQ}} \quad (5p)$$

b)



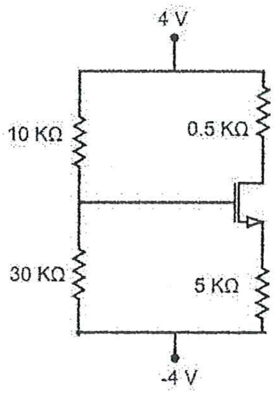
$$r_d = \frac{0.026}{1mA} = 26\Omega \quad (1p)$$

$$r_d // 100 = 26 // 100 = 20.6\Omega.$$

$$v_{out} = \frac{20.6}{20.6 + 100} \times 10 \sin wt\,(mV)$$

$$= 1.71 \sin wt\,(mV) \quad (4p)$$

Q4. The nMOS transistor in the circuit below has the parameters $V_{TN} = 0.8V$ and $K_n = 0.5mA/V^2$. Determine I_D, V_{GS}, and V_{DS}. Justify your results. Show your work.



$$V_G = 4\times\frac{30}{30+10} + \frac{-4\times 10}{30+10} = 4\left(\frac{3}{4}-\frac{1}{4}\right)$$

$$= 4\times\frac{2}{4} = 2V.$$

$$V_{GS} = V_G - (5I_D - 4) = 2 - 5I_D + 4$$

$$= 6 - 5I_D$$

Assume SAT $I_D = K_n(V_{GS}-V_{TN})^2 = 0.5(6-5I_D-0.8)^2$

$$= 0.5(5.2-5I_D)^2$$

$$2I_D = 5.2^2 - 52I_D + 25I_D^2$$

$$25I_D^2 - 54I_D + 27.04 = 0$$

$$I_D = \begin{cases} 1.37\,mA \Rightarrow V_{GS} = 6-5\times1.37 = -0.85 \not> 0.8 & \times \\ 0.79\,mA \Rightarrow V_{GS} = 6-5\times0.79 = 2.056 > 0.8 & \checkmark \end{cases}$$

∴ $\boxed{I_D = 0.79\,mA.}$ and $\boxed{V_{GS} = 2.056\,V.}$

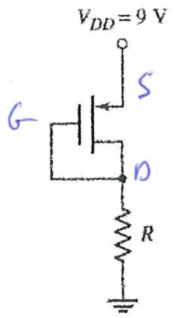
$$V_{DS} = 4 - 0.79\times0.5 - 5\times0.79 + 4 = 3.66\,V.$$

$3.66 > 2.056 - 0.8$ ✓ ∴ SAT.

$\Rightarrow \boxed{V_{DS} = 3.66\,V.}$

Q5.

(a) The pMOS transistor in the figure below has $V_{TP} = -0.7$V and $\lambda = 0$. Find the values of R and the K_p of the transistor so that $I_D = 0.1$ mA and $V_{SD} = 2.5$ V. Justify the state of the transistor. Show your work.



$V_{SG} = V_{SD} \Rightarrow V_{SD} > V_{SG} + V_{TP} \Rightarrow$ Tr is SAT or OFF

Since $I_D = 0.1$ mA > 0

Tr must be SAT.

$I_D = K_p(V_{SG} - 0.7)^2$

$0.1 = K_p(2.5 - 0.7)^2 = K_p \times 1.8^2$

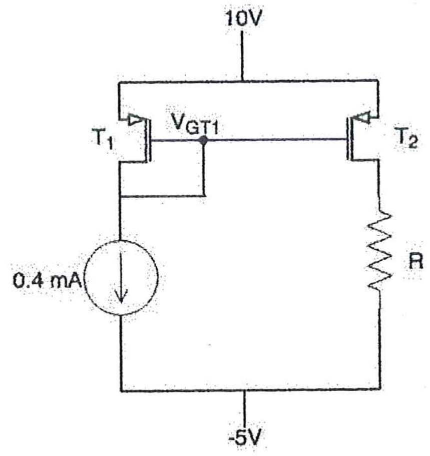
$K_p = \frac{0.1}{(1.8)^2} = 0.0309$ mA/V^2

$9 - V_{SD} - I_D \times R = 0 \Rightarrow 9 - 2.5 = 0.1R$

$R = \frac{6.5}{0.1} = 65$ k

(b) In the circuit below T_1 and T_2 are identical (matched pair) with $V_{TP} = -1$ V and $K_p = 0.1$ mA/V^2.

Find V_{GT1}. Find the range of R for the current mirror to operate properly.



T1 is SAT:

$0.4 = 0.1(V_{SG_1} - 1)^2$

$4 = (V_{SG_1} - 1)^2 \Rightarrow \pm 2 = V_{SG_1} - 1$

$V_{SG_1} = 1 \pm 2$ → $3 > 1$ ✓, $-1 < 1$ ✗

$\therefore V_{SG_1} = 3$V $\Rightarrow \boxed{V_{GT_1} = 7V}$

Assume T_2 is SAT: $\Rightarrow I_{D_2} = 0.4$ mA. $\Rightarrow V_{SD_2} = 10 - (0.4R - 5)$
$= 15 - 0.4R$

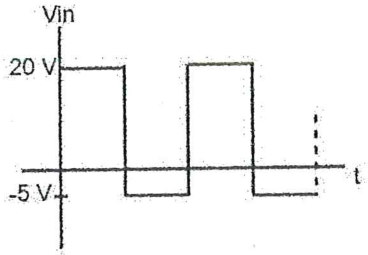
We need $V_{SD_2} > V_{SG_2} + V_{TP}$

$\Rightarrow 15 - 0.4R > 3 - 1$

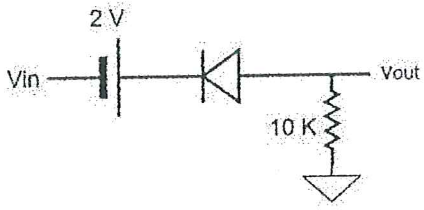
$13 > 0.4R$

$R < \frac{13}{0.4} = 32.5$ k.

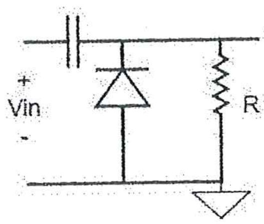
Q6. For the input signal V_{in} as drawn below, find and draw the output signals, V_{out}, for the circuits in (a) and (b). The cutin voltage for the diodes is $V_\gamma = 0.7$ V. Show your work. Initial value of the capacitor voltage is zero. R in (b) is very large.

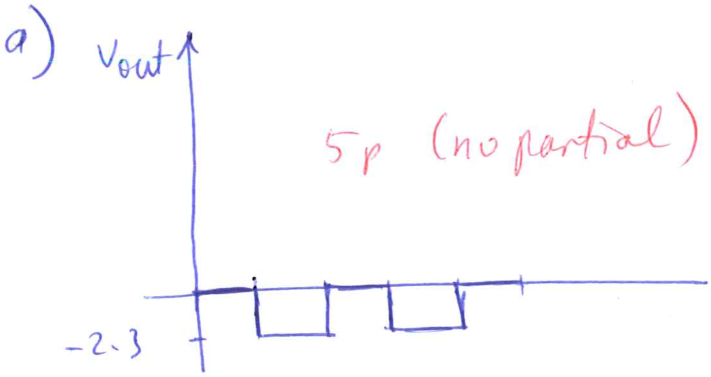


(a)



(b)





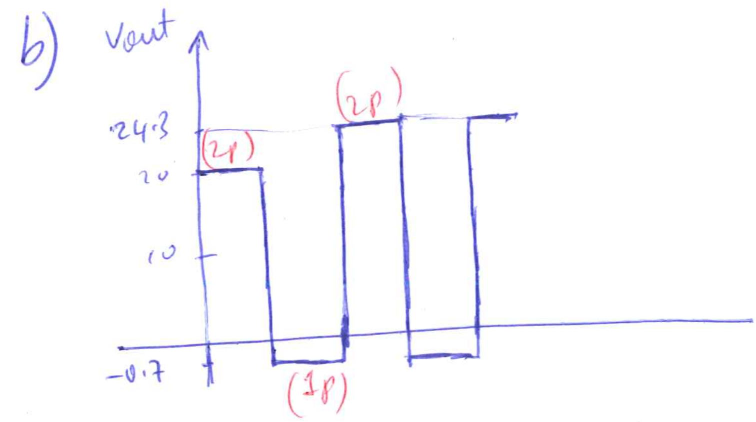


Table 3.1 Summary of the MOSFET current–voltage relationships

NMOS	PMOS
Nonsaturation region ($v_{DS} < v_{DS}(\text{sat})$)	Nonsaturation region ($v_{SD} < v_{SD}(\text{sat})$)
$i_D = K_n[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2]$	$i_D = K_p[2(v_{SG} + V_{TP})v_{SD} - v_{SD}^2]$
Saturation region ($v_{DS} > v_{DS}(\text{sat})$)	Saturation region ($v_{SD} > v_{SD}(\text{sat})$)
$i_D = K_n(v_{GS} - V_{TN})^2$	$i_D = K_p(v_{SG} + V_{TP})^2$
Transition point	Transition point
$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$	$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$
Enhancement mode	Enhancement mode
$V_{TN} > 0$	$V_{TP} < 0$
Depletion mode	Depletion mode
$V_{TN} < 0$	$V_{TP} > 0$

Equation for diode current is:

$$I_D = I_S\left[e^{\left(\frac{V_D}{V_T}\right)} - 1\right]$$