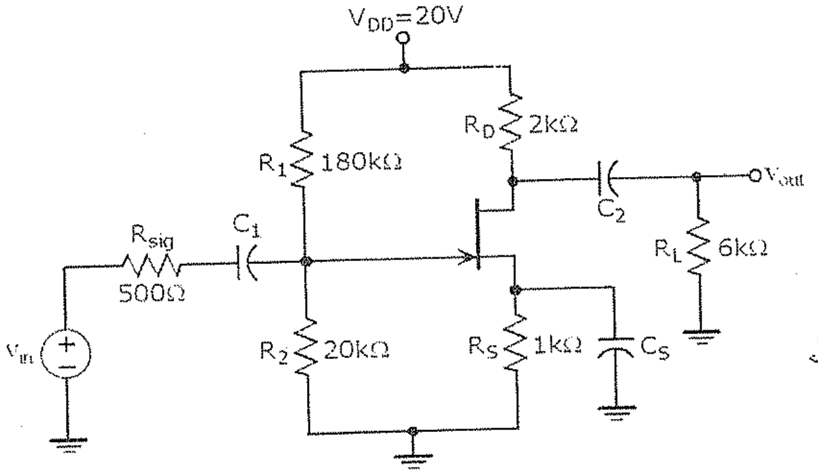
Q4. (20 points) For the JFET amplifier circuit shown below, you are given that $I_{DSS} = 16\ mA$, $V_P = -4\ V$ and $I_{DQ} = 4\ mA$. Assume that the capacitor values are very large.

a. Draw the small-signal ac equivalent circuit and calculate the the small-signal parameter g_m of the transistor.

b. Find the input resistance (R_{in}) and the output resistance (R_{out}) of the amplifier.

c. Determine the voltage gain, $A_v = v_{out} / v_{in}$.

d. Find the maximum possible peak-to-peak undistorted symmetric output voltage swing.



$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

$$V_{GSQ} = (-4)\left(1 - \sqrt{\frac{4}{16}}\right) = -2V$$

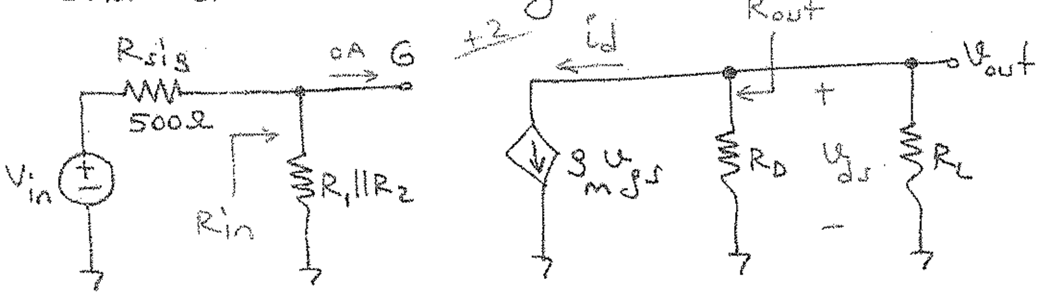
$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{GS}=V_{GSQ}} = \frac{2 I_{DSS}}{(-V_P)}\left(1 - \frac{V_{GSQ}}{V_P}\right)$$

+2

$$g_m = \frac{(2)(16)}{4}(1 - 0.5) = \boxed{4mA/V}$$

SOLUTION:

(a) Assume that the capacitors are short circuit in ac analysis.



$$\boxed{i_d = \frac{-v_{ds}}{R_D || R_L}}$$

ac load line

(b) $R_{in} = R_1 || R_2 = \boxed{18k\Omega}$ +2

To find Rout, we kill v_{in}. Then $v_{gs} = 0$ and $i_d = 0$.

Therefore, $R_{out} = R_D = \boxed{2k\Omega}$ +2

(c) $v_{out} = -g_m v_{gs} (R_D || R_L)$ where $v_{gs} = \dfrac{R_1||R_2}{R_{sig} + R_1||R_2} v_{in}$

+2

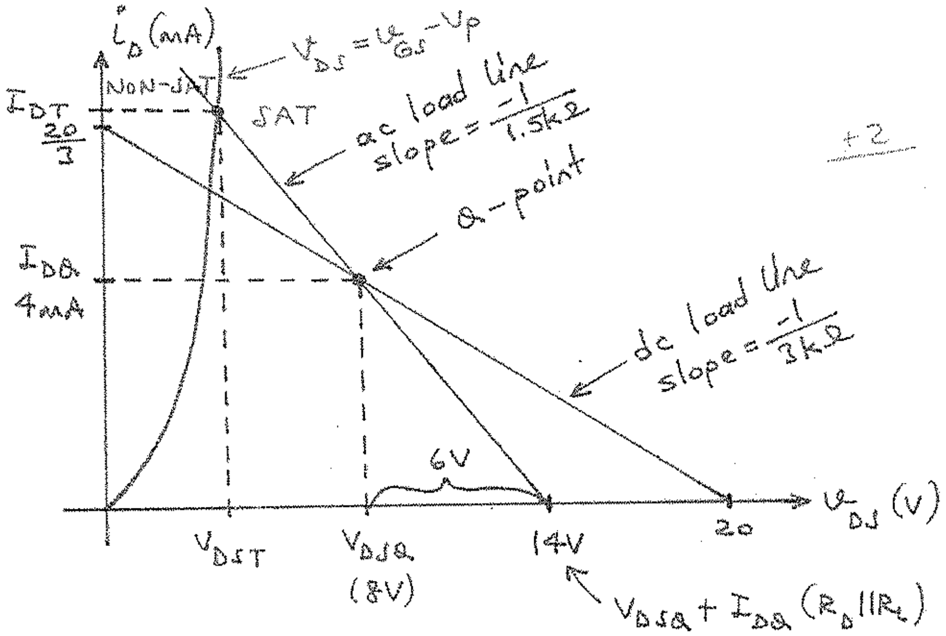
$$A_v = \frac{v_{out}}{v_{in}} = -g_m (R_D||R_L)\left(\frac{R_{in}}{R_{sig} + R_{in}}\right) \quad +1$$

$$\boxed{A_v = -5.838} \quad +1$$

(d) $\boxed{V_{DS} = V_{DD} - I_D(R_D + R_S)}$ dc load line : slope $= \dfrac{-1}{R_D + R_S} = -\dfrac{1}{3k\Omega}$

$V_{DSQ} = 20 - (4mA)(3k\Omega) = 8V$ +1

$\boxed{i_d = -\dfrac{v_{ds}}{R_D \| R_L}}$ ac load line : slope $= \dfrac{-1}{R_D \| R_L} = -\dfrac{1}{1.5k\Omega}$



+2 +1

On the boundary curve between SAT and NON-SAT regions

$$v_{DST} = v_{GST} - V_P \Rightarrow i_{DT} = \frac{I_{DSS}}{V_P^2} v_{DST}^2$$

Using ac load line, we can write that

$$\frac{i_{DT}}{v_{DST} - 14} = \frac{-1}{R_{ac}} \Rightarrow i_{DT} = \frac{14 - V_{DST}}{R_D \| R_L} = \frac{I_{DSS}}{V_P^2} v_{DST}^2$$

$$\frac{14 - v_{DST}}{1.5k\Omega} = \frac{16mA}{16} v_{DST}^2$$

$1.5 v_{DST}^2 + v_{DST} - 14 = 0$

+3 $\boxed{v_{DST} = 2.73985V} \longrightarrow i_{DT} = 7.5068mA$ and $v_{GST} = 0.73985V$

Max. possible positive peak of v_{ds} is 6V.

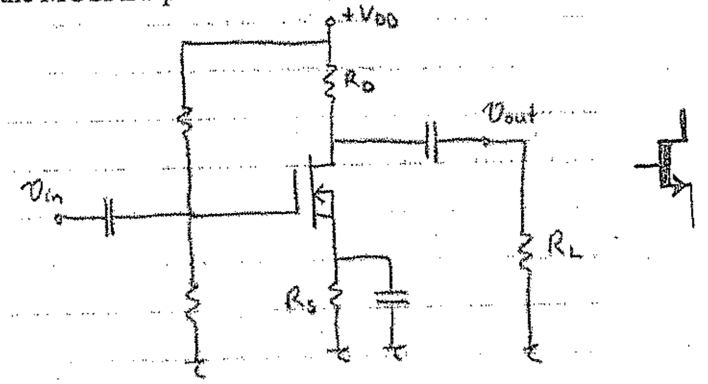
Max. possible negative peak of v_{ds} is 5.2602V

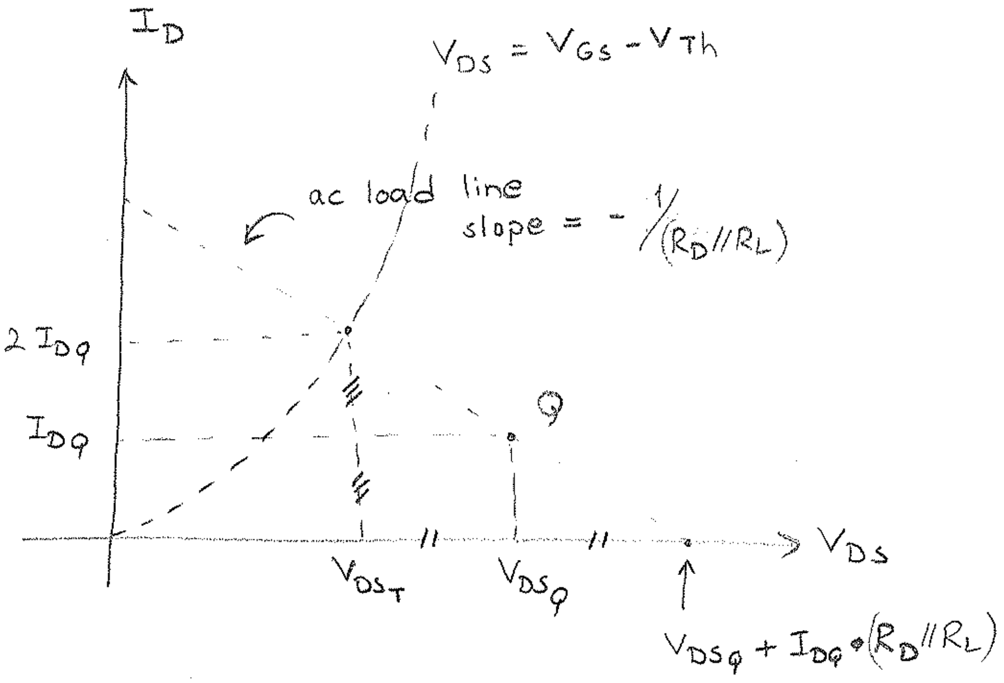
Therefore,

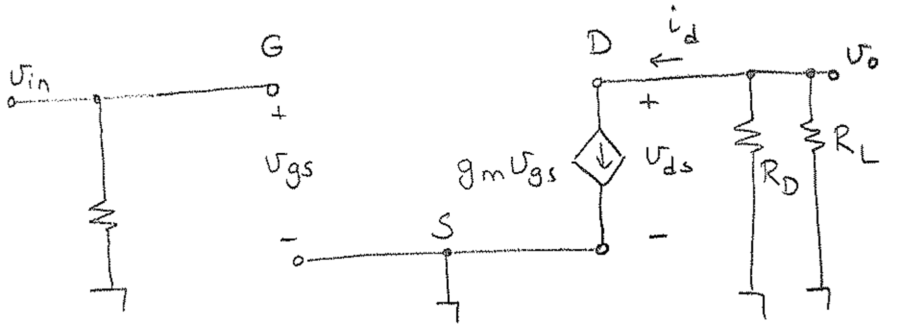
$V_{PP} = 2\min(5.2602, 6) = 2(5.2602)$

$\boxed{V_{PP} = 10.52}$ +1

3. (20 points) Consider the single stage MOSFET amplifier shown in the figure. Your aim is to find the quiescent drain current I_{DQ} so that the maximum undistorted (unclipped) peak-to-peak output voltage swing is as large as possible for a given set of R_D, R_S, R_L, and V_{DD}. Derive an equation for I_{DQ} in terms of the given set of values plus the MOSFET parameters K_n and V_{TH}.







$$\left.\begin{aligned} i_d &= g_m v_{gs} \\ v_{ds} &= -g_m v_{gs}(R_D /\!/ R_L) \end{aligned}\right\} \quad i_d = -\frac{v_{ds}}{(R_D /\!/ R_L)}$$

$$\therefore R_{ac} = -R_D /\!/ R_L$$

$$I_{DQ} \cdot R_S + V_{DSQ} + I_{DQ} R_D = V_{DD}$$

$$\boxed{V_{DSQ} = V_{DD} - I_{DQ}(R_D + R_S)}$$

$$V_{DS_T} = V_{GS_T} - V_{Th}$$

$$I_{DT} = 2 I_{DQ} = K_n (V_{GS_T} - V_{Th})^2$$

$$I_{DT} = 2 I_{DQ} = K_n (V_{DS_T})^2$$

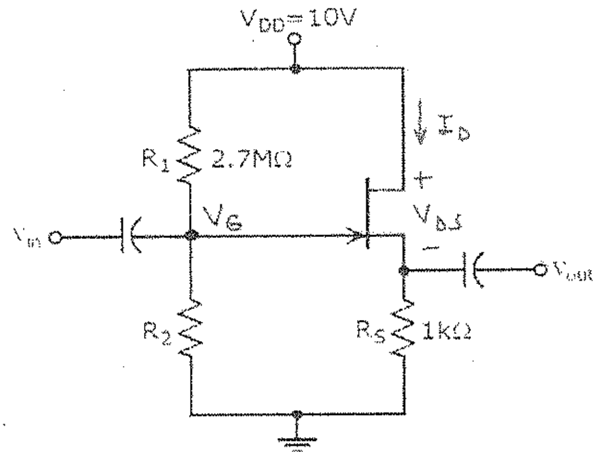
$$2 I_{DQ} = K_n \left[V_{DSQ} - I_D (R_D /\!/ R_L)\right]^2$$

$$2 I_{DQ} = K_n \left[V_{DD} - I_D (R_S + R_D) - I_D (R_D /\!/ R_L)\right]^2$$

1. (30 points) Given $I_{DSS} = 15mA$ and $V_P = -5V$. Assume that the capacitor values are very large. Design the following FET amplifier circuit.

a. Find the value of R_2 such that the transistor operates at the edge of the SAT and NON-SAT regions.

b. Find the value of R_2 such that the undistorted symmetric output voltage swing is as large as possible. And determine the value of the undistorted symmetric output voltage swing ($V_{peak\text{-}to\text{-}peak}$).



SOLUTION:

(a) At the edge of the SAT and NON-SAT regions: +3

$V_{DST} = V_{GST} - V_P$

+2 $V_{DST} = V_{DD} - I_{DT} R_S$ (KVL)

$V_{DST} = V_{DD} - \frac{I_{DSS} R_S}{V_P^2} (V_{GST} - V_P)^2$

$V_{DST} = V_{DD} - \frac{I_{DSS} R_S}{V_P^2} V_{DST}^2$

$0.6 V_{DST}^2 + V_{DST} - 10 = 0$

+5 $\boxed{V_{DST} = \frac{10}{3} V}$ must be positive

Then $V_{GST} = V_{DST} + V_P = \frac{10}{3} - 5$

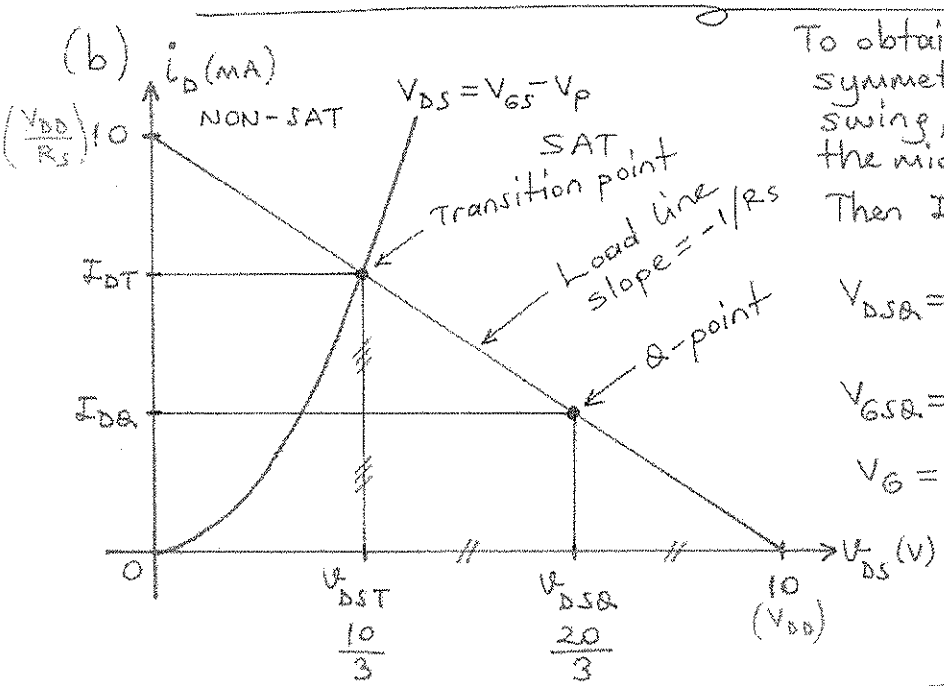
$\boxed{V_{GST} = -\frac{5}{3} V}$

$I_{DT} = \frac{V_{DD} - V_{DST}}{R_S} = \frac{10 - 10/3}{1k\Omega} \Rightarrow \boxed{I_{DT} = \frac{20}{3} mA}$

$V_G = V_{GST} + I_{DT} R_S = -\frac{5}{3} + \left(\frac{20}{3} mA\right)(1k\Omega) \Rightarrow \boxed{V_G = 5V}$

Therefore, $R_1 = R_2$ and $\boxed{R_2 = 2.7M\Omega}$ +5

(b)



To obtain max. undistorted symmetric output voltage swing, Q-point must be in the middle of SAT region.

Then $I_{DQ} = \frac{I_{DT}}{2} = \boxed{\frac{10}{3} mA}$

$V_{DSQ} = V_{DD} - I_{DQ} R_S = \boxed{\frac{20}{3} V}$ +4

$V_{GSQ} = V_P \left(1 - \sqrt{\frac{I_{DQ}}{I_{DSS}}}\right) = \boxed{-2.643V}$

$V_G = V_{GSQ} + I_{DQ} R_S = 0.6903V$

$V_G = \frac{R_2}{R_1 + R_2} V_{DD}$

$\boxed{R_2 = 200.2k\Omega}$ +6

+5 $V_{PP} = 2\left(\frac{10}{3}\right) = \boxed{\frac{20}{3} V}$ maximum.