Bilkent University

Spring 2019-2020

EEE 313: Electronic Circuit Design

Midterm #1

Name and Surname: **Student ID:**

Signature:

Exam Duration: 120 minutes

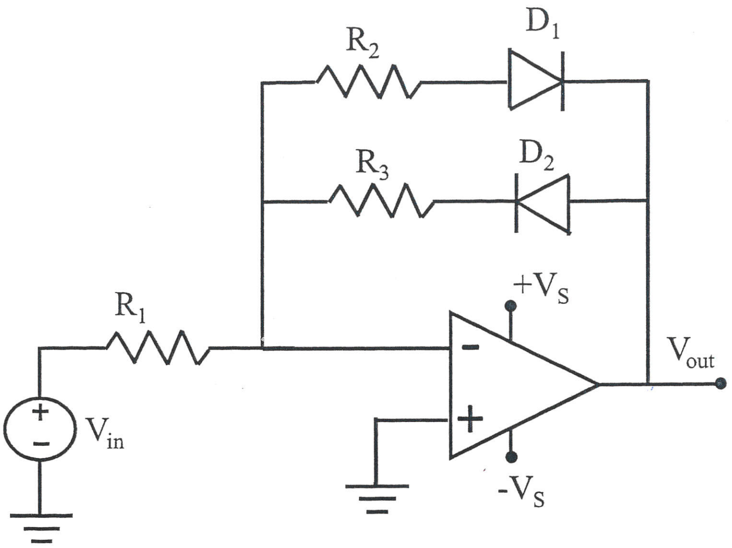
Question#	Your score	Out of
1		25
2		15
3		20
4		20
5		20
Total:		**100**

Instructions:

1. Calculators without extensive memory are allowed
2. Clearly explain all your answers in order to receive credit
3. Put a box around your final answer
4. Cheat sheets are not allowed
5. Indicate the units for your final answers
6. Write your student ID on the bottom of every page

1. (25 points)

a. (10 points)



You are given the OPAMP circuit on the left with two diodes. Plot V_{out}/V_{in} by assuming OPAMP always operates in the linear region without going into saturation. The diodes are ideal with 0V turn on potential. Explain the circuit operation as much as possible. Verify the states of the diodes whenever you make assumptions.

$$\frac{V_{in}-0}{R_1} + \frac{V_{out}-0}{R_{2,3}} = 0 \Rightarrow \frac{V_{out}}{V_{in}} = -\frac{R_{2,3}}{R_1}$$, inverting amplifier. 02

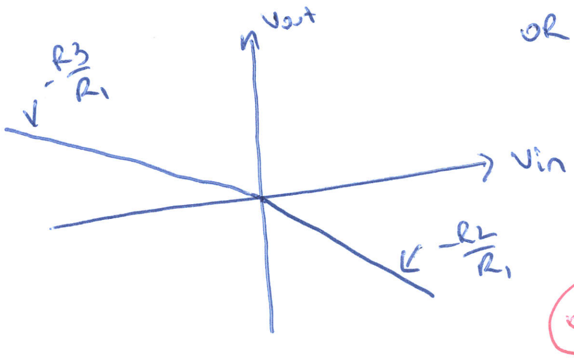
D_1 turns ON when $V_{out} < 0$, $V_{in} > 0$, D2 off

D_2 turns ON when $V_{out} > 0$, $V_{in} < 0$, D1 off

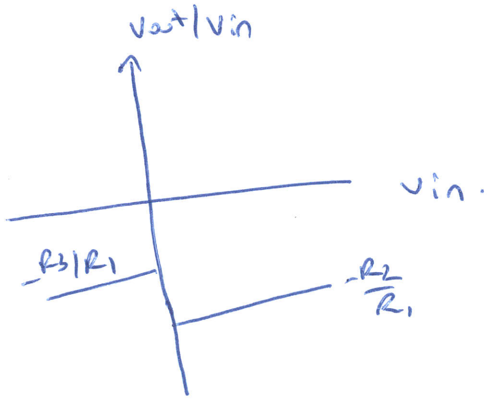
explaining the ckt. operation. 05

So when $V_{in} > 0$ $\frac{V_{out}}{V_{in}} = \frac{-R_2}{R_1}$

$V_{in} < 0$ $\frac{V_{out}}{V_{in}} = \frac{-R_3}{R_1}$



OR



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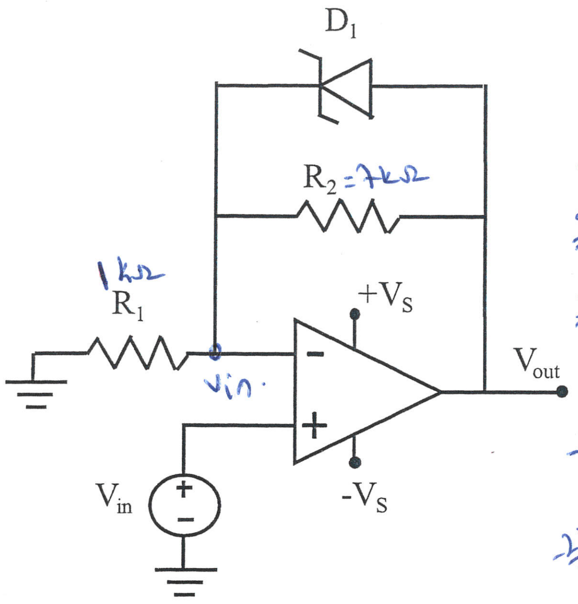
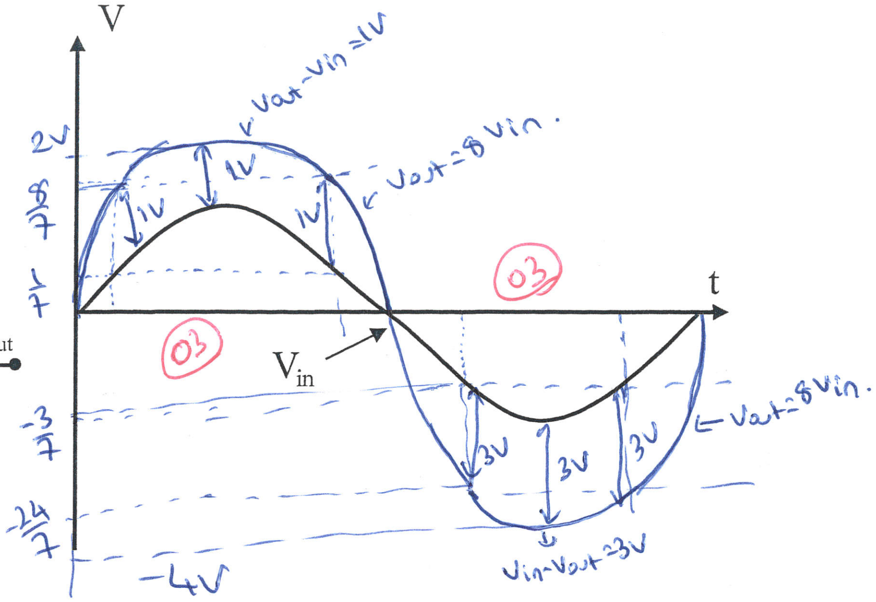
b. (15 points)





The OPAMP circuit is modified with a Zener diode for this part of the question. V_{in}=1sinωt V, R_1=1kΩ, R_2=7kΩ, and the Zener voltage is 3V in reverse bias and V_{on}=1V in forward bias for the Zener diode. By assuming ideal and linear OPAMP operation without saturation, find and plot $V_{out}(t)$ for one period on the provided graph. $V_{in}(t)$ is plotted for reference. Clearly label all the critical voltage values and explain the reasoning behind your answer.

w/o zener

$V_+ = V_- = V_{in}$, $\frac{V_{in}}{R_1} + \frac{V_{in}-V_{out}}{R_2} = 0$ 03 non-inverting amplifier.

$V_{in}\left(\frac{1}{R_1}+\frac{1}{R_2}\right) = \frac{V_{out}}{R_2} \Rightarrow V_{in}\left(\frac{R_1+R_2}{R_1R_2}\right) = \frac{V_{out}}{R_2}$, $\frac{V_{out}}{V_{in}} = 1+\frac{R_2}{R_1} = 8$

~~when~~ The + cycle of Vin, when Vout-Vin<1V regular Vout = 8 Vin.

when Vout-Vin=1V zener turns on forward bias and $\boxed{V_{out}-V_{in}=1V}$

03

7Vin=1V Vin=$\frac{1}{7}$V Vout=$\frac{8}{7}$V Vout follows Vin with 1V increase.

The - cycle of vin:

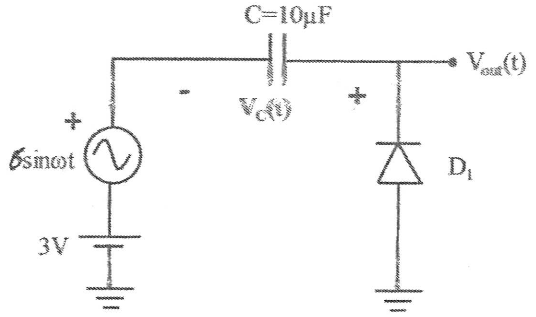
when Vin-Vout<3V regular Vout=8Vin.

03 when Vin-Vout=3V zener turns on reverse bias and Vin-Vout=3V

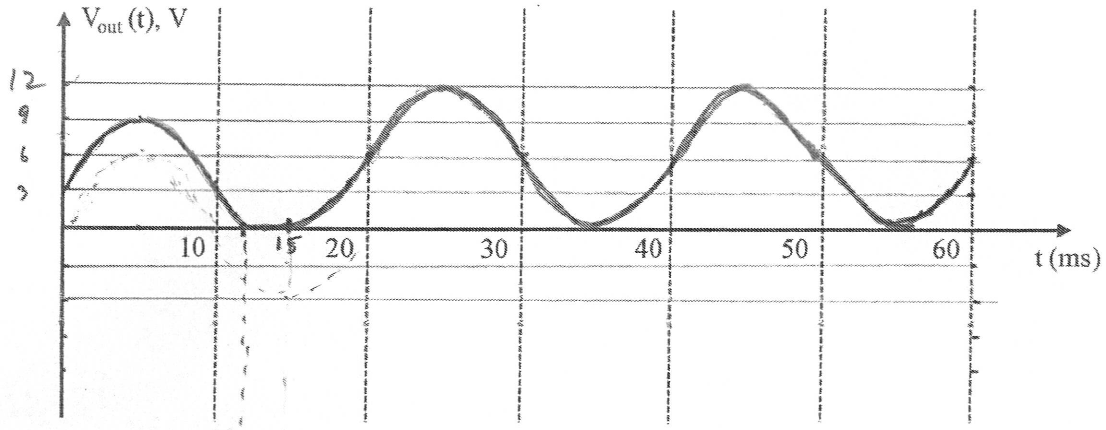
-7Vin=3V Vout follows Vin with 3V decrease.

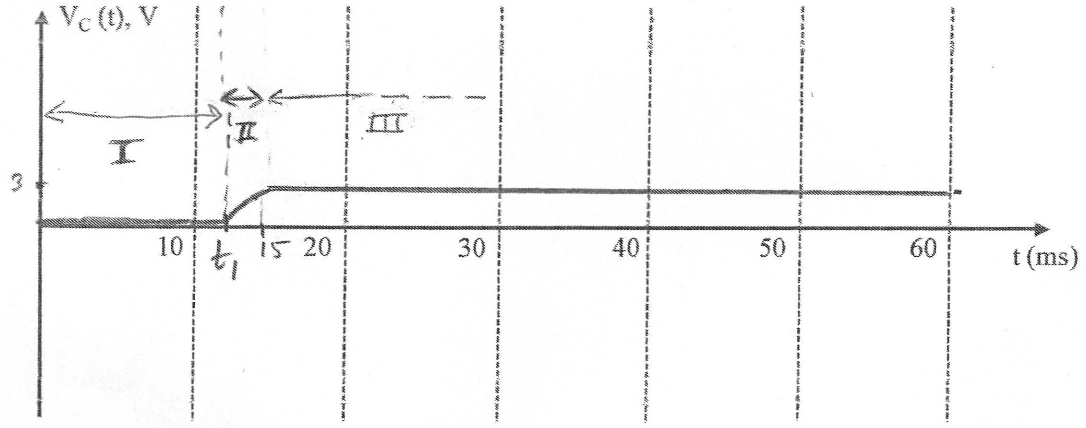
Vin=$-\frac{3}{7}$ Vout=$-\frac{24}{7}$V

2. (15 points)



You are given the clamper circuit shown on the left. Find and plot $V_{out}(t)$ and $V_C(t)$ for $0<t<60$ms by assuming the diode is ideal and $\omega=2\pi f$, f=50Hz. The graphs are provided below. The capacitor voltage at t=0 is 0V, $V_C(0)=0$ V.





$6 \sin wt = 3$

$\sin wt = \frac{3}{6} = 0.5$

$wt = 0.5236$

$t = \frac{0.5236}{2\pi \times 50} = 0,0017\,s = 1.7\,ms$ $\quad t_1 = 11.7$ msec.

phase I : 3p

phase II : 2p

phase III : 8p

t_1 : 2p

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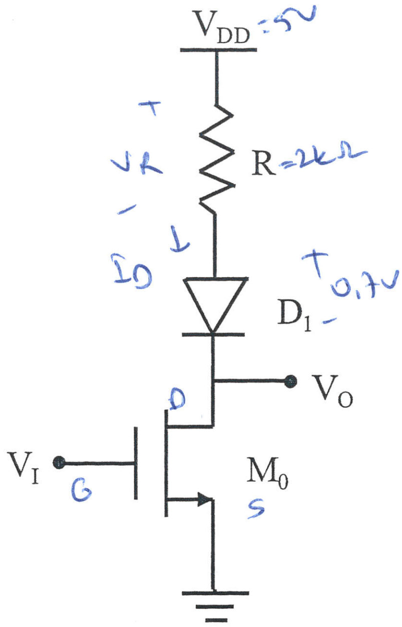
$wt = 30°$

$t = \frac{30°}{360° \times 50} = 0.0017$

3. (20 Points)



For the diode-transistor circuit shown on the left: R=2kΩ, K_N=0.1mA/V^2, V_{TN}=1V, λ=0, and the diode is ideal with V_{ON}=0.7V. V_{DD} = 5V and the input voltage is varied between 0 and 5V.

i. Find V_O when V_I is slightly larger than V_{TN}
ii. Find V_O when V_I =5V
iii. Find the V_I ranges when M0 is OFF, in SAT and in NON-SAT. What is the value of V_I when M_0 moves from NON SAT to SAT?

4

i) when $V_I > V_{TN}$ transistor will start to conduct current I will be slightly larger than zero, diode will turn on $V_o = \underbrace{V_{DD}}_{5} - \underbrace{I_D R}_{\approx 0} - \underbrace{V_{ON}}_{0,7} = \boxed{4,3V}$

ii) $V_I = 5V$ large V_{GS}, transistor will likely be in NON-SAT

$I_D = 0,1 [2(5-1) \cdot V_o - V_o^2]$ 02 , $V_o = 5 - 2I_D - 0,7 = 4,3 - 2I_D$

$I_D = \frac{4,3 - V_o}{2}$ 02

8

$\frac{4,3 - V_o}{2} = 0,1 [8V_o - V_o^2]$ → $V_o^2 - 13V_o + 21,5 = 0$ → $V_o = 11,05$ X 03, $\boxed{V_o = 1,94}$ $I_D = 1,175mA$

$\frac{43}{2} - \frac{10V_o}{2} = 8V_o - V_o^2$

check $\underbrace{V_{GS} - V_{th}}_{5-1} > \underbrace{V_{DS}}_{1,94}$ so NON SAT is correct 01

iii) at the NON-SAT SAT boundary $V_{DS} = V_o = V_{GS} - V_{th} = V_I - 1$

$\frac{4,3 - V_o}{2} = 0,1 \cdot V_o^2$ 03 $0,2V_o^2 + V_o - \cancel{2,15}\,4,3 = 0$ $\boxed{V_o = 2,76V}$ 03

$V_o = -2,76V$ X

6

06

$\boxed{V_I = V_o + 1 = 3,76V}$ V_{tN}

$I_D = 0,1 (2,76)^2 = 0,76mA$

$V_I < 1$ OFF

$1 < V_I < 3,76$ SAT

$3,76 < V_I < 5V$ NON-SAT. 2

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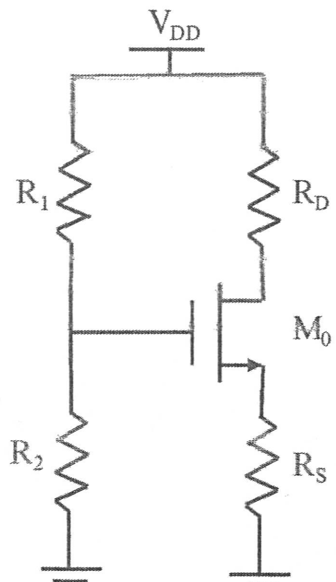
4. (20 Points)



$V_{DD}=10V$
$R_1=R_2=10M\Omega$
$R_S=6k\Omega$
$V_{TN}=1V$
$K_N=0.5mA/V^2$
$\lambda=0$

Find ID and VDS for the circuit shown on the left when

a. $R_D=6k\Omega$
b. $R_D=14k\Omega$

Do not forget to verify the state of the M_0 transistor in each case.

Solution

a) $V_G = \frac{10}{10+10} \times 10 = 5V$. Assume SAT: $I_D = 0.5(V_{GS}-1)^2$

Also $\left.\begin{array}{l} V_G = V_{GS} + I_D R_S \\ 5 = V_{GS} + 6I_D \end{array}\right\} \Rightarrow \frac{5-V_{GS}}{6} = 0.5(V_{GS}-1)^2$

$5 - V_{GS} = 3(V_{GS}^2 - 2V_{GS} + 1)$

$5 - V_{GS} = 3V_{GS}^2 - 6V_{GS} + 3$

$0 = 3V_{GS}^2 - 5V_{GS} - 2 = 0$

$(V_{GS}-2)(3V_{GS}+1) = 0$

$V_{GS} = \begin{cases} 2 > 1 ✓ \\ -\frac{1}{3} > 1 ✗ \end{cases}$ check (1p)

only this (2p)

$V_{GS} = 2V.$

$I_D = \frac{5-2}{6} = 0.5mA.$

$V_{DS} = 10 - 0.5(6+6)$

$V_{DS} = 4V > 2-1$ ✓ check (1p)

$\therefore$ $\boxed{I_D = 0.5mA \quad V_{DS} = 4V}$ (8p)

b) Assume SAT again. All are the same until $V_{DS} = 10 - 0.5(6+14)$
$= 0 > 2-1$ ✗

$\therefore$ TR must be NONSAT.

$I_D = 0.5[2(V_{GS}-1)V_{DS} - V_{DS}^2]$ $\quad V_{GS} = 5 - 6I_D$

$V_{DS} = 10 - (6+14)I_D = 10 - 20I_D$

$2I_D = 2(4-6I_D)(10-20I_D) - (10-20I_D)^2$

$= 2(40 - 80I_D - 60I_D + 120I_D^2) - (100 - 400I_D + 400I_D^2)$

4

$= 80 - 280I_D + 240I_D^2 - 100 + 400I_D - 400I_D^2$

$= -20 + 120I_D - 160I_D^2$

$\Rightarrow 160I_D^2 - 118I_D + 20 = 0 \Rightarrow I_D = \begin{cases} 0.4735mA \Rightarrow V_{GS} = 2.16V > 1 \\ 0.264mA \Rightarrow V_{GS} = 3.416V > 1 \end{cases}$ check (1p)

$I_D \begin{cases} 0.4735 \Rightarrow V_{DS} = 0.5296 < 2.16-1 ✓ \\ 0.264 \Rightarrow V_{DS} = 4.7204 < 3.416-1 ✗ \end{cases}$ check (1p)

only this (2p)

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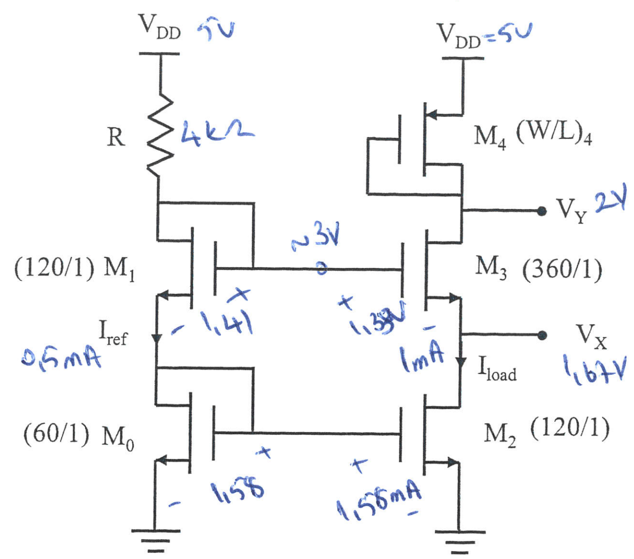
$\therefore$ $\boxed{\begin{array}{l} I_D = 0.4735 mA \\ V_{DS} = 0.5296 V. \end{array}}$ (8p)

5. (20 Points)



V_{DD}=5V
R=4kΩ
V_{TN}=1V for nMOS
V_{TP}=-1V for pMOS
K_P\`=$K_N$\`=50μA/V^2 for all
K_N=(W/L) K_N\`/2
λ=0

M_1 and M_0 forms a cascode current mirror and generates the reference current that is used to bias M_2, M_3, and M_4. Calculate the (W/L) ratio of M_4 to keep M_3 in saturation with minimum V_{DS}. Specify I_{ref}, I_{load}, V_X and V_Y in your solution. Verify the states of all transistors.

$M_1 - M_0$ in SAT by default ($V_{GS} = V_{DS}$)

$V_{GS1} + V_{GS0} = 5 - 4 I_{ref}$. --* (02)

$I_0 = I_1 = I_{ref}$.

$\frac{k_n'}{2} \cdot \left(\frac{W}{L}\right)_1 \cdot (V_{GS1}-1)^2 = \frac{k_n'}{2} \left(\frac{W}{L}\right)_0 (V_{GS0}-1)^2$ (03)

$2 \cdot (V_{GS1}-1)^2 = (V_{GS0}-1)^2$

$V_{GS0} = \sqrt{2} V_{GS1} - \sqrt{2} + 1$

use *

$V_{GS1} + \sqrt{2} V_{GS1} - \sqrt{2} + 1 = 5 - 4 \cdot \frac{0.05}{2} \cdot \frac{120}{1} \cdot (V_{GS1}-1)^2$

$= 5 - 12 (V_{GS1}-1)^2$

$V_{GS1}(1+\sqrt{2}) - \sqrt{2} + 1 = 5 - 12 (V_{GS1}^2 - 2V_{GS1} + 1)$

$-12 V_{GS1}^2 + 24 V_{GS1} - 12$.

$12 V_{GS1}^2 - V_{GS1}(-23 + \sqrt{2}) + 8 - \sqrt{2} = 0$

$\boxed{V_{GS1} = 1.41}$ (03)

$V_{GS1} = 0.39$ X $< V_{TN}$

$V_{GS0} = \sqrt{2} V_{GS1} - \sqrt{2} + 1$

$V_{GS0} = 1.58V$

$I_{ref} = \frac{0.05}{2} \cdot \left(\frac{120}{1}\right) \cdot (1.41-1)^2$ (02)

$\boxed{I_{ref} = 0.5 \text{ mA}}$

$\boxed{I_{load} = \frac{(W/L)_2}{(W/L)_0} \cdot I_{ref} = 1mA}$ (02)

M2 SAT needs to be checked

Assume M_3 is in SAT

$1 = \frac{0.05}{2} \left(\frac{360}{1}\right) \cdot (V_{GS3}-1)^2$

$V_{GS3} = 1.33V$ (03)

$\boxed{V_X = 3 - 1.33 = 1.67V}$

M_2 is in SAT. $1.58 - 1 < 1.67V$

for M_3 to be in SAT with min V_{DS}

$V_{DS3} = V_{GS3} - V_{tn} = 0.33V$ (02)

$V_Y \cancel{=} V_X = 0.33V \Rightarrow \boxed{V_Y = 2V}$

M_4 is in SAT by default $V_{SD} = V_{SG} = 2V$

for M_4

$1mA = \frac{0.05}{2} \cdot \left(\frac{W}{L}\right)_4 (\underset{5-2}{3} - 1)^2$.

(03)

$\boxed{\left(\frac{W}{L}\right)_4 = 10}$

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