Name: ______________________ Section: _______

Signature: ________________ EEE 313 Fall 2010

Bilkent University
Department of Electrical and Electronics Engineering
EEE 313 Electronic Circuit Design
Midterm 1
23 October 2010, 10:00
(4 questions, 120 minutes)

- This is a **closed book**, closed notes exam. No cheat sheet allowed.
- All cell-phones should be completely **turned off**.
- Use a calculator for numerical computations. Carry at least **4 significant digits** during calculations. Your final answer should be at least **3 significant digits**.
- Be sure to write the **units** of all numerical results.
- **Show** all work clearly.
- Please put your **final answer** for each part inside a box for easy identification. Do not give multiple answers, they will not be graded.
- Do not remove the **staple** from the exam sheets or separate pages of the exam. All extra pages must be stamped to your exam.
- You may leave the exam room when you are done. However, please do not leave during the **last five minutes** of the exam.
- At the end of the exam, please stay seated unitl **all** exam papers are collected.

FET equations:

n-channel MOSFET

$i_D = K_n(v_{GS} - V_{Tn})^2$ SAT

$i_D = K_n\left[2(v_{GS} - V_{Tn})v_{DS} - v_{DS}^2\right]$ NON-SAT

p-channel MOSFET

$i_D = K_p(v_{SG} + V_{Tp})^2$ SAT

$i_D = K_p\left[2(v_{SG} + V_{Tp})v_{SD} - v_{SD}^2\right]$ NON-SAT

n-channel JFET

$i_D = \frac{I_{DSS}}{V_P^2}(v_{GS} - V_P)^2$ SAT

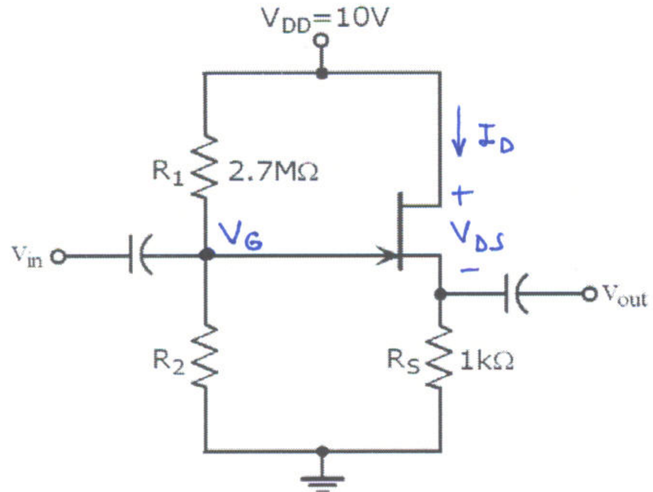
$i_D = \frac{I_{DSS}}{V_P^2}\left[2(v_{GS} - V_P)v_{DS} - v_{DS}^2\right]$ NON-SAT

Please do not write below this line

1. 30 pts.	
2. 15 pts.	
3. 25 pts.	
4. 30 pts.	
Total 100 pts.	

1. (30 points) Given I_{DSS} = 15mA and V_P = -5V. Assume that the capacitor values are very large. Design the following FET amplifier circuit.

- **a.** Find the value of R_2 such that the transistor operates at the edge of the SAT and NON-SAT regions.
- **b.** Find the value of R_2 such that the undistorted symmetric output voltage swing is as large as possible. And determine the value of the undistorted symmetric output voltage swing ($V_{peak\text{-}to\text{-}peak}$).



SOLUTION:

(a) At the edge of the SAT and NON-SAT regions:

$V_{DST} = V_{GST} - V_P$ +3

+2 $V_{DST} = V_{DD} - I_{DT} R_S$ (KVL)

$V_{DST} = V_{DD} - \frac{I_{DSS} R_S}{V_P^2} (V_{GST} - V_P)^2$

$V_{DST} = V_{DD} - \frac{I_{DSS} R_S}{V_P^2} V_{DST}^2$

$0.6 V_{DST}^2 + V_{DST} - 10 = 0$

+5 $\boxed{V_{DST} = \frac{10}{3} V}$ must be positive

Then $V_{GST} = V_{DST} + V_P = \frac{10}{3} - 5$

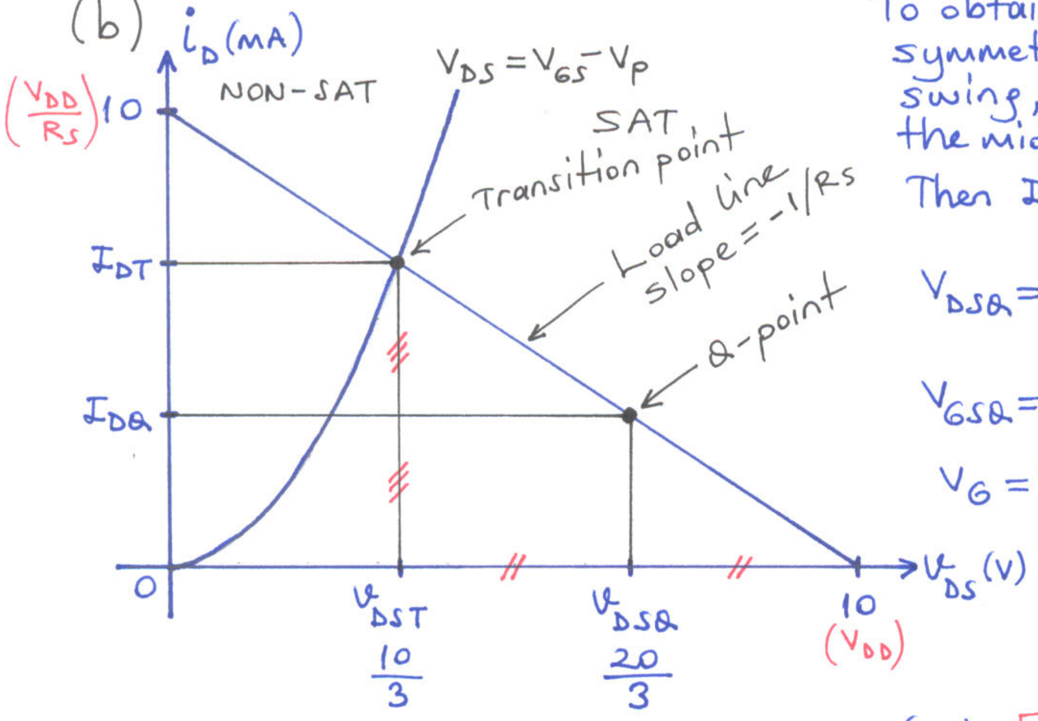
$\boxed{V_{GST} = -\frac{5}{3} V}$

$I_{DT} = \frac{V_{DD} - V_{DST}}{R_S} = \frac{10 - 10/3}{1k\Omega} \Rightarrow \boxed{I_{DT} = \frac{20}{3} mA}$

$V_G = V_{GST} + I_{DT} R_S = -\frac{5}{3} + \left(\frac{20}{3} mA\right)(1k\Omega) \Rightarrow \boxed{V_G = 5V}$

Therefore, $R_1 = R_2$ and $\boxed{R_2 = 2.7M\Omega}$ +5

(b)



To obtain max. undistorted symmetric output voltage swing, Q-point must be in the middle of SAT region.

Then $I_{DQ} = \frac{I_{DT}}{2} = \boxed{\frac{10}{3} mA}$

$V_{DSQ} = V_{DD} - I_{DQ} R_S = \boxed{\frac{20}{3} V}$ +4

$V_{GSQ} = V_P\left(1 - \sqrt{\frac{I_{DQ}}{I_{DSS}}}\right) = \boxed{-2.643V}$

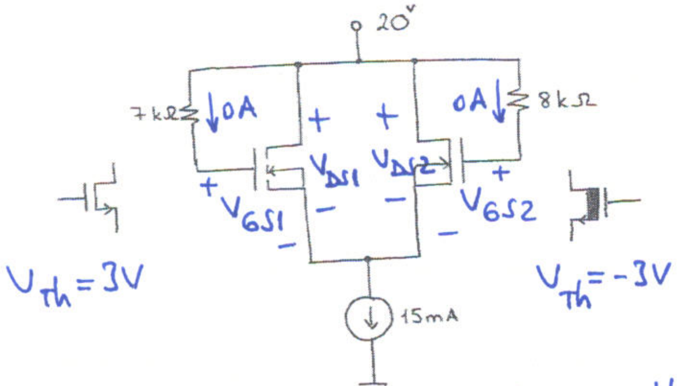
$V_G = V_{GSQ} + I_{DQ} R_S = 0.6903V$

$V_G = \frac{R_2}{R_1 + R_2} V_{DD}$

$\boxed{R_2 = 200.2k\Omega}$ +6

+5 $V_{PP} = 2\left(\frac{10}{3}\right) = \boxed{\frac{20}{3} V}$ maximum.

2. (15 points) In the circuit shown below, determine the states of the transistors and the corresponding bias (I_{DS} and V_{DS}). Justify your answer clearly. K_n=1mA/V^2 and $|V_{Th}|$=3V.
Hint: The absolute value of the threshold values of the transistors are given, be careful about the sign.



SOLUTION:

Since gate current is zero

$V_{GS1} = V_{GS2} = V_{DS1} = V_{DS2}$

For enhancement-mode MOSFET

$V_{GS1} = V_{DS1} \Rightarrow V_{DS1} > V_{GS1} - V_{Th}$

Assume that It is in the SAT region.

For depletion-mode MOSFET

$V_{DS2} = V_{GS2} \Rightarrow V_{DS2} < V_{GS2} - V_{Th} = V_{GS} + 3V$

Assume that it is in the NON-SAT region.

Then $\quad I_{D1} + I_{D2} = 15mA$

$$K_n(V_{GS1}-3)^2 + K_n\left[2(V_{GS2}+3)V_{DS2} - V_{DS2}^2\right] = 15$$

$$(1)(V_{GS}-3)^2 + (1)\left[2(V_{GS}+3)V_{GS} - V_{GS}^2\right] = 15$$

$$V_{GS}^2 - 6V_{GS} + 9 + \left[2V_{GS}^2 + 6V_{GS} - V_{GS}^2\right] = 15$$

$$2V_{GS}^2 = 6 \Rightarrow V_{GS} = \sqrt{3} = 1.732V$$

For enhancement-mode transistor

$V_{GS} < V_{Th} = 3V$. Therefore it must be CUTOFF ($I_{D1} = 0A$)

Then $I_{D2} = 15mA$

$$K_n\left[2(V_{GS2}+3)V_{DS2} - V_{DS}^2\right] = 15$$

$$(1)\left[2(V_{GS}+3)V_{GS} - V_{GS}^2\right] = 15$$

$$2V_{GS}^2 + 6V_{GS} - V_{GS}^2 = 15 \Rightarrow V_{GS}^2 + 6V_{GS} - 15 = 0$$

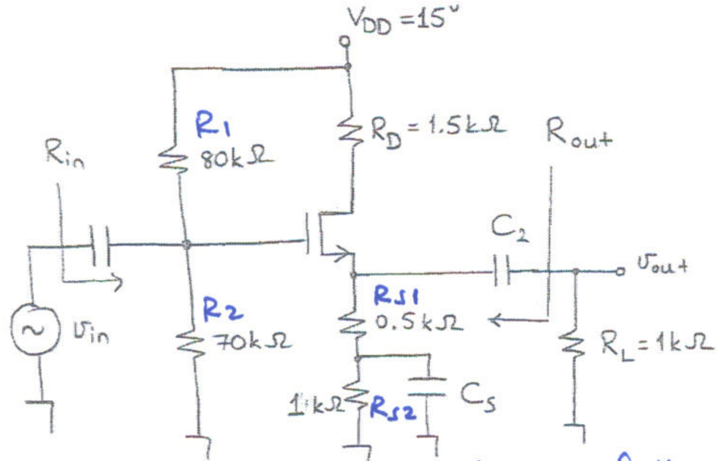
$$\Rightarrow V_{GS} = 1.899V \text{ and } I_{D2} = 15mA$$

Finally

$\boxed{I_{D1} = 0,\ V_{DS1} = 1.899V}$ and $\boxed{I_{D2} = 15mA,\ V_{DS2} = 1.899V}$

3. (25 points) Consider the single stage MOSFET amplifier shown in the figure. $V_{Th} = 2V$ K_n=0.5mA/V^2. Neglect r_o. Assume the capacitors are very large. Also assume that I_{DQ}=2mA. Determine

a. (12 points) The voltage gain, v_o/v_{in}
b. (5 points) The input impedance, R_{in}
c. (8 points) The output impedance R_{out}



SOLUTION:

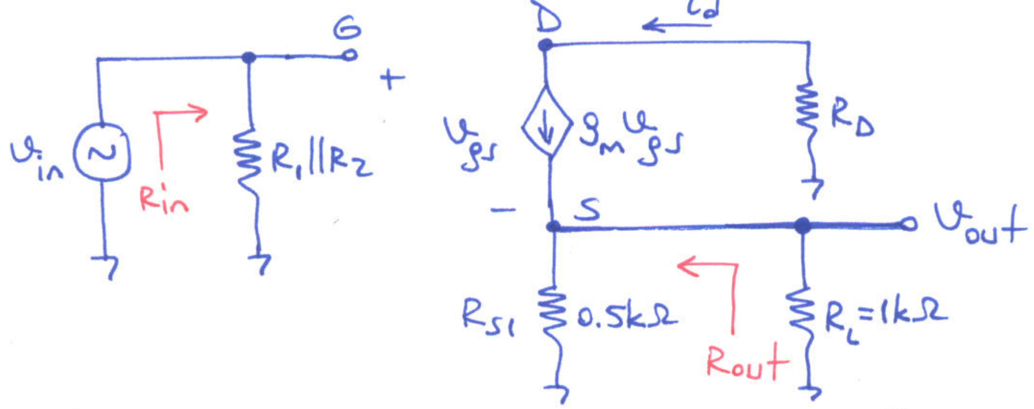
Given that $I_{DQ} = 2mA$

$V_{GSQ} = \sqrt{\frac{I_{DQ}}{K_n}} + V_{TN} = 4V$

$V_{DSQ} = V_{DD} - I_{DQ}(3k\Omega) = 9V$

$g_m = 2\sqrt{K_n I_{DQ}} = 2mA/V$

The AC equivalent circuit is as follows.



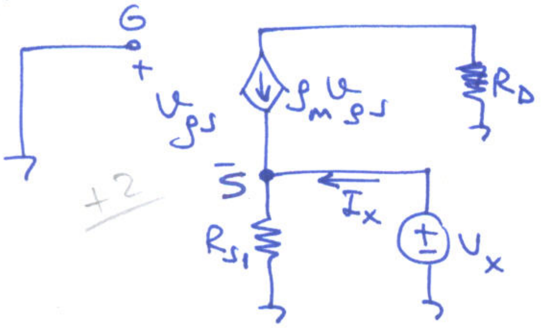
(a) $v_{in} = v_{gs} + v_{out} \Rightarrow v_{gs} = v_{in} - v_{out}$ +3

+3
$v_{out} = g_m v_{gs}(R_{s1}||R_L) = g_m(v_{in} - v_{out})(R_{s1}||R_L)$

+4
$A_v = \frac{v_{out}}{v_{in}} = \frac{g_m(R_{s1}||R_L)}{1 + g_m(R_{s1}||R_L)} = \boxed{0.4}$ +2

(b) $R_{in} = R_1||R_2 = (70k||80k) = \boxed{37.333k\Omega}$

(c) To find Rout, set $v_{in}=0$ and apply a test voltage at the output.



+2

$v_{gs} = -V_x$

Apply KCL at source node.

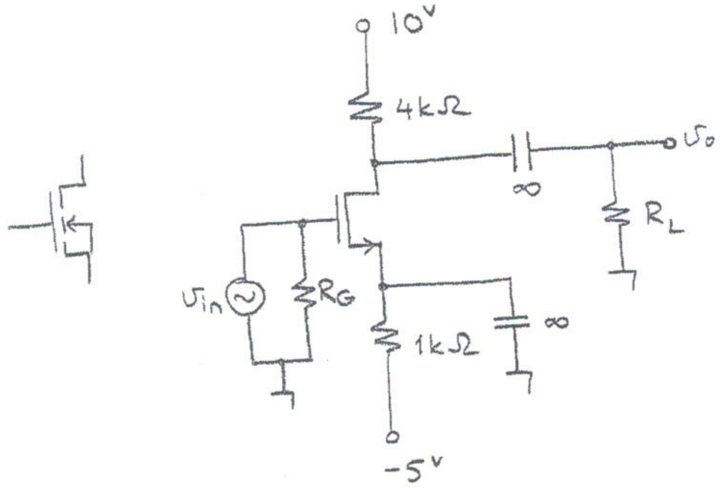
$I_x + g_m v_{gs} = \frac{V_x}{R_{s1}}$ +2

$I_x - g_m V_x = \frac{V_x}{R_{s1}}$

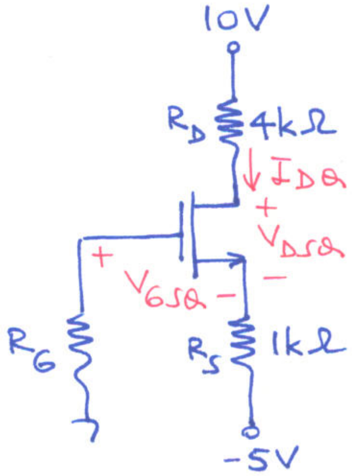
+4

$R_{out} = \frac{V_x}{I_x} = \frac{1}{1/R_{s1} + g_m} = \frac{1}{g_m}||R_{s1} = \boxed{250\Omega}$

4. (30 points) For the amplifier circuit shown below, determine the value of the load resistance, R_L, in order to obtain an undistorted output voltage swing of 3V peak-to-peak. V_{Th}=1V, K_n=0.25mA/V^2. v_{in} is a purely ac voltage signal with zero volts average. Neglect r_o.



SOLUTION:



DC equivalent circuit

DC Analysis:

Apply KVL around gate-to-source loop.

$V_{GSQ} + I_{DQ}R_S - 5 = 0$ where $I_{DQ} = K_n(V_{GSQ} - V_{Th})^2$

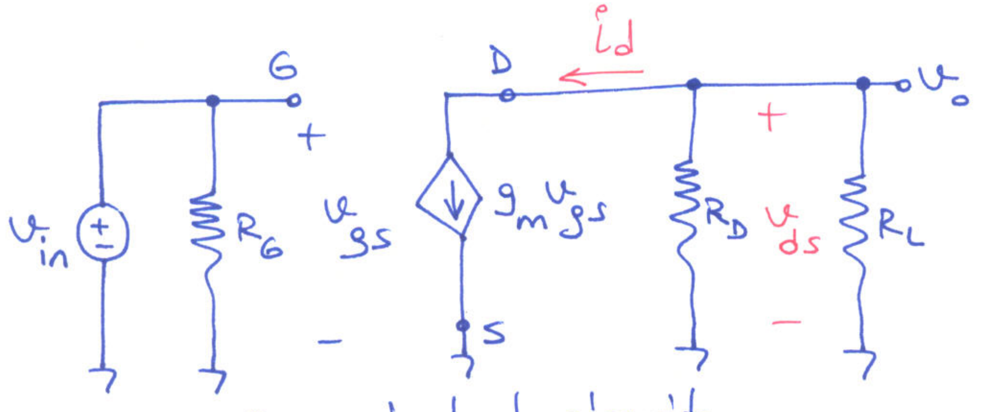
$V_{GSQ} + K_n R_S (V_{GSQ} - V_{Th})^2 - 5 = 0 \Rightarrow 0.25V_{GSQ}^2 + 0.5V_{GSQ} - 4.75 = 0$

Thus, $\boxed{V_{GSQ} = 3.4721\text{V}}$ and $\boxed{I_{DQ} = 1.5279\text{mA}}$

$V_{DSQ} = 15 - I_{DQ}(R_D + R_S) = 15 - (1.5279)(5)$

$\boxed{V_{DSQ} = 7.3605\text{V}}$ $\boxed{V_{DS} = 15 - I_D(R_D + R_S)}$ DC load line eqn.

AC Analysis:



AC equivalent circuit

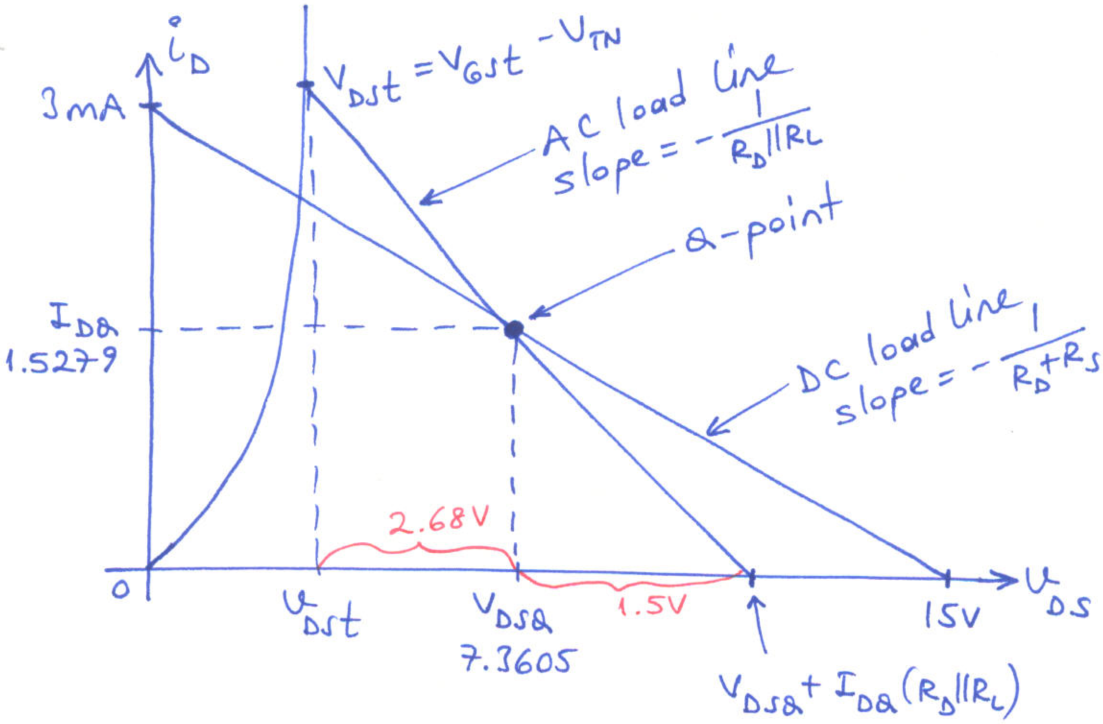
$v_{ds} = -i_d(R_D || R_L)$

$$\boxed{i_d = -\frac{v_{ds}}{R_D || R_L}}$$

AC load line eqn.

Note that AC load line must pass through the DC operating point (Q-point).

$g_m = 2K_n(V_{GSQ} - V_{Th}) = 1.2361\text{mA/V}$



$I_{DQ}(R_D \| R_L) = 1.5V$ is given.

$$R_L = \frac{1.5 R_D}{R_D I_{DQ} - 1.5} = \frac{1.5}{I_{DQ} - \frac{1.5}{R_D}} = \boxed{1.3011 k\Omega}$$

$R_D \| R_L = 981.76\,\Omega$

At the transition point : $V_{DSt} = v_{GSt} - V_{TN}$

where $v_{DS} = V_{DSQ} + v_{ds}$ and $v_{GS} = V_{GSQ} + v_{gs}$

$$v_{DSt} = v_{GSt} - V_{TN}$$

$$V_{DSQ} + v_{ds} = V_{GSQ} + v_{gs} - V_{TN}$$

$$V_{DSQ} - i_d (R_D \| R_L) = V_{GSQ} + v_{gs} - V_{TN} \quad \text{where } i_d = g_m v_{gs}$$

$$V_{DSQ} - g_m v_{gs} (R_D \| R_L) = V_{GSQ} + v_{gs} - V_{TN}$$

$$v_{gs} = \frac{V_{DSQ} - V_{GSQ} + V_{TN}}{1 + g_m (R_D \| R_L)} = 2.2084V \longrightarrow v_{GSt} = 5.6805V$$

$$i_d = g_m v_{gs} = 2.7298 mA \longrightarrow i_{Dt} = 4.2577 mA$$

$$v_{ds} = -i_d (R_D \| R_L) = -2.68V$$

$$v_{DSt} = V_{DSQ} + v_{ds} = \boxed{4.6805V}$$

Then $\boxed{V_{pp} = 3.0V}$