Name: _____

Section: _____

Signature: _____

Bilkent University

Department of Electrical and Electronics Engineering

EEE 313 Electronic Circuit Design

Midterm Examination 2

(7 Questions, 140 minutes)

- This is a **closed book**, closed notes exam.
- All cell-phones should be completely **turned off**.
- Use a calculator for numerical computations. Carry at least **3 significant digits**. Double check your numerical calculations.
- Be sure to write the **units** for all numerical results.
- **Show** all your work clearly and systematically.
- Please put your **final answer** for each part inside a box for easy identification.
- Do not remove the **staple** from the exam sheets or separate the pages of the exam. All extra pages will be stapled to your exam.
- You may leave the exam room when you are done. However, please *do not* leave during the **last five minutes** of the exam.
- At the end of the exam, please stay seated until **all** exam papers are collected.

FET equations:

$$\left.\begin{array}{ll} i_D = K_n(v_{GS} - V_{Th})^2 & \text{SAT} \\ i_D = K_n[2(v_{GS} - V_{Th})v_{DS} - v_{DS}^2] & \text{NON-SAT} \end{array}\right\} \text{n-channel MOSFET}$$

$$\left.\begin{array}{ll} i_D = K_p(v_{SG} + V_{Th})^2 & \text{SAT} \\ i_D = K_p[2(v_{SG} + V_{Th})v_{SD} - v_{SD}^2] & \text{NON-SAT} \end{array}\right\} \text{p-channel MOSFET}$$

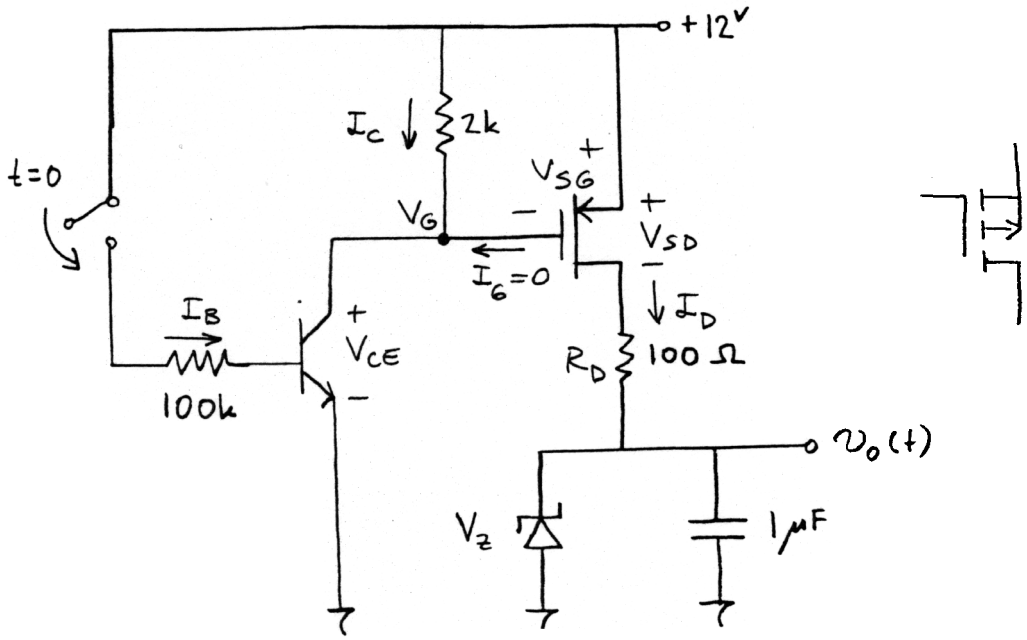
Please do not write below this line.

1.	10 pts.	
2.	10 pts.	
3.	10 pts.	
4.	10 pts.	
5.	10 pts.	
6.	25 pts.	
7.	25 pts.	
Total	100 pts.	

November 29, 2007

1. Consider the circuit shown in the figure. The BJT has $\beta = 120$, $\beta_R = 5$, $V_{BE(ON)} = 0.6$ V, and $V_{CE(SAT)} = 0.2$ V. The p-channel enhancement-mode MOSFET has $\kappa_p = 0.1$ mA/V^2 and $|V_{th}| = 5$ V. For $t \leq 0$, the capacitor voltage is $v_C(t) = 0$. The zener voltage of the zener diode is $V_Z = 4.2$ V. A switch is closed at $t = 0$ as shown in the figure. Determine and plot the output voltage $v_o(t)$ for $t > 0$. Label all critical points on your plot clearly.

(10 pts.)



SOLUTION:

For $t>0$, the switch is closed. Assume that BJT is in saturation.

$I_B = \frac{12-0.6}{100} = 0.114\text{mA}$, $I_c = \frac{12-0.2}{2} = 5.9\text{mA}$, $V_{CE} = 0.2\text{V}$

Since $I_B > 0$ and $I_c < \beta I_B$, our assumption is correct.

Initially, $v_o(0) = 0$

Since $V_G = 0.2\text{V}$, $V_{SG} = 11.8\text{V}$

Assume that MOSFET is biased in the saturation region

$I_D = K_p(V_{SG}+V_{th})^2 = (0.1)(11.8-5)^2$ 4.624 mA

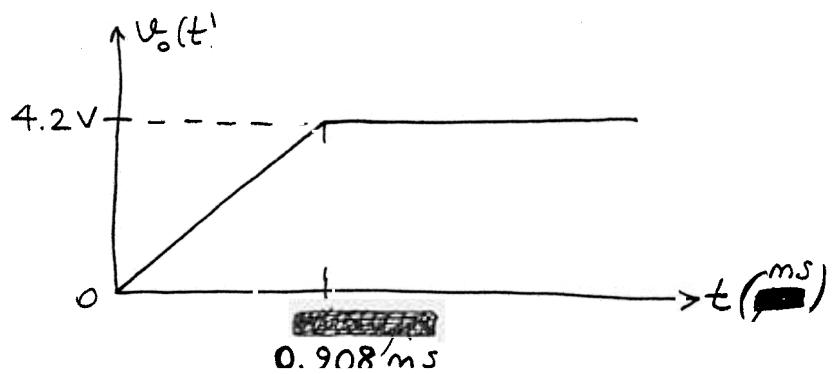
$V_{SD} = 12 - I_D R_D - V_o \Rightarrow V_{SD} = 12-(4.624)(0.1) = 11.54\text{V}$ at $t=0$

$V_{SD} > V_{SG}+V_{th} \Rightarrow$ MOSFET is in saturation

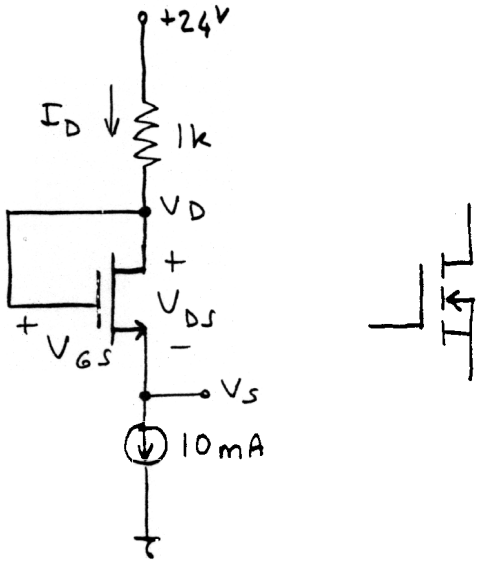
Capacitor is charged with a constant current of 4.624mA until its voltage reaches a value of 4.2V and then the Zener diode will be ON and capacitor voltage will remain constant at 4.2V after this point

$i_C = C\frac{dV_c}{dt} = 4.624\text{mA}$

$\frac{dV_c}{dt} = \frac{4.624\text{mA}}{1\mu\text{F}} = 4624\text{ V/s}$



2. Consider the circuit shown in the figure. The n-channel enhancement-mode MOSFET has $\kappa_n = 0.5$ mA/V^2 and $V_{th} = 2.3$ V. Determine the transistor state, the drain current, and the drain-source voltage. (10 pts.)



SOLUTION:

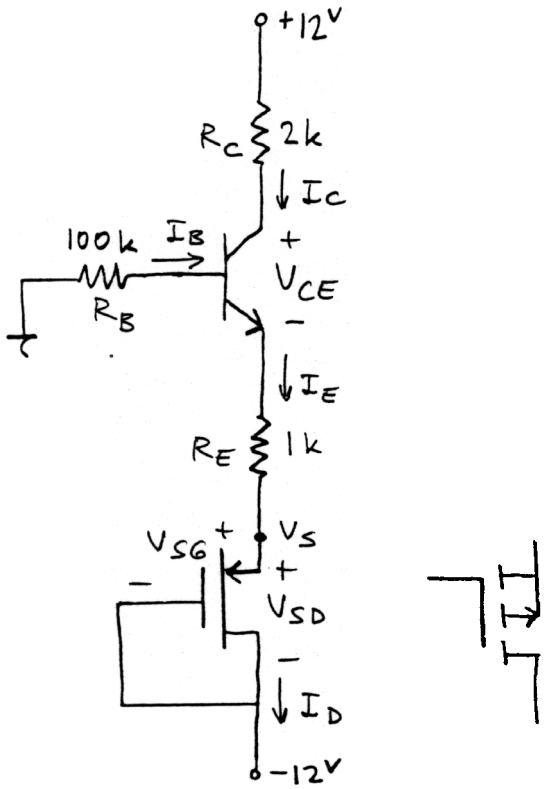
Since $V_{DS} = V_{GS} > V_{GS} - V_{th}$, MOSFET is in the saturation region

$I_D = K_n (V_{GS} - V_{th})^2 = \boxed{10\text{mA}}$

$V_{GS} = \sqrt{\frac{I_D}{K_n}} + V_{th} = \sqrt{\frac{10}{0.5}} + 2.3$

$V_{GS} = 6.772\text{ V} \Rightarrow \boxed{V_{DS} = 6.772\text{V}}$

3. Consider the circuit shown in the figure. The BJT has $\beta = 80$, $\beta_R = 3$, $V_{BE(ON)} = 0.7$ V, and $V_{CE(SAT)} = 0.2$ V. The p-channel enhancement-mode MOSFET has $\kappa_p = 1.0$ mA/V^2 and $|V_{th}| = 2$ V. Determine the states of the transistors, the drain current, the collector current, the source-drain voltage and the collector-emitter voltage. (10 pts.)



SOLUTION:

Since $V_{SD} = V_{SG} > V_{SG} + V_{th}$, MOSFET is in the saturation region.

Let's assume that the BJT is biased in the forward-active region

$I_E = I_D = K_p (V_{SG} + V_{th})^2$ where $V_{th} = -2V$.

Apply KVL around the B-E loop.

$$12 \quad I_B R_B + V_{BE}(on) + I_E R_E + V_{SG} \quad \text{where} \quad I_B = \frac{I_E}{\beta+1} = \frac{I_D}{\beta+1}$$

$$12 = \frac{R_B I_D}{\beta+1} + 0.7 + R_E I_D + V_{SG}$$

$$12 = K_p\left(R_E + \frac{R_B}{\beta+1}\right)(V_{SG} + V_{th})^2 + 0.7 + V_{SG}$$

$$13 = \left(\frac{181}{81}\right)(V_{SG}^2 - 4V_{SG} + 4) + V_{SG} \Rightarrow V_{SG}^2 - 3.5525 V_{SG} - 1.057 = 0$$

$$V_{SG} = \frac{3.5525 \pm \sqrt{16.8483}}{2} \rightarrow V_{SG1} = 3.829\,V \leftarrow \text{Valid solution.}$$

$$\rightarrow V_{SG2} = -0.276\,V$$

$V_{SG} = 3.829V \Rightarrow I_D = (1)(1.829)^2 = \boxed{3.345\,mA}$ and $\boxed{V_{SD} = 3.829V}$

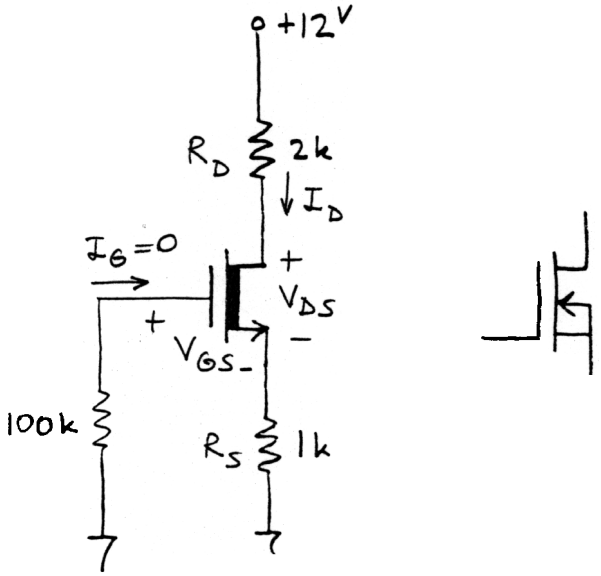
$I_C = \alpha I_D = \left(\frac{80}{81}\right)(3.345) = \boxed{3.304\,mA}$

$V_{CE} = 24 - 2(3.304) - (1)(3.345) - 3.829$

$\boxed{V_{CE} = 10.218V} > V_{CE}(sat)$ Therefore our assumption is correct

$I_B > 0$

4. Consider the circuit shown in the figure. The n-channel depletion-mode MOSFET has $\kappa_n = 2.0$ mA/V^2 and $V_{th} = -1.0$ V. Determine the transistor state, the drain current, the gate-source voltage and the drain-source voltage. (10 pts.)



SOLUTION:

Assume that the MOSFET is in saturation region

Applying KVL around the G-S loop, we have

$V_{GS} + I_D R_S = 0$ where $I_D = K_n (V_{GS} - V_{th})^2$

$V_{GS} + K_n R_S (V_{GS} - (-1))^2 = 0$

$V_{GS} + (2)(V_{GS}+1)^2 = 0 \Rightarrow 2V_{GS}^2 + 5V_{GS} + 2 = 0$

$V_{GS} = \frac{-5 \pm \sqrt{9}}{4}$ → $\boxed{V_{GS} = -0.5\,V}$ ← valid solution

→ $V_{GS} = -2V < V_{th}$ (not valid)

$I_D = (2)(-0.5+1)^2$

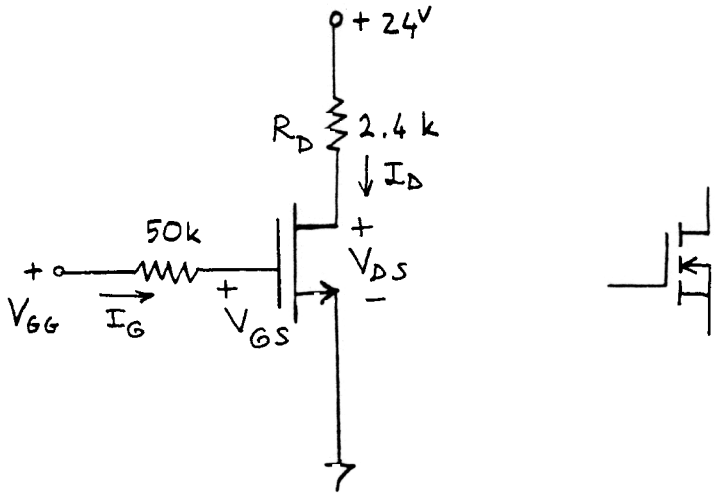
$\boxed{I_D = 0.5\,mA}$

$V_{DS} = 12 - I_D(R_D + R_S) = 12 - (0.5)(3)$

$\boxed{V_{DS} = 10.5\,V}$

Since $V_{DS} > V_{GS} - V_{th}$, our initial assumption is correct.

5. Consider the circuit shown in the figure. The n-channel enhancement-mode MOSFET has $\kappa_n = 0.6$ mA/V^2 and $V_{th} = 2.0$ V. What should be the value of V_{GG} to place the transistor at the transition point between SAT state and NON-SAT state? (10 pts.)



SOLUTION:

At the transition point between the SAT state and NON-SAT state;

$V_{DS} = V_{GS} - V_{th}$ must be satisfied.

Thus

$V_{DS} = 24 - I_D R_D = V_{GS} - V_{th}$

$24 - K_n R_D (V_{GS} - V_{th})^2 = V_{GS} - V_{th} \Rightarrow 1.44(V_{GS} - V_{th})^2 + (V_{GS} - V_{th}) - 24 = 0$

Then $V_{GS} - V_{th} = 3.75$V or $V_{GS} - V_{th} = -4.444$

↑ valid solution

$24 - I_D R_D = 24 \quad K_n R_D V_{DS}^2 \Rightarrow .44 V_{DS}^2 + V_{DS} \quad 24 = 0$

$V_{DS} = 3.75$V

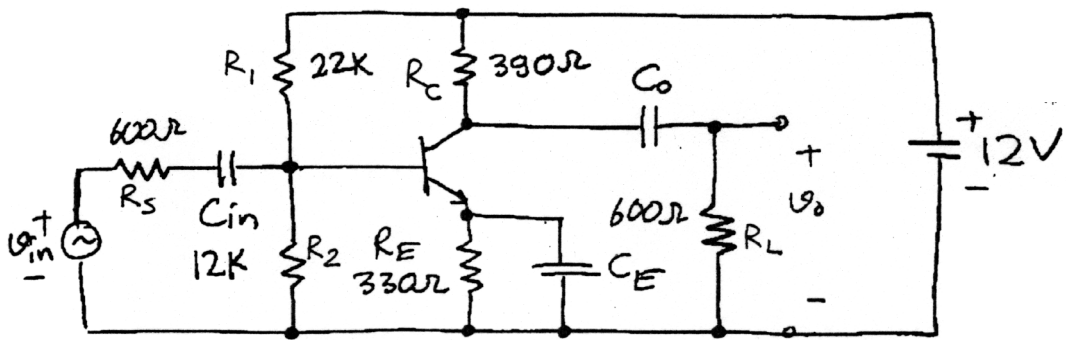
$= V_{GS} - V_{th} \Rightarrow V_{GS} = V_{DS} + V_{th} \quad 3.75 + 2$

$V_{GS} = 5.75$V

Since $I_G = 0$,

$\boxed{V_{GG} = 5.75\text{V}}$ at the transition point

6. (25 points)



For the circuit given above, $\beta = 100$ and $V_{BE(on)} = 0.7$ Volts. Please answer the following:

a) (5 points) Find the state and the D.C. voltages and currents of the transistor.

b) (10. points) Assuming that the capacitors are short for the frequency range of interest, find the voltage gain of the amplifier expressed in dB's and defined as $A_V = v_o/v_{in}$.

c) (10 points) Again assuming that the capacitors are short for the frequency range of interest, find the peak-to-peak undistorted voltage swing at the output.

SOLUTION:

(a) DC analysis (capacitors are open circuit)

$$V_{TH} = \left(\frac{R_2}{R_1+R_2}\right)(12) = 4.235V \;,\; R_{TH} = R_1 \| R_2 = 7.765k\Omega$$

Assume that the transistor is in the forward-active mode.

$$I_{BQ} = \frac{V_{TH} - V_{BE(on)}}{R_{TH} + (\beta+1)R_E} = 86.02\mu A \Rightarrow I_{CQ} = \beta I_{BQ} = \boxed{8.602mA}$$

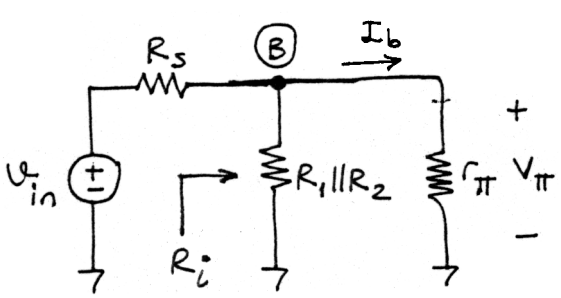
$$V_{CEQ} = 12 - I_{CQ}\left(R_C + \frac{101}{100}R_E\right) = \boxed{5.778V}$$

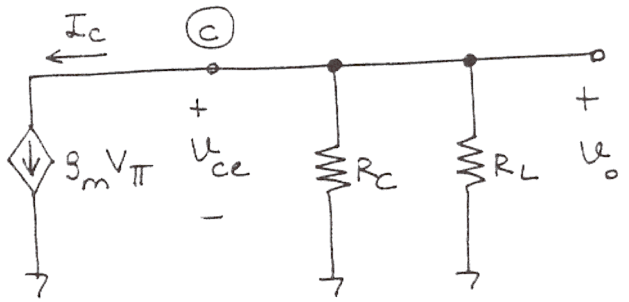
Since $V_{CEQ} > V_{CE}(sat)$, our assumption is correct.

(b) AC analysis (capacitors are short circuit)

$$r_\pi = \frac{V_T}{I_{BQ}} = 302.3\Omega \;,\; g_m = \frac{I_{CQ}}{V_T} = 330.85\,mA/V^2 \qquad r_o \;\; \infty$$

R_E is shorted by C_E





Small-signal equivalent circuit

$= R_1 \| R_2 \| r_\pi = 0.291\,k\Omega$

$g_m V_\pi (R_c \| R_L)$ where $V_\pi = \left(\frac{R_i}{R_i + R_s}\right) V_{in}$

$= \frac{v_o}{v_{in}} \quad - g_m (R_c \| R_L)\left(\quad\right)$

$\boxed{A_V = -25.54}$

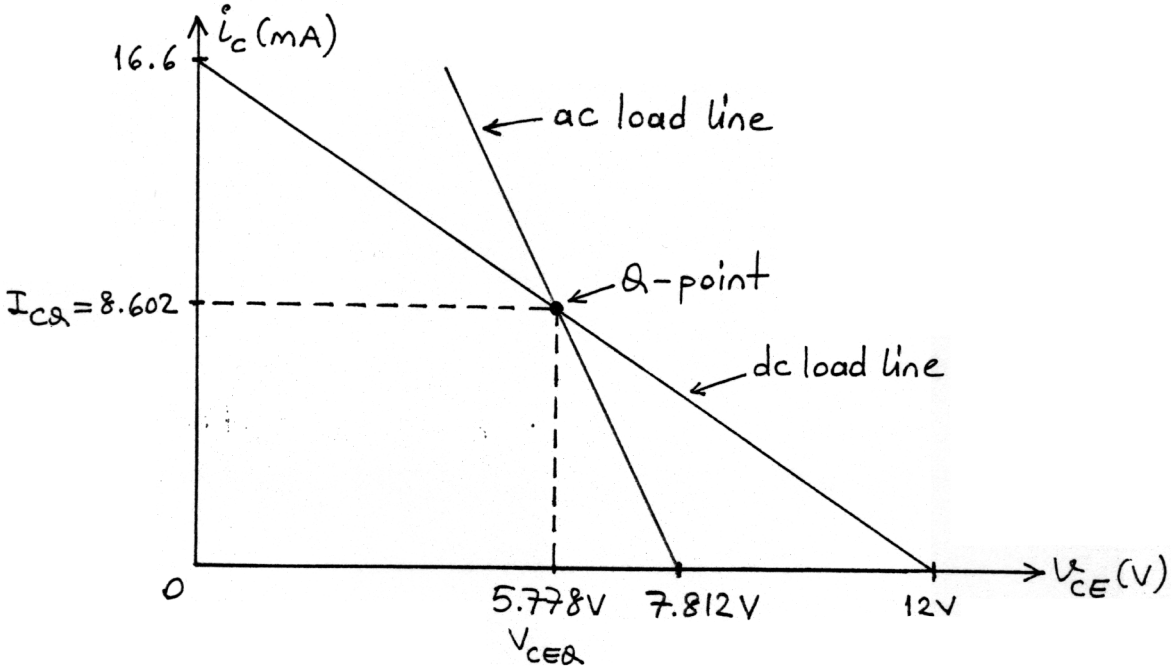
Voltage gain in dB is $20 \log |A_V| = \boxed{28.14\ dB}$

(c) $V_{CE} \quad 12 - I_c\left(R_c + \left(\frac{\beta+1}{\beta}\right) R_E\right)$

$V_{CE} \quad 2 - (0.7233) I_c$: dc load line equation

$v_{ce} \quad -(R_c \| R_L)\, i_c$

$v_{ce} = \quad (0.2364)\, i_c$: ac load line equation



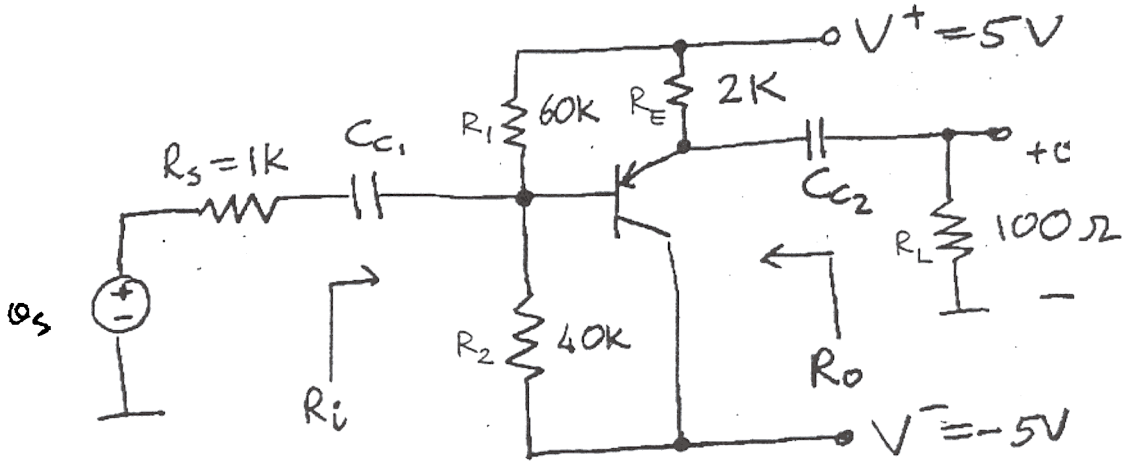
The maximum peak-to-peak undistorted voltage swing at the output

$2(7.812 - 5.778) = \boxed{4.07\ V}$

7. (25 points)

For the following circuit, let $\beta = 120$, $V_A = \infty$ and $V_{EB(on)} = 0.7$ Volts:

a) (5 points) Determine the Q-point values of I_{CQ} and V_{ECQ}.
b) (0 points) Find the small-signal parameters, r_π, g_m and r_o.
c) (10 points) Find the input resistance R_i and output resistance R_o
d) (10 points) Find the small-signal voltage gain, $A_v = v_o/v_s$.



SOLUTION:

(a) DC analysis

$R_{TH} = R_1 \| R_2$ 24kΩ , $V_{TH} = \left(\frac{R_2}{R_1+R_2}\right)(V^+ - V^-)$ V^- -1V

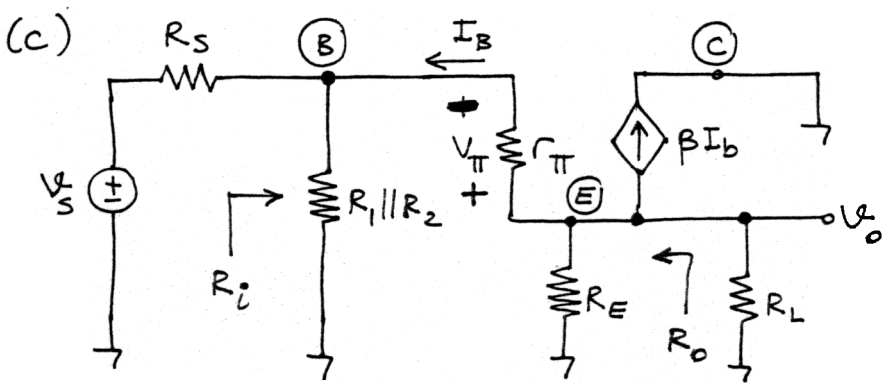
I_{BQ} $\frac{V^+ - V_{TH} - V_{EB(on)}}{R_{TH} + (\beta+1) R_E} = 9.92\,\mu A \Rightarrow I_{CQ} = \beta I_{BQ} =$ **2.391 mA**

$V_{ECQ} = 10 - (2)(2.410) =$ **5.18V**

Since $V_{ECQ} > V_{EC}(sat)$ and $I_{BQ} > 0$, the transistor is biased in forward-active mode.

(b) r_π $\frac{V_T}{I_{BQ}}$ 1.305kΩ , $g_m = \frac{I_{CQ}}{V_T} = 91.96\,mA/V$, $r_o = \frac{V_A}{I_{CQ}} = \infty$

(c)

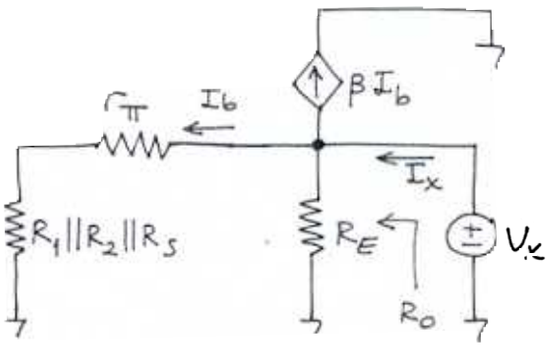


Small-signal equivalent circuit

R $= r_\pi + \beta +)(R_E \| R$ 128 Ω

R $R_s \| R_{ib}$ **8.36kΩ** input resistance

In order to find R_o we set $v_s = 0$



R $\frac{V_x}{I_y}$

$I_x = \frac{V_x}{R_E} + (\beta +)I_L$

where I_b $\frac{V_x}{r + R_1 \| R_s \quad R}$

I $\frac{V_x}{R_E} + \frac{(\beta+1)V_x}{r_\pi + R \| R_s \| R}$

$R = \left(\frac{1}{R_E} + \frac{\beta+1}{+R_1 \| R_s \| R}\right) \quad R_E \| \left(\frac{r_\pi + R_1 \| R_2 \| R_S}{\beta+1}\right)$

$R_o = 18.5\,\Omega$ output resistance

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d v $(\beta \cdot 1) I_b \; R_E \| R_L$ where I_b $\frac{v_i}{R_{ib}}$ and v_o $\left(\frac{R_i^\circ}{R_i + R_S}\right) v$

v $(\beta \; 1)(R_E \| R \;)\left(\frac{1}{R_{ib}}\right)\left(\frac{R_i}{R_i + R_S}\right) v$

A_V $\frac{v_o}{\quad}$ $- \frac{(\beta+1)(R_E \| R_L)}{r + (\beta+1)(R_E \| R_i}\left(\frac{R_i}{R_i + R_S}\right)$

$A_V = 0.802$