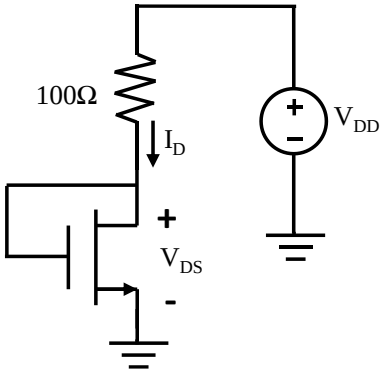
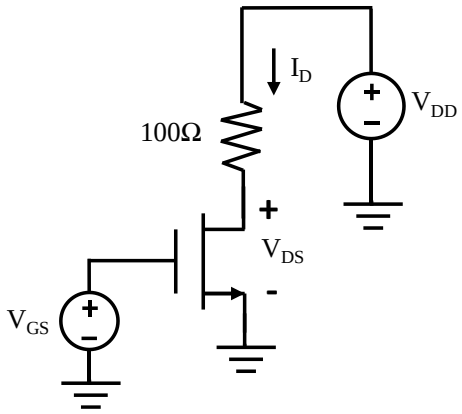
nMOS Common Source Amplifier

You will first characterize an nMOS transistor (2N7000) and then design a single stage voltage amplfier using your characterization results.

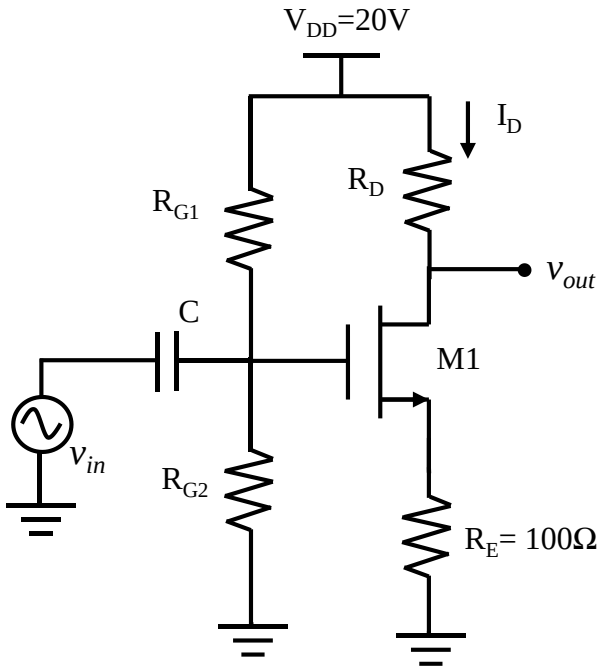
We have limited number of 2N7000s, if the nMOS is damaged during testing you may not be able to get a new one. For that reason please be careful not pass too much current through the transistor during testing. Immediately stop your testing whenever you observe a drain current (I_D) larger than 50mA during testing. Although it will make your characterization one step longer 100Ω current protection resistor has been added to test circuits in Fig1.a&b. Do not skip these resistors and use them during your characterization.



***a.** Test circuit for finding V_{TH}*



***b.** Test circuit to plot I_D-V_{DS} curves*



***c.** Common source amplifier to be designed*

***Figure 1:** Test circuits and the common source amplifier*

The specifications for the circuit in Fig1.c are
$R_{in} > 30k\Omega$
$R_{out} < 2k\Omega$
$10mA < I_D < 15mA$
$|A_V| = |v_{out} / v_{in}| > 9$ when v_{in}=100mV_{pp} sine wave @ 10kHz

Follow the below steps for the lab

1. Set up the circuit in Fig.1.a to find the threshold voltage (V_{TH}) of the transistor, do not skip the 100Ω resistor. Slowly increase V_{DD} while recording I_D till I_D=30mA. Plot I_D vs V_{DS} and determine V_{TH}. You can assume transistor is ON when I_D=1mA. Note that $V_{DS}=V_{DD}-I_D*R$.
2. Setup the circuit in Fig1.b to obtain the I_D-V_{DS} curve of the transistor. For each

sweep fix V_{GS} and slowly change V_{DD} while recording I_D. Generate at least 3 I_D-V_{DS} curves, for $V_{GS}=V_{TH}+0.3V$, 0.4V, and 0.5V. What is the K_N and λ of this transistor? Note that $V_{DS}=V_{DD}-I_D*R$.

3. Design the common source amplifier shown in Fig1.c to meet the given specifications. You should determine the value of the all the unknown resistors and the capacitor. Calculate g_m and r_o based on your findings from part 2. Show v_{in} and and v_{out} on the same scope screen to demonstrate the gain. Increase v_{in} up to the point where you observe distortion on v_{out} and show these plots in your report. What determines the maximum input voltage?
4. Connect a parallel capacitor (same value as C) to R_E and report your gain. Explain the change in your gain.

Answer all the above questions with the required plots in your report. Include all the component values, DC operating point of the transistor, and clearly explain your design procedure. We assume you are familiar with the output impedance of the signal generators in the lab, see lab 2 notes if you don't remember. For each case above (parts 1, 2, and 3), present and explain your results and procedures in your report. Use graphs, screenshots, tables etc.

You should be in the lab and have your circuit ready during the check-out. You are expected to demonstrate a working set-up and be able to explain how the circuit works and what your results are. Your assistant may ask you questions about your lab and also your preliminary work (if any). You are expected to work individually and also demonstrate that you fully understand the purpose and results of the lab. You will also write a report about the lab (If you do not pass your check-out, you will not be eligible for submitting your report).

This will be a two-week lab covering the weeks of October 16 and 23. The deadline to submit your report is Wednesday, November 8th, 23:55.