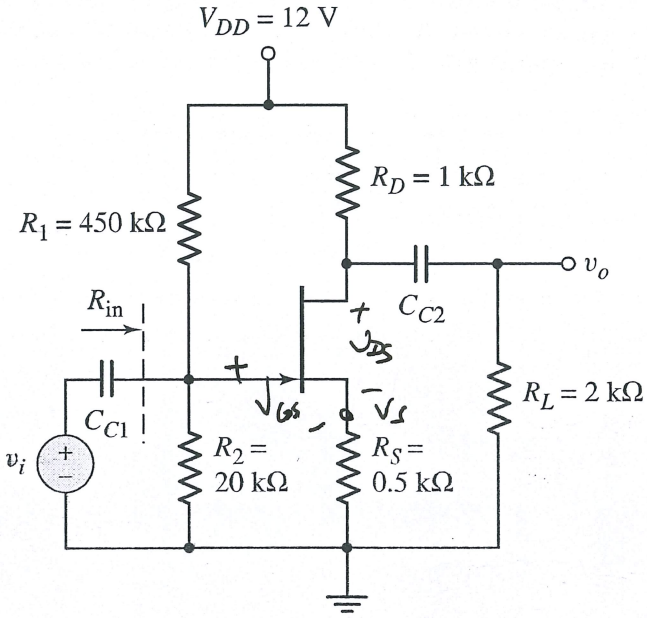
1. Perform DC analysis on the circuit shown in the figure below involving an n-channel JFET: The quiescent value of V_{DS} is desired to be $V_{DSQ} = 5$ V. If $I_{DSS} = 10$ mA, determine I_{DQ}, V_{GSQ}, and V_P. Write your answers in the box below; only the values there will be taken into consideration when grading.

I_{DQ}	V_{GSQ}	V_P
4.67mA	~~0.5V~~ −1.82V	−5.75V

4.67mA −1.82V −5.75V



$V_{DS} = V_{DD} - I_D \cdot (R_S + R_D)$

$5V = 12V - I_D \cdot (0.5 + 1) \Rightarrow I_{DQ} = 4.67mA$

$V_S = I_D \cdot R_S = (4.67)(0.5) = 2.33V$

Voltage divider since no current into gate:

$V_G = \frac{R_2}{R_1 + R_2} \cdot V_{DD} = \frac{20}{450+20} \cdot 12 = 0.511V$

$V_{GSQ} = V_G - V_S$
$= 0.511 - 2.33$
$= -1.82V$

$I_D = I_{DSS} \cdot \left(1 - \frac{V_{GS}}{V_P}\right)^2 \Rightarrow 4.67 = 10 \cdot \left(1 - \frac{(-1.82)}{V_P}\right)^2$

$\Rightarrow V_P = -5.75V$

Grading Key for Problem 1

This problem aims to test skills in DC analysis using basic operational characteristics of JFETs.

Correct application of KVL to the JFET analysis: 5 pts

Correct determination of I_{DQ}: 5 pts

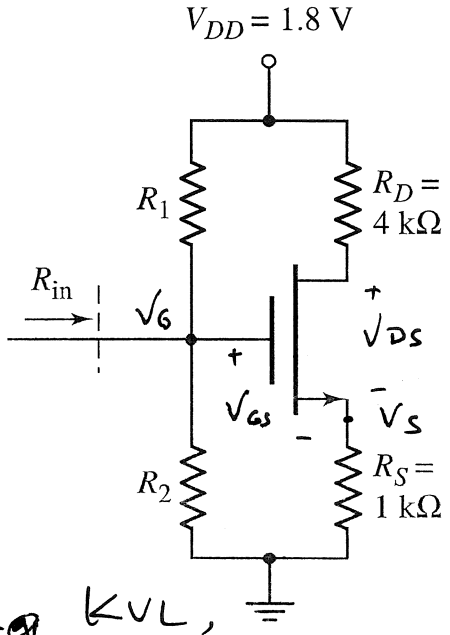
Knowledge that negligible current flows into the gate (and that therefore a voltage divider is formed): 5 pts

Correct determination of the V_{GSQ} result: 4 pts

Application of the correct current expression in saturation mode: 4 pts

Determination of the correct V_P: 2 pts (1 pts only if sign is incorrect).

2. Consider the circuit shown in the figure. The n-channel enhancement-mode transistor's threshold voltage is $V_{TN} = 0.4$ V. The voltage drop across R_S is required to be 0.20 V. Design the transistor K_n such that $V_{DS} = V_{DS}(\text{sat}) + 0.4$ V, and find R_1 and R_2 such that $R_{in} = 200$ kΩ. Write your answers in the box below; only the values there will be taken into consideration when grading.



K_n	R_1	R_2
1.25 mA/V²	360kΩ	450kΩ

$V_S = 0.2V = I_D \cdot R_S = I_D \cdot 1k\Omega$

$I_D = 0.2\,mA$

We know the transistor is in SAT mode,

Given $V_{DS} = V_{DS}(sat) + 0.4V$ & using KVL,

we have: $V_{DS} = V_{DD} - I_D \cdot (R_D + R_S) = 1.8V - 0.2mA(4k\Omega + 1k\Omega)$

$V_{DS} = 0.8V$

Then $V_{DS}(sat) = 0.8V - 0.4V = 0.4V$

(V_{DS} given)

The condition for saturation limit is: $V_{DS}(sat) = V_{GS} - V_{TN} \Rightarrow 0.4 = V_{GS} - 0.4$

$\Rightarrow V_{GS} = 0.8\,V$

In SAT mode, $I_D = K_n \cdot (V_{GS} - V_{TN})^2$

$\Rightarrow 0.2\,mA = K_n \cdot (0.8V - 0.4)^2 \Rightarrow K_n = 1.25\,mA/V^2$

Using KVL, $V_G = V_{GS} + I_D \cdot R_D = 0.8V + (0.2\,mA)\cdot(1k\Omega) = 1.0V$

Since $R_{in} = R_1 \| R_2$, $V_G = 1V = \frac{R_{in}}{R_1} \cdot V_{DD} = \frac{1}{R_1}(200)\cdot(1.8) \Rightarrow R_1 = 360k\Omega$

$R_1 \| R_2 = R_{in} = 200k\Omega$ (specified) $\Rightarrow R_2 = 450k\Omega$

Grading Key for Problem 2

Recognition that the transistor is in saturation mode: 4pts

Correct application of KVL to determined the Q-point values: 4 pts

Correct determination of the numerical values: 7pts

Usage of the voltage divider feature in finding R_1 and R_2: 4 pts

Correct determination of the values of R_1 and R_2: 6pts