20-5-2021

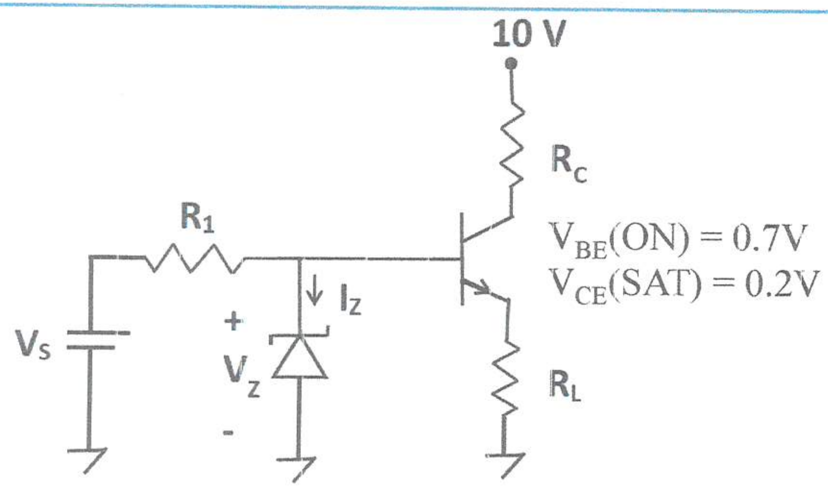
BILKENT UNIVERSITY Department of Electrical and Electronics Engineering

EEE313 Electronic Circuit Design Final Exam

4 questions 150 minutes

PART-1, 2 QUESTIONS 75 MINUTES

- **Instructions:**
- Calculators without extensive memory are allowed
- Clearly explain all your answers in order to receive credit
- Put a box around your final answer
- Cheat sheets are not allowed
- Indicate the units for your final answers
- Write your name and student ID on the bottom of every page
- Mail your pdf solutions to eee313exam@bilkent.edu.tr with your student ID number as subject
- Also upload your pdf solutions to Moodle

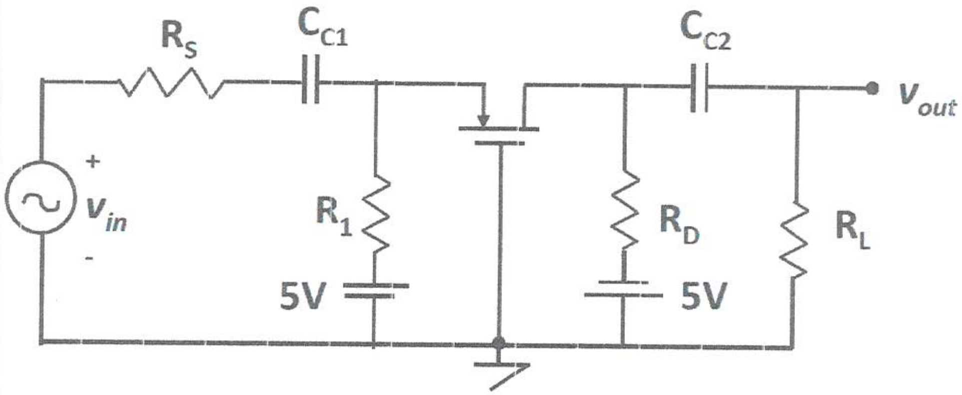


Q1. (20 points) For the buffered regulator shown above, $V_{Z0} = 6V$ and $R_1 = 0.5k\Omega$. The DC voltage source V_S may be between 9V and 12V. The load resistor R_L may be between 50Ω and 100Ω. I_Z must be greater than 0.1mA for the Zener to be in the Zener region, and the maximum allowable power dissipation in the Zener is 66mW.

a) Find the range of acceptable β of the transistor so that the Zener current remains within acceptable limits under all conditions stated above for V_S and R_L (assuming the transistor is Forward Active.).

b) For the β range found above find the maximum value of R_C so that the transistor remains in the Forward Active state.

c) If the load resistor is accidentally shorted ($R_L \rightarrow 0$), how much current goes through R_C? Take R_C as the maximum value found in part b. Assume I_Z is negligible if $V_Z < V_{Z0}$.



Q2. (30 points) The parameters of the transistor in the circuit above are $K_p = 1$ mA/V², $V_{TP} = -1.5$ V, and $\lambda = 0$. The other circuit component values are $R_S = 200\Omega$, $R_1 = 1.2k\Omega$, $R_D = 1.2k\Omega$, $R_L = 50k\Omega$, $C_{C1} = 4.7\mu F$, $C_{C2} = 1\mu F$, $C_{gs} = 10pF$, and $C_{gd} = 4pF$. v_{in} is a small-signal ac source.

a) Determine the quiescent current and voltage values of the transistor. Verify the state of the transistor.

b) Determine the small-signal midband gain $A_{MB} = v_{out}/v_{in}$.

c) Find the -3dB lower cut-off frequency f_L of this amplifier.

d) Find the -3dB upper cut-off frequency f_H of this amplifier.

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PART-2, 2 QUESTIONS 75 MINUTES

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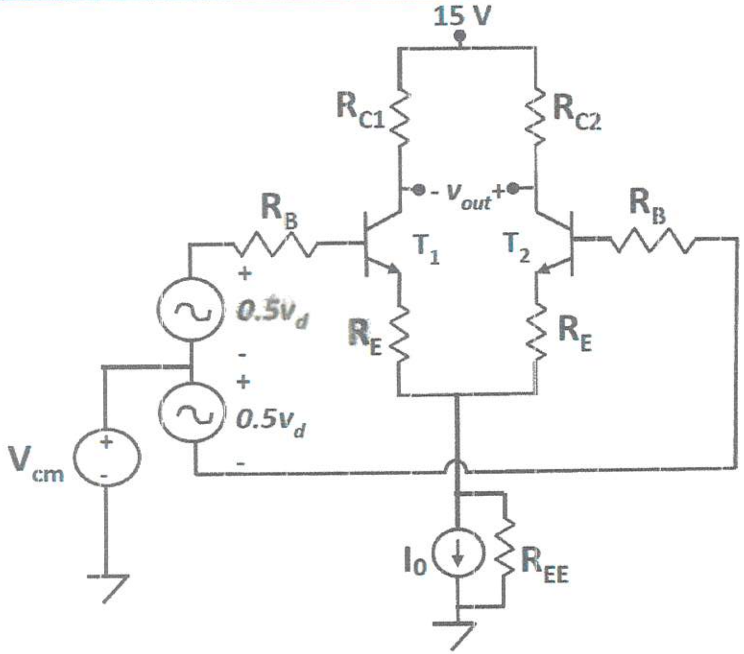


For T1 and T2
$\beta = 100$, $V_A = \infty$,
$V_{BE}(ON) = 0.7V$
$V_{CE}(SAT) = 0.2V$
V_T=0.026V
$R_{C1} = R_{C2} = 10k\Omega$
$R_E = 150\Omega$
$R_B = 5k\Omega$
$R_{EE} = 200k\Omega$
$I_0 = 1mA$.

Q3. (30 points) In the above diff amp $\mathbf{V_{cm} = V_Q} + \boldsymbol{v_{cm}}$ where $\mathbf{V_Q = 5V}$, v_{cm} is the small-signal common-mode input voltage, and v_d is the small-signal differential input voltage.

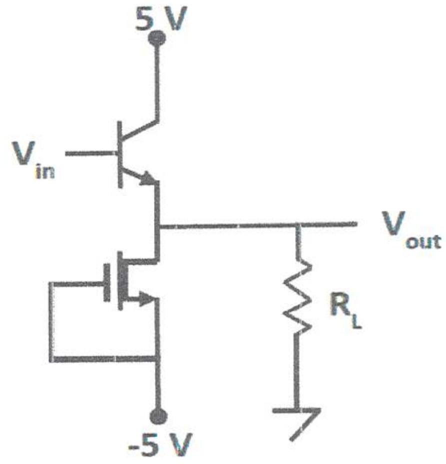
a) For when the small input signals are zero (i.e. $v_{cm} = v_d = 0$), find the collector currents, small signal transistor parameters, and verify the states of the transistors. Note: Do not ignore the base currents and the current on R_{EE}.

b) Derive and find the small signal differential gain v_{out}/v_d.

c) Derive and find the worst-case common mode small-signal gain v_{out}/v_{cm} if R_{C1} and R_{C2} are accurate to ±1%.

d) Derive and find the small-signal common mode input resistance R_{icm}

e) Derive and find the small-signal differential input resistance R_{id}.



Q4. (20 points) In the above voltage buffer, the **npn BJT** has the parameters $V_{BE}(ON) = 0.7V$, $V_{CE}(SAT) = 0.2V$, $\beta = 100$, $V_A = \infty$, and the **depletion mode nMOS** transistor has the parameters $K_n = 0.2mA/V^2$, $\lambda = 0$, and $V_{TN} = -1.8V$. Take V_T=0.026V.

a) For $R_L = \infty$, find the range of V_{in} so that both transistors are active i.e. F.A. for the BJT and SAT for the nMOS.

b) If V_{out} is a sinusoidal with peak voltage of 2V, find the minimum value of R_L for which the condition that both transistors are active is not violated.

c) For $R_L = 500\Omega$ derive and find the small signal gain v_{out}/v_{in} of this buffer for $V_{in} = 0.7V + v_{in}$ where v_{in} and v_{out} are a small signal.