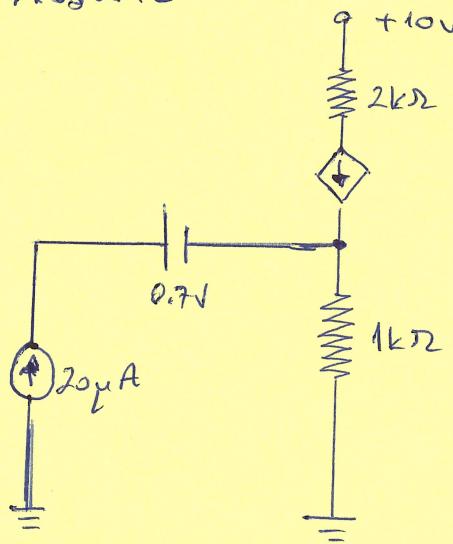


1.

Assume ACT mode & draw the equivalent circuit:



The current source determines the base current; $I_B = 20 \mu A$ 3 pts

Then, $I_C = \beta \cdot I_B = 100 \cdot 20 \mu A = 2 mA$ 2 pts

Also, $I_E = I_C + I_B = 2.2 mA$ 2 pts

Now, we can use KVL on the E-C side to determine V_{CE} :
2 pts

$$10V = 2k \cdot 2mA - V_{CE} - 1k \cdot 2.02mA \Rightarrow V_{CE} = 3.98V \approx 4V$$

3 pts

Now, verify the ACT mode:

$$V_{CE} \approx 4V > V_{CE(SAT)} = 0.2V \rightarrow \text{ACT mode is verified.}$$

2- This problem can become confusing due to the very large number of possible states ($3 \times 3 \times 2 \times 2 \times 2 = 72$). However, the great majority of them are easily seen to be impossible. So, let's approach carefully.

The first (and very simple) possibility is that everything is off. But this is clearly not possible; see B-E port of T1.

If D1 is ON and current flows into the base of T1, then using KVL:

$$3V = 160k\Omega \times I_{B1} + \underbrace{0.7}_{D1} + \underbrace{0.7}_{V_{BE,1(\text{on})}} \Rightarrow I_{B1} = \frac{1.6V}{160k\Omega}$$

Therefore $I_{B1} = 10\mu A$

{ mostly correct approach, but getting stuck with wrong assumptions ~ 5/10. Small numerical mistakes, but otherwise correct 8/10, grade scales around this guideline }

Following E terminal of T1 to ground, C terminal to T2, all the way to 10V, it is clear that T1 cannot be REACT and must be SAT or ACT.

Let's assume T1 is ACT:

$$\text{Then, } I_{C1} = \beta \cdot I_{B1} = 100 \times 10\mu A = 1mA$$

This is also base current of T2; $I_{B2} = I_{C1}$

Now, we need to guess the state of T2. It cannot be ACT mode, since that would imply $I_{E2} = \beta \cdot I_{B2} = 100mA$, not possible due to the 1kΩ resistor.

Let's assume SAT mode for T2:

$$V_{EC2} = V_{CE(SAT)} = 0.2$$

Now KVL from 10V to ground: $10V = 1k \cdot I_{E2} + \underbrace{V_{EB(SAT)}}_{0.2V} + \underbrace{V_Z}_{4.8V}$

$$\Rightarrow I_{E2} = 5mA$$

$$I_{C2} = 4mA$$

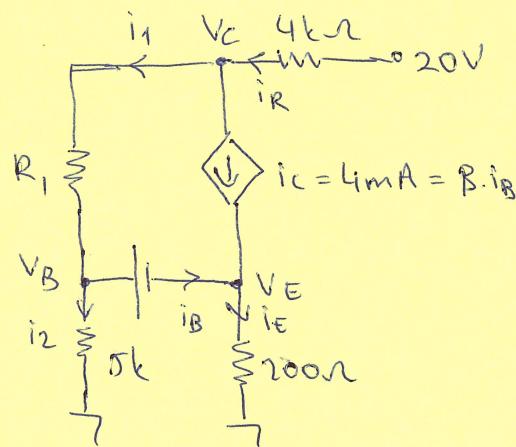
$$\text{Since } I_{E2} = I_{C2} + I_{B2} \Rightarrow 5mA = 4mA + 1mA \Rightarrow$$

Finally, let's verify using KVL from 10V to base of T2 to ground of T1:

$$10V = \underbrace{I_{E2} \times 1k}_{5V} + \underbrace{V_{EB,2(\text{on})}}_{0.7V} + \underbrace{V_{D2}}_{0.7V} + V_{CE,1} \Rightarrow V_{CE,1} = 3.6V > 0.2 = V_{CE(SAT)}$$

verified

3(a) Assume the transistor is in ACT state;



$$i_B = \frac{i_C}{\beta} = \frac{4\text{mA}}{80} = 50\mu\text{A}$$

$$i_E = (\beta + 1) \cdot i_B = 4.05 \text{ mA} \quad (2 \text{ pts})$$

$$V_E = 4.05 \text{ mA} \cdot 200\Omega = 810 \text{ mV}$$

$$V_B = 0.7V + 0.810V = 1.510V$$

$$i_2 = \frac{1.510V}{5k} = 0.302 \text{ mA}$$

$$i_1 = i_B + i_2 = 0.05 + 0.302 = 0.352 \text{ mA} \quad (2 \text{ pts})$$

$$i_R = i_C + i_1 = 4 + 0.352 = 4.352 \text{ mA} \quad (3 \text{ pts})$$

$$\Rightarrow V_C = 20V - 4k \cdot 4.352 \text{ mA} = 2.592 \text{ V} \quad (3 \text{ pts})$$

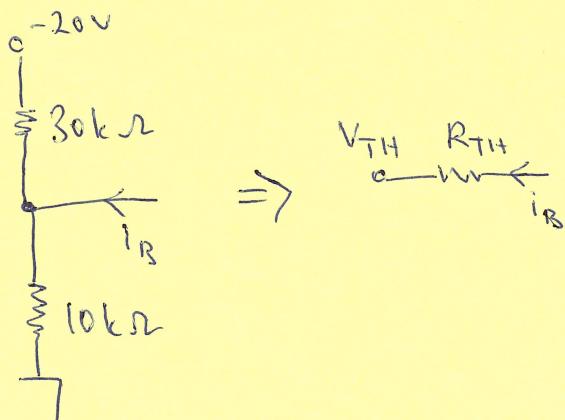
$$[V_{CE} = V_C - V_E = 2.592 - 0.81V = 1.791V] > V_{CE(\text{SAT})} \Rightarrow \text{Our assumption is correct.}$$

$$[R_1 = \frac{V_C - V_B}{i_1} = \frac{2.592 - 1.510}{0.352 \text{ mA}} \text{ V} = 3.074 \text{ k}\Omega]$$

Thus, transistor is in active state.

3 (b) We can use Thevenin equivalent circuit to simplify the question.

In that case;

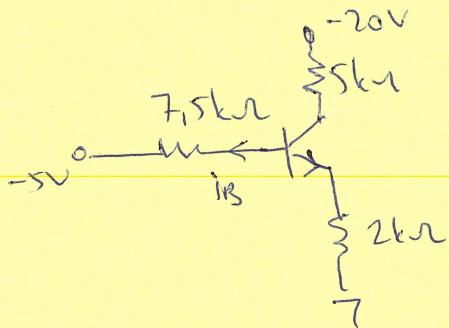


$$\text{where } V_{TH} = \frac{(-20V) \cdot 10k\Omega}{40k\Omega}$$

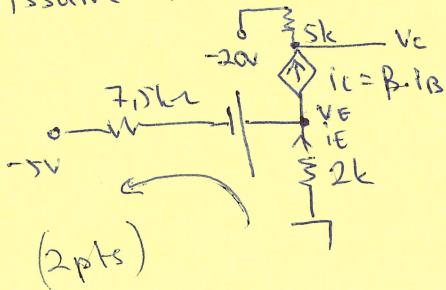
$$= -5V \text{ and}$$

$$R_{TH} = \frac{10k\Omega \cdot 30k\Omega}{40k\Omega} = 7.5k\Omega$$

Total circuit looks like this;



Assume the transistor is in ACT ~~state~~,



Using KVL;

$$\begin{aligned} 0 &= 2k \cdot i_E + 0.7V + 7.5k \cdot i_B - 5V \\ &= (2k \cdot 101 + 7.5k) i_B - 4.3V \end{aligned} \quad (3 \text{ pts})$$

$$\Rightarrow i_B = \frac{4.3V}{209.5k} = 20.525 \mu A$$

(3 pts)

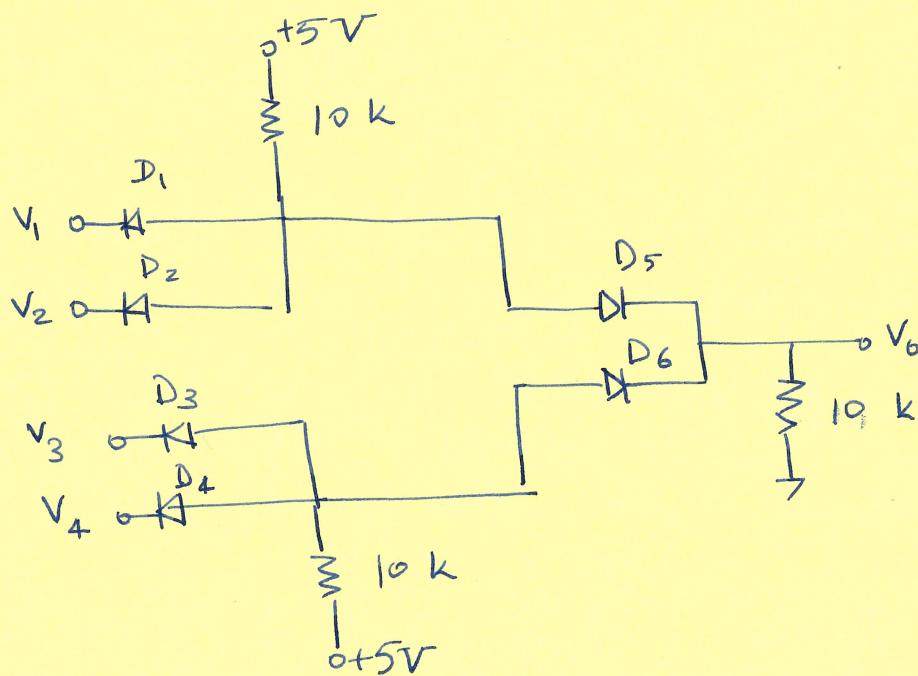
$$\boxed{i_C = \beta i_B = 2.052 \text{ mA}}, \quad i_E = 2.073 \text{ mA}$$

$$V_E = 0 - 2k \cdot i_E = -4.146V$$

$$\Rightarrow \boxed{V_{EC} \approx 5.6V} \quad (3 \text{ pts})$$

$$V_C = -20 + 5k \cdot i_C = -9.74V$$

4



Just consider upper branch of the cct:

(2pts) $v_1 = 0, v_2 = 0 \rightarrow D_1 \& D_2$ are OFF!

D_5 does not matter - No current on it.

~~$v_1 = 0, v_2 = 1 \rightarrow D_1$~~ is ON!, D_2 is OFF!

D_5 does not matter - No current on it.

(2pts) $(v_1, v_2) \rightarrow (0, 0) \rightarrow v_o = 0 \quad (1, 1) \Rightarrow v_o = 1$

~~$(0, 1) \rightarrow v_o = 0$~~] symmetry!

$(1, 0) \rightarrow v_o = 0$

$v_1 = 1, v_2 = 1 \rightarrow D_1 \& D_2$ are OFF!

D_5 is ON!

ideal diode

$$v_o \approx \frac{5}{20k} \cdot 10k = 2.5 [V] \text{ consider as } 1!$$

(2pts) Since circuit is symmetric, the same should apply to $D_3, D_4 \& D_6$. Thus

v_1	v_2	v_3	v_4	v_o
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
1	0	0	0	0
1	1	0	0	1
1	0	1	0	0
0	1	1	0	0
1	1	1	0	1