Two stage BJT amplifier:
Common emitter stage cascaded with push-pull voltage buffer

Preliminary work:
The circuit shown in Fig.1 will be used in Lab4. Find the data sheets and SPICE models of the transistors BC238, BD135, and BD136. Study and understand the properties of these transistors.

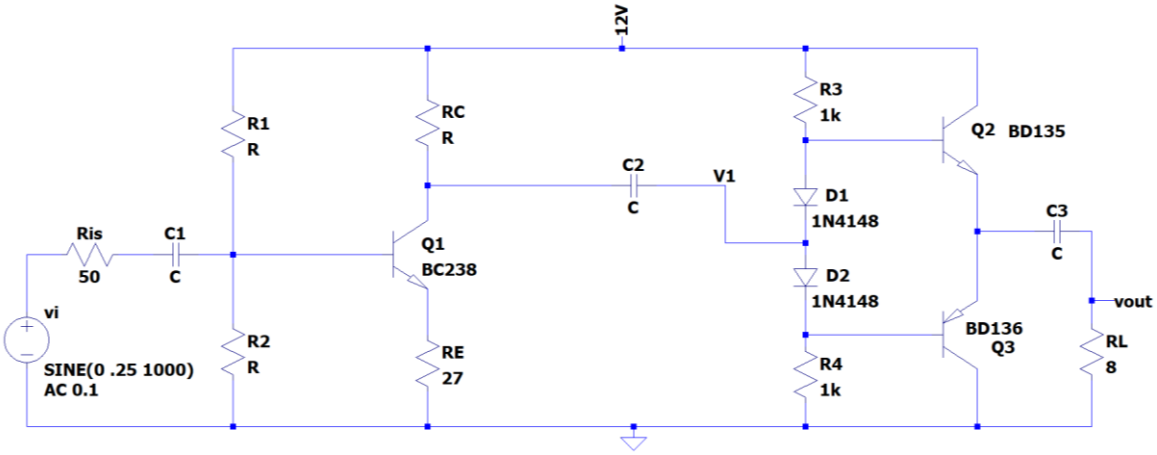

Figure 1: BJT circuit for lab 4.

Lab work:
A:
A1. Set up the circuit in LTSpice. R_E is already given as 27Ω. Output load is an 8Ω power resistor representing a loudspeaker. R_{is} is the source resistance of the signal generator in the lab and is 50Ω. The first stage of the amplifier should have a gain of about -10 without the second stage connected (i.e. when C_2 is removed). The overall gain should be around -5. The output should not get clipped up to an ac input of 0.5V peak. Determine R_1, R_2, and R_C to meet these specifications. Measure the exact values of the gain and R_{in} seen from point V_1 to the right. Also measure the input and output impedance of the amplifier.

Note1: The impedance seen at point V_1 to the right is $1k//1k//(\beta+1)*8 \approx 400\Omega$.
Note2: At this stage set the capacitors to very high values so that they may be considered as short at 1KHz.

A2. Take C_1=10μF, C_2=100μF, and C_3=1000μF. Plot using Spice the Magnitude Bode plot of the output and determine f_L and f_H which are the -3dB low and high cutoff frequencies of the amplifier, respectively. Although not covered in the class yet, f_L is set by the external capacitors and f_H is set by the internal device capacitances. For f_L you can think that the external capacitors see an equivalent resistor and the RC circuit acts like a low pass filter. These will be covered in the lectures in the following weeks.

A3. What is the purpose of the diodes D_1 and D_2? Short them and comment on the result.

Check point#1: You should come to the lab and show your simulation results to your TA on the week of November 20th.

B:
B1. Set up the circuit in the lab. First, without ac input, check your Q-point values. Adjust

values to get desired levels.

B2. Apply 0.1sinwt and measure voltage gain. Adjust parameters to get the desired gain (f = 1KHz).

B3. Apply 0.1sinwt, 02sinwt, 0.3sinwt, 0.4sinwt, and 0.5sinwt and in each case measure the voltage gain and the harmonic content.

B4. Determine the maximum peak input without clipping at the output.

B5. Measure f_L and f_H.

Check point#2: You should demonstrate the working circuit to your TA on the week of November 27th. It might be more convenient to complete the hardwarer implementation in the week of Nov. 20th but it is up to you.

We assume you are familiar with the output impedance of the signal generators in the lab, see lab1 notes if you don't remember.

You should be in the lab and have your circuit ready during the check-out. You are expected to demonstrate a working set-up and be able to explain how the circuit works and what your results are. Your assistant may ask you questions about your lab and also your preliminary work (if any). You are expected to work individually and demonstrate that you fully understand the purpose and results of the lab.

In writing your report explain what you have done (simulations, circuits, oscilloscope connections, procedures, etc), what you have obtained (values, graphs, tables, screenshots, etc), and your comments. Report your Spice circuits and results also. Include all the component values, DC operating point of the transistor, and clearly explain your optimization procedure.

The deadline to submit your report is Sunday, December 10th, 23:55.