

Name: _____

Section: _____

Signature: _____

EEE 313 Fall 2014-2015

Bilkent University
Department of Electrical and Electronics Engineering
EEE 313 Electronic Circuit Design

Midterm 1

25 October 2014, 10:00
(4 questions, 120 minutes)

- This is a **closed book**, closed notes exam. No cheat sheet allowed.
- All cell-phones should be completely **turned off**.
- Use a calculator for numerical computations. Carry at least **4 significant digits** during calculations. Your final answer should be at least **3 significant digits**.
- Be sure to write the **units** of all numerical results.
- **Show** all work clearly.
- Please put your **final answer** for each part inside a box for easy identification. Do not give multiple answers, they will not be graded.
- Do not remove the **staple** from the exam sheets or separate pages of the exam. All extra pages must be stamped to your exam.
- You may leave the exam room when you are done. However, please do not leave during the **last five minutes** of the exam.
- At the end of the exam, please stay seated until **all** exam papers are collected.

FET equations:

n-channel MOSFET

$$i_D = K_n (v_{GS} - V_{Th})^2 \quad \text{SAT}$$
$$i_D = K_n [2(v_{GS} - V_{Th})v_{DS} - v_{DS}^2] \quad \text{NON-SAT}$$

p-channel MOSFET

$$i_D = K_p (v_{SG} + V_{Tp})^2 \quad \text{SAT}$$
$$i_D = K_p [2(v_{SG} + V_{Tp})v_{SD} - v_{SD}^2] \quad \text{NON-SAT}$$

n-channel JFET

$$i_D = \frac{I_{DSS}}{V_p^2} (v_{GS} - V_P)^2 \quad \text{SAT}$$
$$i_D = \frac{I_{DSS}}{V_p^2} [2(v_{GS} - V_P)v_{DS} - v_{DS}^2] \quad \text{NON-SAT}$$

Please do not write below this line

1. 25 pts.	
2. 20 pts.	
3. 25 pts.	
4. 30 pts.	
Total 100 pts.	

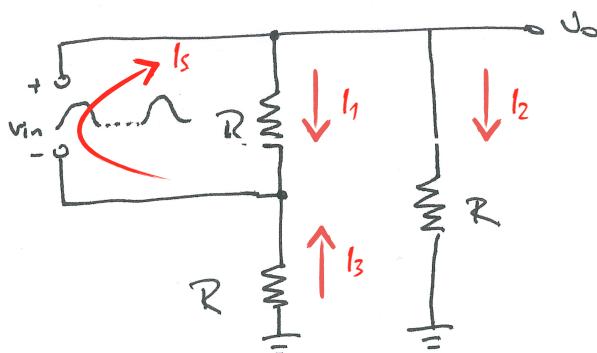
1. (20 points) The input signal V_i is a sinusoid with an amplitude of 20 V. For the diode assume $V_g=0$ V (i.e., V_{on} voltage) and that the diodes are ideal. All resistors are equal to $10 \text{ k}\Omega$. Determine the output signal V_o .

When $V_i(t)$ is going through its positive cycle

(shown in black), the diode

on the left is reverse biased
(open circuit) and the diode on
the right is forward biased (shorted),

so the circuit looks like:



$$\text{KCL at node } A, I_s = I_1 + I_2$$

$$\text{KCL at node } B, I_s = I_1 + I_3$$

Therefore, $I_2 = I_3$. Since $R I_2 = V_o$, then $R I_3 = V_o$, as well.

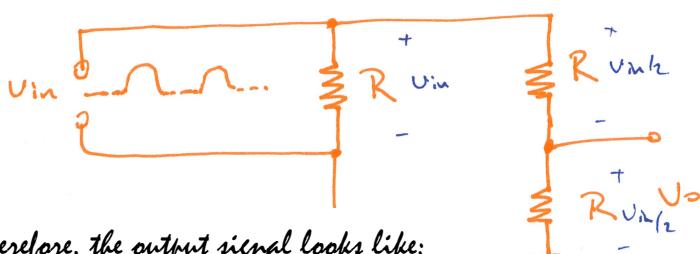
Writing KVL around the three resistors,

$$R I_2 = R I_1 - R I_3, \text{ and since } R I_1 = V_{in} \text{ and } R I_2 = R I_3 = V_o,$$

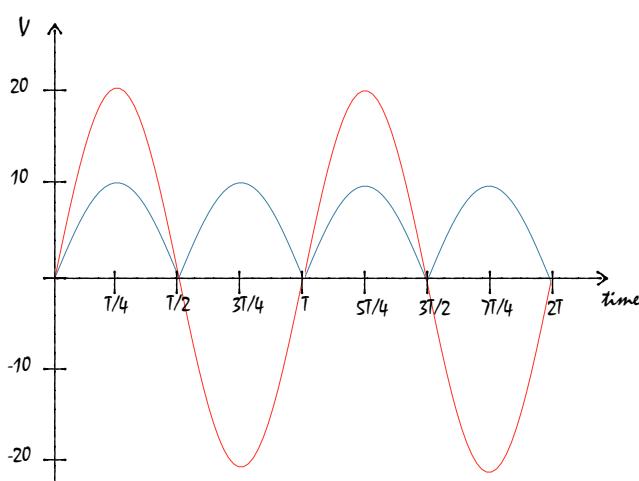
$$V_o(t) = V_{in}(t)/2.$$

Similarly, when $V_i(t)$ is going through a negative half-cycle

the circuit looks like:



Therefore, the output signal looks like:

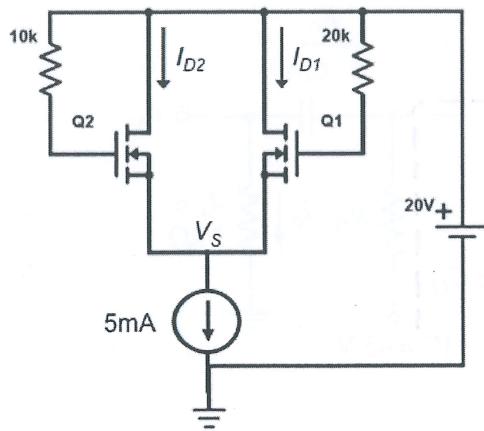


$$\text{Therefore } V_o(t) = \frac{|V_{in}(t)|}{2}$$

during the negative half cycles. Notice that the circuit was drawn with poles of V_{in} inverted.

2. (20 points) For the following circuit, find the states of the n-channel MOS enhancement mode transistors Q1 and Q2, assuming that $V_{Tn1} = V_{Tn2} = 2.5V$, and $K_{n1} = 4$ mA/V^2 , $K_{n2} = 1 \text{mA/V}^2$.

Q ₁ state	Q ₂ state	I _{D1}	I _{D2}	V _S
SAT	SAT	4mA	1mA	15.5V



Gate currents are zero

$$V_{GS1} = V_{GS2} = V_{GS} = V_{DS}$$

assume SAT for Q₁ & Q₂

$$(V_{GS} - V_{Th} < V_{DS})$$

$$I_{D1} = K_{n1} (V_{GS} - V_{Th})^2$$

$$I_{D2} = K_{n2} (V_{GS} - V_{Th})^2$$

$$I_{D1} + I_{D2} = 5 \text{ mA}$$

$$I_{D1} = 4 \text{ mA} \quad I_{D2} = 1 \text{ mA}$$

$$4 \text{ mA} = 1 \text{ mA/V}^2 (V_{GS} - 2.5)^2$$

$$V_{GS} = 4.5 \text{ V} = V_{DS}$$

$$V_S = 15.5 \text{ V}$$

$$15.5 - 2.5 = 12.5 \text{ V} + 2.5 \cdot 0.4 \text{ V} + 2.5 \cdot 0.1 \text{ V} = 12.75 \text{ V}$$

$$\boxed{12.75 \text{ V} = 12.5 \text{ V}}$$

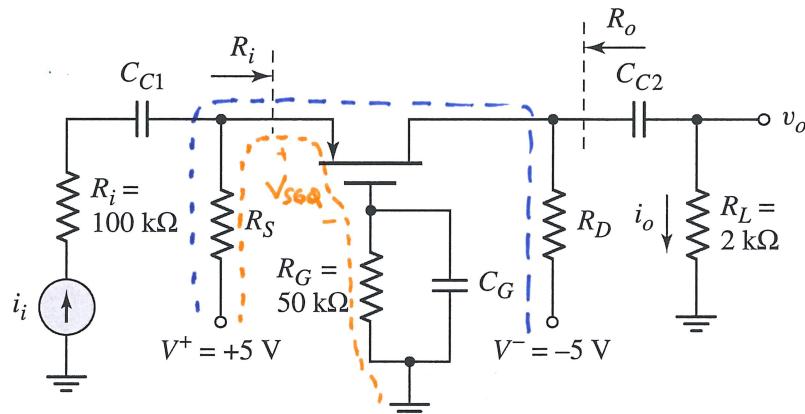
All we have to do is to find the voltage across the load and then

$$12.75 - 0.4 \text{ V} + 0.1 \text{ V} + 0.1 \text{ V} = 12.4 \text{ V}$$

across (load)

$$\boxed{12.4 \text{ V} = 0.4 \text{ V} \cdot (0.4 + 0.1) \cdot 75.0 + 0.1 = 0.1}$$

3. (30 points) Consider the p-channel MOS common-gate circuit in the figure. The transistor parameters are: $V_{TP} = -1$ V, $K_p = 0.5$ mA/V², and $\lambda = 0$. (a) Determine R_S and R_D such that $I_{DQ} = 0.75$ mA and $V_{SDQ} = 6$ V. (b) Determine the input impedance R_i and the output impedance R_o . (c) Determine the load current i_o and the output voltage v_o , if $i_i = 5 \sin(\omega t)$ μ A. Assume all capacitors are very large. V^+ and V^- are applied DC voltages.



(a) DC analysis

$$\text{Use } I_{DQ} = K_p \cdot (\sqrt{V_{SGQ}} + \frac{V}{R_G})^2 \Rightarrow \sqrt{V_{SGQ}} = 2.225 \text{ V}$$

$\downarrow \quad \downarrow \quad \downarrow$

$0.75 \text{ mA} \quad 0.5 \text{ mA/V}^2 \quad 1 \text{ V}$

Now apply KVL from the V^+ port to gate ground. Assuming current into gate is negligibly small,

$$+5 \text{ V} = I_{DQ} \cdot R_S + \sqrt{V_{SGQ}} \Rightarrow R_S = \frac{5 - 2.225}{0.75}$$

$\downarrow \quad \downarrow$

$\text{given as} \quad \text{calculated}$
 $0.75 \text{ mA} \quad \text{above}$

$R_S = 3.70 \text{ k}\Omega$

Apply KVL again, from the V^+ port to the V^- port over R_S , the transistor and R_D :

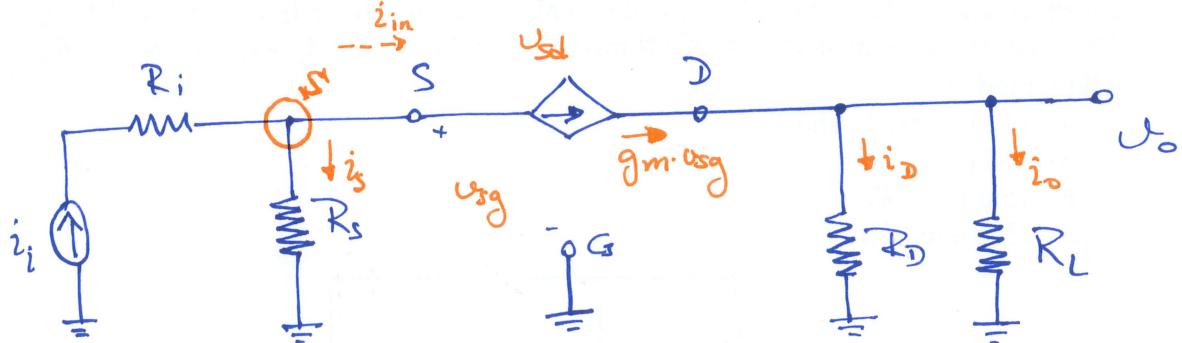
$$+5 \text{ V} = I_{DQ} \cdot R_S + \sqrt{V_{SDQ}} + I_{DQ} \cdot R_D - 5 \text{ V}$$

$\downarrow \quad \downarrow \quad \downarrow$

$\text{found above} \quad 6 \text{ V (given)} \quad 0.75 \text{ mA (given)}$

$$10 = 6 + 0.75(3.70 + R_D) \Rightarrow R_D = 1.63 \text{ k}\Omega$$

(b) Input impedance, R_{in} , is given by $R_{in} = \frac{V_{SD}}{i_i}$
 (we set up the small-signal AC equivalent circuit first, below)



$$R_{in} = \frac{V_{SD}}{i_{in}} = \frac{V_{SD}}{g_m V_{sg}} = \frac{1}{g_m} \quad \boxed{R_{in} = 0.816 k\Omega}$$

$$g_m = 2\sqrt{K_p \cdot I_{DQ}}$$

$$= 2\sqrt{0.5 \cdot 0.075} = 1.225 \text{ mA/V}$$

Output impedance
 is $R_o = R_L = 1.63 k\Omega$

(c) Start by writing KCL at node S: $i_i = i_s + g_m \cdot V_{sg}$

Moreover, voltage drop across R_s is

the same as V_{sg} , so: $V_{sg} = i_s \cdot R_s \Rightarrow i_i = \frac{V_{sg}}{R_s} + g_m \cdot V_{sg}$

Therefore,

$$V_{sg} = \frac{i_i \cdot R_s}{1 + g_m \cdot R_s}$$

On the right side of the transistor, current, $g_m V_{sg}$, is split into the R_D and R_L branches, which act as current dividers.

$$i_o = \frac{g_m \cdot V_{sg} \cdot R_D}{R_D + R_L}$$

Inserting the expression for V_{sg} into the equation directly above:

$$i_o = i_i \cdot \frac{g_m \cdot R_s \cdot R_D}{(1 + g_m \cdot R_s)(R_D + R_L)} = \frac{i_i \cdot R_D}{R_D + R_L} \cdot \frac{g_m \cdot R_s}{1 + g_m \cdot R_s}$$

$$i_o = i_i \cdot \left(\frac{R_D}{R_D + R_L} \right) \cdot \left(\frac{R_s}{R_s + 1/g_m} \right)$$

Plugging in the values, we obtain:

$$i_o = i_i \cdot \left(\frac{1.63}{1.63 + 2} \right) \left(\frac{3.70}{3.70 + 0.82} \right) i_i = 0.368 i_i$$

Thus,

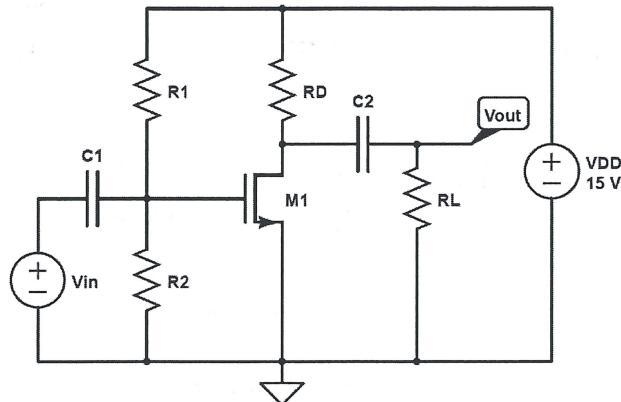
$$i_o = 1.84 \sin(\omega t) \mu A \quad \text{given } i_i = 5 \sin(\omega t) \mu A$$

$$v_o = i_o \cdot R_L \Rightarrow$$

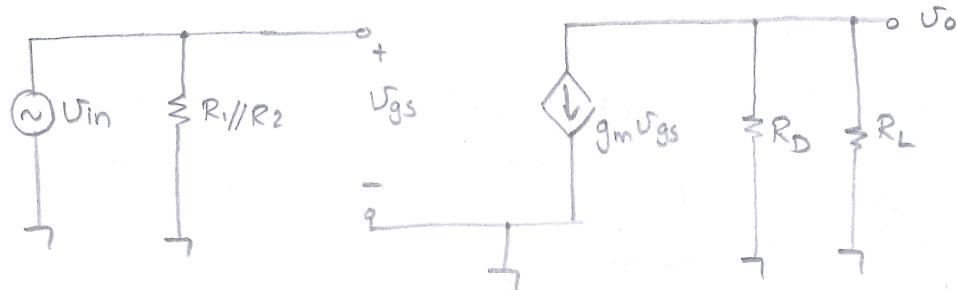
$$v_o = 3.68 \sin(\omega t) \mu V$$

4. (30 points) Design the common source circuit below using an n-channel enhancement-mode MOSFET. The quiescent values are to be $I_{DQ} = 5\text{mA}$ and $V_{GSQ} = 4\text{V}$. The transconductance is $g_m = 10\text{mA/V}$. Let $R_L = 1\text{k}\Omega$, $A_v = v_{out}/v_{in} = -5$, $R_{in} = 48\text{k}\Omega$. Find:

- (10 points) R_1 and R_2
- (10 points) R_D
- (5 points) K_n
- (5 points) V_{tn}



Small signal ac equivalent



$$A_v = -g_m(R_D \parallel R_L)$$

$$-5 = -10 \frac{\text{mA}}{\text{V}} (R_D \parallel R_L)$$

since $R_L = 1\text{k}\Omega \Rightarrow R_D = 1\text{k}\Omega$

$$R_{in} = R_1 \parallel R_2 = 48\text{k}\Omega$$

$$V_{GSQ} = 4\text{V} = 15\text{V} \frac{R_2}{R_1 + R_2}$$

$$g_m = 2\sqrt{K_n I_{DQ}}$$

$$10 \frac{\text{mA}}{\text{V}} = 2\sqrt{K_n \cdot 5\text{mA}}$$

$$25 \frac{\text{mA}}{\text{V}^2} = 5 \text{mA/V}$$

$$R_2 = 4R$$

$$R_1 = 11R$$

$$R_2 \approx 65.45 \text{k}\Omega$$

$$R_1 \approx 180 \text{k}\Omega$$

$$K_n = 5 \frac{\text{mA}}{\text{V}^2}$$

$$I_{DQ} = K_n (V_{GS} - V_{Th})^2$$

$$5\text{mA} = 5 \frac{\text{mA}}{\text{V}^2} (V_{GS} - V_{Th})^2$$

since $V_{GS} = 4\text{V} \Rightarrow V_{Th} = 3\text{V}$