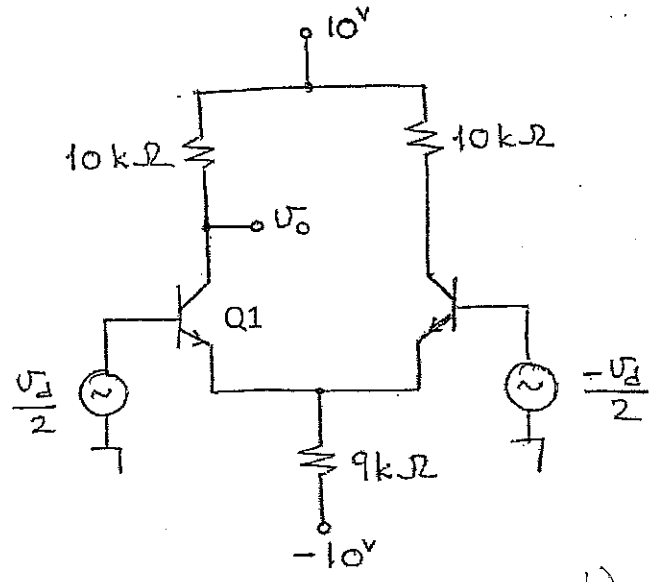
3. (20 points) For the circuit given below, the transistors are identical and $\beta=99$, $V_{BE(ON)}=1V$, $V_{CESAT}=0V$, $r_o=\infty$.

i. (05 points) Determine the DC base current of Q1

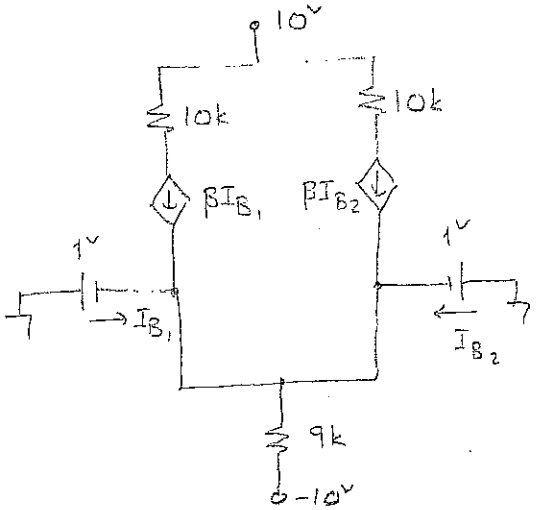
ii. (05 points) Draw the ac equivalent circuit

iii. (10 points) Find the single-sided voltage gain, v_o/v_d.



a) TR are in F.A.

Dc eq.



since identical : $I_{B_1}=I_{B_2}=I_B$

$I_{E_1}=I_{E_2}=I_E$

$$2I_E=\frac{(0-1^V)-(-10^V)}{9k}$$

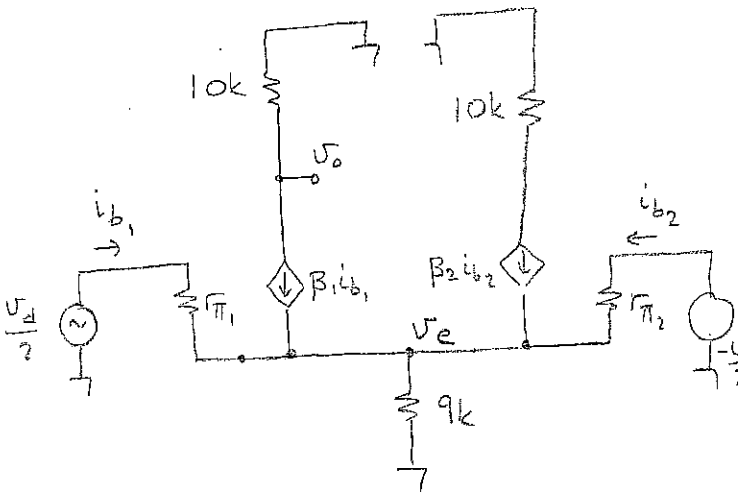
$$I_E=0.5\,mA$$

$$\boxed{I_B=5\mu A}$$

$I_{B_1}=I_{B_2} \Rightarrow r_{\pi_1}=r_{\pi_2}$

$$r_\pi=\frac{26mV}{5.2k}$$

b) ac eq.



c) $v_o=-\beta i_{b_1}\cdot 10k=-\beta i_b 10k$

emitter node: $(\beta+1)i_{b_1}+(\beta+1)i_{b_2}=\frac{v_e}{9k}$

$$\frac{v_d}{2}-r_\pi i_{b_1}=v_e=-\frac{v_d}{2}-r_\pi i_{b_2}$$

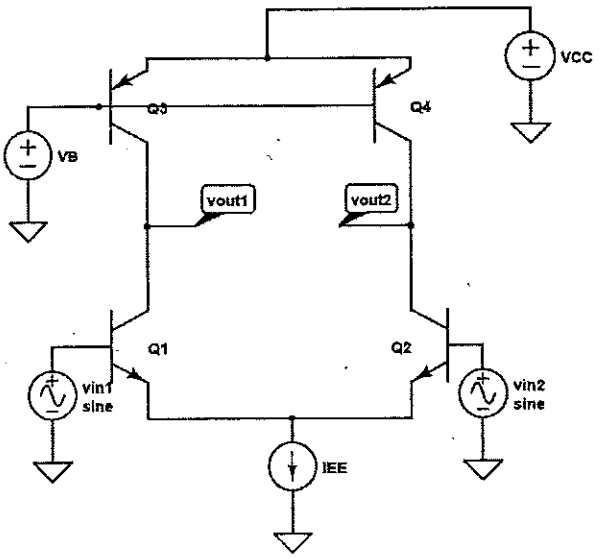
$$\left.\begin{aligned}\frac{v_d}{2}-r_\pi i_{b_1}&=v_e\\ \frac{v_d}{2}+r_\pi i_{b_2}&=v_e\end{aligned}\right\} \Rightarrow i_{b_1}=-i_{b_2}=i_b$$

$v_e=0$

$$\frac{v_d}{2}=r_\pi i_b$$

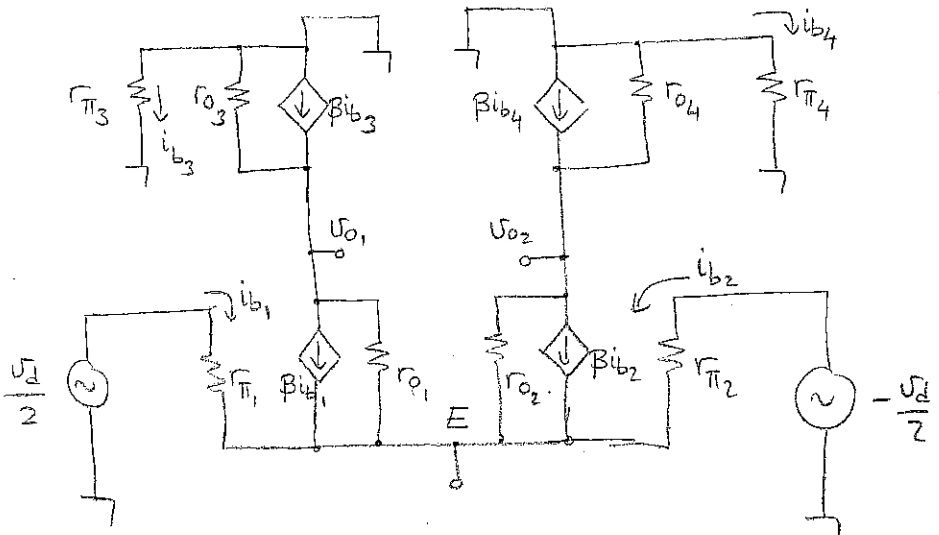
$$\boxed{\frac{v_o}{v_d}=\frac{-\beta\cdot 9ok}{2r_\pi}=-95.19}$$

2. (20 points) Figure below illustrates an alternative implementation of a differential amplifier. Draw the small signal ac equivalent circuit. Calculate the differential voltage gain parametrically. (Calculate $\frac{v_{out1} - v_{out2}}{v_{in1} - v_{in2}}$). Assume Q_1 and Q_2 are matched and Q_3 and Q_4 are matched. Please DO NOT ignore r_o.
Please *WRITE CLEARLY, NO PARTIAL GRADE IF I CANNOT READ*!!



Due to center symmetry node E is virtual ground.

$$v_{o1} = -g_m v_{\pi_1} (r_{o1} // r_{o3})$$
$$v_{o2} = -g_m v_{\pi_2} (r_{o2} // r_{o4})$$



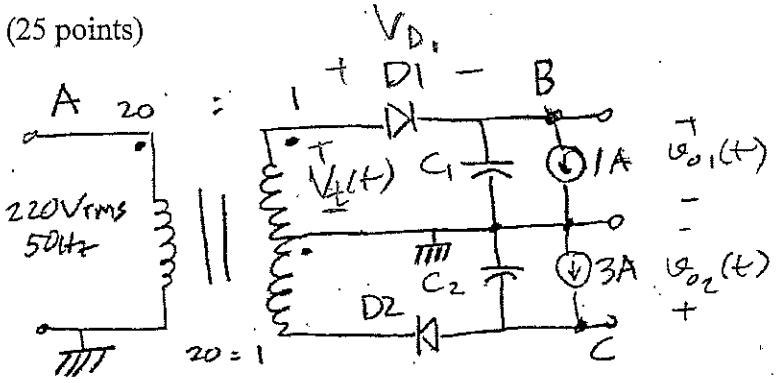
$i_{b_3} = i_{b_4} = 0$ since they are current between two grounded nodes

due to identical biasing
$r_{o1} = r_{o2}$
$r_{o3} = r_{o4}$

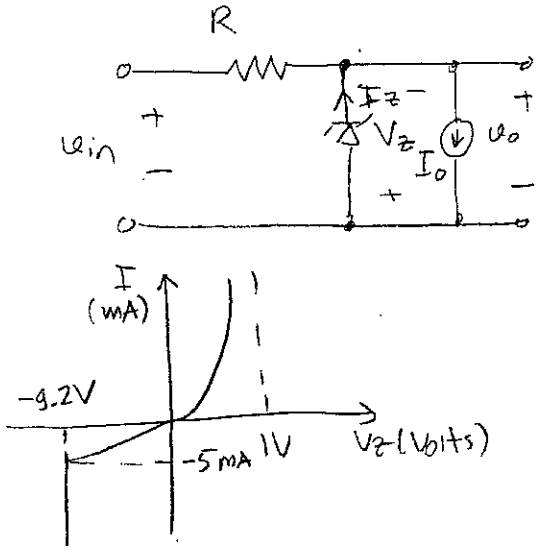
$$v_{o1} - v_{o2} = -g_m (r_{o1} // r_{o3}) (v_{in1} - v_{in2})$$ since $v_{in1} = v_{\pi_1}$, $v_{in2} = v_{\pi_2}$

$$\frac{v_{o1} - v_{o2}}{v_{in1} - v_{in2}} = -g_m (r_{o1} // r_{o3})$$

5. (25 points)



(I)

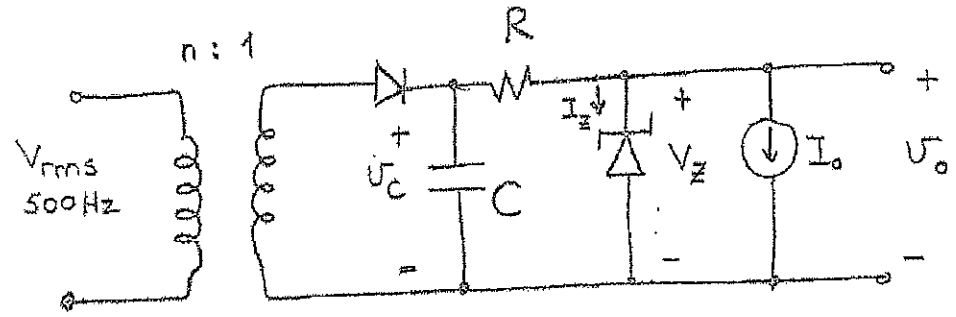


(II)

At the circuit given at (I), C1=10000μF, V2=15000μF, Vγ=1 Volts. Each of the secondary winding of the transformer has the transformer ratio of 20:1. Please answer the following:

a) (5 points) Find the ripple voltage on $V_{O1}(t)$ and $V_{O2}(t)$.
b) (5 points) Find the peak reverse voltages on diodes D1 and D2.
c) (5 points) Plot $V_{O1}(t)$ and $V_{O2}(t)$ on the same graph showing the voltages and timing properly.
d) (5 points) Would you get electric shock if you touch the points marked A,B and C. Please answer and explain each one seperately.
e) (5 points) At the circuit given at (II), a regulator circuit and the V-I characteristics of the zener diode used at the regulator is given. The ranges of v_{in} and Io are given as follows; $12V<v_{in}<20V$ and $10mA<Io<30mA$. Find the value of R which preserves regulation and which minimizes the zener diode power dissipation at the same time.

2. (15 points) For the circuit shown below, the capacitor voltage varies between 13V and 18V. Let $V_\gamma = V_{ON} = 1.5V$ and $V_Z = 12V$. The DC output current requirement is between $200mA > I_O > 20mA$. Also assume that R = 15Ω and C = 1mF. What is the minimum power rating of the zener diode? Calculate source and load regulation. (*Hint: What is the maximum power dissipation that the zener diode has to tolerate?*)



power rating ← $P_z(min) \geq$ max power dissipation of zener diode

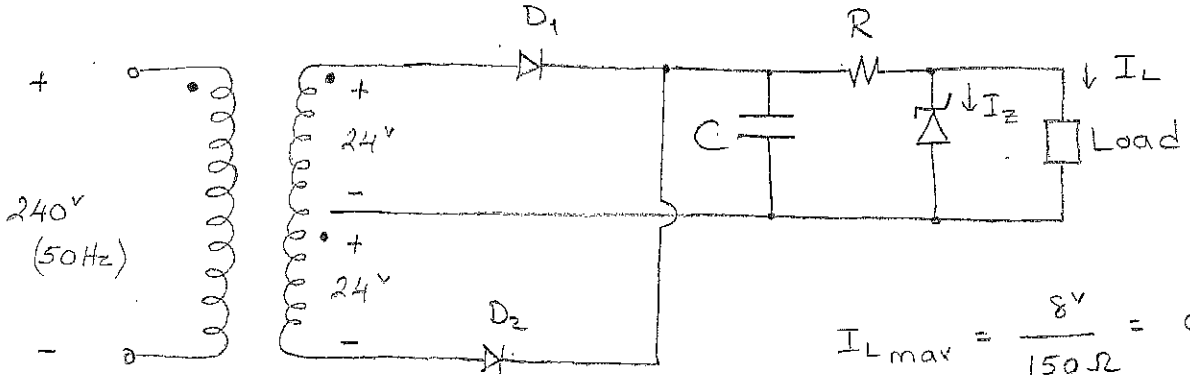
$$I_z(max) \cdot V_z(max) = \left[\frac{18^V - 12^V}{15\Omega} - 20mA\right] \cdot 12^V$$

$$P_z(min) \geq (380mA) \cdot 12^V = 4.56 \text{ Watt}$$

$$\text{source regulation} = \frac{12-12}{12} = 0\ \%$$

$$\text{load regulation} = \frac{12-12}{12} = 0\ \%$$

5. (25 points) Design a **full-wave regulated** power supply using 10:1 center-tapped transformer and an 8 V Zener diode. The power supply must provide a constant 8 V to a load varying from 150 to 400 Ω. The input voltage is 240 V (rms), 50 Hz. You may use ideal diodes with $V_\gamma = V_{ON} = 0V$. The power rating of the Zener diode is 1.5 W.



Full wave rectifier 4 points

Filter circuit 4 points

Regulator circuit 4 points

Correct connection 4 points

Critical parameters 9 points

$$I_{L\,max} = \frac{8^V}{150\,\Omega} = 0.053\bar{3} = 53.\bar{3}\ mA$$

$$I_{L\,min} = \frac{8^V}{400\,\Omega} = 20\,mA$$

$$P_{max} = 1.5\,W = I_{z_{max}} \cdot 8^V$$

$$I_{z_{max}} < 187.5\,mA$$

$$I_{z_{max}} = \frac{24^V - 8^V}{R} < 187.5\,mA$$

$$R > 85.33\,\Omega$$

$$I_{L_{min}} = 20\,mA \qquad \frac{24^V - 8^V}{R} > 20\,mA$$

$$\Rightarrow R < 800\,\Omega$$

choose C very large!

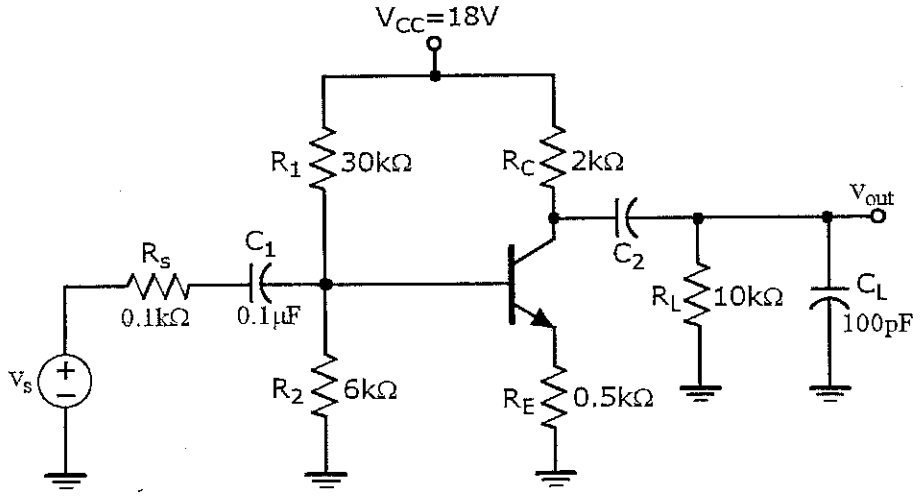
2. (25 points) For the following BJT amplifier circuit, let $\beta = 120$ and $V_{BE(ON)} = 0.7V$. You are given that $I_{CQ} = 4.21374\ mA$ and the small-signal parameters are $r_\pi = 740.435\Omega$ and $g_m = 162.067\ mA/V$. Assume that the output coupling capacitor (C_2) is very large and the lower and upper corner frequencies are far apart.

a. Draw the small-signal ac equivalent circuit and determine the small-signal midband voltage gain, $A_v = v_{out} / v_{in}$.

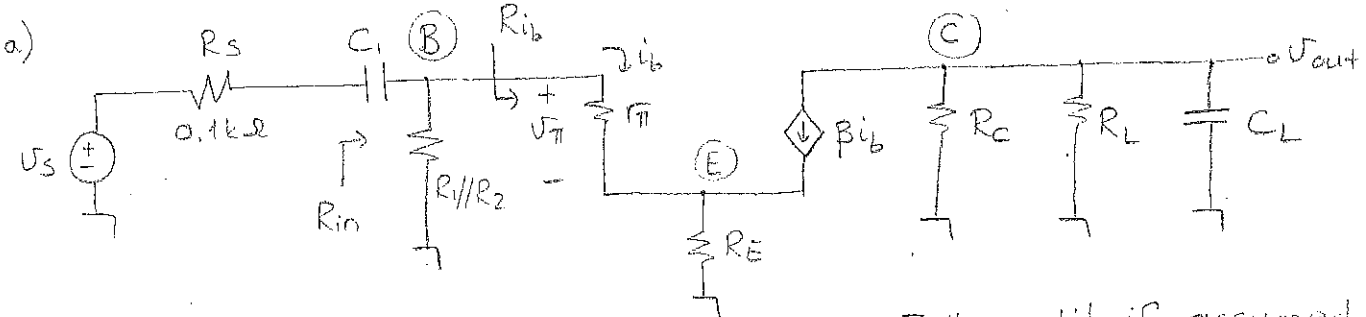
b. Find the corresponding 3dB lower corner frequency by taking into account the effect of input coupling capacitor (C_1), only.

c. Find the corresponding 3dB upper corner frequency by taking into account the effect of load capacitor (C_L), only.

d. Considering the combined effect of both capacitors (C_1 and C_L), sketch the Bode plot for the magnitude of the voltage gain of the amplifier.



a)



in the midband, we assume that the input capacitor C_1 is short circuit and C_L is open circuit.

Full credit if assumed C_L short and solved correctly.

$$R_{ib} = r_\pi + (\beta+1) R_E = 61.2404 k\Omega$$

$$R_{in} = R_1 // R_2 // R_{ib} = 4.6226 k\Omega$$

$$V_{out} = -\beta i_b (R_C // R_L)$$

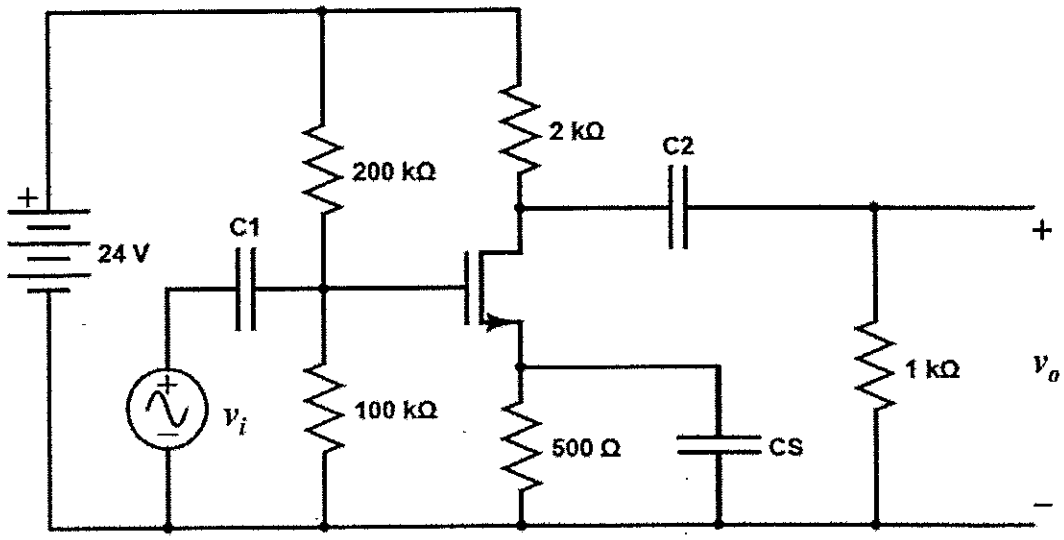
$$= -\beta (R_C // R_L) \frac{R_{in}}{R_{ib}(R_s + R_{in})} V_s$$

$$A_V = \frac{V_{out}}{V_s} = \frac{-\beta R_{in} (R_C // R_L)}{R_{ib}(R_s + R_{in})} = \frac{-120(2k // 10k)}{61.2404k} \frac{4.6226k}{4.7226k} = -3.1967$$

(6 points)

4. (30 points) Consider the single stage FET amplifier shown in the figure. The transistor parameters are $|K_n| = 1mA/V$ and $|V_t| = 3V$. The DC solution of the circuit yields a quiescent-point drain current of 5.36 mA.

a. Find the midband gain $A_v = v_o/v_{in}$ in dB units.
b. Determine the maximum peak-to-peak undistorted output voltage swing, V_{pp}
c. Determine the values of C_1 and C_2 so that the corner frequencies due to the input and output coupling capacitors are the same and equal to 100 Hz. Assume that the bypass capacitor C_S is short circuit at this frequency.
d. Using the capacitor values found in the previous part, determine the lower 3-dB corner frequency of the amplifier due to the combined effect of both coupling capacitors, again assuming that the bypass capacitor C_S is short circuit at 100 Hz.
e. Determine the smallest possible value of C_S such that the corner frequencies associated with this capacitor are below 10 Hz.
f. Determine the higher 3-dB corner frequency of the amplifier and draw the overall frequency-response. Use $C_{gs} = C_{gd} = 1$ pF.

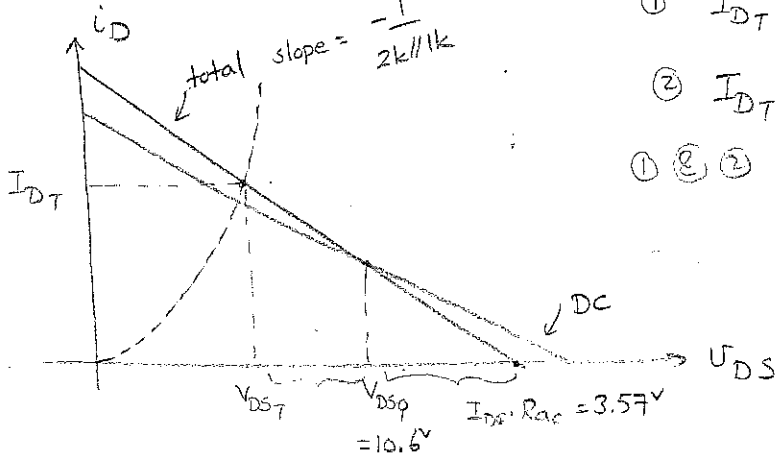


a) $g_m = 2\sqrt{K_n I_D} = 4.63\ mA/V$

$v_o = -g_m v_{in}\ (2k \| 1k) \Rightarrow A_v = -3.0869$

$20\log|A_v| = \boxed{9.79\ dB}$

b)



① $I_{DT} = K_n (V_{DST})^2$

② $I_{DT} \cdot \frac{2}{3} = 14.17 - V_{DST}$

① & ② $\frac{2}{3} v_{DST}^2 + v_{DST} - 14.17 = 0$

$v_{DST} = 3.921^V$

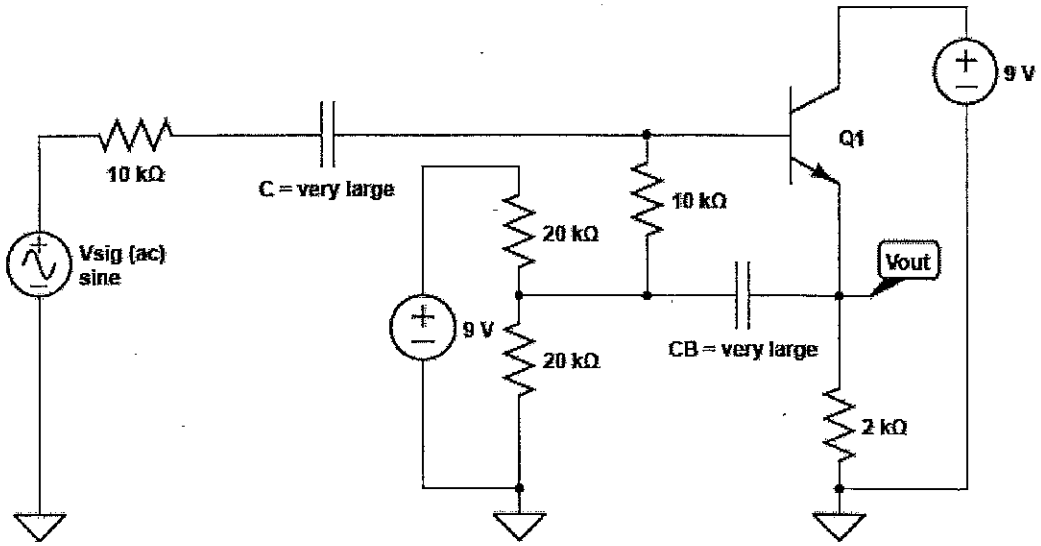
$V_{pp} = 2 \times \min(3.57^V, 6.68^V) = \boxed{7.14^V}$

4. (30 points) The circuit below is called a boot-strapped follower. Assume that β=100, $V_A \to \infty$, $V_{BE(ON)} = 1V$ and $V_{CE(SAT)} = 0.2V$.

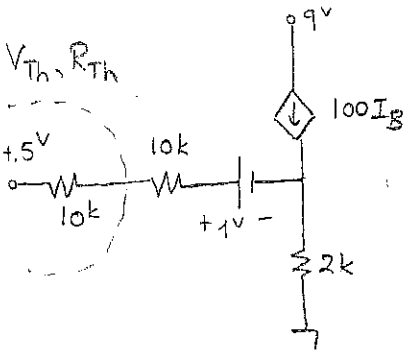
(a) Find the DC emitter current and g_m.

(b) Determine the input resistance and the voltage gain, $A_v = v_{out}/v_{sig}$

(c) Repeat part (b) for the case when C_B is open circuited. Compare the results. What are the advantages of bootstrapping? Explain!



a) DC Equiv.



$4.5^V = 1^V + I_B \cdot 20k + I_E \cdot 2k$

$3.5^V = I_B \cdot 222k \Rightarrow I_B = 15.766\,\mu A$

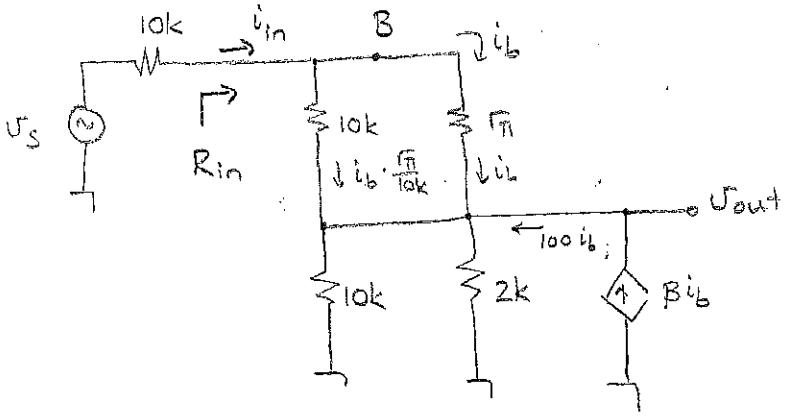
$I_C = 1.576\,mA$

$I_E = 1.592\,mA$

$g_m = \frac{I_{CQ}}{nV_T} = \frac{1.576\,mA}{26mV} = 60.615\,mS$

$r_\pi = \frac{nV_T}{I_{BQ}} = 1.649\,k\Omega$

b) ac equiv.



$v_{out} = \left(100i_b + i_b + i_b\frac{r_\pi}{10k}\right)(10k//2k)$

$v_s = v_{out} + i_b r_\pi + 10k\left(i_b + i_b\frac{r_\pi}{10k}\right)$

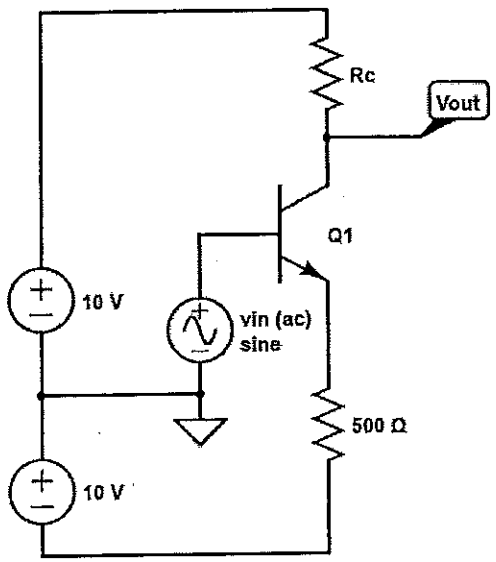
$A_v = \frac{\left(101 + \frac{r_\pi}{10k}\right)(10k//2k)}{\left(101 + \frac{r_\pi}{10k}\right)(10k//2k) + 2r_\pi + 10k}$

$R_{in} = \frac{v_{out} + i_b r_\pi}{i_{in}} = \frac{168.60k}{1 + \frac{r_\pi}{10k}} = \frac{168.60k}{1.1649}$

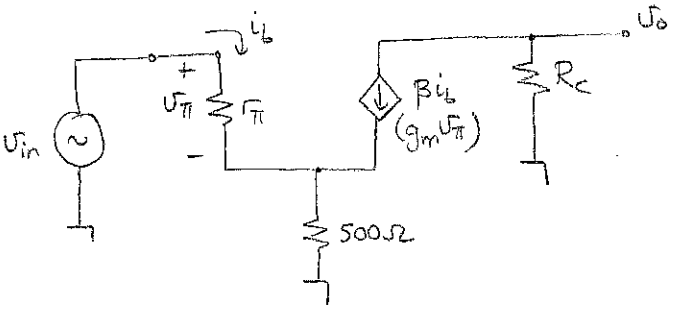
$A_v = \frac{(101.1649)(1.667k)}{168.60k + 10k + 3.298k} = \frac{168.60k}{181.898k} = 0.926$

$R_{in} = 144.7k\Omega$

3. (30 points) Gilbert's boss asked him to design the amplifier shown below and he expects to know what is the maximum voltage gain (does not have to be symmetric) that can be achieved with this stage. Please help Gilbert to find the maximum possible gain v_o/v_{in} and determine the value of collector resistance, R_C, and the DC collector current, I_{CQ}. Assume that β=199, $V_A \to \infty$, $V_{BE(ON)} = 1V$ and $V_{CE(SAT)} = 0.2V$. Show the transistor operating point (Q-point) of your design on a proper current-voltage graph of the transistor. Explain why you chose this Q-point. *Hint: Consider the maximum possible peak gain. Show all steps clearly!*



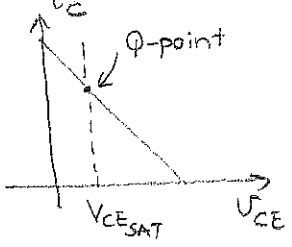
For amplifier, operate in F.ACT



$$v_o = -\beta i_b R_c$$

$$v_{in} = i_b \left(r_\pi + 500 \cdot (\beta+1) \right)$$

$$A_v = \frac{-\beta R_c}{r_\pi + 500(\beta+1)}$$

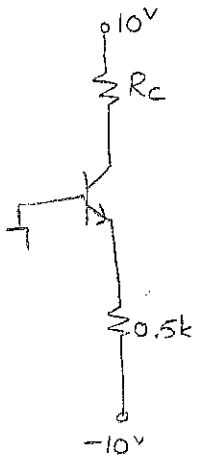


For max A_v R_c ↑

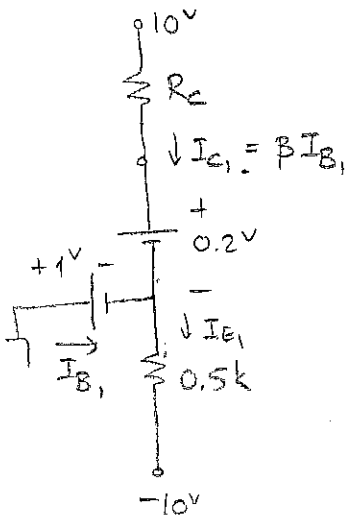
for high R_c ⇒ Q_1 can fall to SAT state

choose R_c to operate at SAT/ACT

DC Equiv.



ACT/SAT



$$I_{E_1} = \frac{-1^V - (-10^V)}{0.5k} = 18mA$$

$$I_{B_1} = \frac{18mA}{200} = 90\mu A$$

$$I_{C_1} = 90\mu \cdot 199 = 17.91mA$$

$$R_c = \frac{10^V - (-1^V + 0.2^V)}{17.91m} = 603\Omega$$

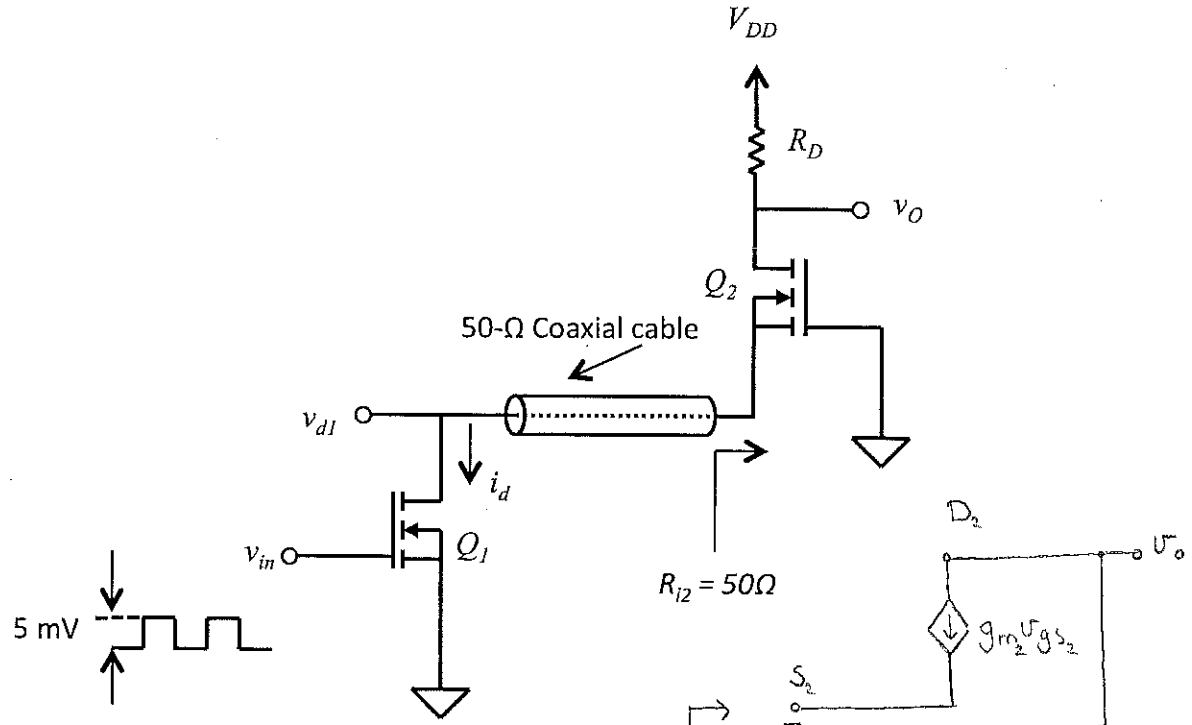
$R_c = 603\Omega$

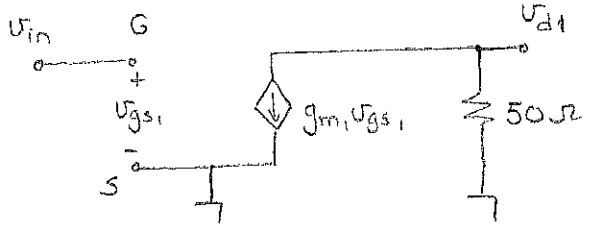
$$r_\pi = \frac{0.026^V}{90\mu A} = 0.288k\Omega$$

$$A_v = \frac{-199 \cdot 603\Omega}{288\Omega + 500\Omega \cdot 200} = -1.196$$

3. (30 points) The figure shown below is a scheme for coupling and ampifying a high frequency pulse signal. The circuit utilizes two MOSFETs whose bias details are not shown and a 50-Ω coaxial cable. The transistors are identical. Transistor Q_1 operates as a common-source amplifier and Q_2 as a common-gate amplifier. For proper operation, transistor Q_2 is required to present a 50-Ω resistance to the cable. This situation is know as "proper termination" of the cable and ensures that there will be no signal reflection coming back on the cable. When the cable is properly terminated, its input resistance is 50Ω.

a. What must g_{m2} be?
b. If Q_1 is biased at the same point as Q_2, what is the amplitude of the current pulses in the drain of Q_1?
c. What is the amplitude of the voltage pulses at the drain of Q_1?
d. What value of R_D is required to provide 1-V pulses at the drain of Q_2?





$50\,\Omega = \frac{1}{g_{m2}} \Rightarrow g_{m2} = 20\,mS$

$g_{m1} = g_{m2} = 20\,mS$

$i_{d1} = g_{m1} v_{gs1} = g_{m1} v_{in}$

$i_{d1} = 20\,\frac{mA}{V} \cdot 5\,mV = 100\,\mu A$

$v_{d1} = -i_{d1} \cdot 50\,\Omega = -5\,mV$

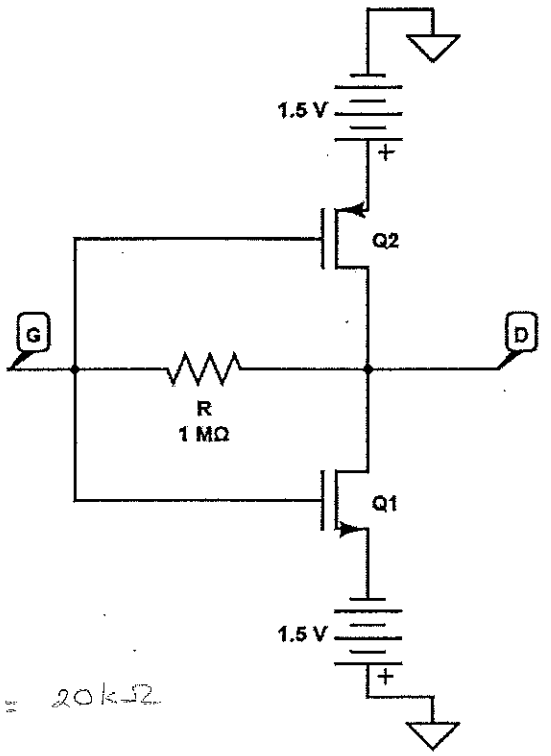
$v_o = -g_{m2} v_{gs2} \cdot R_D$

$1^V = -20\,\frac{mA}{V} \cdot (-5\,mV)\, R_D$

$\Rightarrow R_D = 10\,k\Omega$

3. (25 points) The MOSFETs in the circuit below are matched, having $K_n = K_p = 1$ mA/V^2 and $|V_t| = 0.5V$. The resistance R = 1 MΩ.

a. For G and D open, what are the drain currents I_{D1} and I_{D2}?
b. For $r_o \to \infty$, what is the voltage gain of the amplifier from G to D?
c. For finite r_o ($|V_A| = 20V$), what is the voltage gain from G to D?
d. For finite r_o ($|V_A| = 20V$), what is the input resistance at G?



a) $I_{D_1} = I_{D_2}$

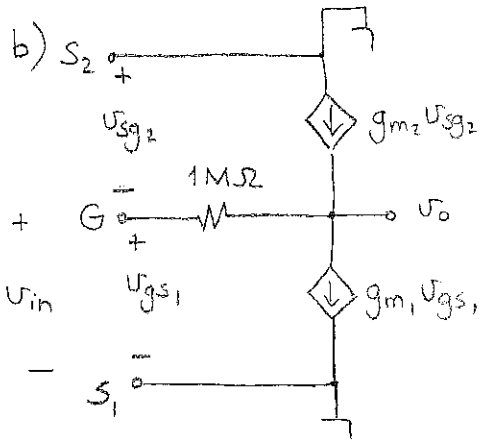
$I_{D_1} = 1 \cdot (V_{GS} - V_{Th})^2 = (V_G + 1.5 - 0.5)^2$

$I_{D_2} = 1 \cdot (V_{SG} + V_{Th})^2 = (1.5 - V_G - 0.5)^2$

$\Rightarrow V_G = 0 \Rightarrow I_{D_1} = I_{D_2} = 1mA$

$g_m = 2 \cdot K_n (V_{GS} - V_{Th}) = 2 mA/V$

b)



$\frac{v_{in} - v_o}{1M\Omega} + g_{m_2} v_{sg_2} = g_{m_1} v_{gs_1}$

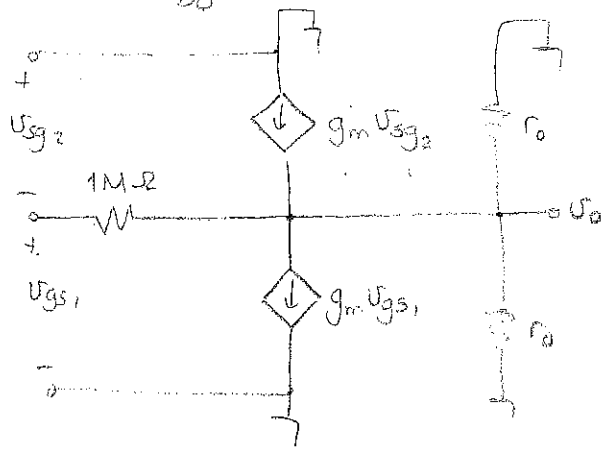
$\frac{v_{in} - v_o}{1M\Omega} + g_m (-v_{in}) = g_m v_{in}$

$\frac{v_o}{1M\Omega} = \frac{v_{in}}{1M\Omega} - 2 g_m v_{in}$

$v_o = v_{in} \left(1 - 2 \cdot 2 \frac{mA}{V} \cdot M\Omega\right)$

$\frac{v_o}{v_{in}} = 1 - 4 \cdot 10^{-3+6} = -3999$

c) $r_o = \frac{V_A}{I_{DQ}} = 20 k\Omega$



$\frac{v_{in} - v_o}{1M\Omega} + g_m (-v_{in}) = \frac{v_o}{10k} + g_m v_{in}$

$v_{in} \left(\frac{1}{1M\Omega} - 2g_m\right) = v_o \left(\frac{1}{10k} + \frac{1}{1M\Omega}\right)$

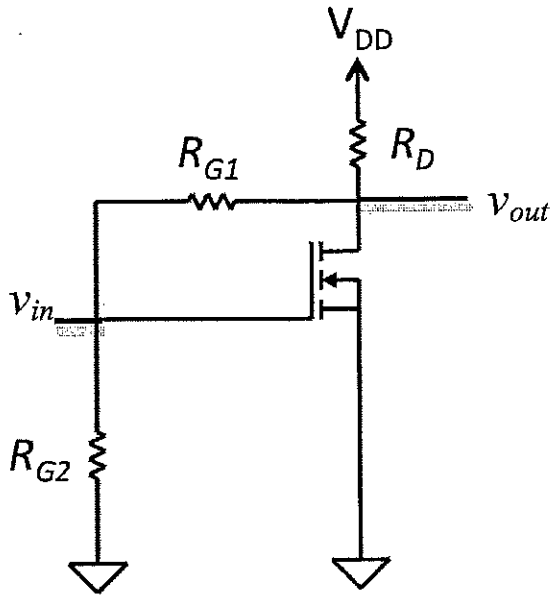
$\frac{v_o}{v_{in}} = \frac{1 - 2 \cdot 2 \cdot 10^{-3+6}}{1 + 100} = \frac{-3999}{101} = -39.59$

d) $R_{in} = \frac{v_{in}}{\left(\frac{v_{in} - v_o}{1M\Omega}\right)}$

$R_{in} = 1M\Omega \left(\frac{v_{in}}{v_{in} - v_o}\right) = 10^6 \Omega \left(\frac{1}{1 + 39.59}\right)$

$R_{in} = 24.6346 k\Omega$

1. (20 points) This is a design question. You are expected to apply concepts you learned in the class. Use a 6-Volt supply with an NMOS transistor for which V_{Th} =1.2^V, K_n=3.2mA/V^2. Provide a design which biases the transistor at I_{DQ}=2 mA with a 4-Volt peak-to-peak symmetric undistorted voltage swing at the drain. Use 22MΩ as the largest resistor in the feedback-bias network. Choose values for R_D, R_{G1} and R_{G2} specifying values to two significant digits. Please answer the following parts below for guidance. No partial credit for subsections. Please be careful with your calculations, use a calculator if necessary.



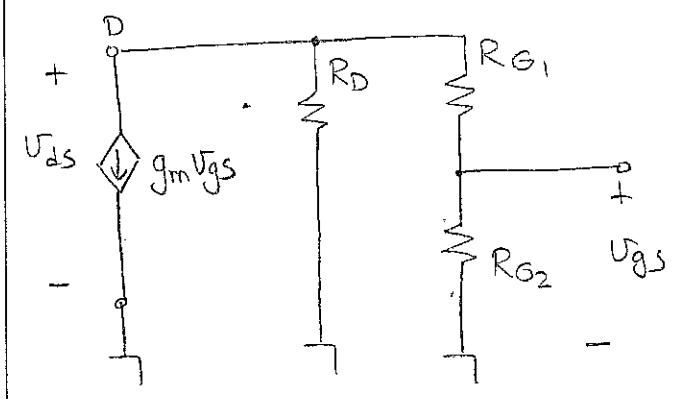
a. (2 points) Find the DC gate-to-source voltage, V_{GSQ}, if I_{DQ}=2 mA

V_{GSQ} = 1.99^V

$I_D = K_n (V_{GS} - V_{Th})^2 = 2mA$

$K_n = 3.2\,mA/V^2$ $V_{Th} = 1.2^V$

b. (3 points) Draw the small signal ac equivalent circuit.



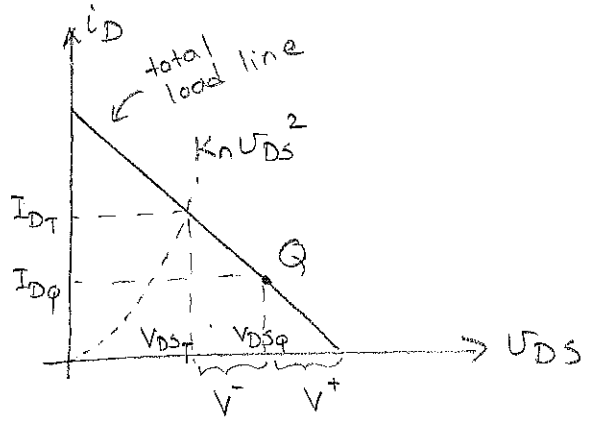
c. (2 points) Find a relation between i_d and v_{ds} (ac signals) and determine the slope of the ac load line **parametrically**.

Slope $= \frac{-1}{R_{ac}} = \frac{-1}{R_D // (R_{G1}+R_{G2})}$

$v_{ds} = -i_d R_{ac}$

$= -i_d \left[R_D // (R_{G1}+R_{G2}) \right]$

d. (3 points) On the i_D vs v_{DS} (total signals) axes, plot the total load line. Label the Q-point, I_{DQ}, V_{DSQ}. Also show and label, on this plot, the point V_{DST} and I_{DT} corresponding to (SAT)-(NON-SAT) state boundary for the swing.



e. (2 points) Given that the designed amplifier should have 4V **peak-to-peak** symmetric undistorted output voltage swing. Find the value of R_{ac}.

$R_{ac} = 1k\Omega$ since $V^+ = V^- = 2^V$ $I_{DQ} R_{ac} = 2^V$

f. (8 points) Find the values of R_{G1}, R_{G2}, and R_D.

R_{G1}= 2.4599kΩ	R_{G2}= 4.343kΩ	R_D= 1.1723kΩ

$V_{GSQ} = V_{DSQ} \frac{R_{G2}}{R_{G1}+R_{G2}}$ $K_n V_{DST}^2 = I_{DT} = 4mA \Rightarrow V_{DST} = 1.118^V$

$V_{DSQ} = 3.118^V$

DC load line $\frac{6^V - 3.118^V}{R_D} = 2mA + \frac{3.118^V}{R_{G1}+R_{G2}}$