ECD Lab Report 4

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Introduction:

The purpose of this lab is to get accustomed to bipolar junction transistors (BJT) and implement a push pull voltage buffer that is cascaded into a common emitter stage. For this purpose, 2 NPN BJTs, which are BC238, BD135, and 1 PNP BJT, BD136 are used. The two main requirements for this lab are to have around –10 gain from common emitter stage and reduce that gain to –5 through push pull voltage buffer. Here is the expected LTSpice Model:

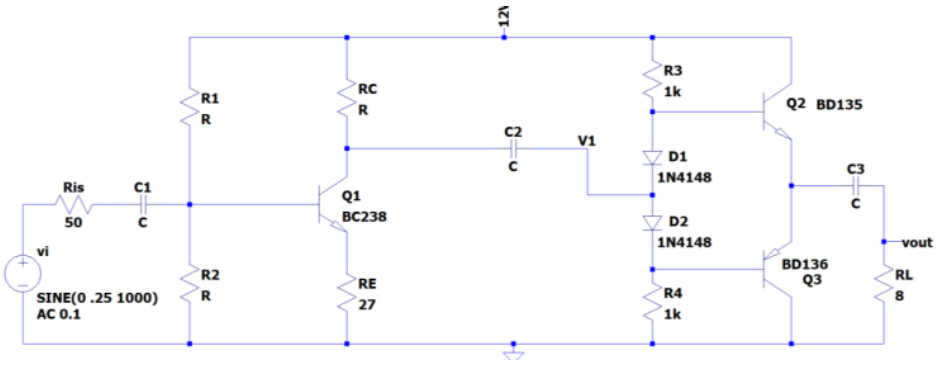

Figure 1: LTSpice Model for Lab 4

For this purpose, we need to decide on the values of R1,R2 and RC. To make a working circuit.

Software Implementation

A1)

Choice of RC, R1 and R2

Considering the small signal model of the common emitter stage when C2 is cut off we expect –10 gain and we expect to see –5 gain. From the datasheet the of BC238, the threshold voltage was chosen as $V_{BE(ON)} = 0.62\,V$. B was chosen as 200. Now we can do DC analysis to decide on the values of the R1 and R2 and RC. Here is the DC analysis of the common emitter circuit.

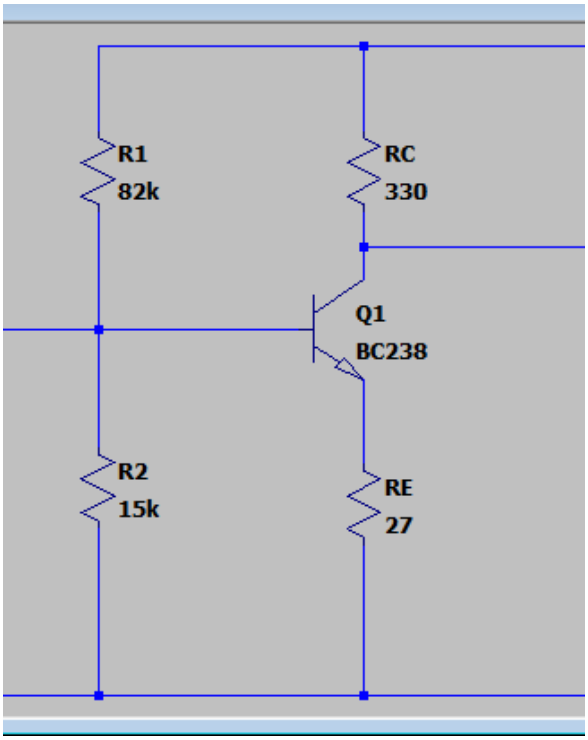

Figure 2: DC Analysis of Common Emitter Circuit

$$V_{TH} = \frac{R2}{R1 + R2} \cdot 12V$$

$$R_{TH} = \frac{R2 \cdot R1}{R1 + R2}$$

After the Thevenin equivalent looking at base current and doing KVL we get:$V_{TH} = I_{BQ} \cdot R_{TH} + V_{BE(ON)} + R_E(B + 1) \cdot I_{BQ}$

$$I_{BQ} = \frac{V_{TH} - V_{BE(ON)}}{R_E \cdot (B + 1) + R_{TH}}$$

Picking $R1 = 82K \; and \; R2 = 15K$ we found all these values as:

- $V_{TH} = 1.855V$
- $R_{TH} = 12.68k$
- $I_{BQ} = 68.2\,\mu A$
- $I_{CQ} = 13.64\,mA$

Now from here let's calculate $r_\pi \; and \; gm$ then we can move on to calculation of the gain. Note that thermal voltage V_T as 26mV

- $r_\pi = \frac{V_T}{I_{BQ}} = \frac{26mV}{47\mu A} = 0.381k\Omega$
- $gm = \frac{B}{r_\pi} = 524.93\frac{mA}{V}$

Now let's look at the small signal model of common emitter part when the push pull buffer is cut off and derive the gain equation.

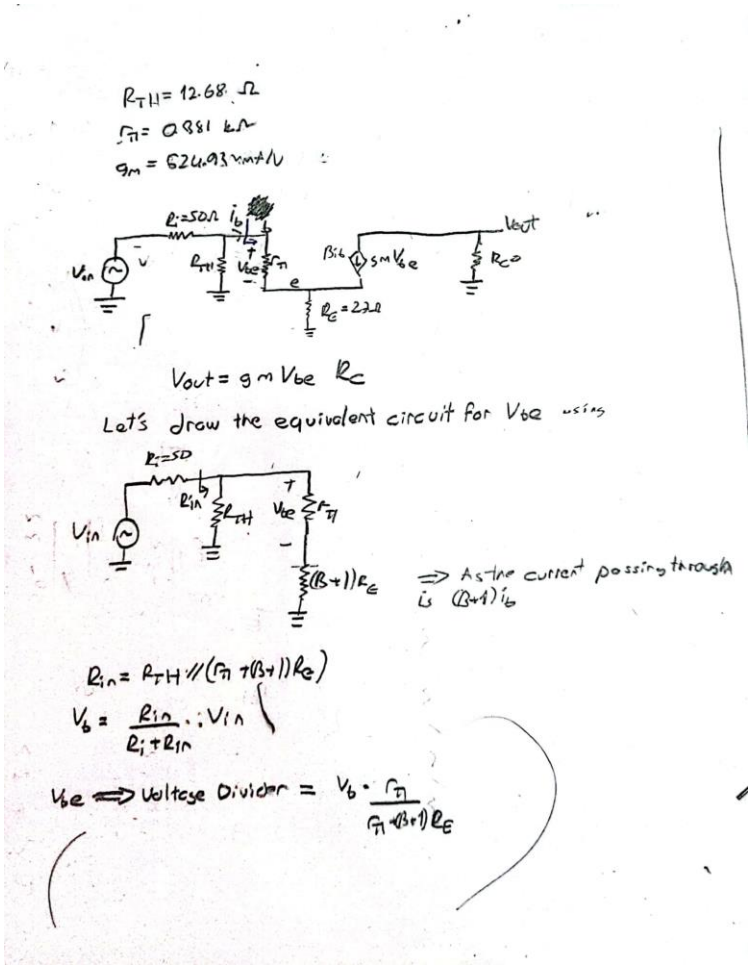

Figure 3: Small Signal Model of Common Emitter

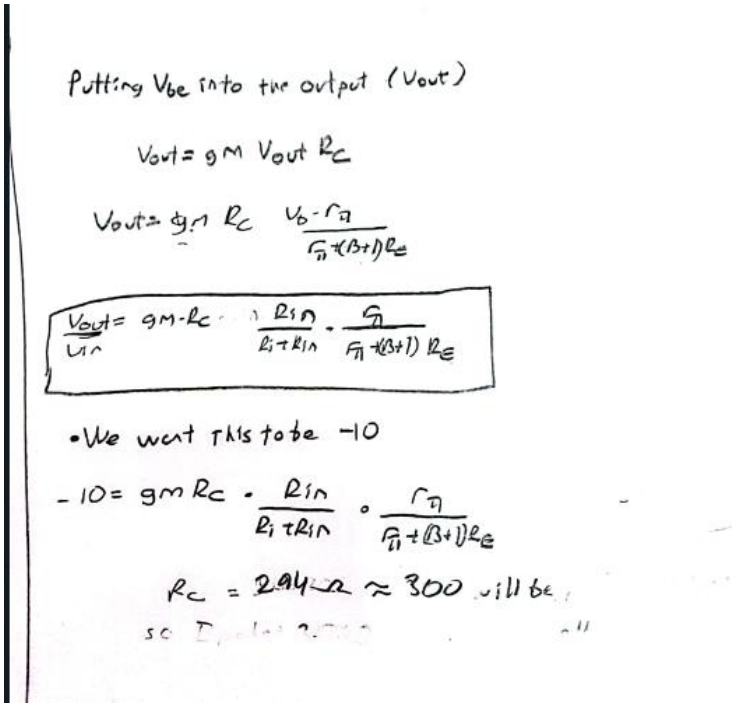

Figure 4: RC calculation from Common Emitter

From the gain equation, which is rewritten below, the only missing value is RC hence RC was found as $R_C \cong 300\Omega$. I picked 330 to be able to use the model in the hardware as well.

$$\frac{Vout}{Vin} = gm \cdot R_C \cdot \frac{r_{pi}}{r_{pi} + (B+1)R_E} \cdot \frac{R_{in}}{R_{in} + R_i}$$

Figure 5: Gain Equation

Now let's show the end circuit and LTSpice simulation:

Figure 6: LTSpice Model of the Circuit

Looking at the gain on the common emitter when C2 is cut off:

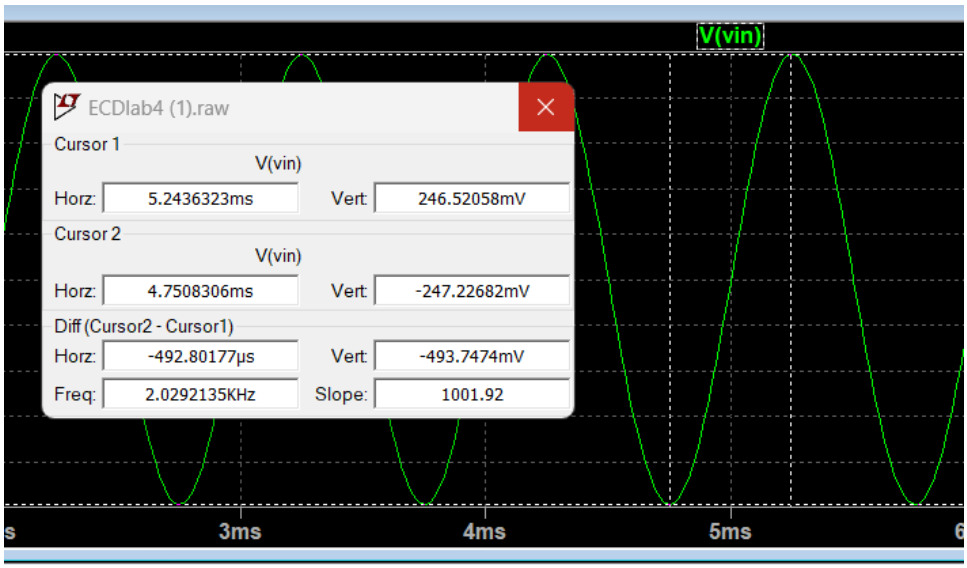

Figure 7: Input Voltage after Ri=50Ω

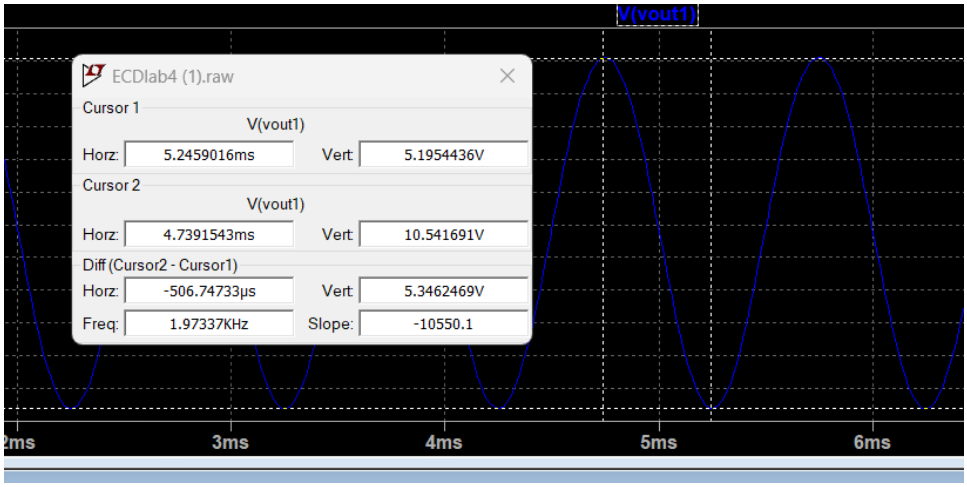

Figure 8: Output Voltage of the Common Emitter

From here we calculate the gain as,

$$\frac{Vout}{Vin} = -10.82$$

Though the gain is higher than 10 it is still within the %10 percent error rate and as I didn't include Ro and picked a different RC value than I supposed to it is to be expected.

Looking at the total gain:

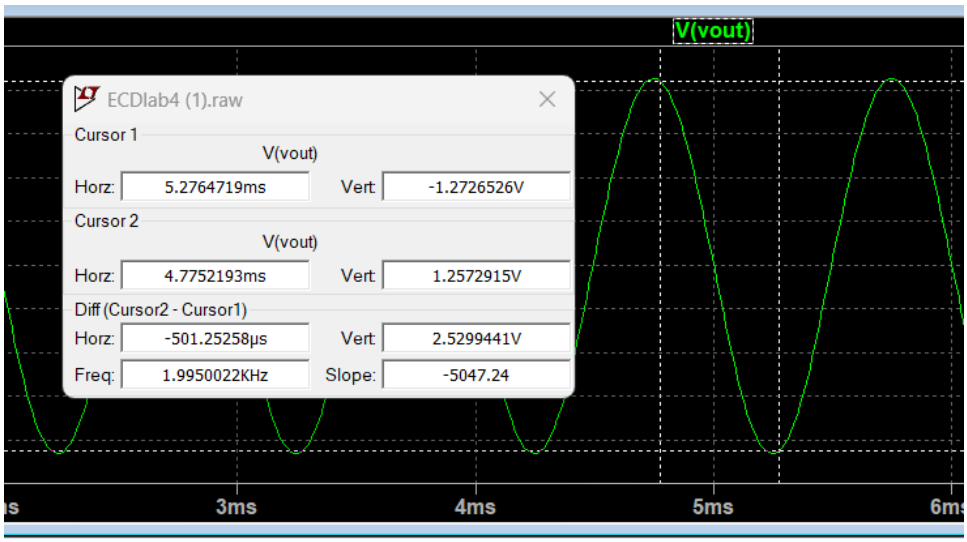

Figure 9: Total Gain

The total gain can be calculated as

$$\frac{Vout}{Vin} = -5.12$$

In this case is error is much less with 2.4%. We can now move on

Resistance seen from right of V1

I decided to pursue an unconventional way for this: Considering the small signal model in figure 3, to be able to have half the gain once the resistor is added there should be a relation between the vouts of the voltage. Hence we calculate the $R_{eq} = 297\Omega$

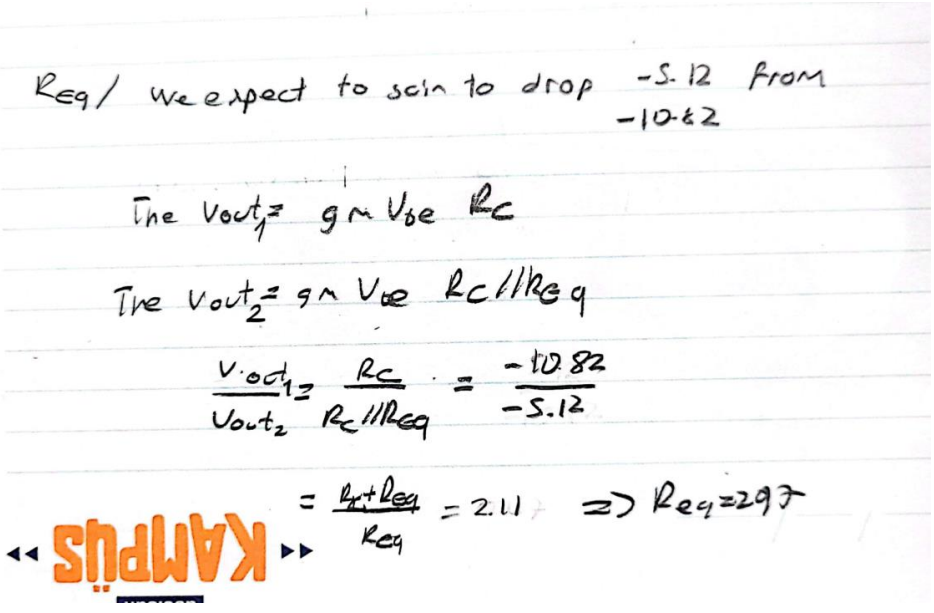

Figure 10: $R_{eq} = 297\Omega$

Input Impedance

Input impedance was calculated in figure 3 as:

$$R_{in} = R_{TH}//(r_\pi + (B+1)R_E) = 3.983k\Omega$$

Output Impedance of the Amplifier

Looking at the small signal model of the amplifier we find $R_{=}156\Omega$

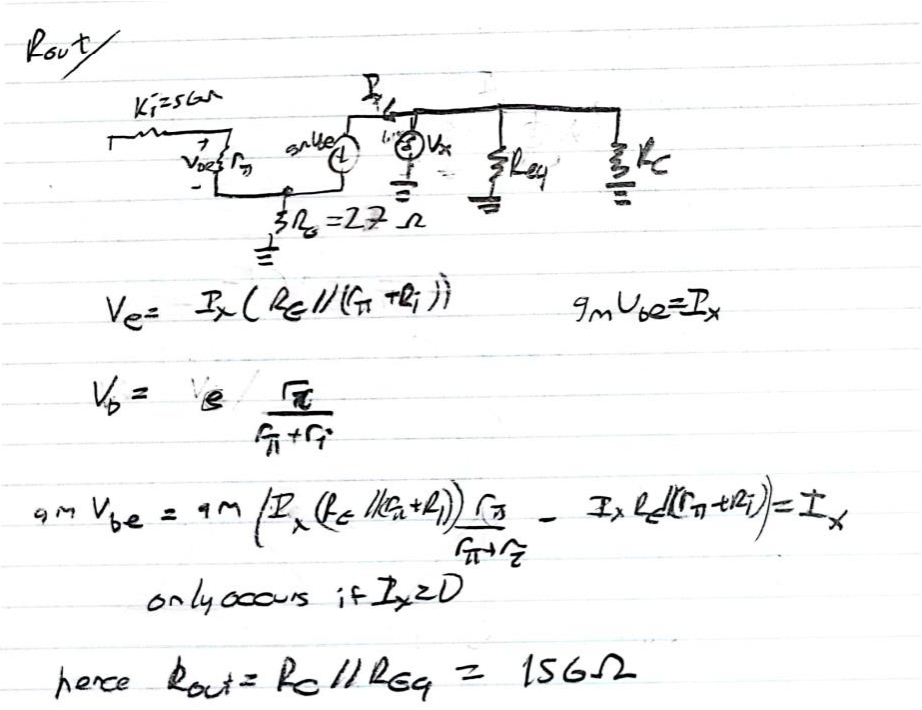

Figure 11: $R_{=}156\Omega$

A2)

In this part C1,C2 and C3 was picked $10\mu F,\ 100uF, 1000uF$. Doing the AC analysis the Magnitude Bode plot was obtained.

We expect $20\log(5) = 13.97Db$ gain.

Looking at the simulation we can see that we get 13.98 DB gain which is extremely close to wanted decibel gain.

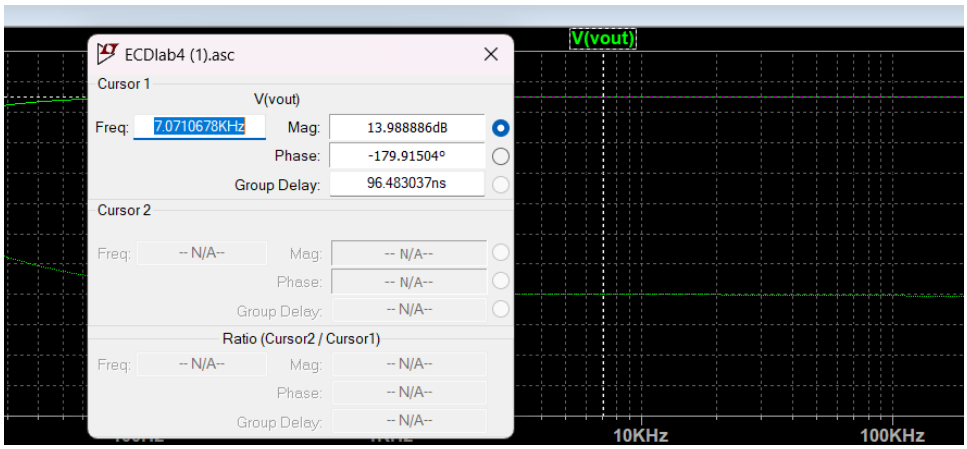

Figure 12: The total DB gain

f_L and f_H values

We will find f_L and f_H at –3dB which means we need to find at which point the gain goes down to 10.98 dB. While f_L is caused by the external capacitors, f_H is decided by internal capacitors of the BJTs.

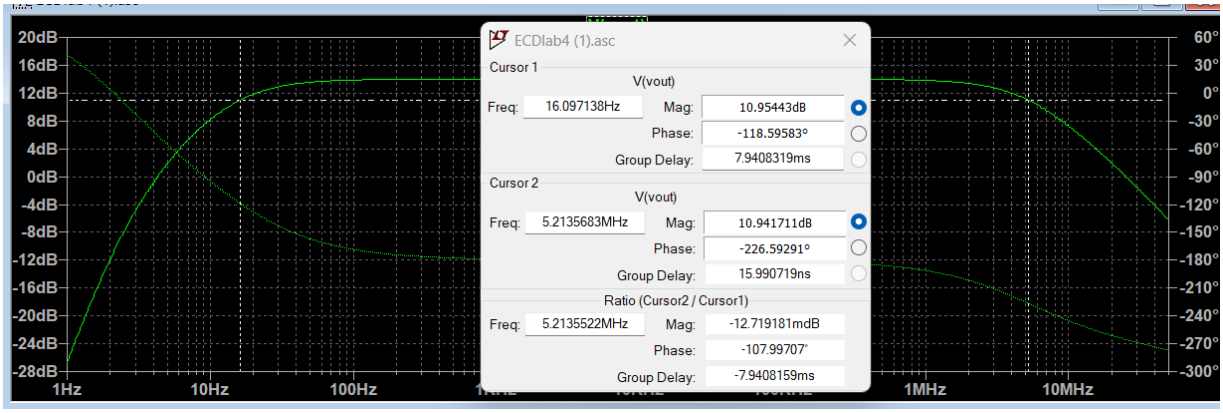

Figure 13: f_L and f_H values

It can be seen that

- f_L: $16Hz$
- f_H: $5.21MHz$

A3)

Purpose of Diodes

Normally a push pull voltage buffer works by activating one BJT at the upcycle of the input and activating the other one when the input reaches the downcycle. For this to occur we need to alter the base voltage to have a diode that is forward active at a longer duration and eliminate disturbances

Essentially the diode connected to base of QBD135 increases V1 by 0.7V, which is diodes' assumed threshold voltage, on the base. The diode connected to QBD136 decreases V1 by 0.7v on its base. As we considered $V_{BE(ON)} = 0.62V$ earlier, by increasing the voltage on the base of the NPN BJT and decreasing the voltage on the base of the PNP BJT we ensure that the BJTs will always stay forward active.

If we shorten the diodes, then we expect to see points where output voltage stays 0 for a while as both of the BJT's are off.

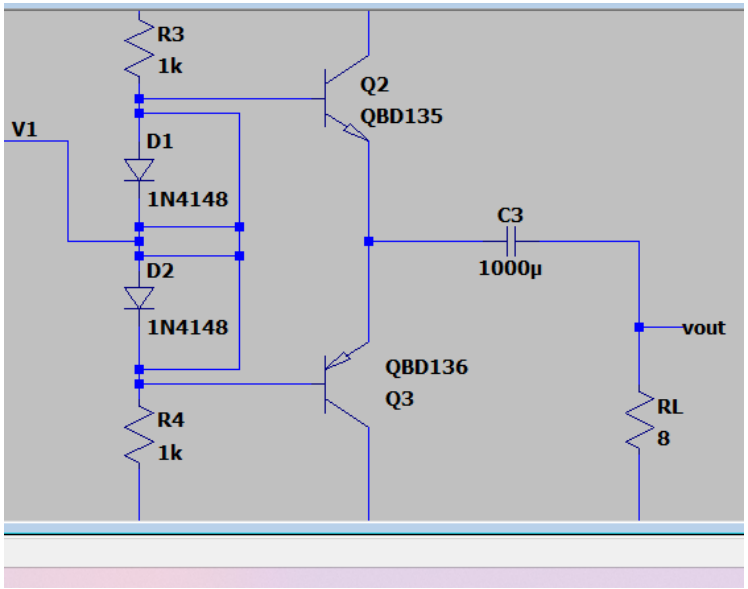

Figure 14: Shorted Circuit

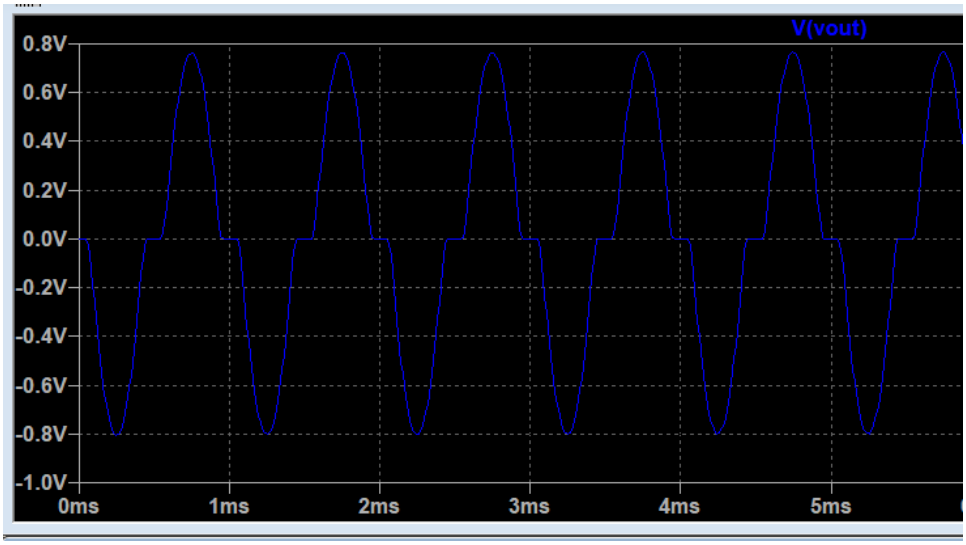

Figure 15: Output voltage when Short-circuited

As expected there are points where both BJT's are off and as a result we get 0Volt in the output.

We can also see this from the current passing through the BJTs.

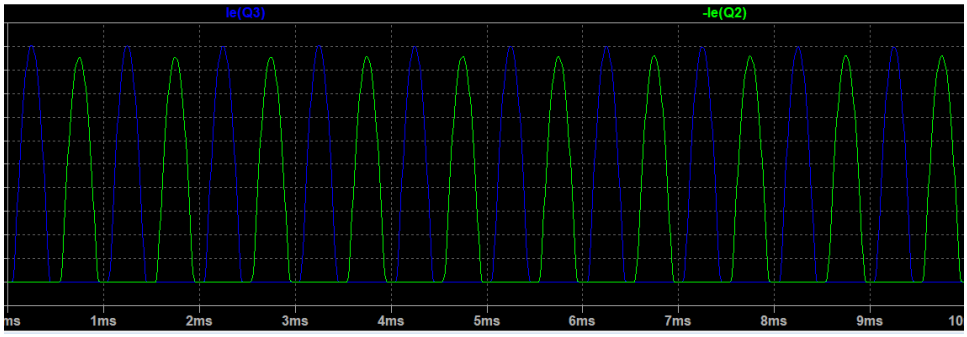

Figure 16: Current Passing through the BJT when Short-Circuited

As there are times where no current passes from both BJT's we will find 0 voltage on the output. In the normal case with diodes there is always a BJT that carries current to the load this can be observed from the figure below

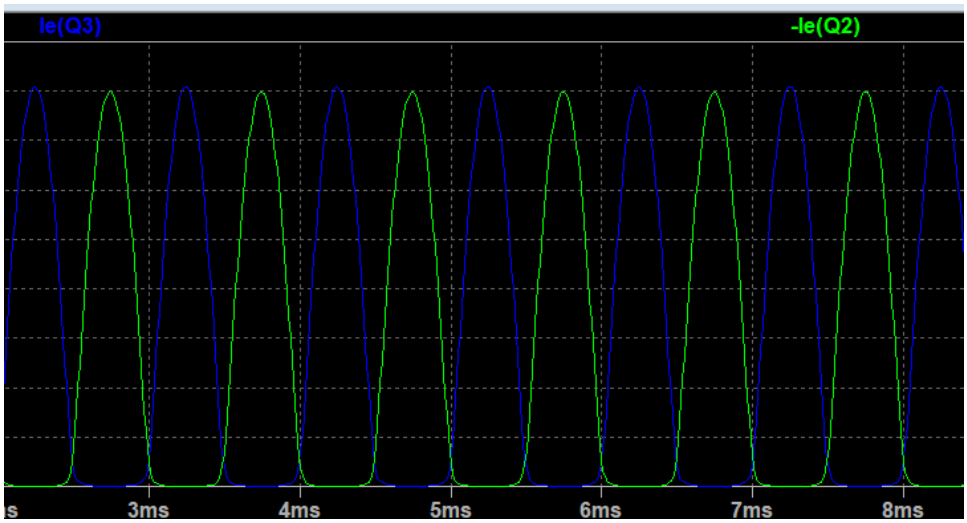

Figure 17: Current Passing through BJT's when Diodes are Connected

Hardware Implementation

Here is the circuit used in the hardware implementation:

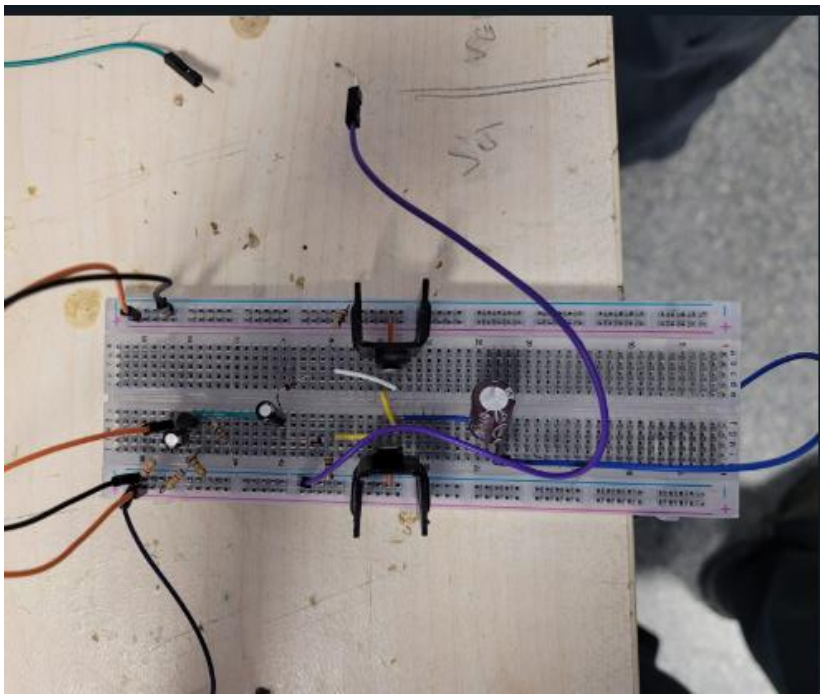

Figure 18: Circuit used in the hardware implementation

Same values were used in the hardware implementation as in the software.

The only change was the 8Ω which was changed to a 7.2Ω resistor.

B1. Q point values

Here are the wanted Q point values according to software simulation, I didn't include all the pictures to not make it overcrowded.

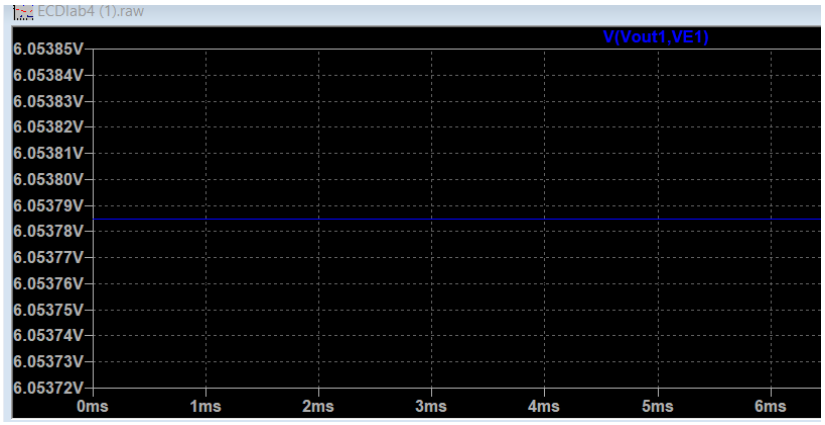

Figure 19: $V_{CE}\ of\ BC238 = 6.05V$

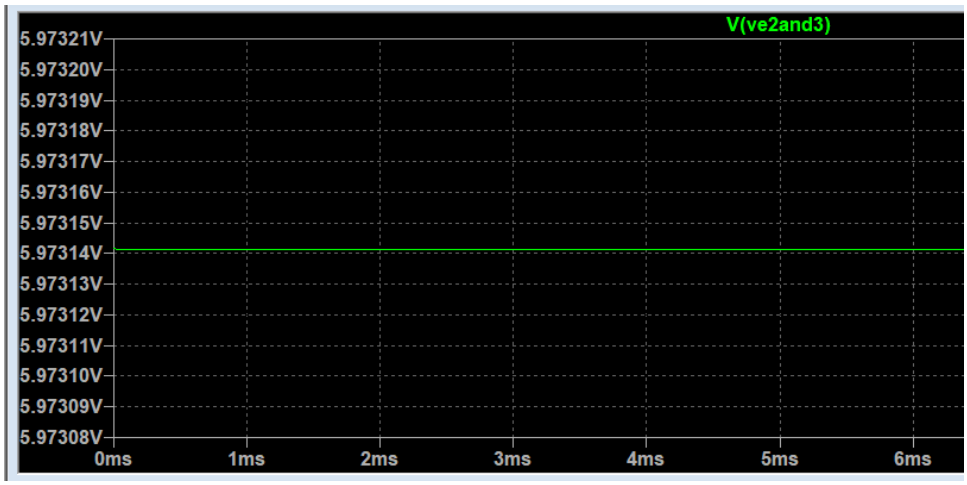

Figure 20: $V_E\ of\ QBDs = 5.97V$

We can calculate V_{CE} of each as 6.03 and 5.97V respectively.

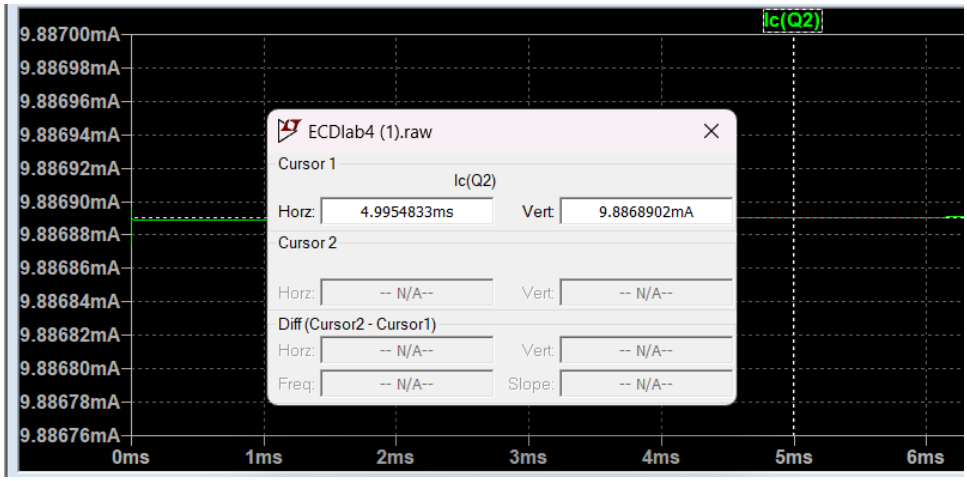

Figure 21: IC2 of NPN QBD135

	Expected	Measured
$V_{CE,1}\ (BC238)$	6.05V	5.77V
$I_{C1}\ (BC238)$	16.65mA	17.39mA
$V_{CE,2}\ (QBD135)$	6.02V	6.15V
$I_{C2}\ (QBD135)$	9.88mA	11.94mA
$V_{CE,3}\ (QBD136)$	5.98V	5.85V
$I_{C3}\ (QBD136)$	9.92mA	11.4mA

Table 1: Measured vs Expected Q point Values

Here is the data for some of the Q point values:

Figure 22: VC and VE of BC238

From here we can calculate $V_{CE1} = 5.77V \; and \; I_{C1} = 17.39mA$ from Ohm's Law

Now looking at Q2 and Q3,

Figure 23: VE2=VE3

We find $V_{CE2} = 6.15V \; and \; V_{CE3} = 5.85V$

Finally the current values,

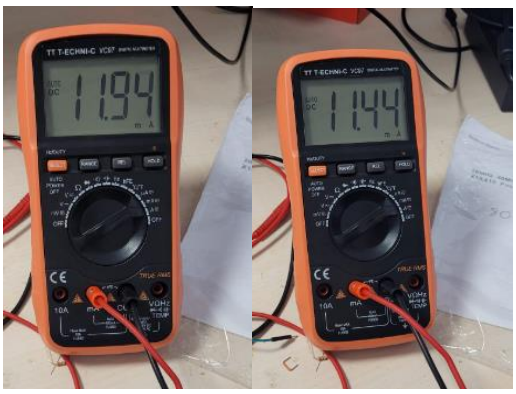

Figure 24: IC2 and IC3

Though the collector currents are a bit high the voltage values I found suggested I was working more or less in the wanted circuit and hence I decided to move on to B2 without making any adjustments

B2)

Gain at 1kHZ when 0.1sinwt is applied:

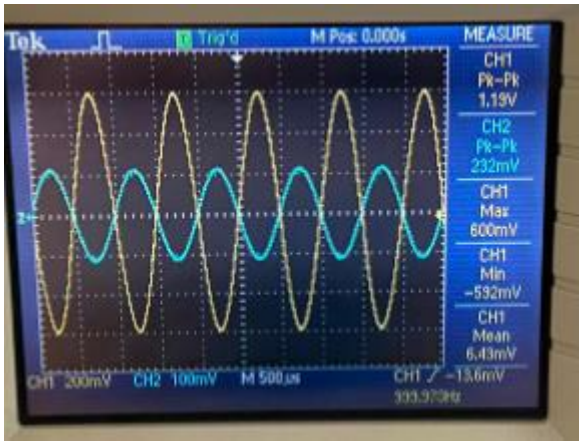

Figure 25: Gain at 1khz

We calculate the gain as $\frac{Vout}{Vin} = \ -5.129$. This is extremely close to what we found in software analysis.

B3)

We found the gain for 0.1sinwt as –5.129. Here is the data for 0.2sinwt, 0.3sinwt, 0.4sinwt, 0.5sinwt

Figure 26: Gain of 0.2 sinwt (left) and gain of 0.3sinwt

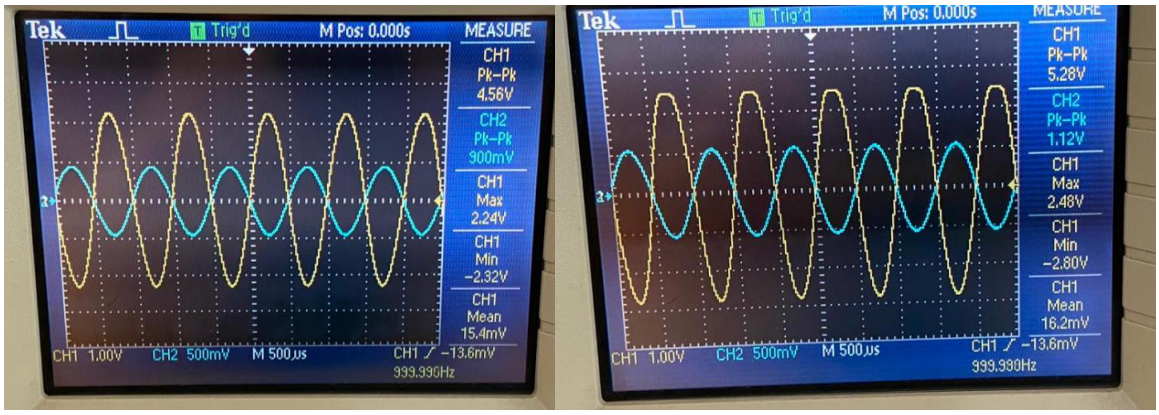

Figure 27: Gain of 0.4sinwt (left) and 0.5sinwt (right)

Note that the signal is saturated for 0.5sinwt

	0.1sinwt	0.2sinwt	0.3sinwt	0.4sinwt	0.5sinwt
Vin	232mV	448mV	680mV	900mV	1.12V
Vout	1.19V	2.36V	3.48V	4.56V	5.28V
Gain	-5.128	-5.326	-5.11	-5.06	-4.71

Table 2: Gains for different amplitudes

Looking at the harmonic content here is a picture from each input's frequency content. Considering the distortion at 0.5sinwt we expect to see most harmonics at this point. We can consider a periodic functions Fourier transform which is an impulse train at the fundamental frequency. Hence, we expect to see impulses around the harmonics.

- 0.1sinwt

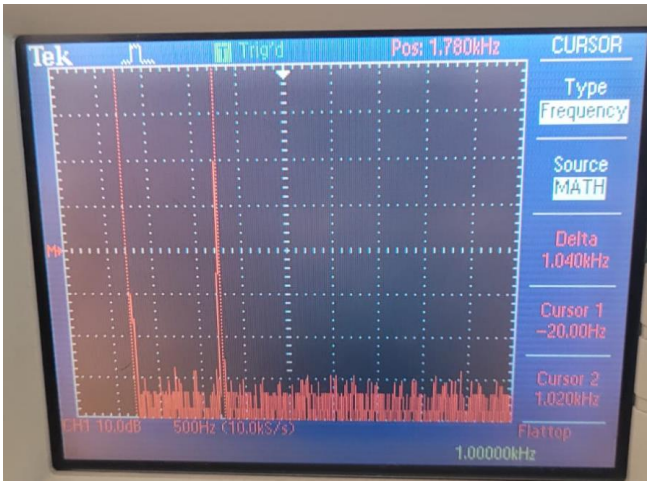

Figure 28: Harmonic content at 0.1sinwt

- 0.2sinwt

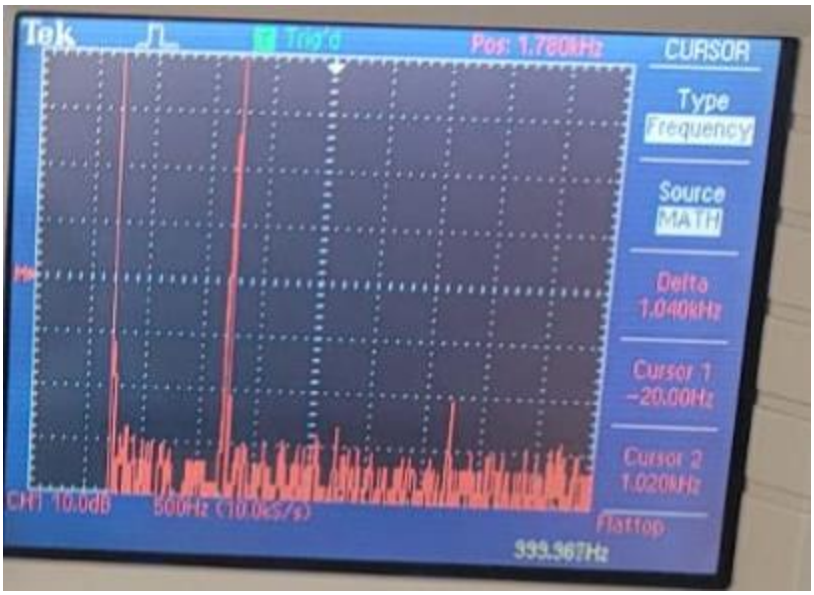

Figure 29: Harmonic content at 0.2sinwt

- 0.3sinwt

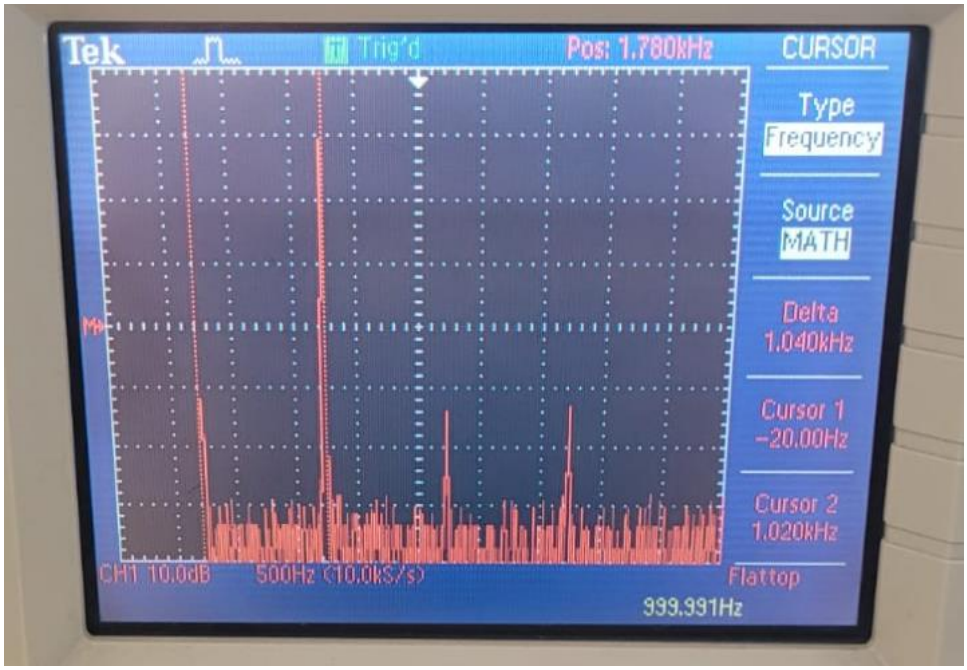

Figure 30: Frequency content at 0.3sinwt

Noting that there is another harmonic at 2kHz and 3kHz.

- 0.4sinwt

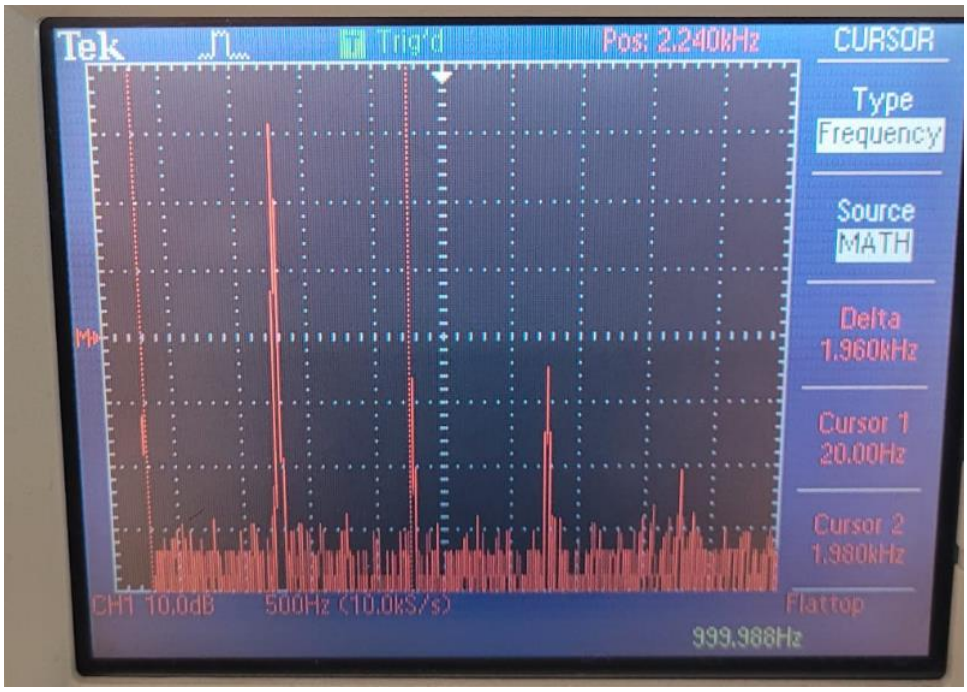

Figure 31: Frequency Content at 0.4sinwt

- 0.5sinwt

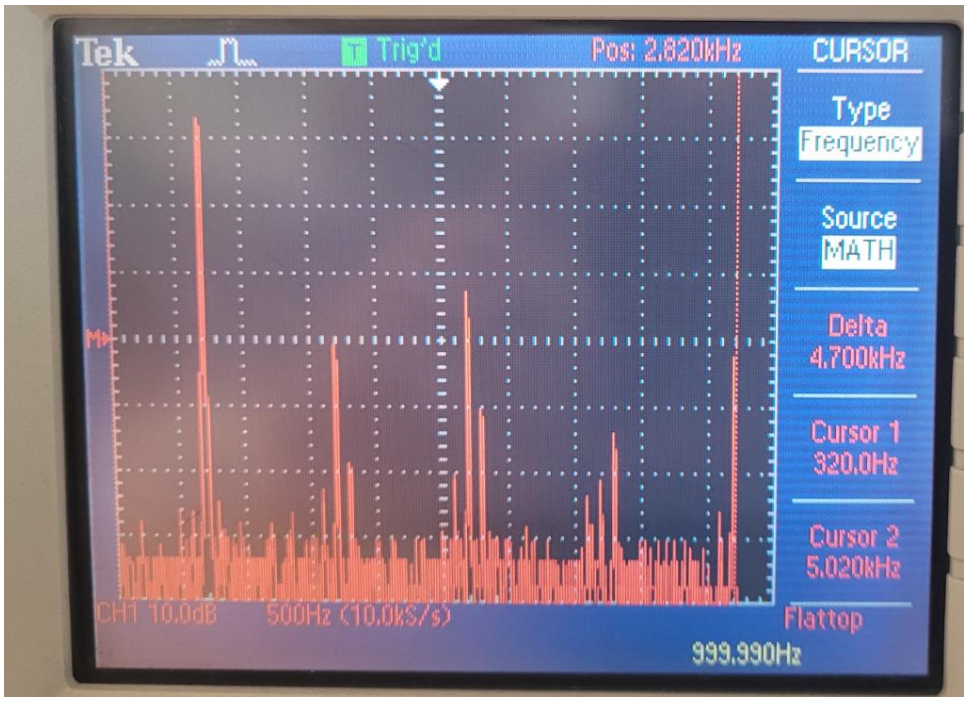

Figure 32: Frequency Content at 0.5sinwt

As we have a saturated signal at 0.5sinwt if consider the saturated part as a periodic square function, it makes sense as the Fourier series coefficients occur at harmonics. This causes the harmonic content to be more distorted as we also don't have proper sinusoidal signal anymore as well which will alter the

frequency domain's behavior. For cases other than 0.5sinwt, one can easily see there is little to no distortion around harmonics. Finally, as the magnitude of the signal was increased the magnitude in the frequency domain increased.

B4) Maximum input without the clip

The input signal stopped clipping at 0.470sinwt.

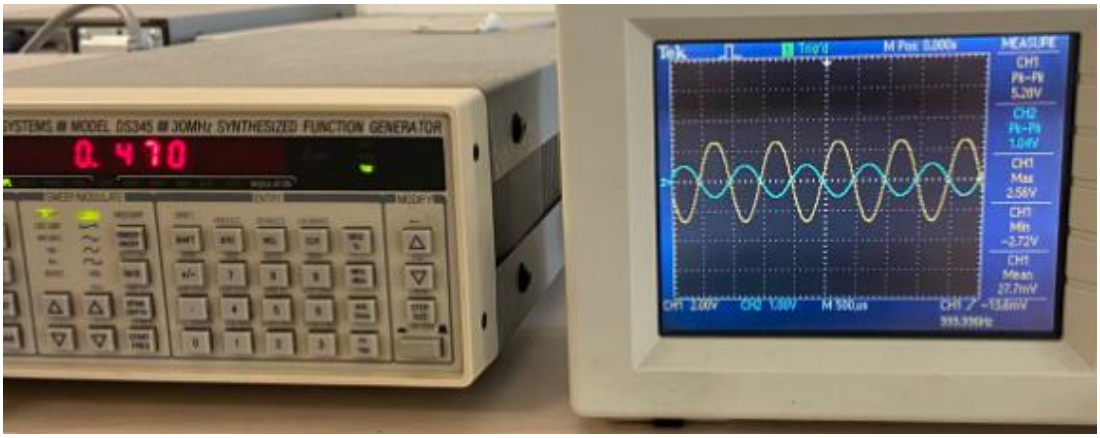

Figure 33: Maximum input without the clip

Gain was –5.074 in this case.

B5) $f_L \; and \; f_H$

To find the $f_L \; and \; f_H$ we need to find the gain for 0.1sinwt as dB and then find the points where the gain is 3db lower than what we have measured.

Then our gain can be measured as $20 \log \left| \frac{Vout}{Vin} \right| = 20 \log(5.128) = 14.2dB$

We are looking for frequencies where gain is around 11.2dB

- f_L

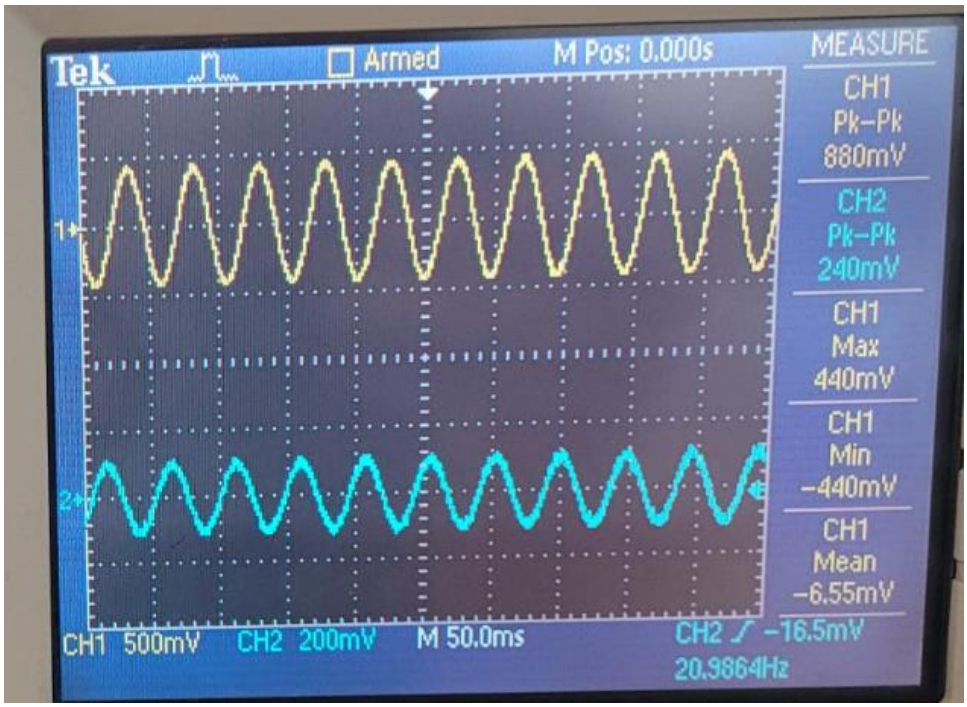

Figure 34: $f_L = 21Hz$

At 21Hz the gain was $20 \log\left(\frac{880}{240}\right) = 11.28dB$ which makes 21Hz a good fit for low frequency cutoff point. It is about 4 Hz higher than the software implementation.

- f_H

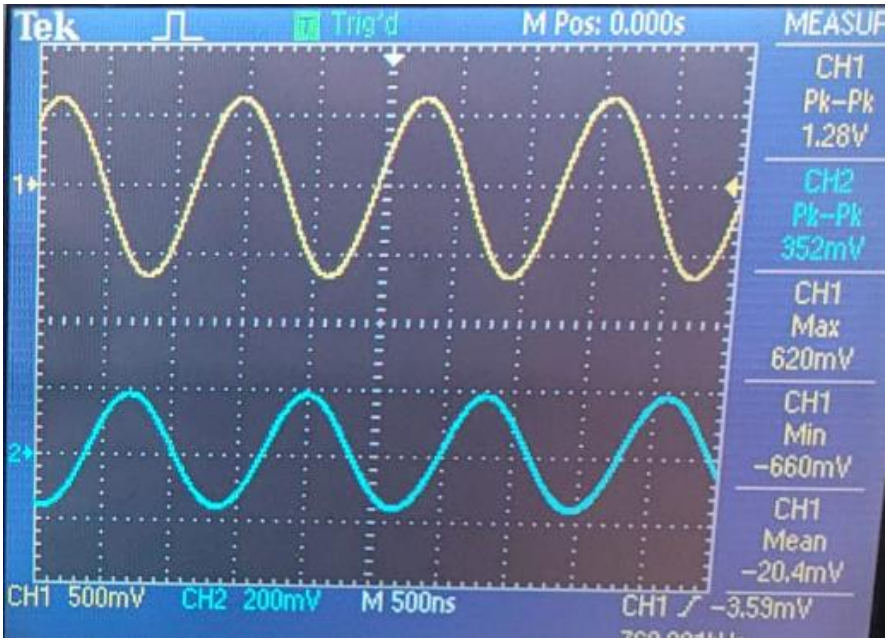

Figure 35 : $f_H = 7MHz$

At 7MHz, the gain was found as$20\log\left(\frac{1.28}{0.352}\right) = 11.20$. However, this value is 1.6MHz higher than what is wanted which could be due to transistors temperature rise as the circuitry is being used.

Here are two values that is outside $f_L \; and \; f_H$ range. We expect to see lower gain.

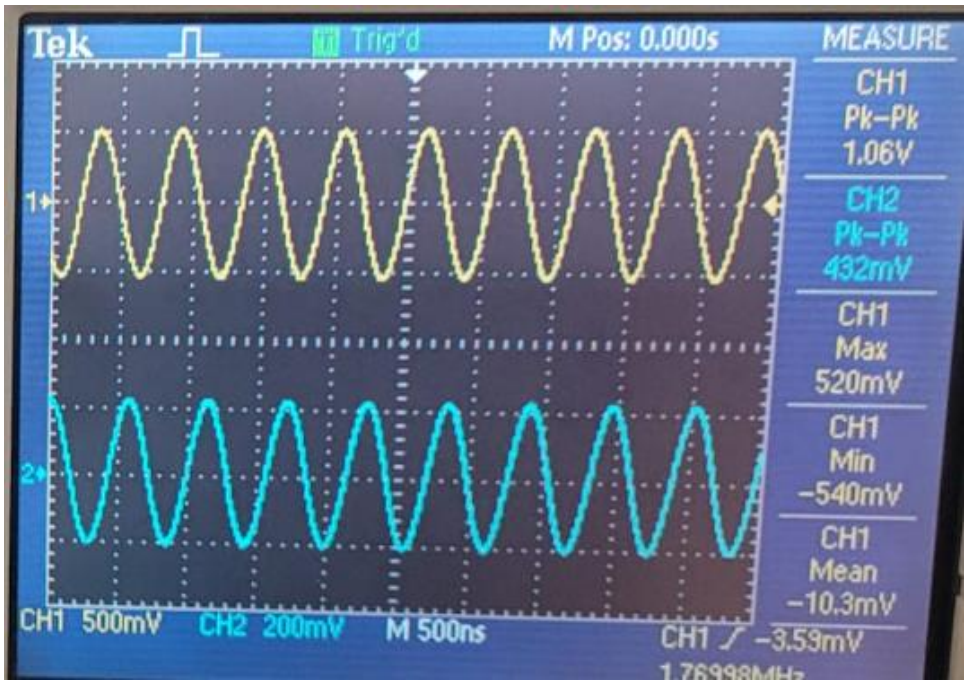

Figure 36: f=17.7Mhz

We find the gain as $20\log\left(\frac{1.06}{0.432}\right) = 7.79dB$

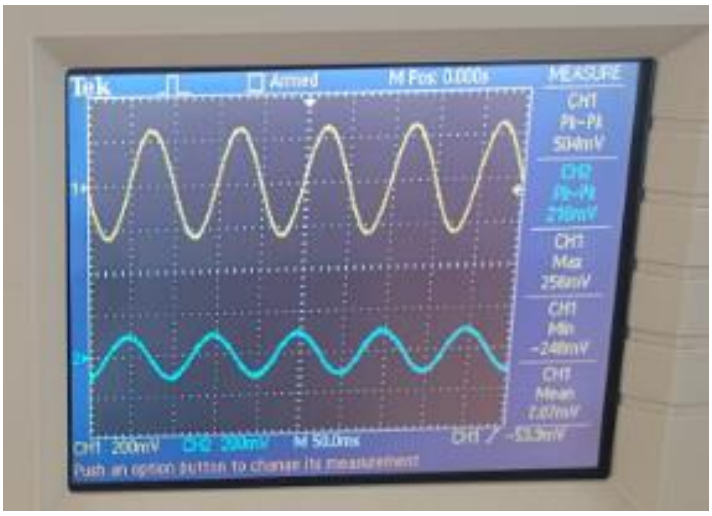

Figure 37: f= 10Hz

We find the gain as $20\log\left(\frac{0.504}{0.216}\right) = 7.35dB$. As expected, the gains were lower as the frequency choices were outside the bandwidth

Conclusion:

In this I learnt the basic behavior of a common emitter amplifier and how to use it with a push pull voltage buffer to create gain within the desired range. To begin with, I learnt how the choice for DC bias affects the overall circuit both when it comes to DC analysis and small signal analysis. One step that was hard in this part was to decide on the actual value of the RC, as considering how looking from the right the resistance seen is 400ohm one should also have RC as 400ohms so that the gain would be halved. However, increasing the RC creates a chance of saturation so it was hard to bias to circuit appropriately. There is also the possibility that the written value given in the hint is not factually correct. Hence, I decided to go other way around and tried several R1 and R2 combinations where I can use a healthy RC choice that was close to ones available in the lab. Yet the Q point values I found were the ones that had the most error, which is mostly due to unavailability to calculate Ro, the resistance of BJT, and BJT's heating as time goes on, which alters the current, DC voltages and small signal analysis

The diodes as a voltage step up and a voltage step down was observed and I realized how changing voltage from one node to other can allow us to observe one signal without turning any of the BJT's off. Otherwise, we need to wait until the base voltage is high or low enough. Moreover, the point off clipping was observed which happened when the BJT was in saturation condition. This clipping also allowed me to observe how much the harmonic content gets distorted by the clipped signal.

Gain wise the circuit worked properly however cutoff frequencies were not really a match which was probably due to capacitance changes in BJT due to heat, this is especially the case for f_H. Forf_L, the mismatch was probably due to nonideal capacitors.