Circuit Theory 202

Lab4

Waveform Generator

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Purpose:

The purpose of this lab is to generate the voltage waveform in figure 1 using OPAMP and RC circuits.

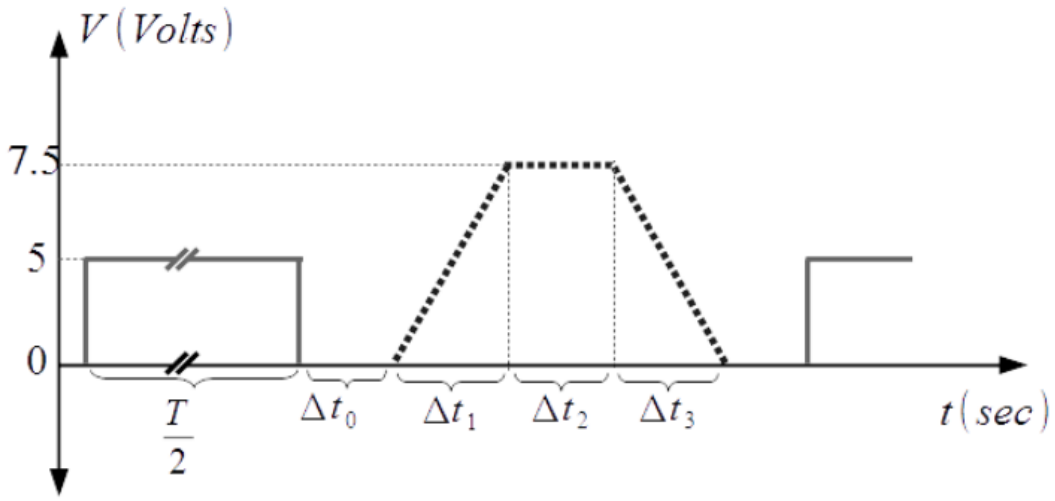

Figure 1: Input in gray line output in dashed line

With the specifications,

$$\Delta t_0 = 3ms, \quad \Delta t_1 = 2ms, \quad \Delta t_2 = 3ms, \quad \Delta t_3 = 2ms$$
Input peak voltage: $5V$
Output peak voltage: $7.5V$
Input frequency: $f < 50Hz, \quad T = \frac{1}{f}$

Figure 2: Lab Specifications

For this lab 20Hz frequency was picked

Methodology:

To begin with let's start by shifting the generated waveform, to be able to create the desired circuit we need to create two waveforms one of which is shifted to right by 3ms while the other one shifted to the right by 10ms(3+2+3+2ms). Throughout the design LM324 OPAMP is used.

Inputs for the OPAMP are,

Vcc+ = 9Volts

Vcc- = 0V

Vcomp = 2.5V

Vinput = 5 Volt Pulse with 20Hz frequency

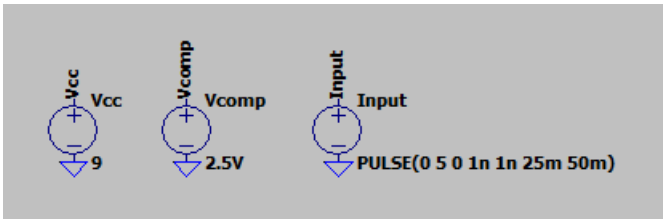

Figure 3: Used Voltages

To be able to create the shifts we need, a delay circuit is needed to be used in the lab. For this purpose, a comparator OPAMP circuit can be used. As can be seen in figure 2 and 3, V_- has the threshold voltage that is Vcomp and V_+ has the RC circuit. Comparator's working mechanism is when input (V+) is higher than the reference voltage, the OPAMP is positively saturated,

whereas if input is smaller than the reference voltage, the OPAMP will be negatively saturated. Considering comparator's working principle we need to find out when the V+ will surpass the reference voltage (Vcomp).

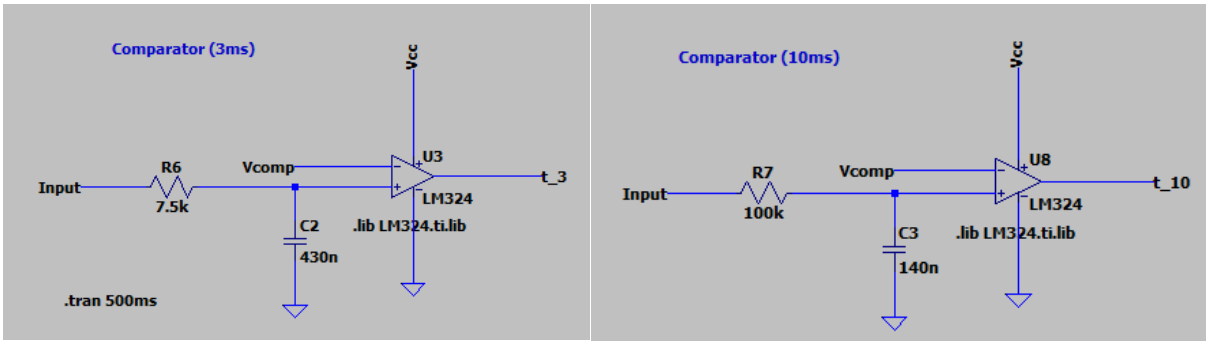

Figure 4 &5 : 3ms and 10ms Comparator Delay Circuit

As can be seen in figure 4 and 5, V_- has the threshold voltage that is Vcomp and V_+ has the RC circuit.

The calculations concerning this circuit are on the node between resistor and capacitor:

$$\frac{dV_c}{dt} * C = \frac{V_{inp} - V_c}{R}$$

$$\frac{dV_c}{dt} * C + \frac{V_c}{R} = \frac{V_{inp}}{R}$$

To find the natural response we start from the characteristic equation:

$$\lambda C + \frac{1}{R} = 0$$

$$\lambda = -\frac{1}{C * R}$$

$$V_{cnatural} = b_1 * e^{-\frac{t}{R*C}}$$

Using Undetermined Coefficient method we can find the forced response in such case our bases is

{A}

Inserting this into the equation we get,

$$\frac{A}{R} = \frac{V_{inp}}{R}$$

$$V_{cforced} = V_{inp}$$

Considering V_{inp} is 5 volts and at t = 0, V_c = 0V we can say that,

$$b_1 = -5$$

From here we get V_c as,

$$V_c(t) = -5e^{-\frac{t}{R*C}} + 5$$

As we are trying to create a 3ms and 10ms delay, V_+ (V_c) should pass 2.5V volts respectively at 3ms and 10ms. Inserting these time values into the equation we have found we get,

$$R_1 * C_1 = 0.0043 \text{ for 3ms}$$

- R_1 = 10kΩ
- C_1 = 430nF

$$R_2 * C_2 = 0.0144 \text{ for 10ms}$$

- R_2 = 1kΩ
- C_2 = 420nF

Due to comparator, OPAMPs will only work on saturation voltages 9V and 0V.

The next step is to turn these square voltage outputs to trapezoids, that is to say that we should create the suitable rise and fall time for the circuit. As it is known that integrator OPAMP triangulates a square waveform we can benefit from that to create rise and fall times that we need.

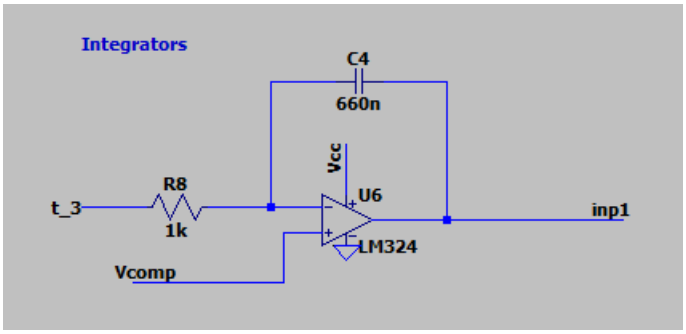

Fig 6: Integrator Opamp for first wave

To be able to create 2ms rise and fall time lets start off by doing KCL on the V^- node.

$$\frac{V_{input} - V^-}{R} = C\frac{dV_c}{dt}$$

$$\frac{V_{input} - V^+}{RC}dt = dV_c$$

Let's take integral on both sides,

$$\frac{V_{input} - V^+}{RC} * t + B = V_c$$

B= 0 as Vc = 0 at t=0,

$$\frac{2.5}{RC} * t = V_c$$

At t=2ms, the Vc has to be 7.5Volt as we need output voltage to be 7.5volts.

$$\frac{1}{RC} * 2ms = 3$$

$$RC = 6.666 * 10^{-4}$$

- For R I have picked 1kΩ
- For C I have picked 660nF

As both integrators are in need of 2ms rise and fall time I used the same values on both integrators.

Now we have two waveforms in our hands with 2ms rise and one of them is shifted 3ms while the other one is shifted 10ms. To be able to achieve the final waveform, we need to find a way to subtract these waveforms from each other allowing us to achieve our aim. For that I used a subtractor OPAMP.

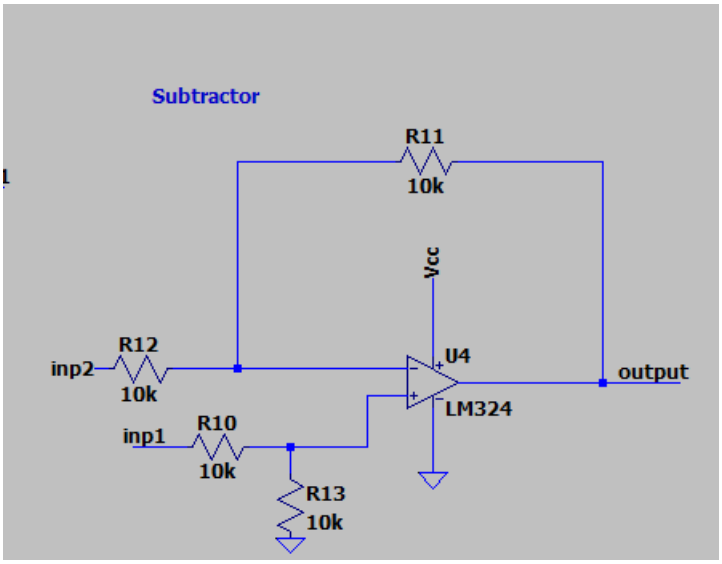

Fig 7: Subtractor OPAMP

Using node equations V^- we get,

$$\frac{Inp2 - V^-}{R_{12}} = \frac{V^- - V_{out}}{R_{11}}$$

$$V^- = (\frac{Inp_2}{R_{12}} + \frac{V_{out}}{R_{11}}) * \frac{R_{11} * R_{12}}{R_{11} + R_{12}}$$

Using Node Equations in V^+ we get,

$$\frac{Inp1 - V^+}{R_{10}} = \frac{V^+}{R_{13}}$$

$$V^+ = \frac{Inp1}{R_{10} * (R_{10} + R_{13})} * (R_{10} * R_{13})$$

Knowing $V^+ = V^-$ we have,

$$\frac{Inp1}{R_{10} * (R_{10} + R_{13})} * (R_{10} * R_{13}) = (\frac{Inp_2}{R_{12}} + \frac{V_{out}}{R_{11}}) * \frac{R_{11} * R_{12}}{R_{11} + R_{12}}$$

If all resistors have the same value we will have:

$$Inp1 - Inp2 = V_{out}$$

Now our circuit is finally ready for use

Software Result:

With all the preparation done in methodology here is the resulting circuit and its results. To reduce error caused by 3ms comparator circuit, I have replaced 10k ohm with 7.5k ohm.

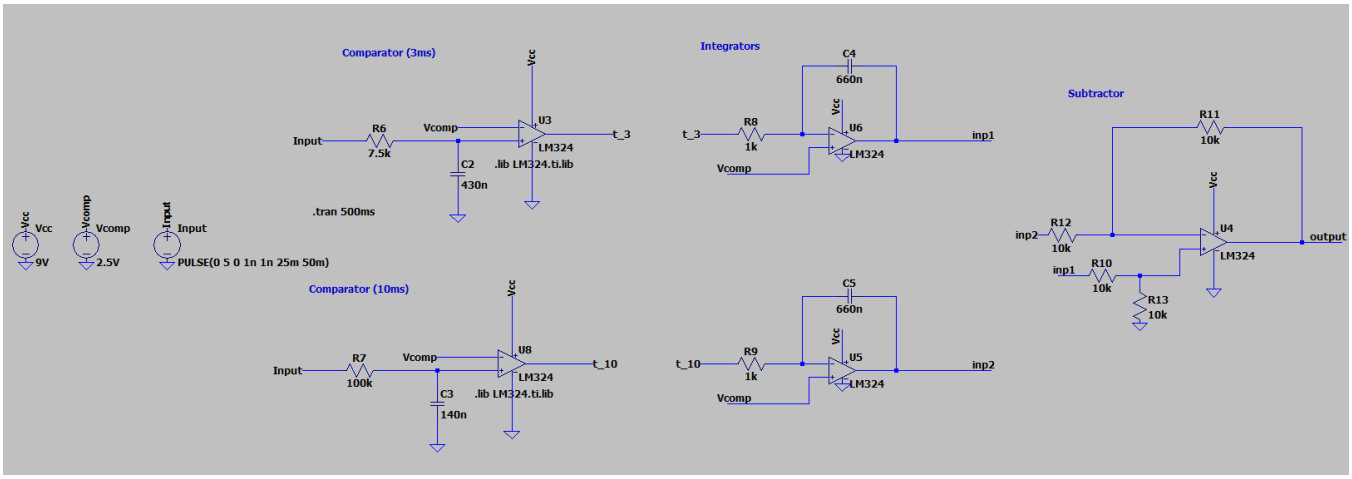

Fig 8: Waveform Generator Circuit

- **Comparator Delays**

Now after the main part is over let's show that comparators are working,

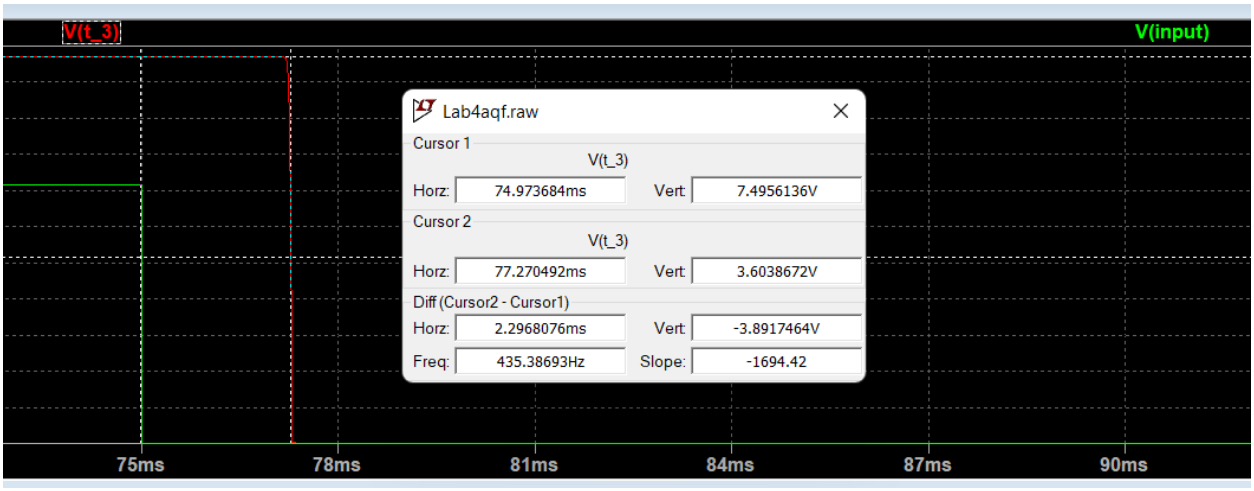

Fig 9: 3ms Delay from comparator 1=2.30ms

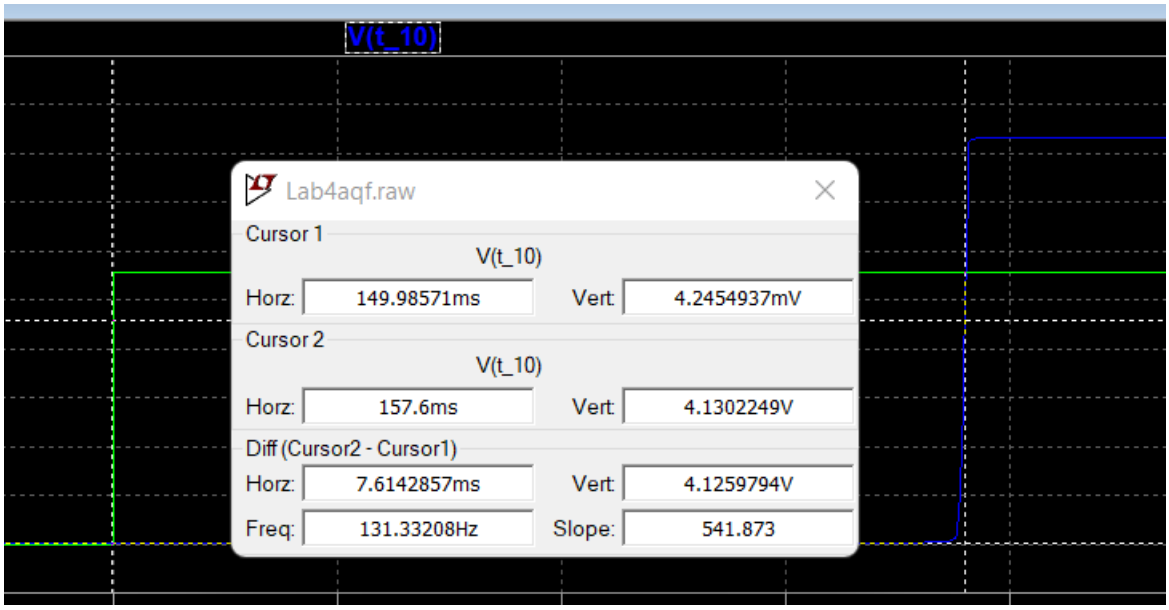

Fig 10: 10ms delay from comparator 2 = 7.61ms

The reason why we are not getting the expected values will be explained in the conclusion.

- **Integrator**

Let's show that we have 2ms rise time.

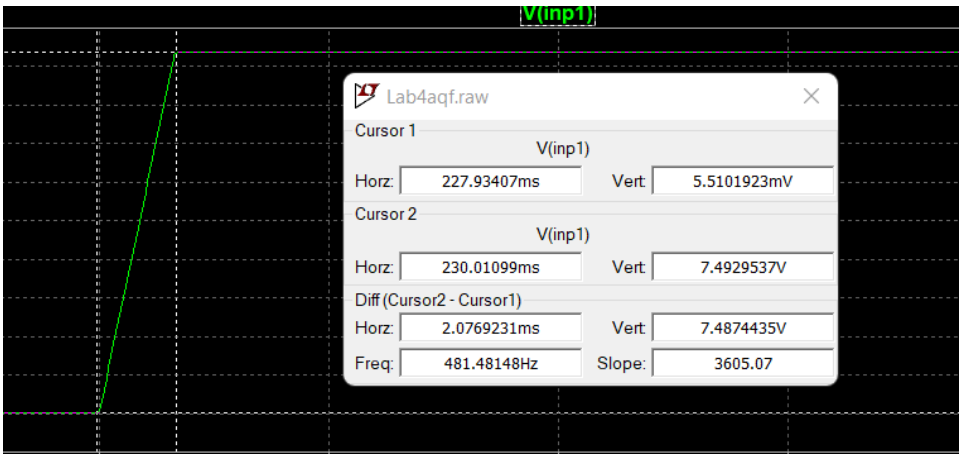

Fig 11: 2ms rise time = 2.07ms for inp1

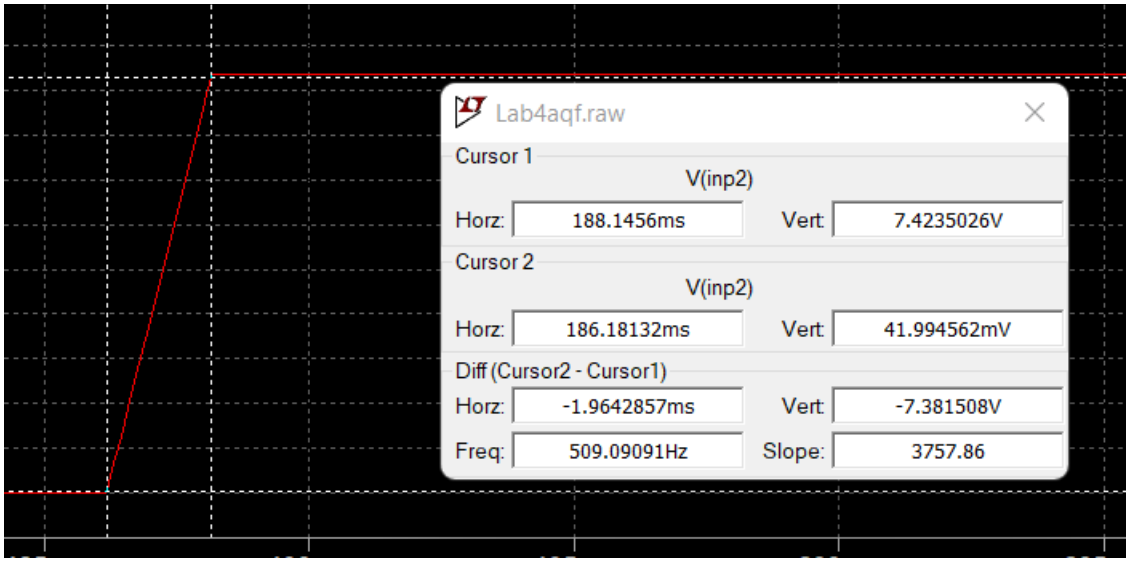

Fig 12: Rise time of 1.96ms in inp1

The fall time is lower normally. However, it is not a problem with the help of subtractor circuit. As subtractor circuit I did subtracts the rise times from each other.

- Subtractor

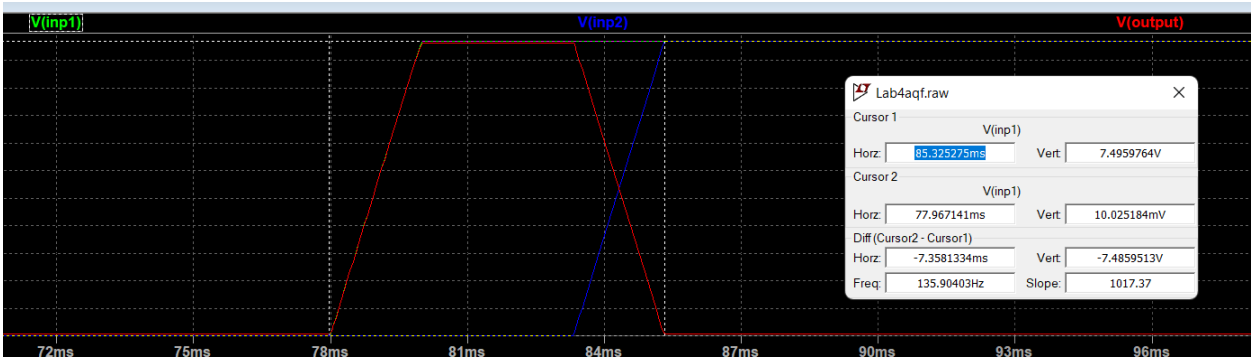

Fig 13: Subtractor Circuit on rise time= 7.35ms

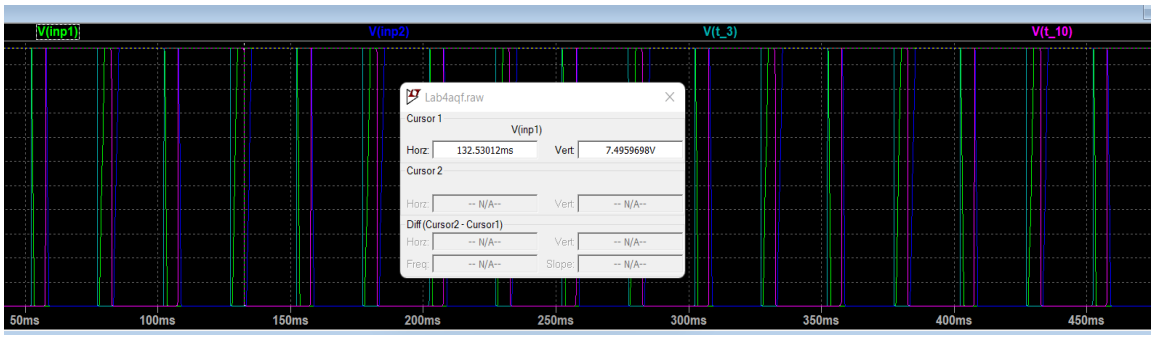

Fig 14: 7.49 Volts on 4 OPAMPs up to now

- **Final results**

Fig 14: Δt0=2.98ms

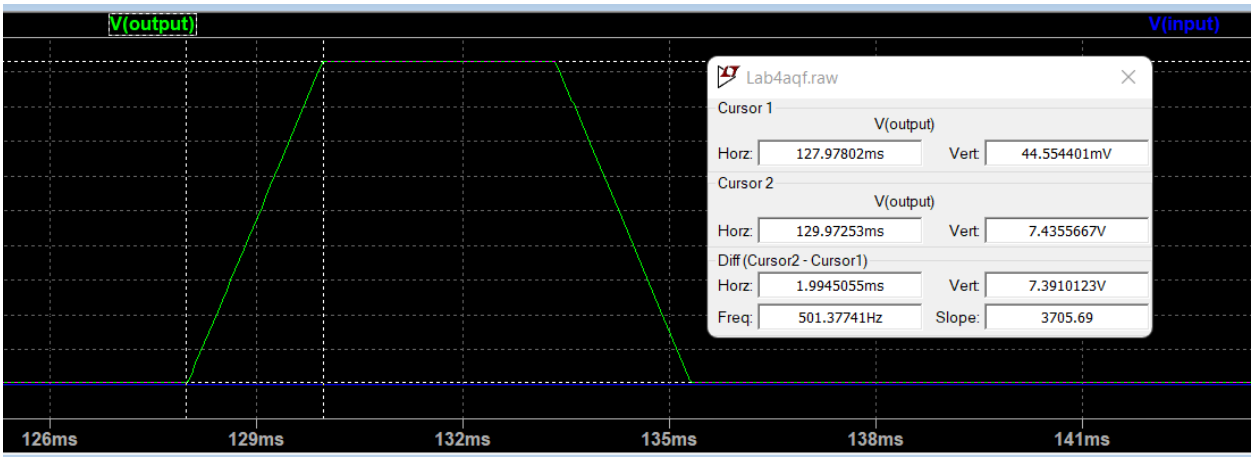

Fig 15: Δt1= 1.99ms

Fig 16: Δt2=3.29ms

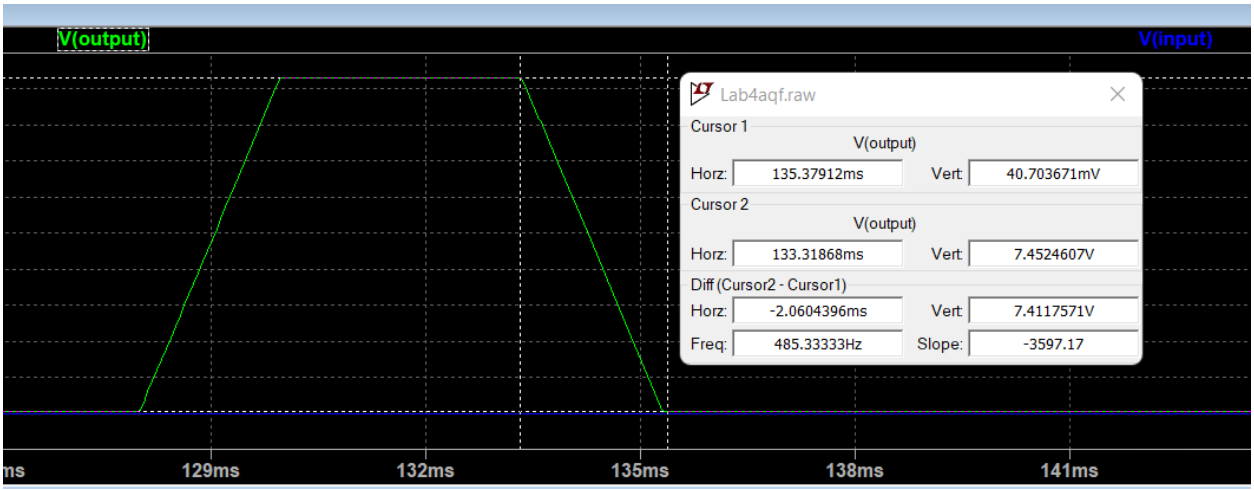

Fig 17: Δt3= 2.06ms

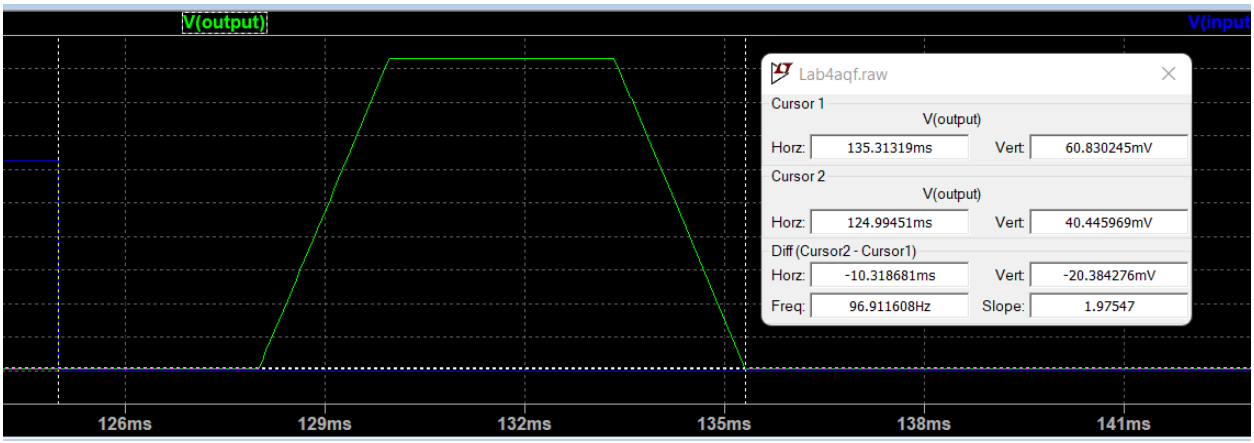

Fig 18: Δt_{total} = 10.31ms

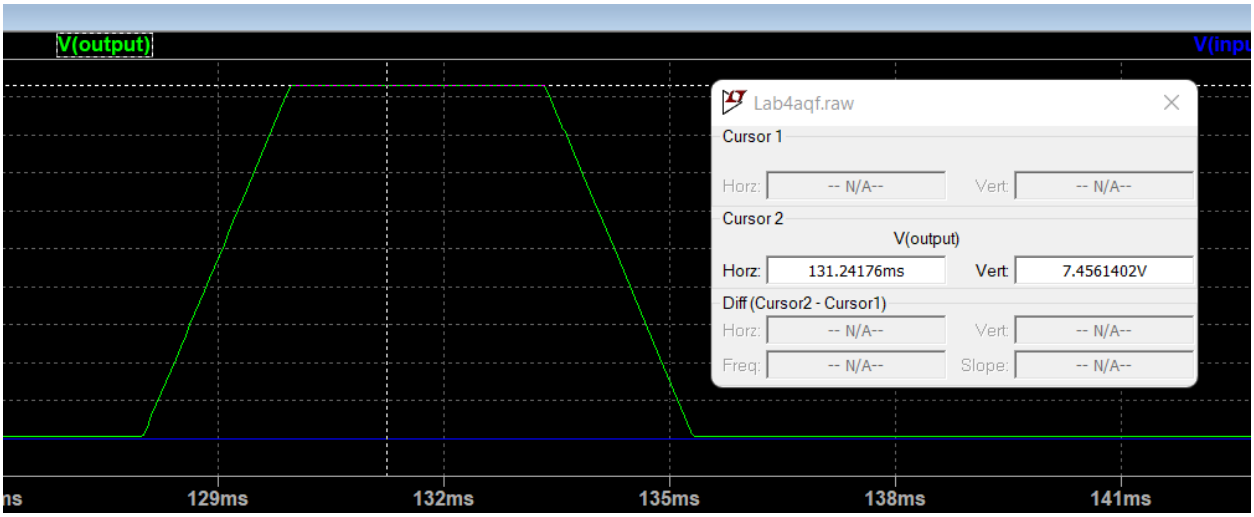

Fig 19: V_{output}=7.45V

	Δt0	Δt1	Δt2	Δt3	Δt_{total}	Voltage
Expected	3ms	2ms	3ms	2ms	10ms	7.5V
Results	2.98ms	1.99ms	3.29ms	2.06ms	10.31ms	7.45V
Error	0.6%	0.5%	9.67%	3%	%3.1%	0.6%

Table 1: Results of waveform

Hardware Results:

The specifications of hardware is as follows:

- Vinp=2.5 Sinusodial Vpp with 20Hertz frequency
- V_{offset}= 1.25 Volt for the circuit system so that the any discrepancy caused by the OPAMPs are eliminated and voltage is carried to the positive side.
- V_{cc}^{+}= 9V and V_{cc}^{-}= 0V
- Vcomp= 2.55V

Fig 20 a&b: Vcc values

Fig 21 a,b,c: Frequency, Voltage and Offset

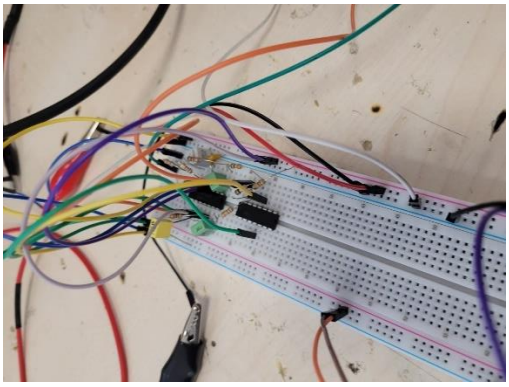

Fig 22: Implemented Circuit

There were also some changes made in the circuit as to create more accurate output, most of the changes are changes regarding the closest standard values.

- 3ms Comparator
- 7.5kohm -> 7.2k
- 430nF -> 420nF
- 10ms Comparator
- 140nF -> 150nF
- Integrators
- The capacitors were initially 680nF however after finding the total duration longer than the wanted range I have reduced them into 560nF.

Now let’s start off with the 3ms comparator and go one by one,

3ms Comparator

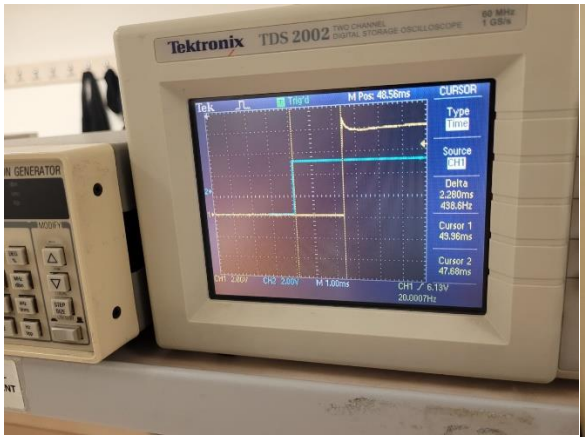

Fig 23a: 2.28ms delay

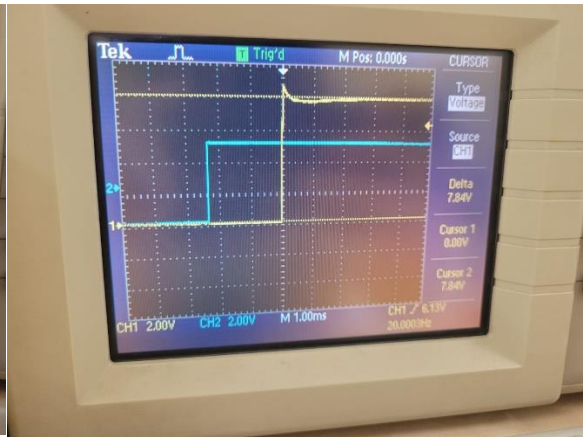

Fig 23b: 7.84V output

	Software	**Hardware**	**Error**
Delay	2.30ms	2.28ms	0.86%
Voltage	7.49V	7.84V	4.67%

Table 2: 3ms Comparator Values

10ms Comparator

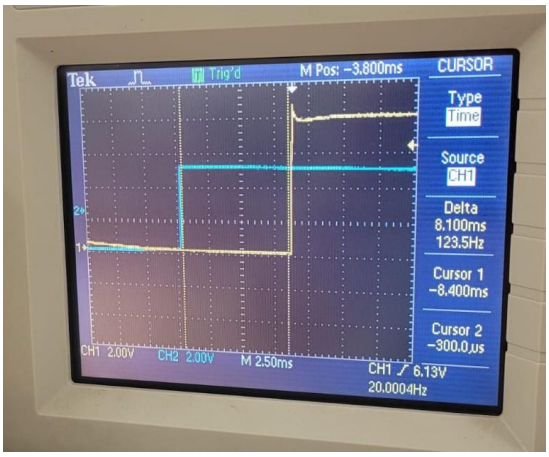

Fig 24a: 8.1ms delay

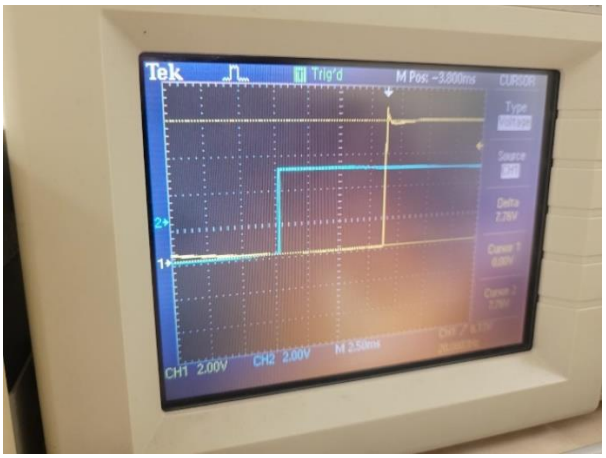

Fig 24b: 7.76V output

	Software	**Hardware**	**Error**
Delay	7.61ms	8.1ms	6.43%

Voltage	7.49V	7.76V	3.6%

Table 3: 10ms Comparator Values

Integrators

- Both integrators had the same voltage.

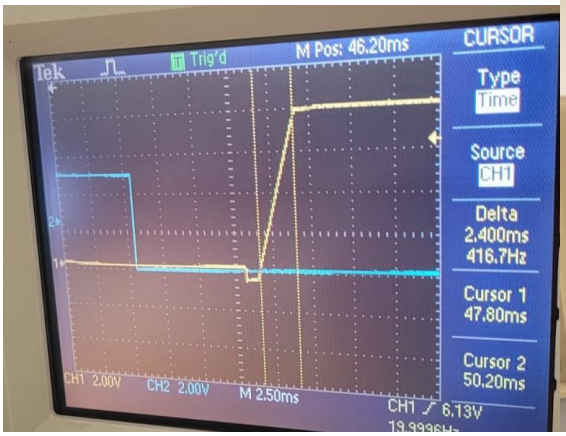

Fig 25a: 2.4ms rise time (from 3ms comp.)

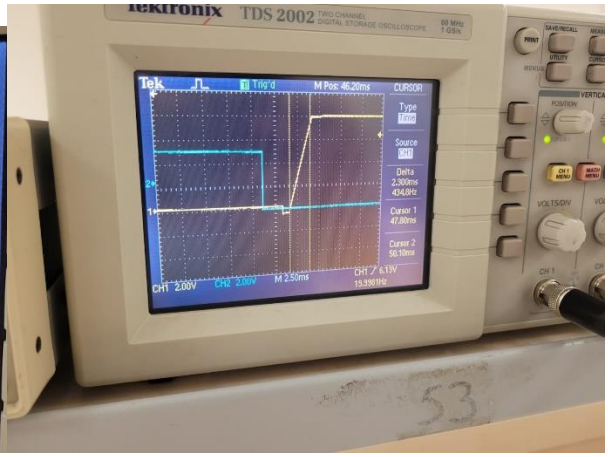

Fig 25b: 2.3ms rise time (from 10ms comp.)

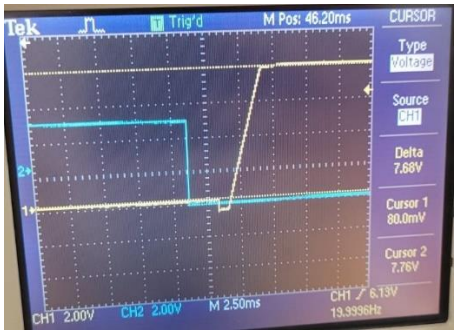

Fig 25c: 7.68V

	Software	**Hardware**	**Error**
Rise time(Comp 3ms)	2.07ms	2.4ms	15.94%
Rise Time(Comp 10ms)	1.96ms	2.3ms	17.3%
Voltage	7.49V	7.68V	2.53%

Table 4: Integrator Values

Resulting Circuit after the Subtractor Opamp

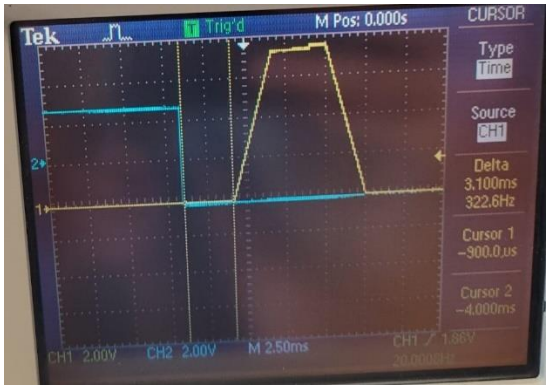

Fig26: Δt0=3.1ms

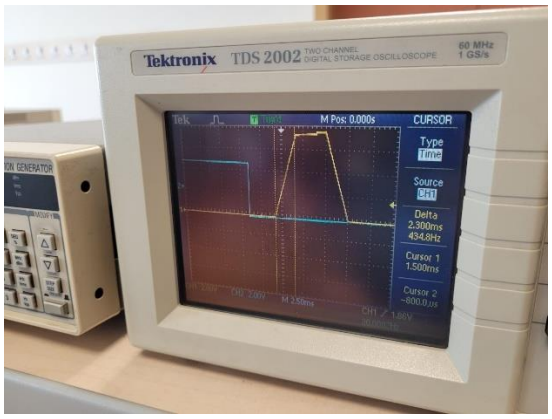

Fig 27: Δt1=2.3ms

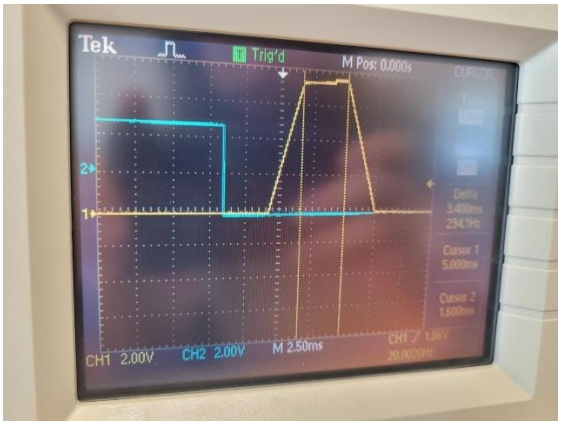

Fig 28: Δt2= 3.4ms

Fig 29: Δt3 = 2.4ms

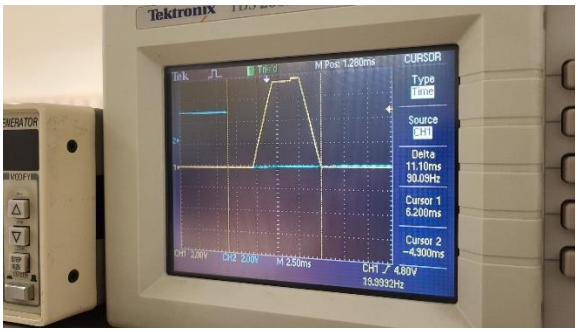

Fig30: Δt_{total} = 11.10ms

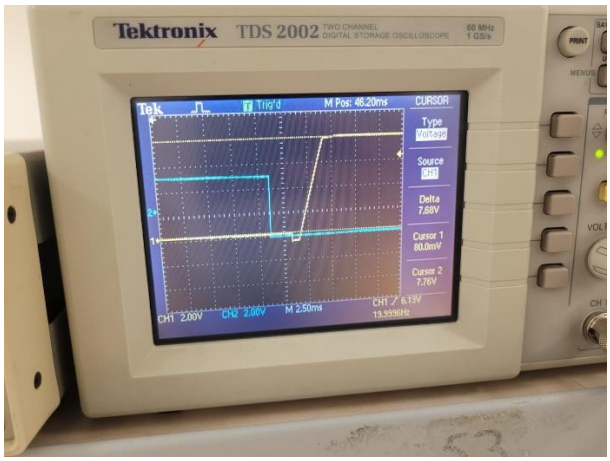

Fig 31: V_{final}= 7.68V

	Δt0	Δt1	Δt2	Δt3	Δt_{total}	Voltage
Expected	3ms	2ms	3ms	2ms	10ms	7.5V
Results	3.1ms	2.3ms	3.4ms	2.4ms	11.1ms	7.68V

Error	3.33%	15%	13.3%	20%	11%	2.4%

Table 5: Outputs Value

- Final Remark on Hardware

As we have picked 2.55V as Vcomp we should expect the integration to start around that voltage which can be seen in fig 32.

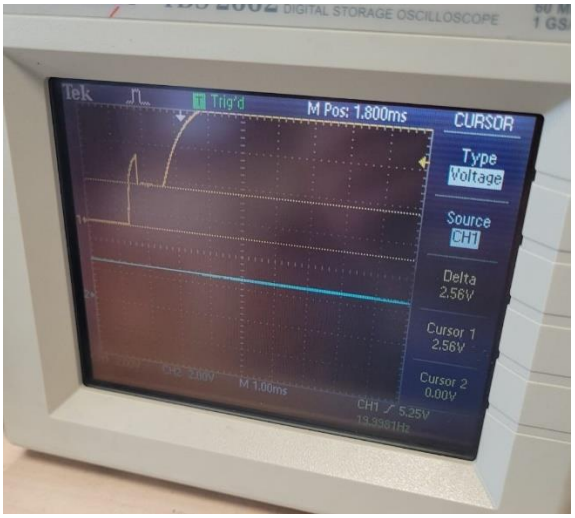

Fig 32: Integration Occurring at 2.56V

Moreover the delays was fixed by the added delays from the integrator circuit, can be seen in figure 33(a) and figure 33(b).

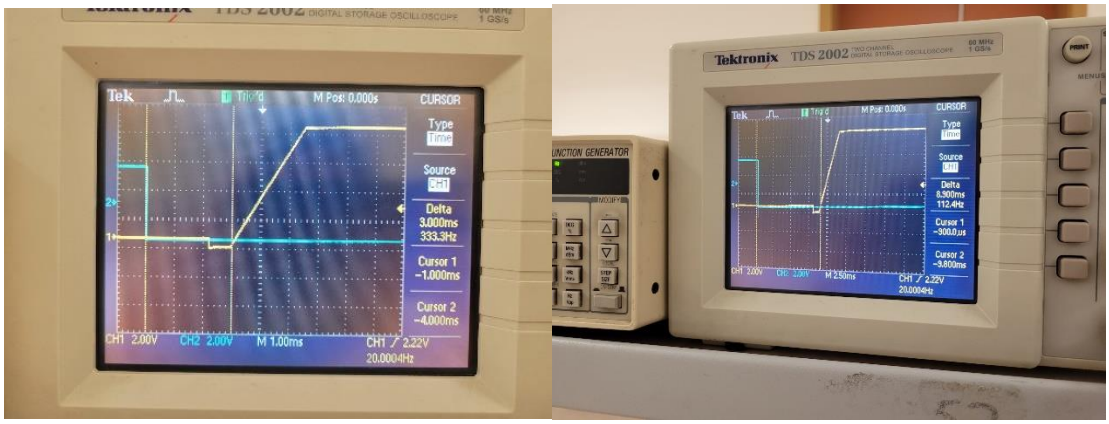

Fig 33 a&b: 3ms and 10ms Comp+Integrator Opamps

Conclusion

This lab was the first lab where I had to built multiple smaller circuit that are connected with each other where each subcircuit has its own function.

To explain this lab further, let's start off with comparator circuits. Especially in 3ms, the first delay was higher than the expected value of 3ms. For that I had to reduce the resistor value of comparator to an appropriate value which would cause the delay to go down in as time constant is smaller.

On integrator circuit, I had to go down a smaller value on capacitors hardware labs as the initial rise time I had found was higher. The same time constant idea was applicable here as well. However, whether one should reduce the resistor values or capacitor values depends on how complex the integrator circuit is. If there had been more than one resistor, it would be smarter to reduce capacitor values as it would certainly cause time constant go down. Another way of reducing rise time can also be increasing the Vcomp. This causes integration to start at a later point reducing the total time spent in rise time.

The subtractor focused on subtracting the rise times of the circuit which helped me reach the expected result as if I had done this on the fall times the result would be different. This was due to fall time of the integrator circuit being shorter than the rise time of it.

The incorrect delays in comparator circuits were fixed by the integrator circuit. As the integrator circuit also adds a delay. However, as you can see there are still some errors. For this, it can be said that LM324's continuous and numerous use probably increased the error in Hardware even after changing several resistor and capacitor values proving that we are not using an ideal OPAMP.

Finally, it can be said that this lab was extremely useful on learning how different types of OPAMPs work together and how to transform a given waveforms behaviour to a different behavior.