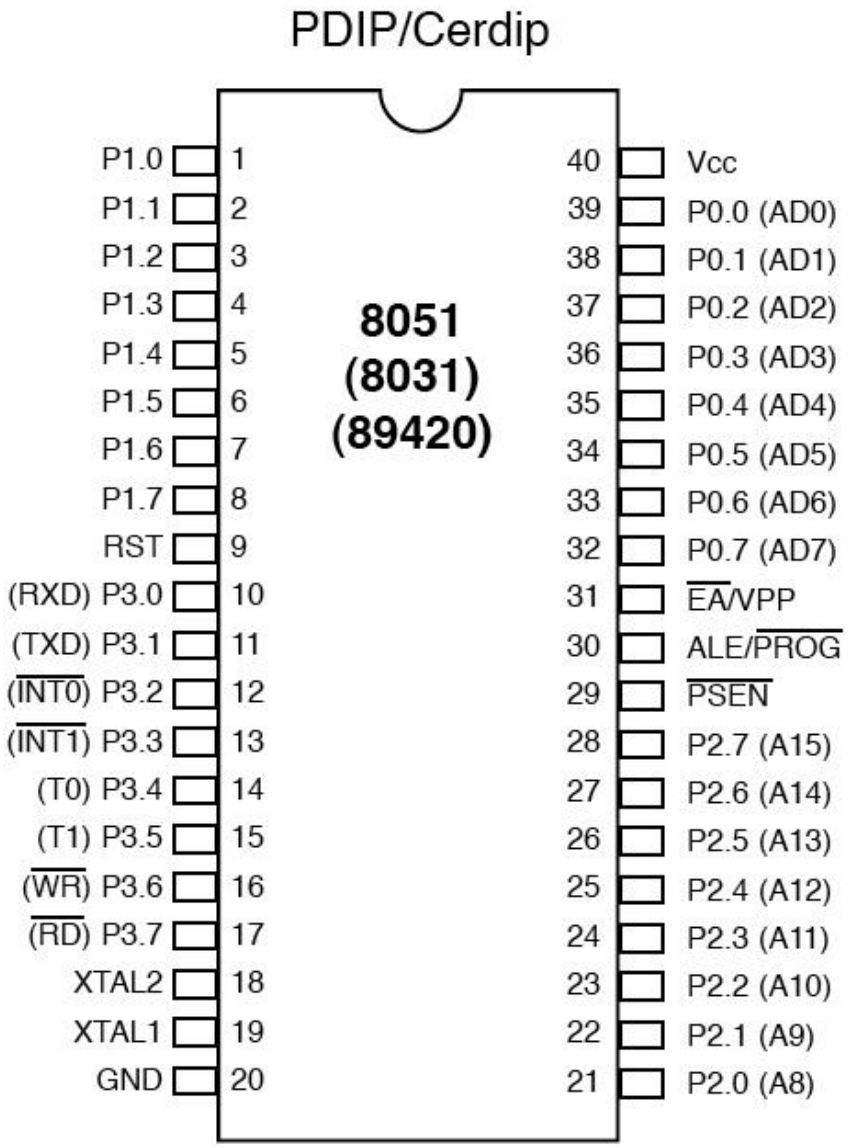
Module 4

I/O Ports and Their Programming

8051 Pin diagram



- Figure 4-1. 8051 Pin Diagram
- The 8051 family members all have 40 pins.
  - Vcc, GND, XTAL1, XTAL2,... (See Chapter 8).
  - I/O port pins
    - The four ports: Port 0, Port 1, Port 2, and Port 3
    - Usually we call them as P0, P1, P2, and P3.
    - Each port uses 8 pins.

I/O Port Pins

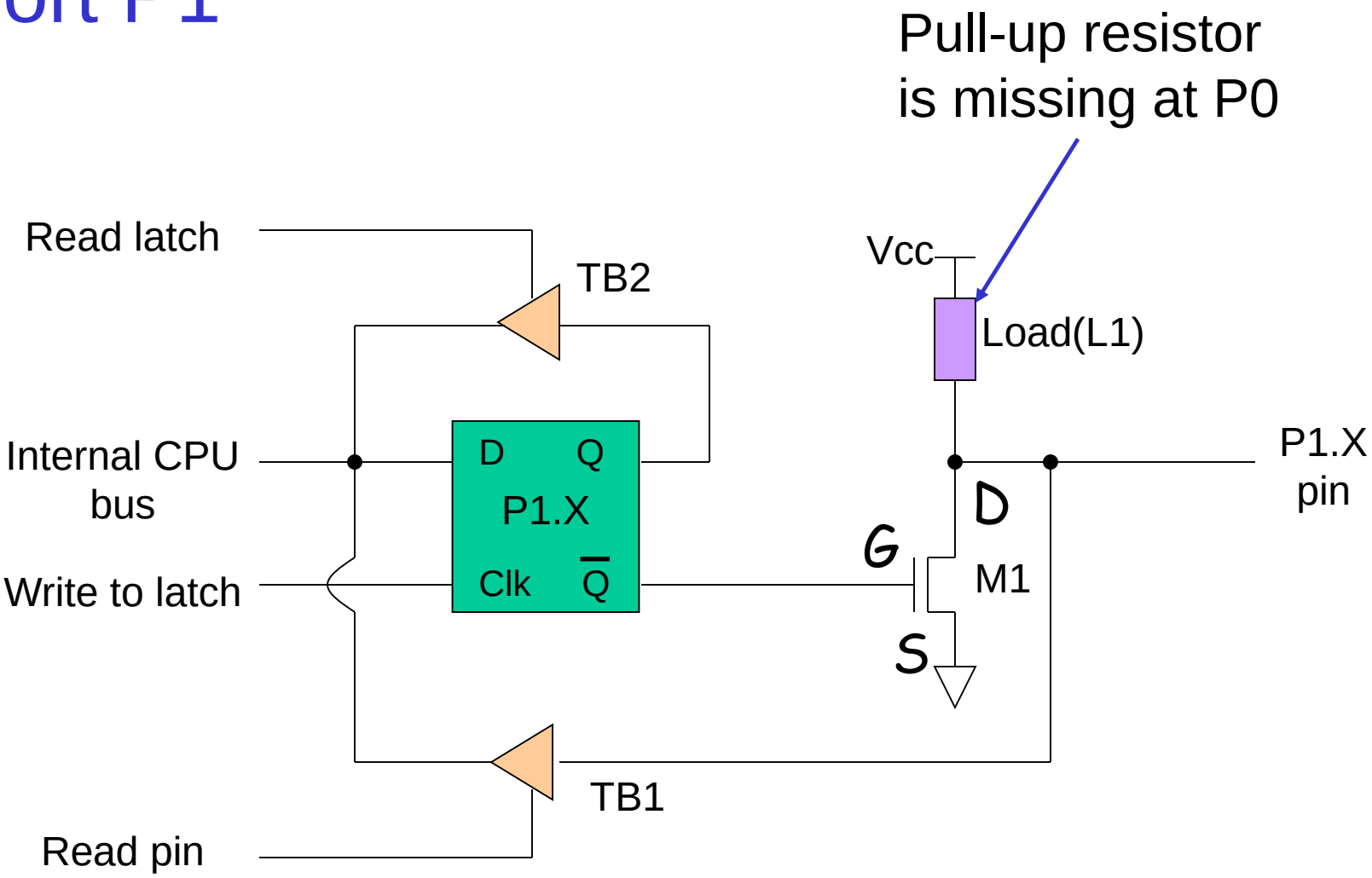
- The 8051 has four I/O ports
  - Port 0 pins 32-39 P0.0 to P0.7
  - Port 1 pins 1-8 P1.0 to P1.7
  - Port 2 pins 21-28 P2.0 to P2.7
  - Port 3 pins 10-17 P3.0 to P3.7
  - Each port has 8 pins.
    - Named P0.X , P1.X, P2.X, P3.X X=0,1,...,7
    - P0.0 is the bit 0 (LSB) of P0
    - P0.7 is the bit 7 (MSB) of P0
    - These 8 bits form a byte.
    - Note that 8 pins of port can work independently.
- Each port can be used as input or output (bi-directional).

Ports 2 and 3

- In an 8031-based system, P2 is used to provide address A8-A15.
- Although port 3 can be used as simple I/O port, this is not the way it is most commonly used.
- Port 3 has the additional function of providing certain signals.

P3 Bit	Function	Pin
P3.0	RxD	10
P3.1	TxD	11
P3.2	$\overline{\text{INT0}}$	12
P3.3	$\overline{\text{INT1}}$	13
P3.4	T0	14
P3.5	T1	15
P3.6	$\overline{\text{WR}}$	16
P3.7	$\overline{\text{RD}}$	17

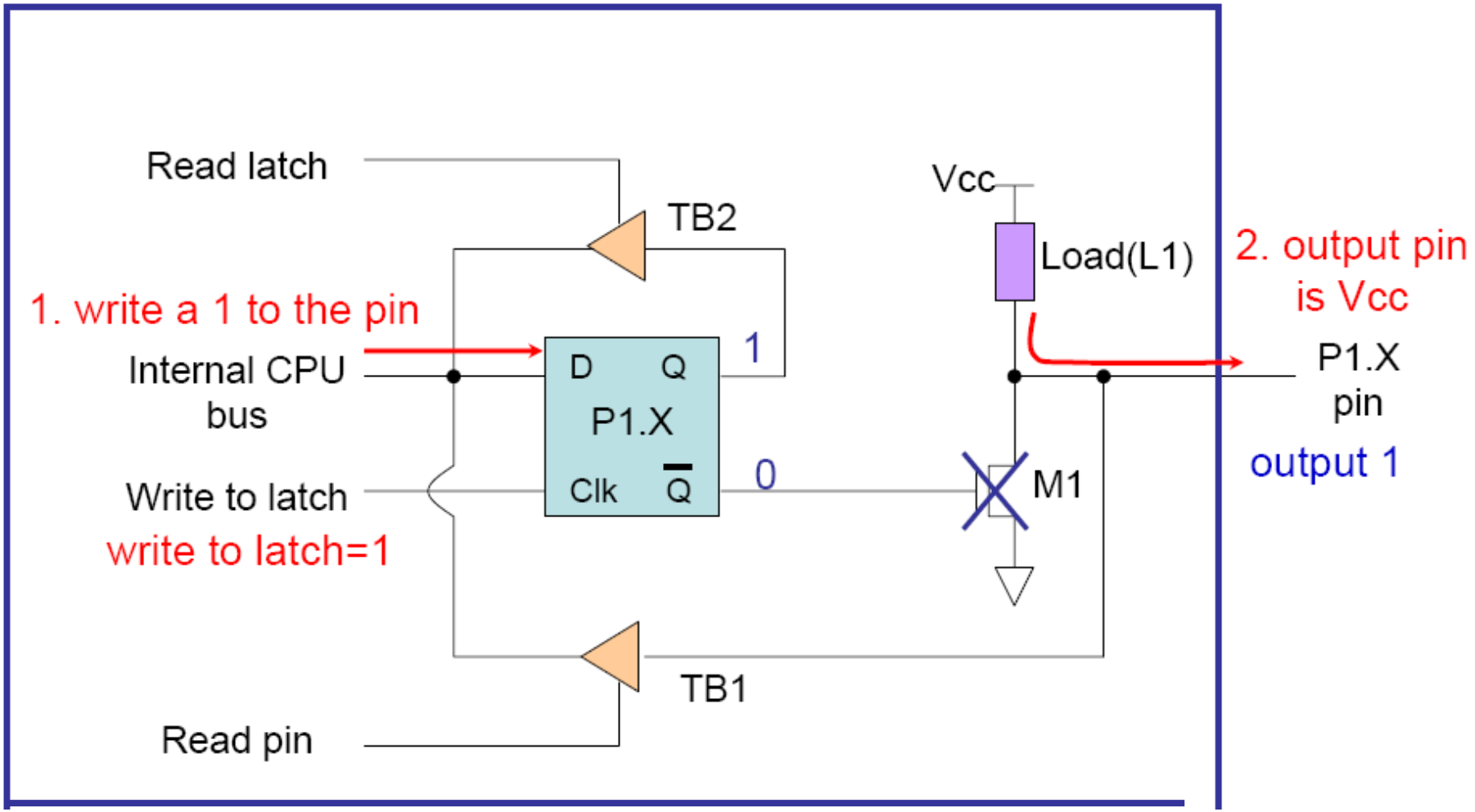
Port P1


Pull-up resistor
is missing at P0
Read latch
TB2
Vcc
Load(L1)
Internal CPU
bus
D
Q
P1.X
Clk
Q
P1.X
pin
Write to latch
G
D
M1
S
TB1
Read pin

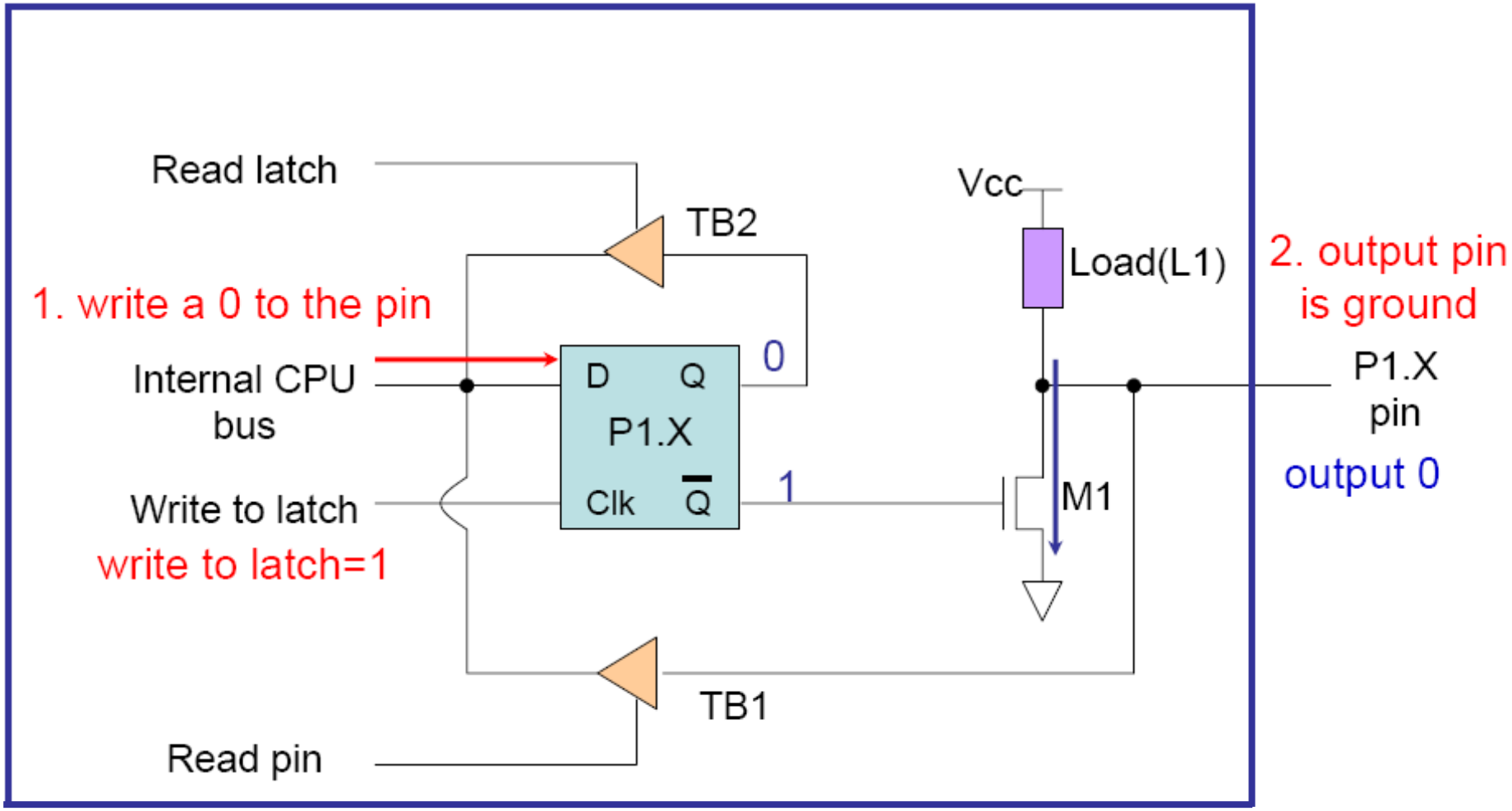
Port pins

- Each pin of I/O ports
  - Internal CPU bus communicates with CPU
  - A D latch stores the value of this pin
    - D latch is controlled by “Write to latch”
      - Write to latch 1: write data into the D latch
  - Two Tri-state buffers
    - TB1: controlled by “Read pin”
      - Read pin = 1 (TB1=1) read the data present at the pin
    - TB2: controlled by “Read latch”
      - Read latch=1 (TB2=1) read value from internal latch
  - A transistor M gate
    - Gate = 0, output = 1
    - Gate = 1, output = 0

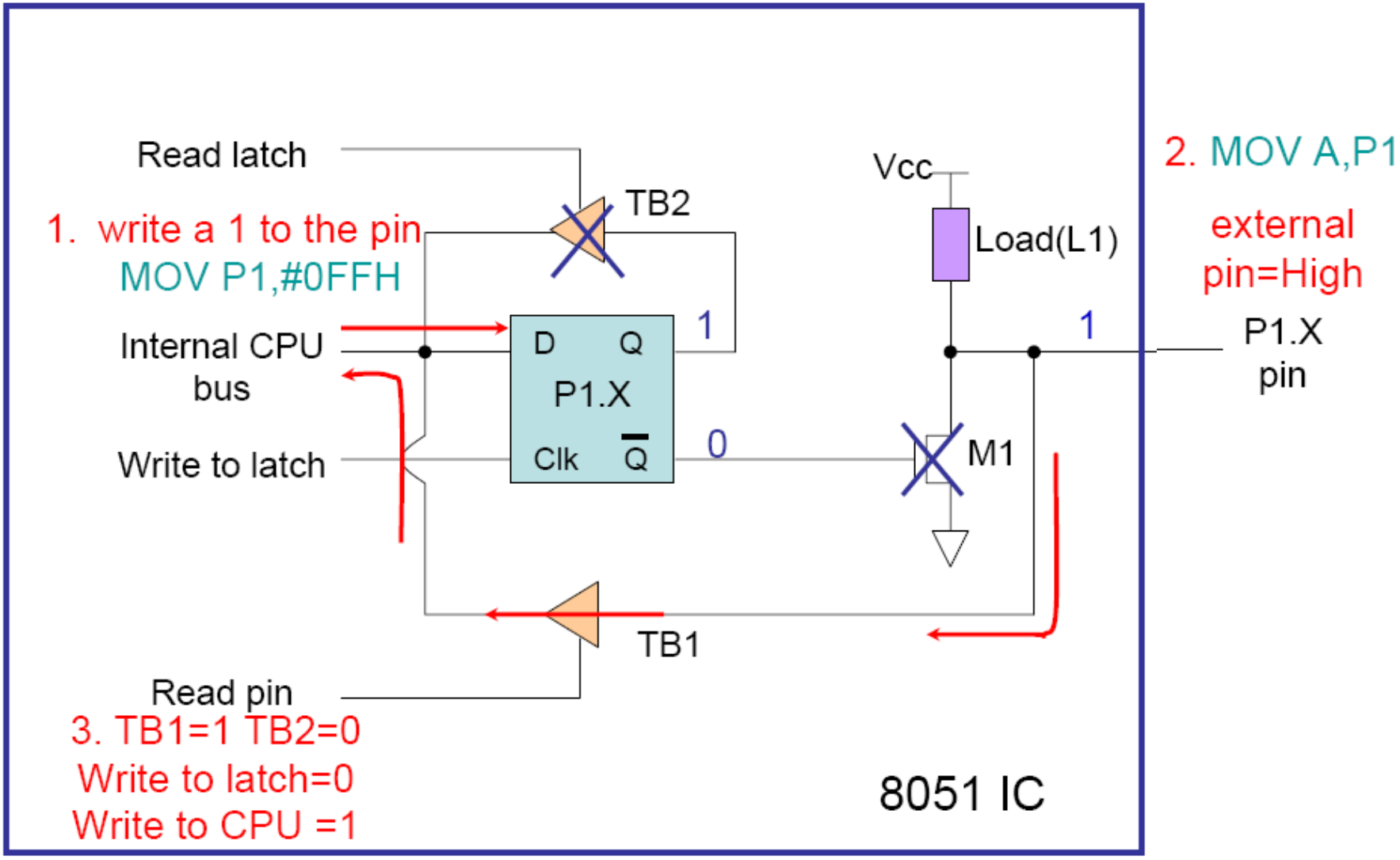
Writing 1 to output pin P1.X



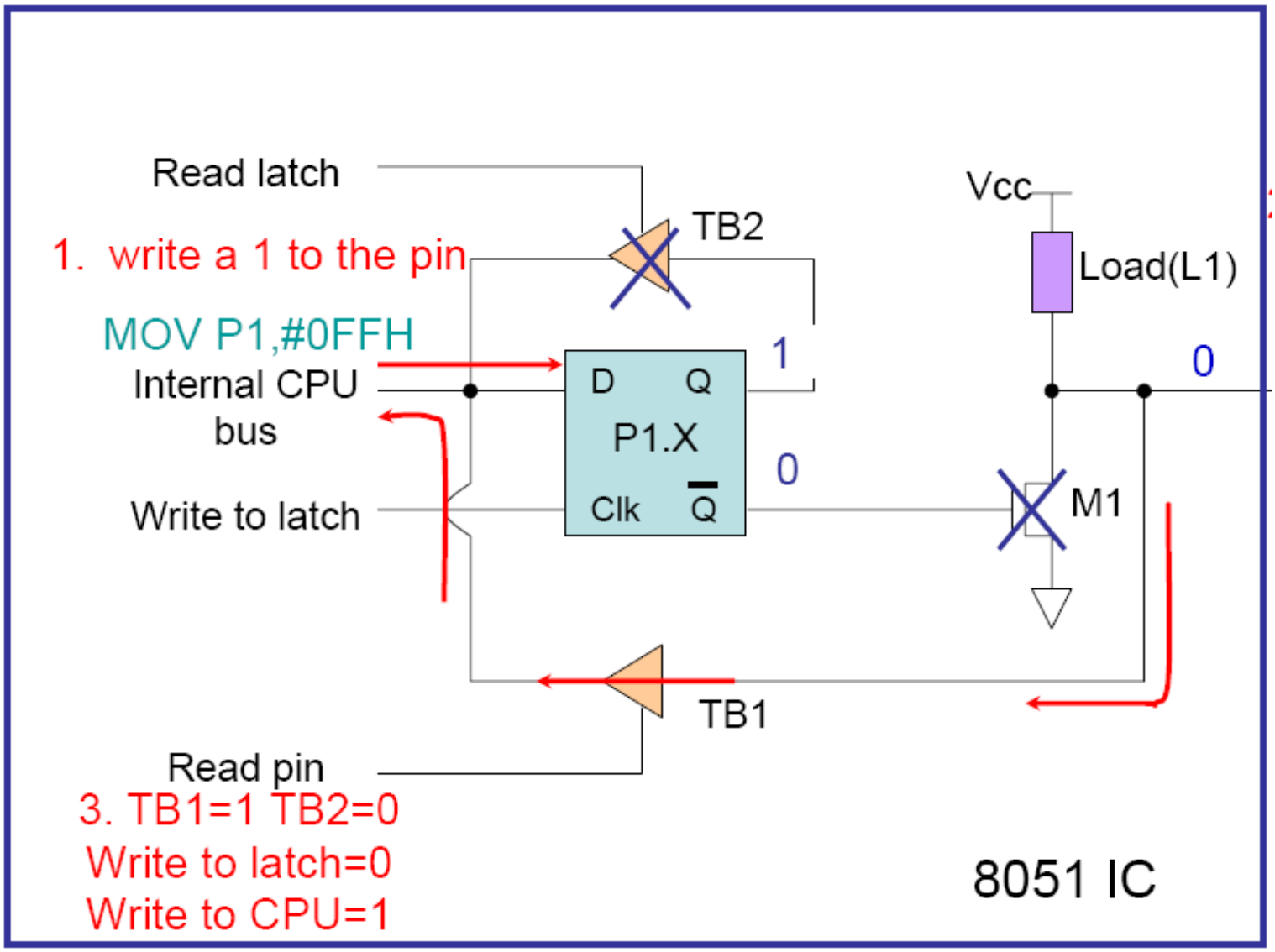
Writing 0 to output pin P1.X



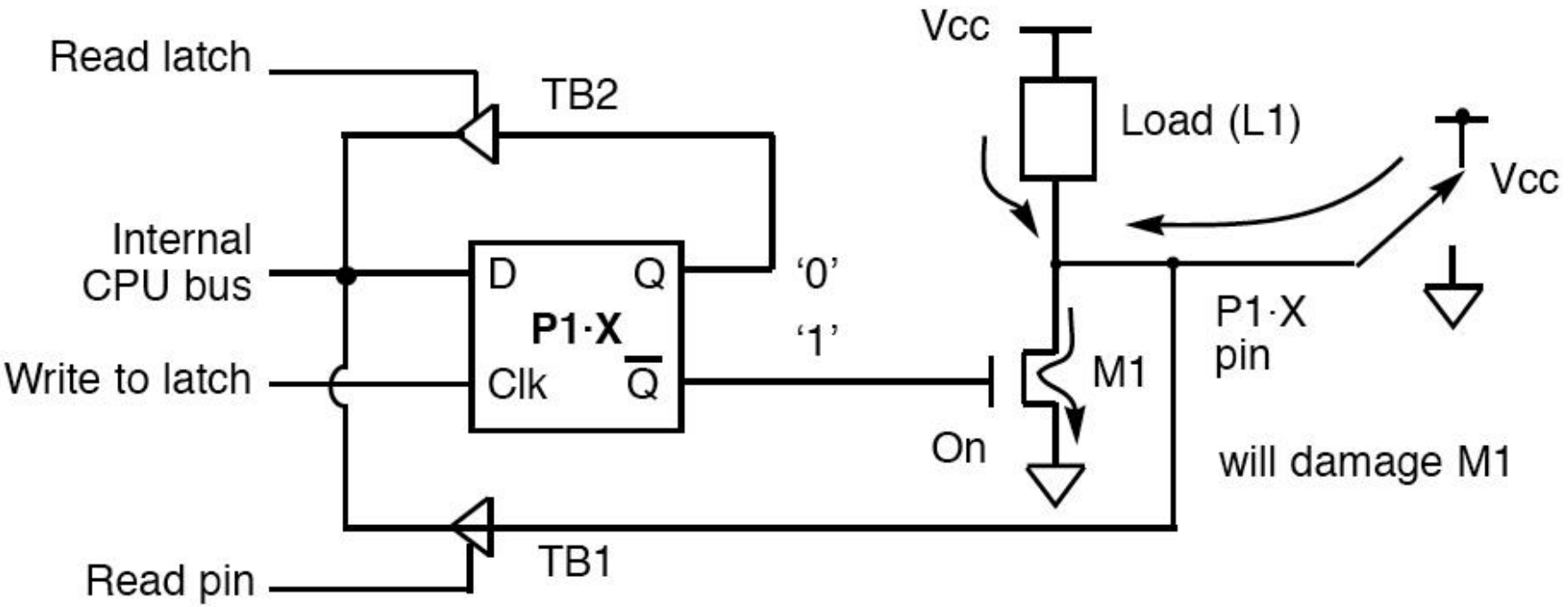
Reading High at Input Pin



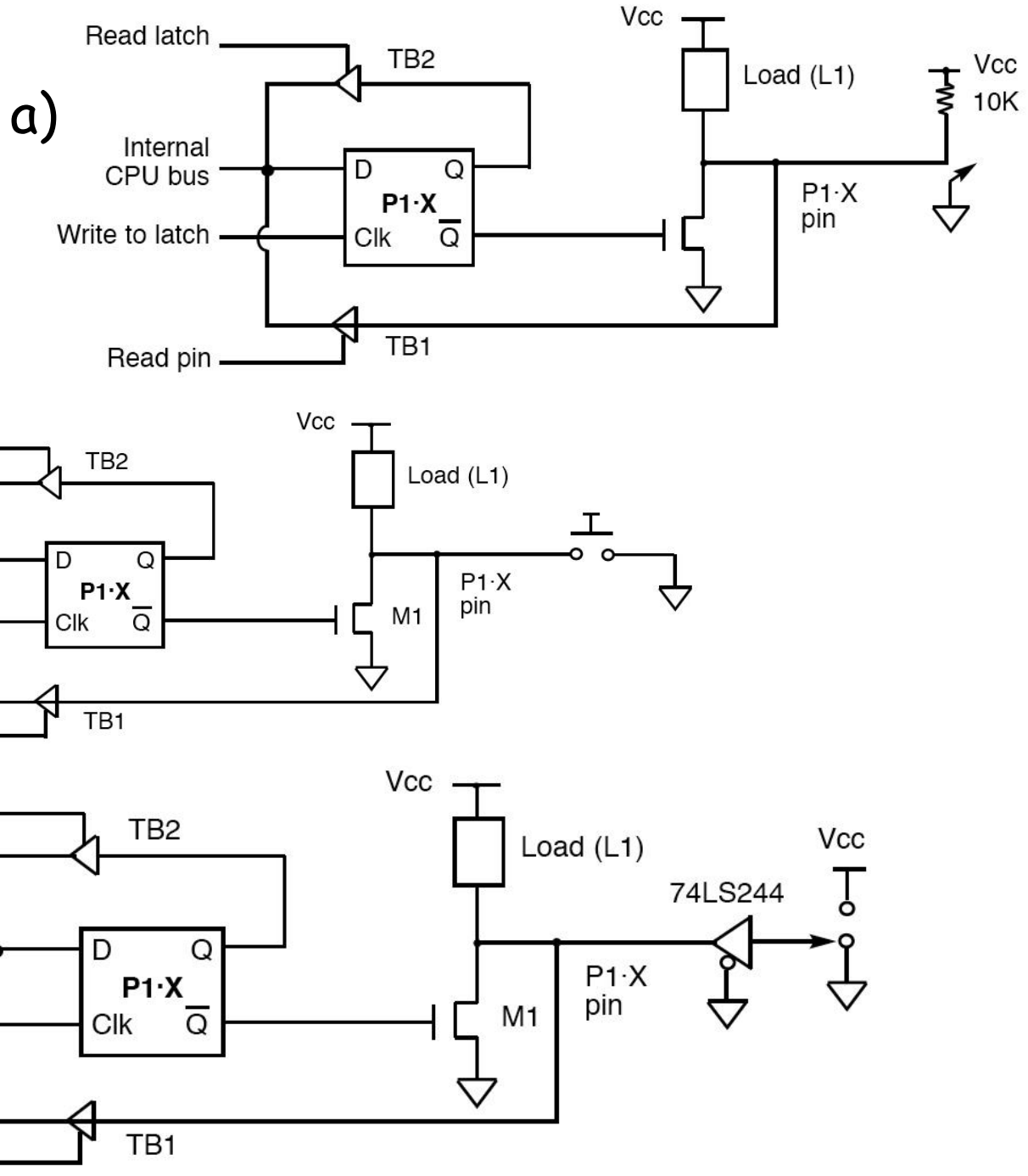
Reading Low at the Input Pin



Never connect direct Vcc to Port Pins



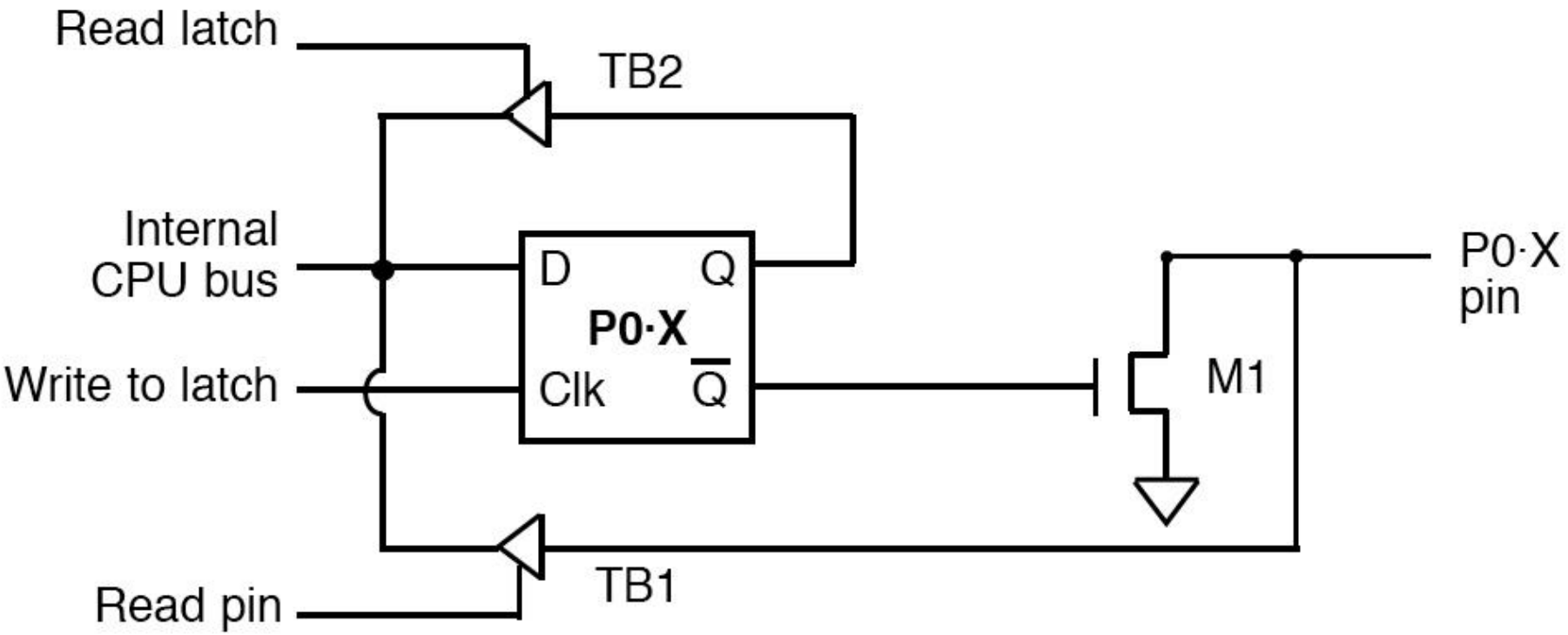
Ways


a)
Read latch
TB2
Internal
CPU bus
Write to latch
D
Q
P1·X
Clk
Q
Read pin
TB1
Vcc
Load (L1)
Vcc
10K
P1·X
pin
b)
Read latch
TB2
Internal
CPU bus
Write to latch
D
Q
P1·X
Clk
Q
Read pin
TB1
Vcc
Load (L1)
M1
P1·X
pin
c)
Read latch
TB2
Internal
CPU bus
Write to latch
D
Q
P1·X
Clk
Q
Read pin
TB1
Vcc
Load (L1)
M1
74LS244
Vcc
P1·X
pin

Other Pins

- P1, P2, and P3 have internal pull-up resisters.
  - P1, P2, and P3 are not open drain.
- P0 has no internal pull-up resistors and does not connect to Vcc inside the 8051.
  - P0 is open drain.
  - Compare the figures of P1.X and P0.X
- However, for a programmer, it is the same to program P0,P1,P2, and P3.
- All the ports, upon a RESET, receive a FFh

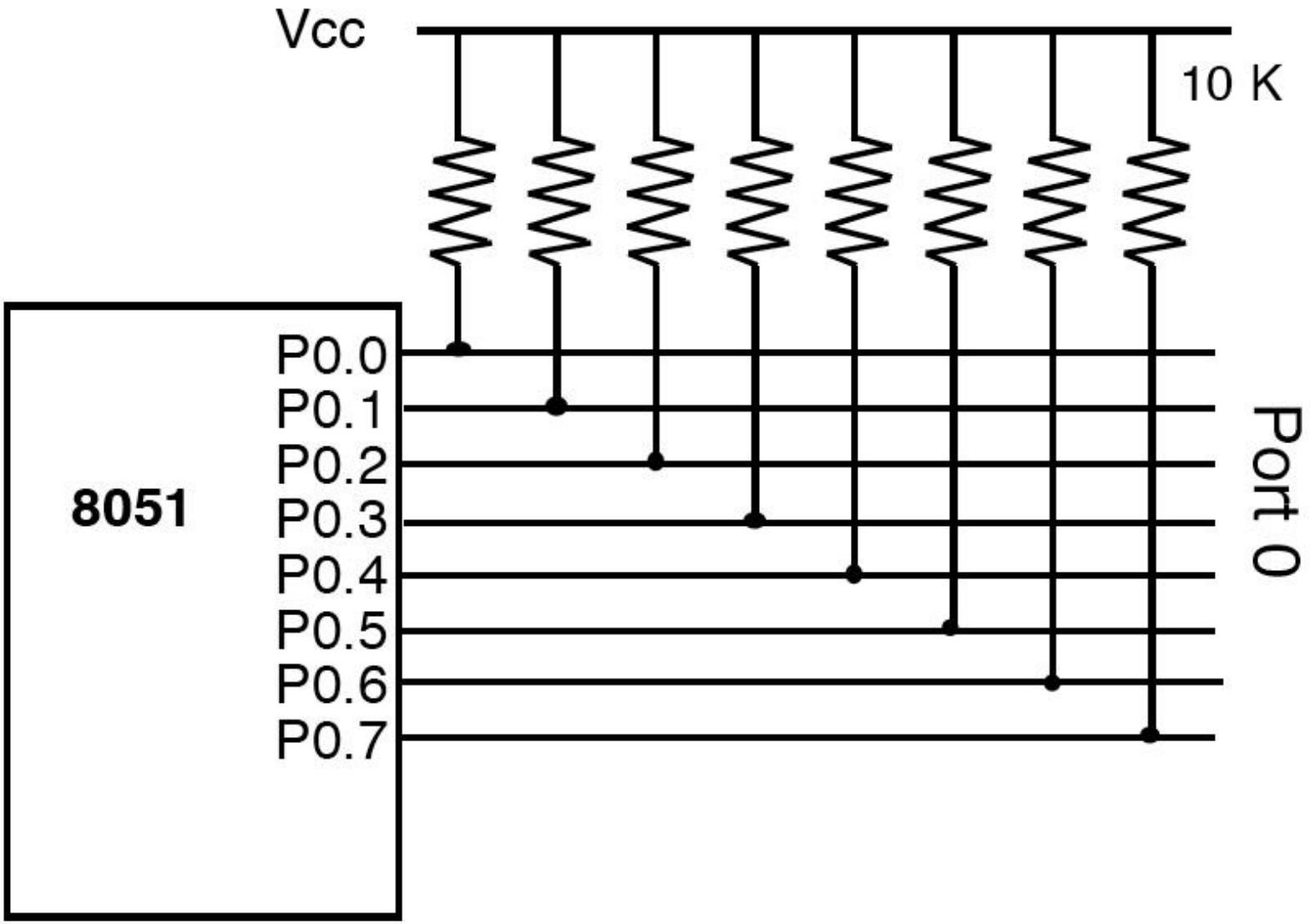
P0 Structure



P0 Structure

- P0 is an open drain. The reason is to multiplex address and data.
- Open drain is a term used for MOS chips in the same way that open collector is used for TTL chips.
- When P0 is used for simple data I/O we must connect it to external pull-up resistors.
- Each pin of P0 must be connected externally to a 10K ohm pull-up resistor. Then P0 can be an input or output port.
- In an 8031-based system, P0 are used to provide address A0-A7. (See Chapter 14)

Port 0



8051 Fan-out for P1,P2,P3

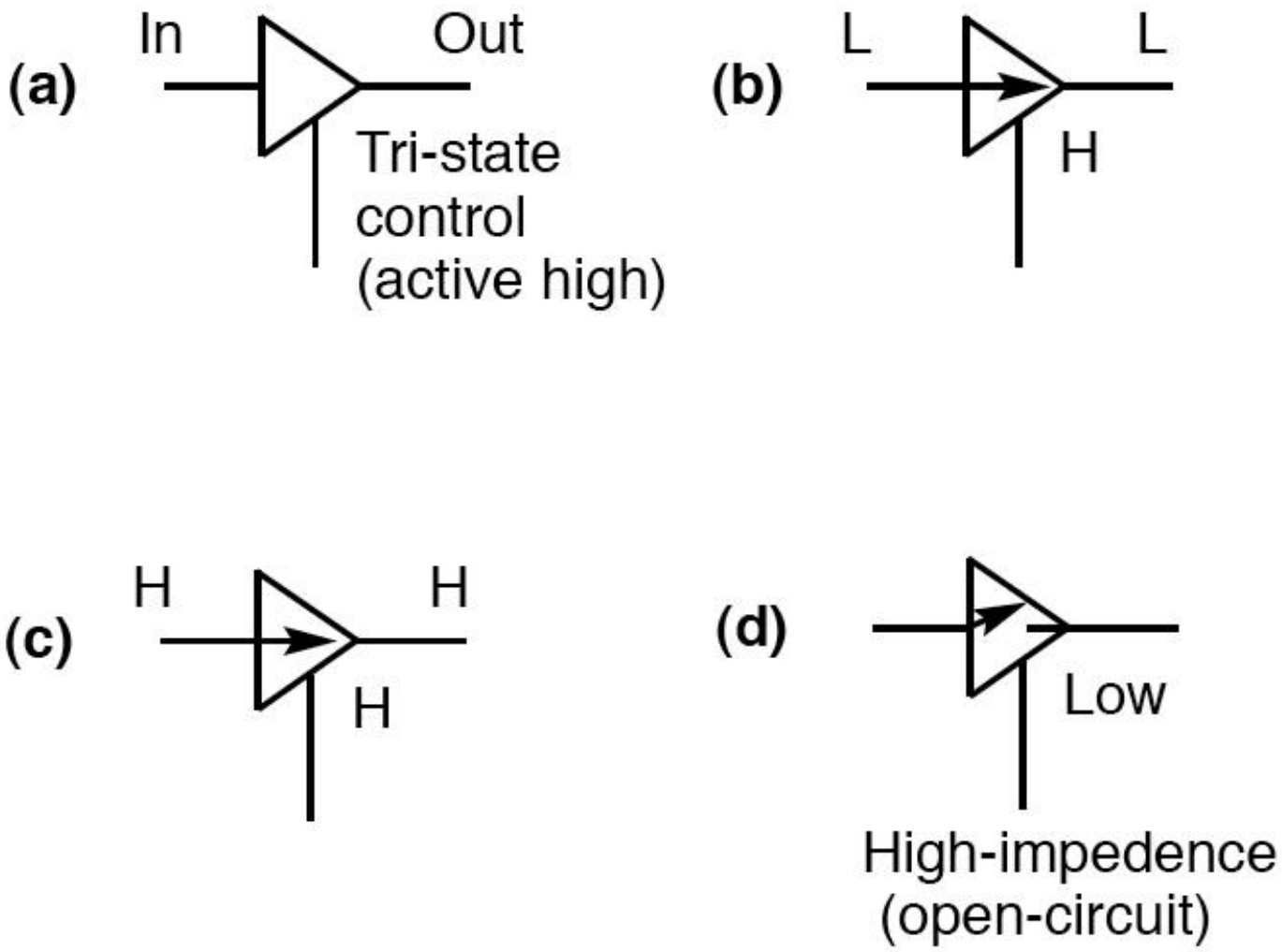
Pin	Fan-out
IOL	1.6 mA
IOH	60 µA
IIL	50 µA
IIH	650 µA

Note: P1, P2, and P3 can drive up to 4 LS TTL inputs when connected to other IC chips.

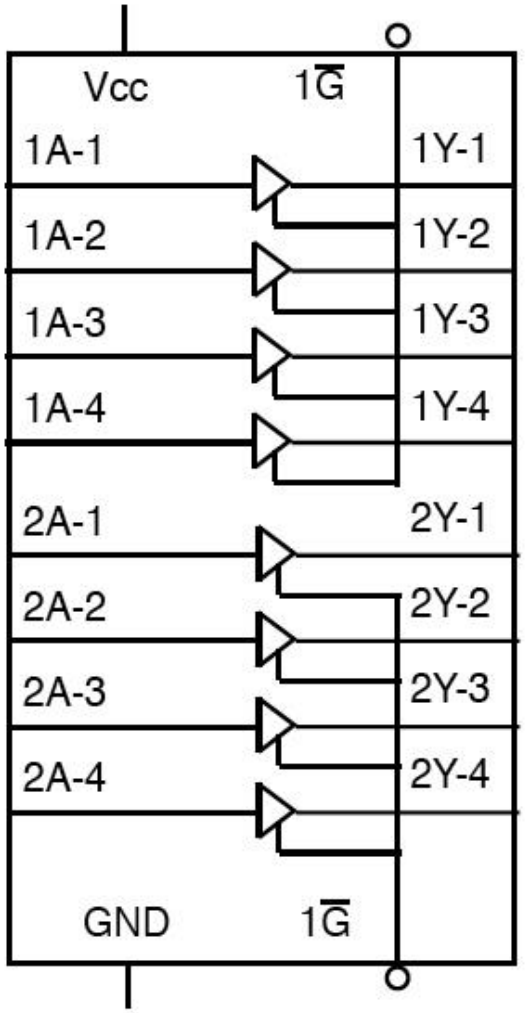
IOL = **Current Output Low**.
IOH = Current Output High.
Those are the currents when output of the digital device is low or high.
That much current can be sourced or sinked by the device.

IIH (high input current) is the leak current when a high level is input to the input pin.
IIL (low input current) is the leak current when a low level is input to the input pin.

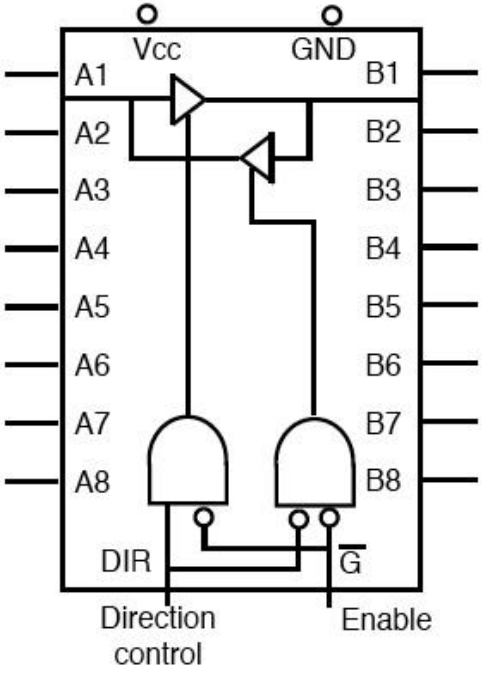
What if the 8051 cannot drive a load – use buffers



74LS244



74LS245



Function Table

Enable $\overline{G}$	Direction control DIR	Operation
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Isolation

	I_{OH} (mA)	I_{OL} (mA)
74LS244	3	12
74LS245	3	12

How to program for input

- In order to make P1 an input port, the port must be programmed by writing 1 to all the bits.

```
        MOV  A,#0FFH ;A=11111111B
        MOV  P1,A    ;make P1 an input port
BACK:   MOV  A,P1    ;get data from P1
        MOV  P2,A    ;send data to P2
        SJMP BACK
```

  - The pin value is sent to CPU, but not saved in latch .
  - To be an input port, P0, P1, P2 and P3 have similar methods.

Port Read

- When reading ports, there are two possibilities :
  - Read the input pin to CPU (from *external pin value*)

```
MOV  A, P1
JNB    P2.1, TARGET   ; jump if P2.1 is not set
JB     P2.1, TARGET   ; jump if P2.1 is set
```

Mnemonic	Example	Description
MOV A, PX	MOV A, P2	Bring into A the data at P2 pins
JNB PX.Y,..	JNB P2.1, TARGET	Jump if pin P2.1 is low
JB PX.Y,..	JB P1.3, TARGET	Jump if pin P1.2 is high
MOV C, PX.Y	MOV C, P2.4	Copy status of pin P2.4 to CY

Port Read - more

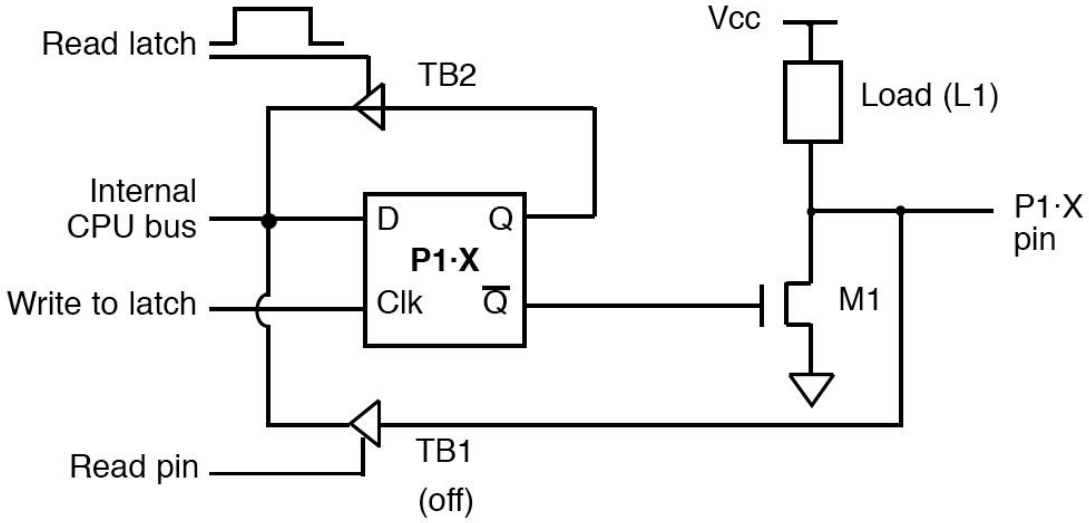
- or Read the *internal latch* of the output port (and then *output*).
  - ANL P1, A ; P1 ← P1 AND A
  - ORL P1, A ; P1 ← P1 OR A
  - INC P1 ; increment P1

Read-Modify-Write Instructions

Mnemonic		Example	
ANL	Px	ANL	P1,A
ORL	Px	ORL	P2,A
XRL	Px	XRL	P0,A
JBC	PX.Y,TARGET	JBC	P1.1,TARGET
CPL	PX.Y	CPL	P1.2
INC	Px	INC	P1
DEC	Px	DEC	P2
DJNZ	PX.Y,TARGET	DJNZ	P1,TARGET
MOV	PX.Y,C	MOV	P1.2,C
CLR	PX.Y	CLR	P2.3
SETB	PX.Y	SETB	P2.3

Note: x is 0, 1, 2, or 3 for P0 - P3.

Reading the Latch using Read-Modify-Write Instructions



- ANL P1,A
- The read latch activates TB2
- This data is ANDed with register A
- The result is overwritten to the latch