I-TLC

Project: Design an intelligent traffic light controller and implement a Verilog code with a finite state model for its functionality.

Description :

This design aims to eliminate need of a traffic officer for control and clears the traffic in a better way.

For this,I have considered a four way road.one way is main road and other is side road.

Main road is considered to have huge traffic and has to be cleared as soon.

Side road is for the local people, both pedestrains and vehicles. Proper safety must be taken for crossing the road .These two roads are considered to be intersecting perpendicularly.

A sensor should also present at the side road which should sense high when a pedestrian or vehicles is observed on side road.

This design prioritises to allow heavy traffic to flow .

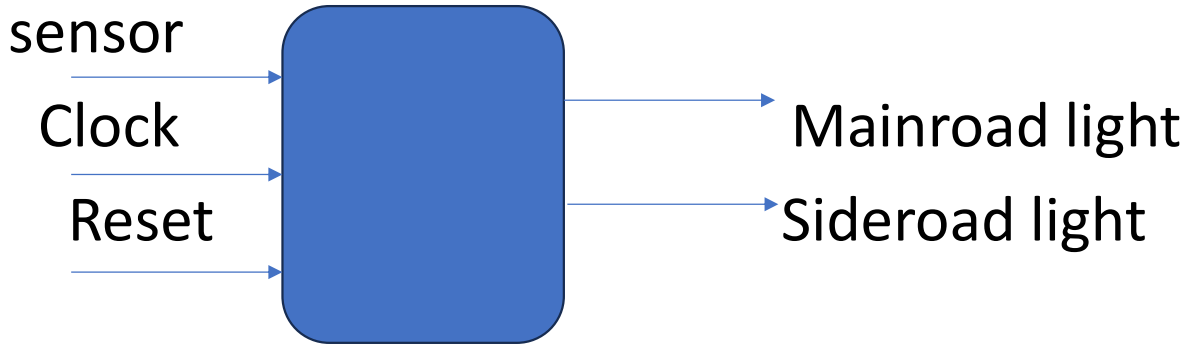
Traffic rule that is followed-

Red light: The vehicle has to be stopped completely.

Yellow/Amber light: slow down your vehicle,move carefully and stop vehicle before Zebra lines.

Green light: You can move your vehicle at your speed.

Block diagram-

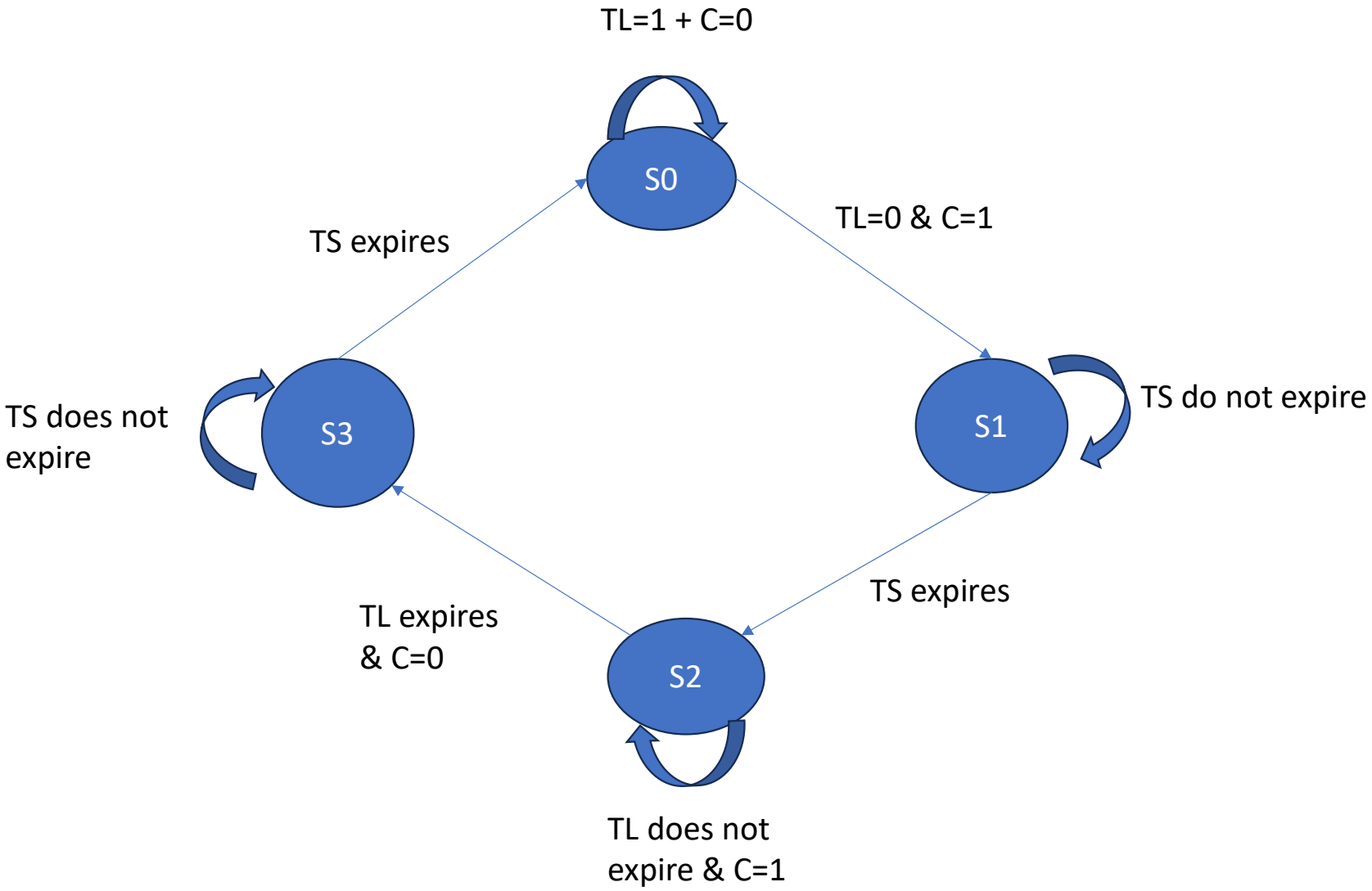


State assignment and Declarations-

State	Main road output	Side road output
S0	001	100
S1	010	100
S2	100	001
S3	100	010

- MSB denotes red light
- LSB denotes green light
- TL- Timer large(10 sec)
- TS- Timer small(6 sec)

State Diagram-


TL=1 + C=0
S0
TL=0 & C=1
TS expires
S3
TS does not expire
S1
TS do not expire
TS expires
TL expires & C=0
S2
TL does not expire & C=1

Simulation result-