جامعة بيرزيت

BIRZEIT UNIVERSITY

Faculty of Engineering & Technology
Department of Electrical & Computer Engineering
ENEE4113-COMMUNICATIONS LAB
Exp 9 : Delta Modulation (Linear & DCDM)
Report #2

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9/8/2024

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1. Abstract

The experiment aims to study two types of Delta-Modulation and demodulation and compare them to sow the power points of each one. It also includes the pulse height, granular noise, slope overload, and dynamic of both LDM and DCDM.
Moreover, this experiment shows that reducing the step and increasing the sample frequency helps to increase the accuracy, while DCDM reduces the slope overload effect .
Last of all, it compares the reconstructed efficiency of the DCDM against the LDM.

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2.Theory

2.1 Delta modulation:

Delta modulation is a process mainly used in the transmission of voice information. It is a technique where analog-to-digital and digital-to-analog signal conversion are seen. Delta modulation (DM) is an easy way of DPCM. In this technique, the difference between consecutive signal samples is encoded into n-bit data streams. In DM, the data which is to be transmitted is minimized to a 1-bit data stream.[1]

2.2 Block Diagram of Delta Modulator:

The sampling rate is comparatively very high in the delta modulation technique. The value of the step size after quantization is smaller. In the delta modulation process, the quantization design is easy and simple, and it gives the user the option to design the bit rate.

The delta modulator includes a 1-bit quantizer and a delay circuit along with two summer circuits. The output of the delta modulator will be a stair-case approximated waveform. The step size of this waveform is the delta (Δ). The output quality of the waveform is moderate. In order to obtain a high ratio signal-to-noise, DM must adapt oversampling techniques. In oversampling techniques, the analog signal is sampled many times higher than the Nyquist rate.[1]

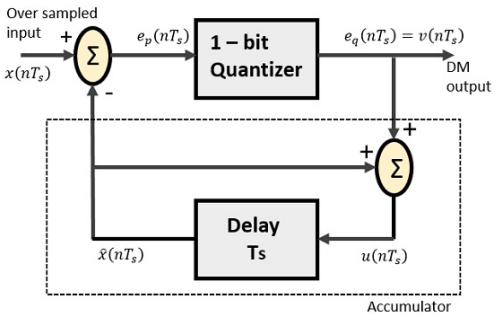

Figure 1: Block diagram for delta modulation [2]

2.3 Advantages of Delta Modulation:

- Design is easy and simple.
- It is a 1-bit quantizer.
- Modulator & demodulator can be designed easily.
- In delta modulation, the quantization design is very simple
- The bit rate can be designed by the user [1]

2.4 Disadvantages of Delta Modulation:

- When the value of the delta is small, slope overload distortion is seen, which is a type of noise.
- When the value of delta is large, granular noise is seen, which is a type of noise.[1]

2.5 Adaptive Delta Modulation:

This is a type of delta modulation technique. In digital modulation, there is a problem in determining the step size, which may have an influence on the quality of the wave, which is produced as output. We require a larger step size in the steep slope of the modulating signal, and a small step size is required when the message has a small slope. This kind of detail is ignored in Delta Modulation techniques. So, we need to have control over the step size according to our requirements so that we are able to obtain the sample output in the required fashion. This is the main concept behind adaptive Delta Modulation.

The block diagram of adaptive delta modulation is shown below in figures 2 and 3 which includes an ADM transmitter & receiver. The transmitter has a summer, a quantizer, a delay circuit, and a logic circuit. Here, the step size is kept fixed between some predefined maximum and minimum values. [3]

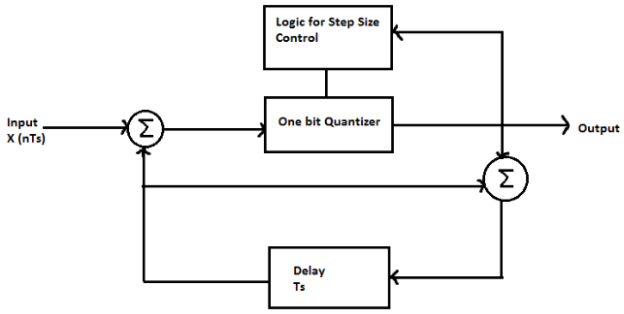

Figure 2: Adaptive Delta Modulation Transmitter[3]

The upper limit is used to control the slope overload distortion and the lower limit is used to control the granular noise. The step size increase or decreases based on a certain set of rules.

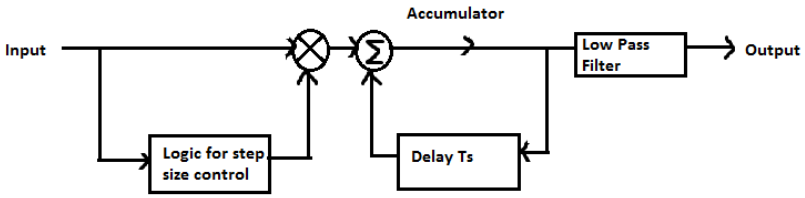

Figure 3: Adaptive Delta Modulation Reciver [3]

The ADM receiver has two parts. The first part is used to produce the step size from the incoming bits. The bits are then applied to the second part of the receiver which contains an accumulator. The function of the accumulator is to build up the staircase waveform. The signal is then passed through a low pass filter which is used to smoothen the staircase waveform and reconstruct the original signal. [3]

2.6 Differences between Delta Modulation & Adaptive Delta Modulation:

- In delta modulation, the step size cannot be varied. It remains fixed for the entire signal. However, in the case of ADM, the step size can be varied according to the variation of the signal.
- In delta modulation, slope overload distortion and granular noise can be present but in ADM, quantization noise is present. The other types of errors are mainly avoided.
- This modulation utilizes the bandwidth a lot more efficiently as compared to that of delta modulation.
- ADM has a wider dynamic range than delta modulation. [3]

2.7 Quantization Errors in Delta Modulation:

2.7.1 Slope-overload distortion:

This distortion arises because of large dynamic range of the input signal.

We can observe from figure4 below , the rate of rise of input signal x(t) is so high that the staircase signal cannot approximate it, the step size 'Δ' becomes too small for staircase signal u(t) to follow the step segment of x(t).

Hence, there is a large error between the staircase approximated signal and the original input signal x(t) which is called slop-overload error. [4]

2.7.2 Granular or Idle Noise:

Granular or Idle noise occurs when the step size is too large compared to small variation in the input signal.

This means that for very small variations in the input signal, the staircase signal is changed by large amount (Δ) because of large step size.

Figure 4 below shows that when the input signal is almost flat , the staircase signal u(t) keeps on oscillating by ±Δ around the signal.

The error between the input and approximated signal is called granular noise.

The solution to this problem is to make the step size small . [4]

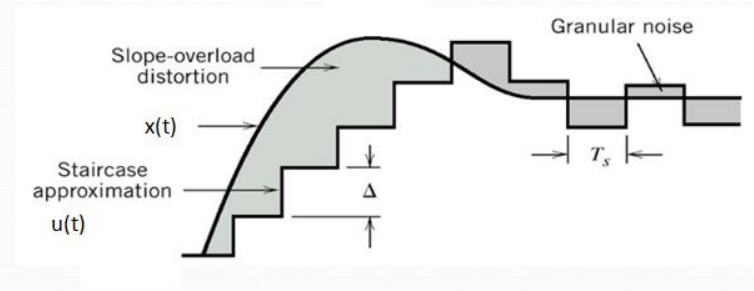

Figure 4: Quantization Errors in Delta Modulation [4]

2.8 Line Coding Schemes:

The data and signals representing data can be either analog or digital. The process of line coding converts the digital data into digital signals.

Using the Line Coding technique, we can easily convert a given sequence of various bits into a digital signal. The sender-side encodes the digital data into the digital signals, while the receiver-side recreates this digital data by decoding the received digital signal. [5]

2.8.1 Unipolar Scheme:

NRZ (Non-return to Zero) – It is a type of Unipolar scheme in which the bit 0 gets defined by the zero voltage and the bit 1 gets defined by the positive voltage. The signal here never returns to zero while in the middle of a bit. Hence, it is known as NRZ. [5]

2.8.2 polar Scheme:

- NRZ-I and NRZ-L – Both of these are kind of similar to the unipolar scheme of NRZ, but the difference is that in this case, we use two voltage/ amplitude levels. In the case of NRZ-Level (NRZ-L), the value of the bit gets determined by the level of the voltage. Here, binary 0 maps to a low logic level, while binary 1 maps to a high logic level. On the other hand, in the case of NRZ-Invert (NRZ-I), the two-level signal consists of a transition at the boundary only if the bit that is going to be transmitted next is logical 1. This transition is not at all present if the next bit to be transmitted is logical 0.

- RZ (Return to Zero) – The RZ scheme is one solution to the problem of NRZ- that uses three values- negative, positive, and zero. In the mid of each bit, the signal gets to 0 in this scheme signal. The RZ encoding requires greater bandwidth, which is its primary disadvantage. Complexity is another problem because it uses three different voltage levels. Due to all these deficiencies, we don't use this scheme anymore today. It has now been replaced with differential Manchester and Manchester schemes now – that perform much better. [5]

2.8.3 Bipolar Scheme:

three voltages: negative, positive, and zero. Here, the voltage level is zero for one data element. While for the other element, the voltage level alternates between negative and positive.

This scheme (bipolar) acts as an alternative to the NRZ. The signal rate in this scheme is very similar to that of the NRZ. But here, we have no DC component, because the voltage zero represents one bit while the other one keeps alternating every time. [5]

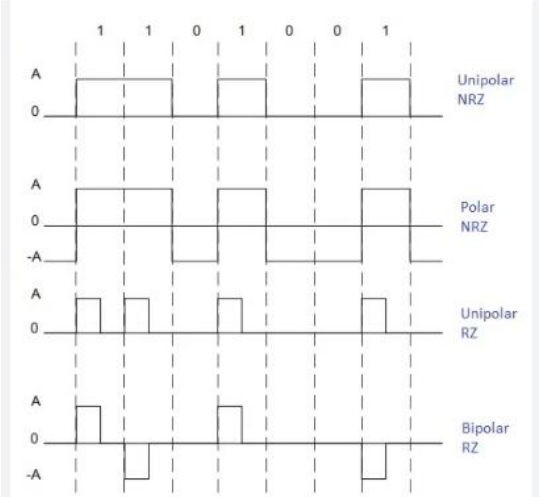

Figure5 : Line Coding Schemes [6]

3.Procedure and Discussion

3.1 Prediction signals in Linear delta modulation (LDM) :

The objective of this part is to compare the original message signal with the predicted signal for the Linear Delta Modulation.

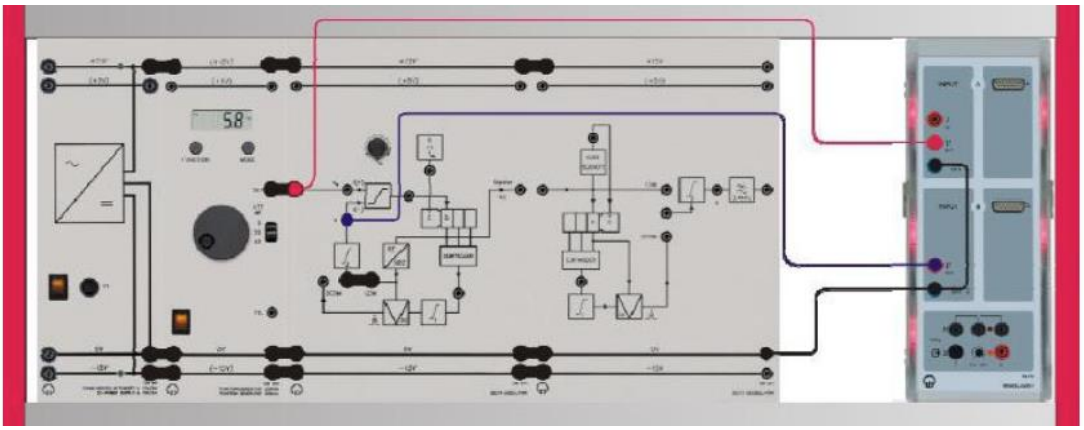

Figure 6:circuit for Prediction signals in LDM and DCDM

we connect the circuit as shown in figure 6 then set the Clock frequency f_{Clock} = 100 kHz (max) , Set the function generator to: Sine, f_m = 100 Hz, V_{SS} = 1V and and the bridging plug was set to LDM using a wire instead of the plug.

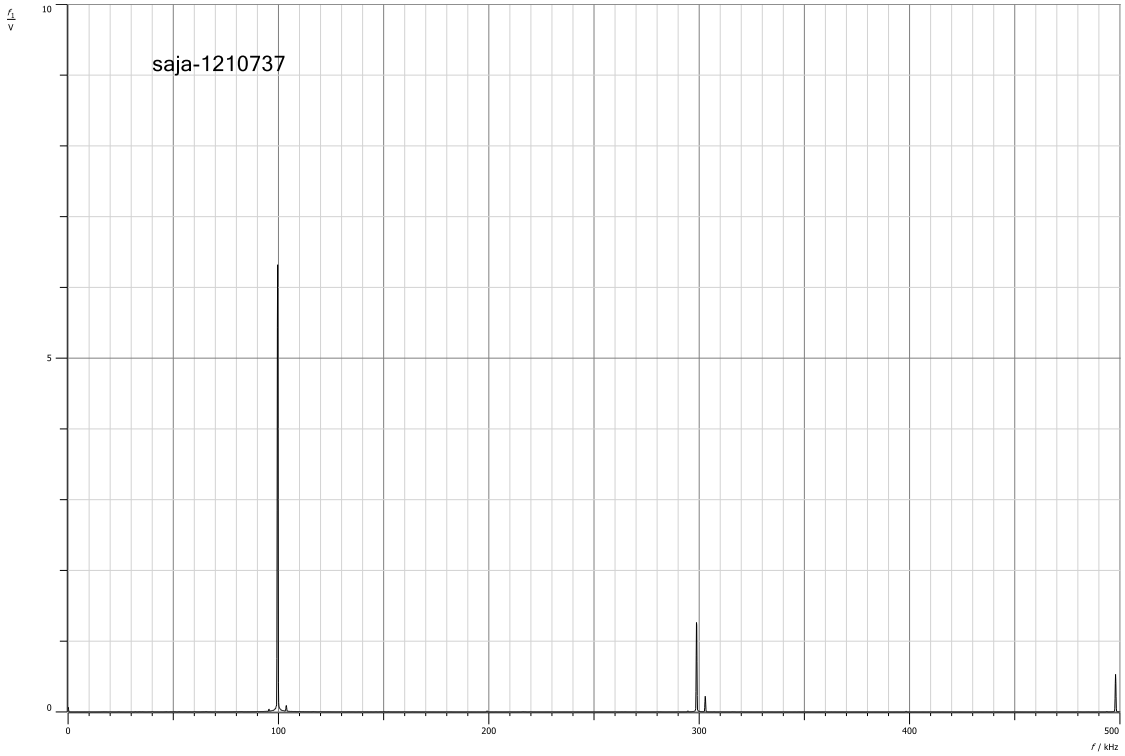

Figure 7: spectrum of Clock frequency fClock = 100 kHz (max)

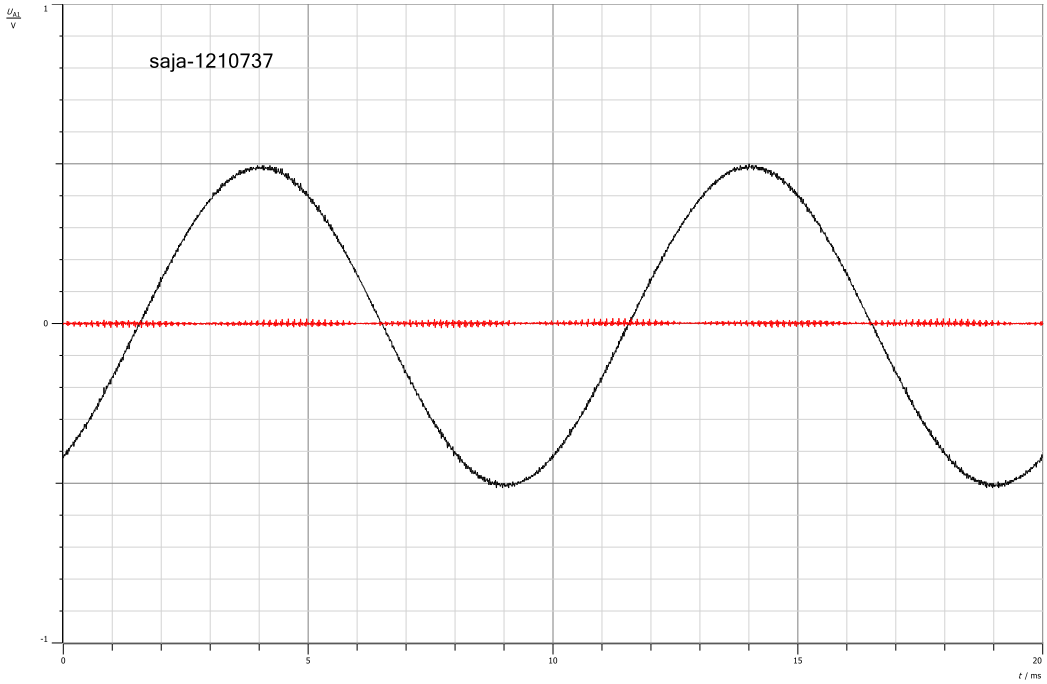

Figure 8:message signal - Sine, fm = 100 Hz, VSS = 1 V in time domain

then , At the output of the integration block (∫ 2), the prediction signal X(t) was connected to the CASSY Sensor UB1, and the modulating signal Sm(t) to the CASSY Sensor UA1.

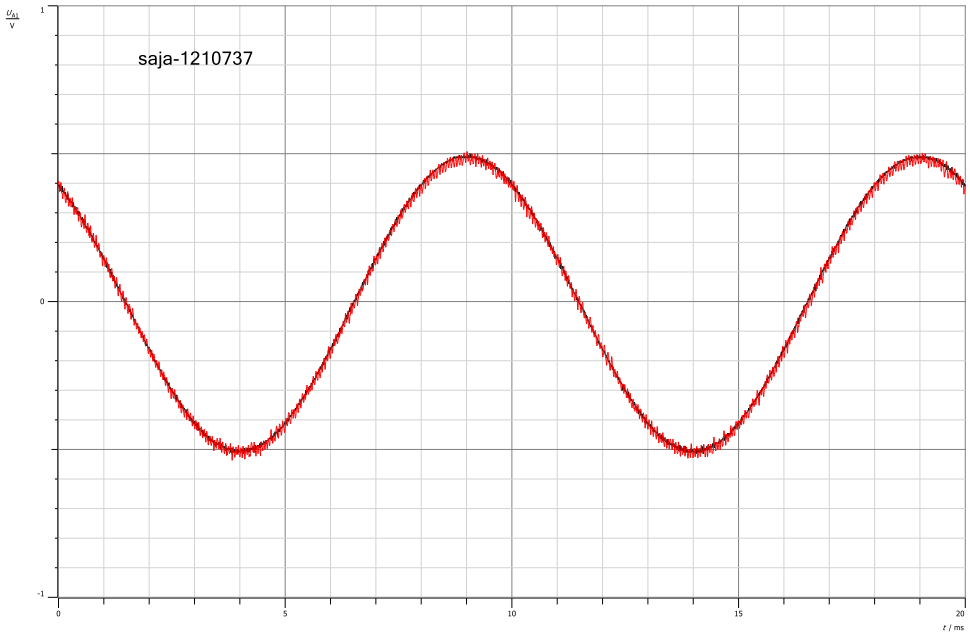

Figure 9:Prediction signal in LDM at maximum value of f_{clock}=100khz

Then , Reduce the clock frequency gradually to Clock frequency f_{Clock} = 10 kHz (min) and repeat the measurement.

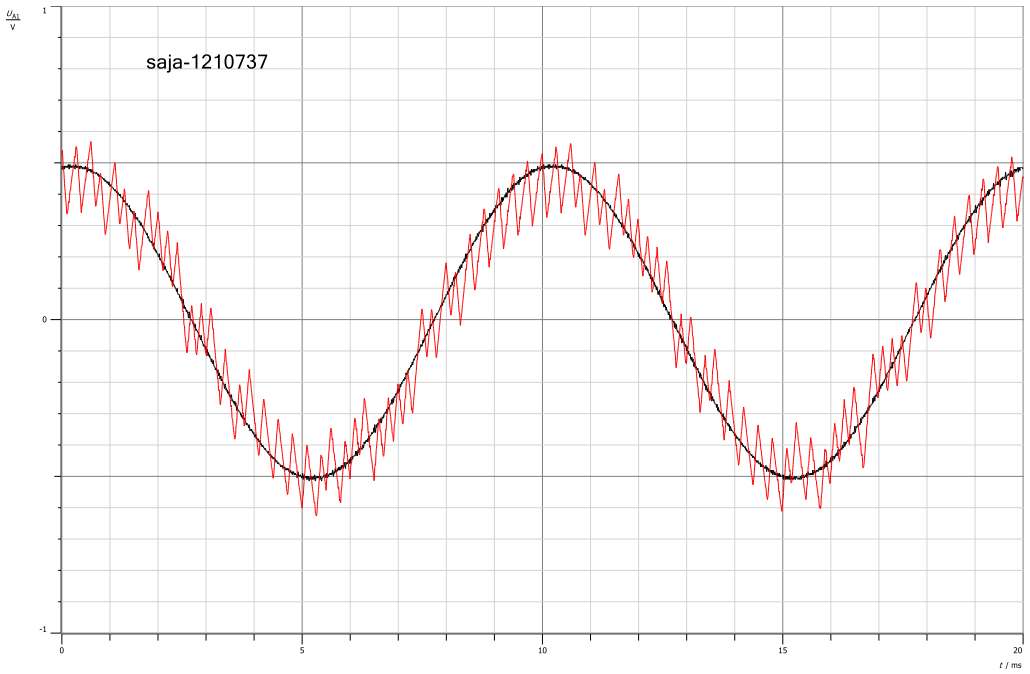

Figure 10:Prediction signal in LDM at minimum value of f_{clock}= 10kHz

It was observed that the prediction improved with a higher clock frequency. This is because increasing the clock frequency results in more samples and readings over time, leading to more accurate predictions and greater similarity between the original and predicted signals.

3.2 Prediction signals in Digital Controlled Delta Modulation (DCDM):

The previous setup was utilized to compare the original message signal with the predicted signal in the Digital Controlled Delta Modulator. The bridging plug was set to DCDM, and the same measurements from part 1 were repeated. The results are shown below:

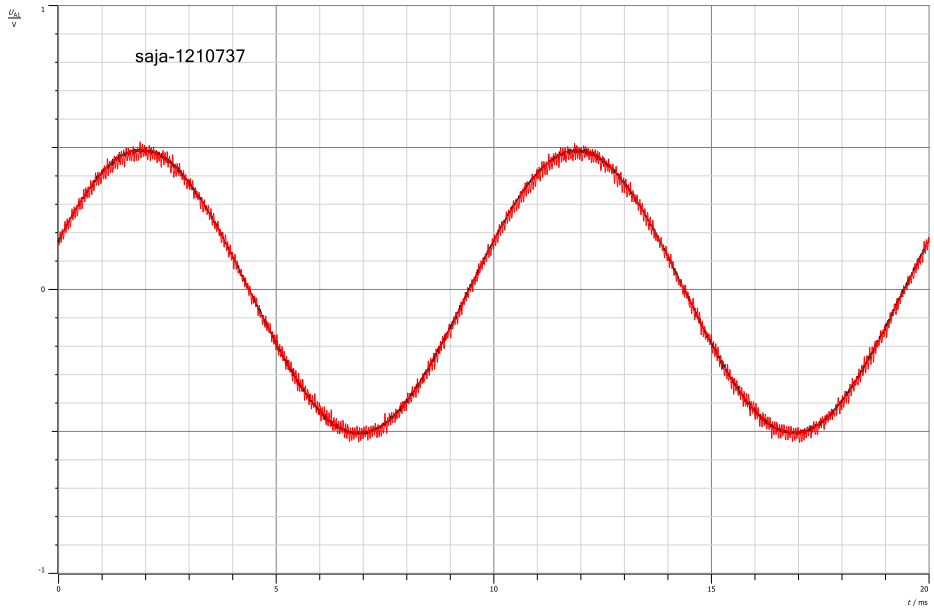

Figure 11:Prediction signal in DCDM at maximum value of f_{clock}=100khz

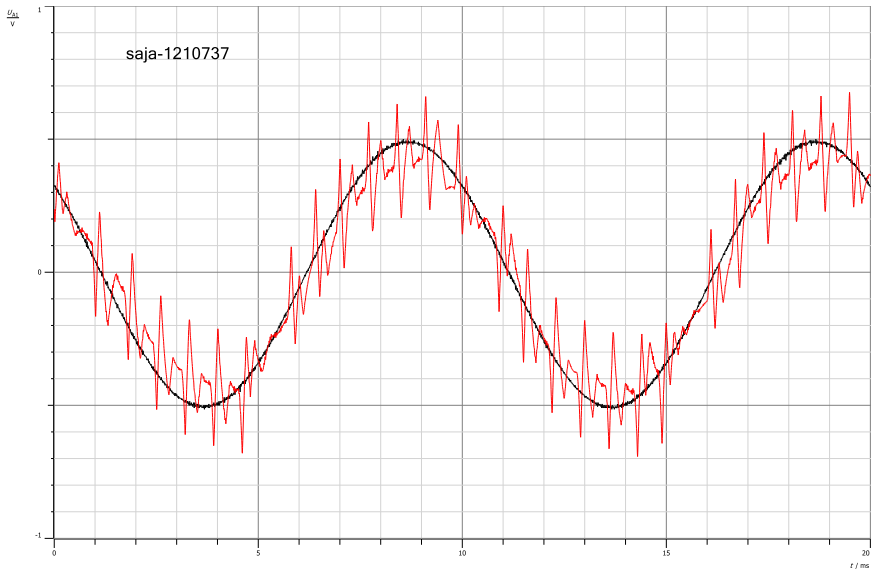

Figure 12:Prediction signal in DCDM at minimum value of fclock=10khz

This section confirmed the conclusion from the previous part: a higher clock frequency leads to a more accurate prediction. When the clock frequency was reduced to 10 kHz, the time increased, and the error became larger compared to when the clock frequency was higher. As a result, the predicted signal did not match the original message signal as closely.

It was also noted that LDM and DCDM differ in their approach:

- LDM uses a fixed step size to quantize the difference between successive samples of the input signal, resulting in a fixed delta and a single reading for prediction. In contrast
- DCDM dynamically adjusts the step size based on the input signal's characteristics, resulting in a variable delta and three readings for prediction.

The key difference between LDM and DCDM lies in how the step size is managed. In LDM, the step size remains constant throughout the modulation process, whereas in DCDM, it is digitally controlled and adapts to changes in the input signal, making DCDM more effective.

3.3 Output signals of the LDM modulator (RZ/NRZ):

The objective of this part is to find the type of signals used to represent the modulated delta signal and the signal used in the feedback path to generate the prediction.

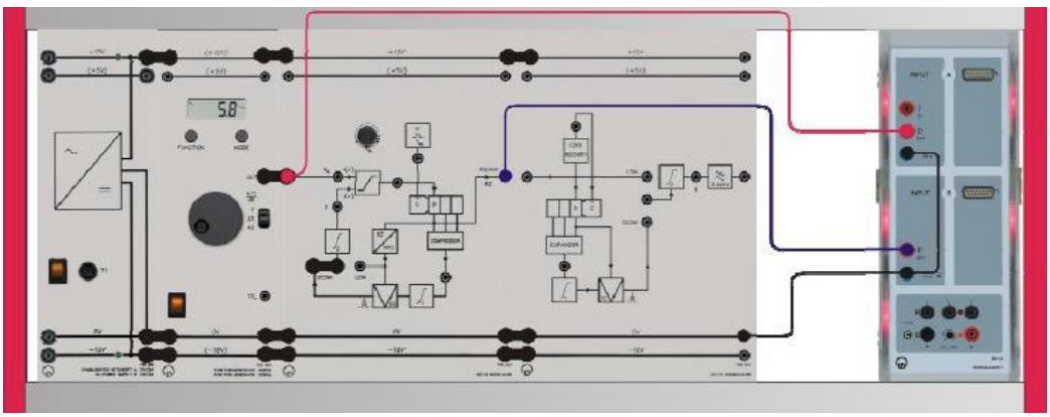

Figure 13:circuit for Output signals of the LDM modulator (RZ/NRZ) part

The clock frequency was set to the minimum value of 10 kHz, and the function generator was configured to produce a sine wave with a frequency of 100 Hz and a peak-to-peak voltage of 1V. The bridging plug was set to LDM (at the input of ∫2). At the input of the integration block (∫2), the LDM signal was connected to the CASSY Sensor UA1, and the DM signal from the output of the DM modulator (bipolar, RZ) was connected to the CASSY Sensor UB1. The F9 key was pressed to start the measurement, and the results are displayed in the following figure:

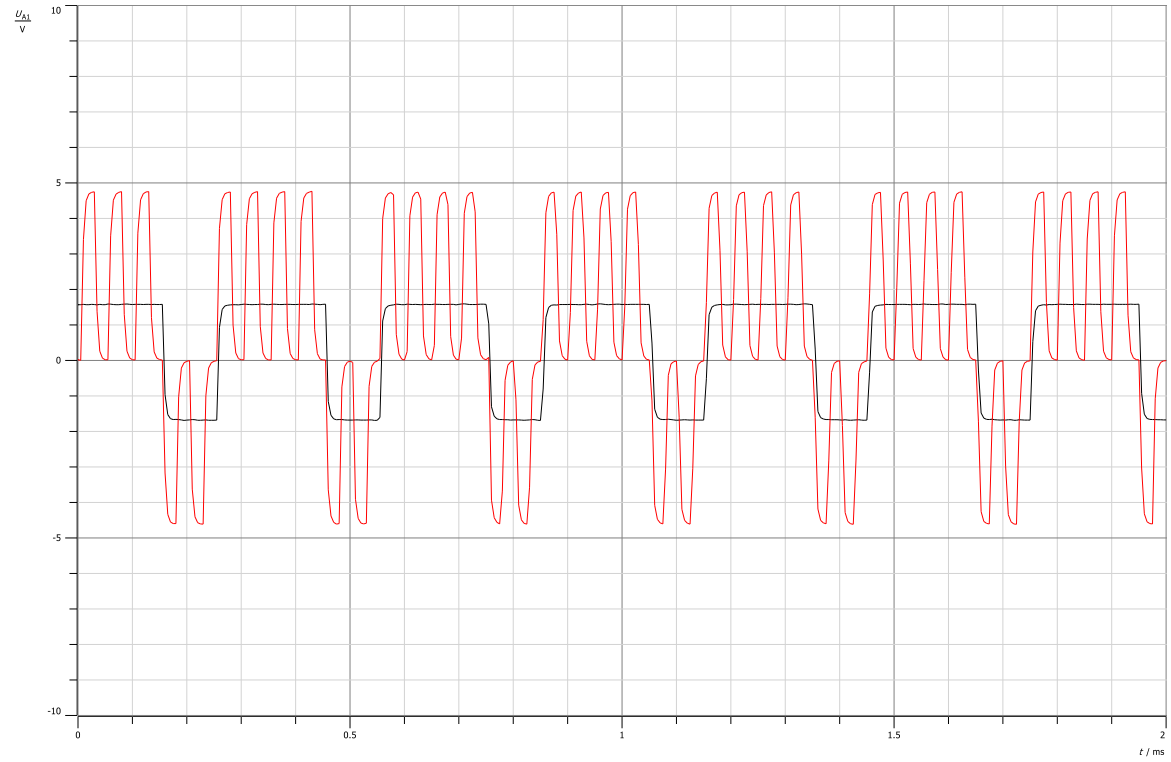

Figure 14:Output signals of the LDM modulator (RZ/NRZ)

It was observed that in the bipolar RZ line coding technique, the first bit '1' was represented by a positive amplitude, while the second '1' was represented by a negative amplitude, with alternating polarity for subsequent bits. Similarly, '0' bits followed the same alternating pattern. Additionally, each bit duration was divided into two equal intervals.

3.4 Granular noise in LDM:

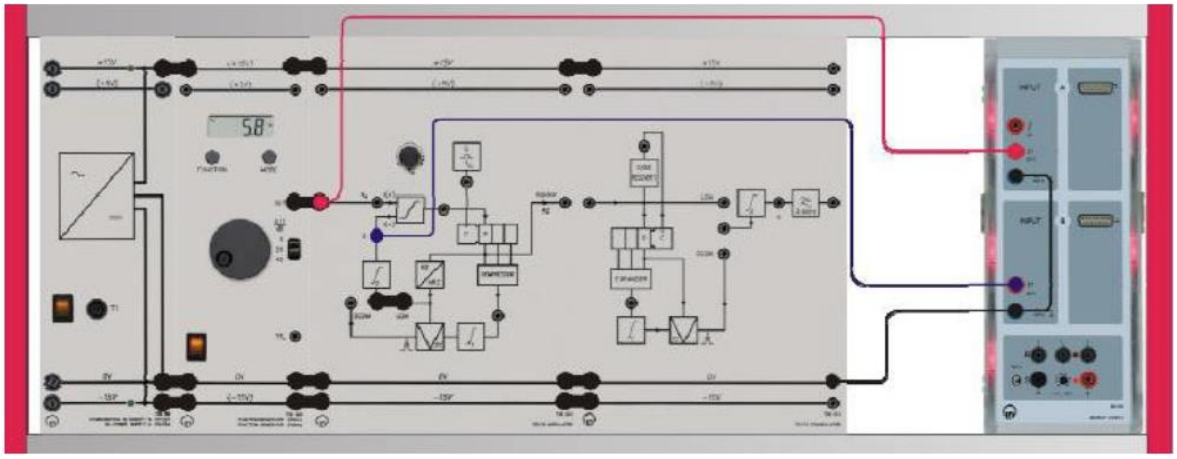

Figure 15:circuit for granular noise in LDM and DCDM

We connect the circuit in figure below setting the clock frequency to the minimum value (10kHz), the function generator to pulse train with fm =200Hz, Vss = 2V and d% = 50 and the bridging plug to LDM at the input of the integrator.

The modulating signal Sm(t) was connected to the CASSY Sensor UA1, while the prediction signal X(t) at the output of the integrator was connected to UB1. The measurement was initiated, and the results are shown below:

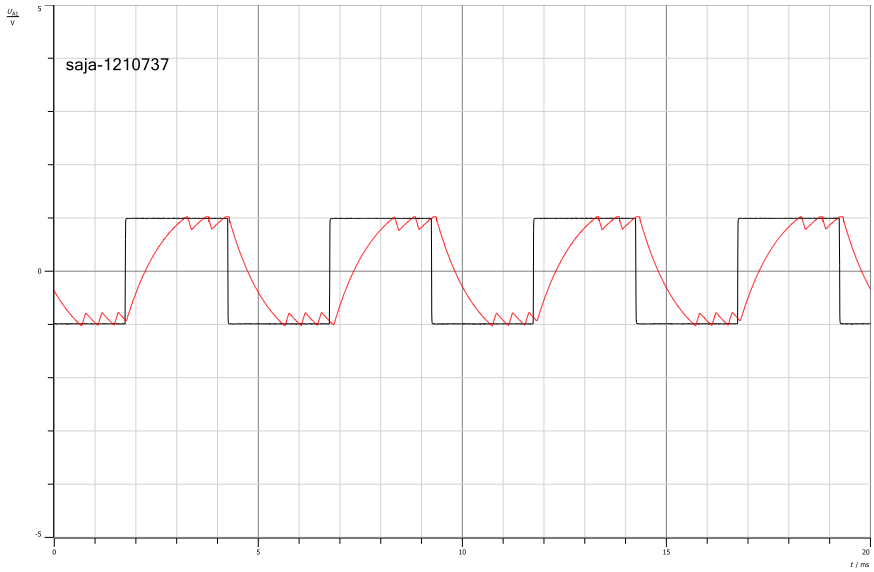

Figure 16: moulating signal m(t) and LDM Predicted Signal X(t) when clock frequency= 10KHz and messege was pulse train

A noticeable error is shown in figure 16 above as the modulator was linear at first and then went up and down at the same period of the stable state, and this causes a little high error.

Then we change the clock frequency to maximum (100KHz) and repeat the measurement :

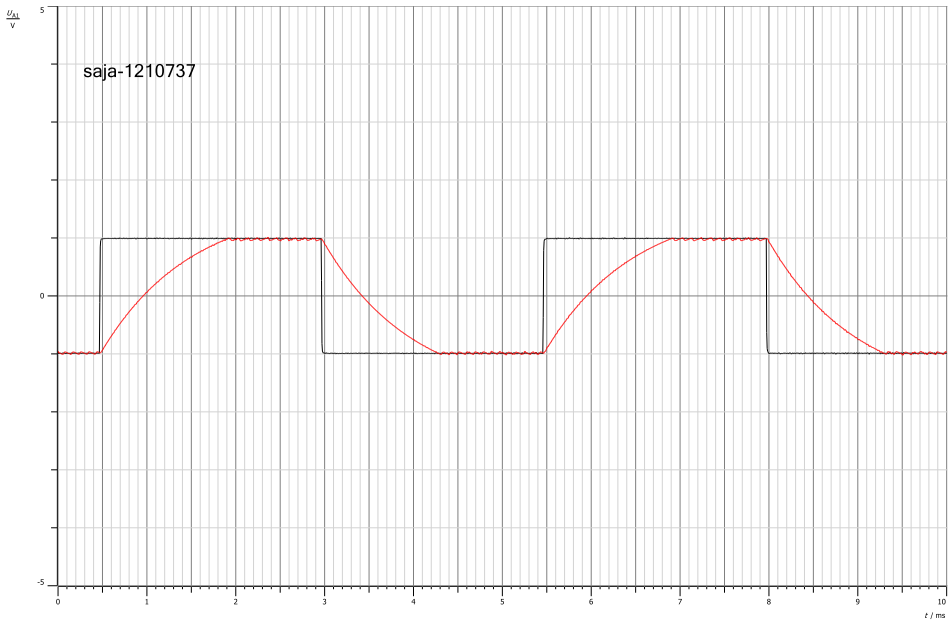

Figure 17:moulating signal m(t) and LDM Predicted Signal X(t) when clock frequency= 100KHz and messege was pulse train

It was observed that increasing the clock frequency reduced the error, as the up and down movements of the predictor became smaller.

Then ,The bridging plug connecting the function generator to the delta modulator input was removed, and the delta modulator input was grounded. The results are shown below:

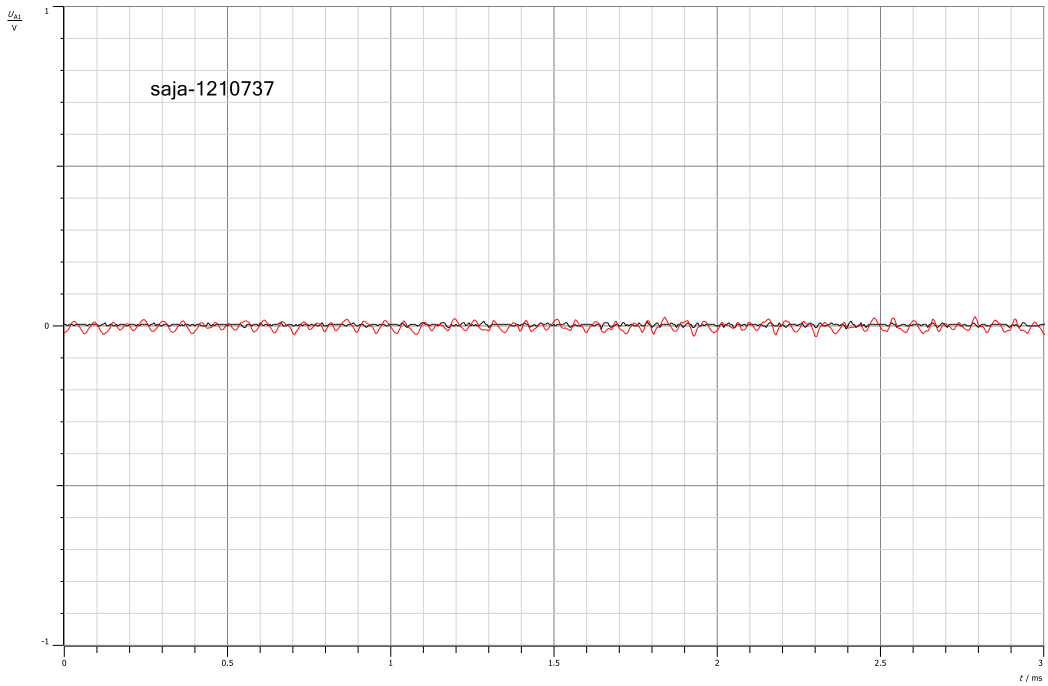

Figure 18:moulating signal m(t) and LDM Predicted Signal X(t) when clock frequency= 100KHz and m(t) =0

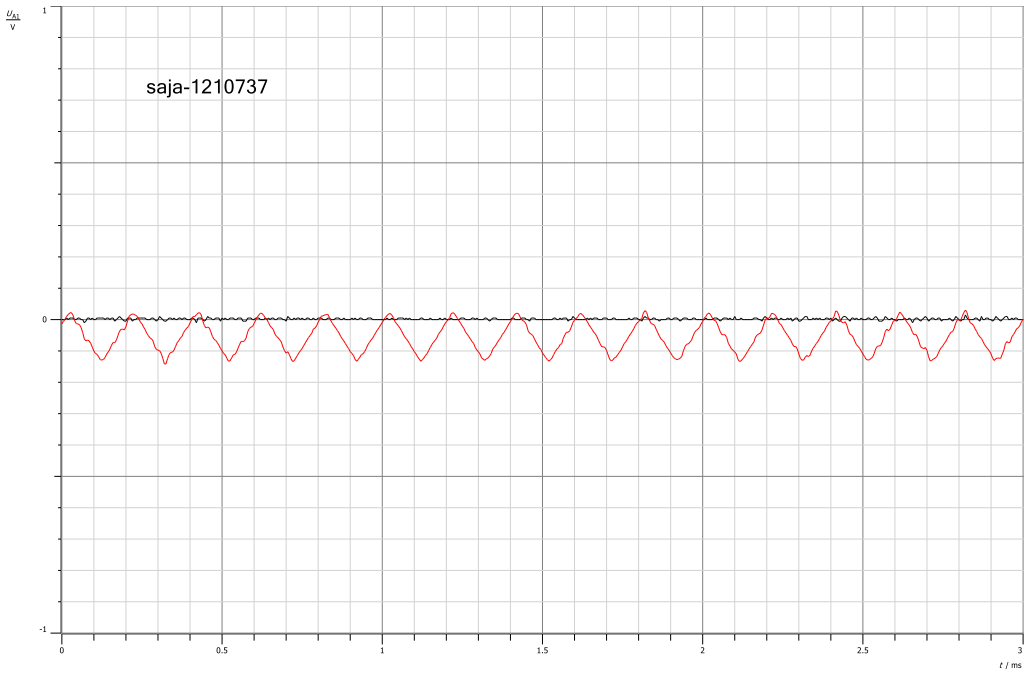

Figure 19:moulating signal m(t) and LDM Predicted Signal X(t) when clock frequency= 10KHz and m(t) =0

It can observed that even when the modulated signal is zero the distortion is less with lower clock frequency.

3.5 Granular noise in DCDM:

We repeat the previous part but with setting the bridging plug at the input of the integrator to DCDM. The results are shown in the following figures:

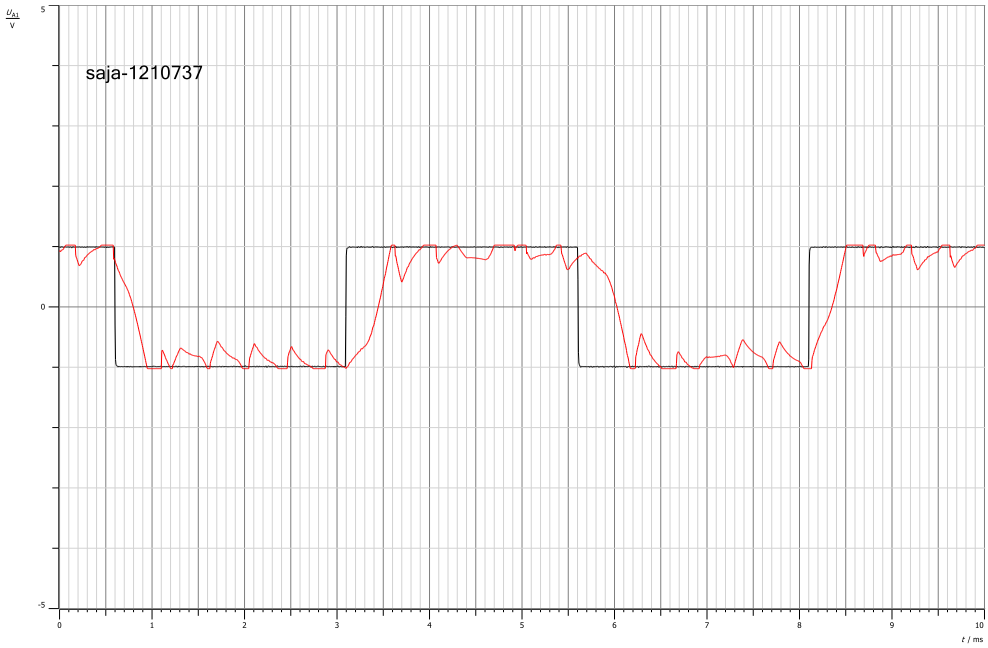

Figure 20:moulating signal m(t) and DCDM Predicted Signal X(t) when clock frequency= 10KHz and messege was pulse train

In Figure 20 , Significant fluctuations were observed, as the modulator moved up and down in relatively large and uneven steps. As a result, the error was substantial due to the lack of a consistent step size, and the adaptive system did not recognize the steady state present in the signal.

Then we change the clock frequency to the maximum value which is 100kHz :

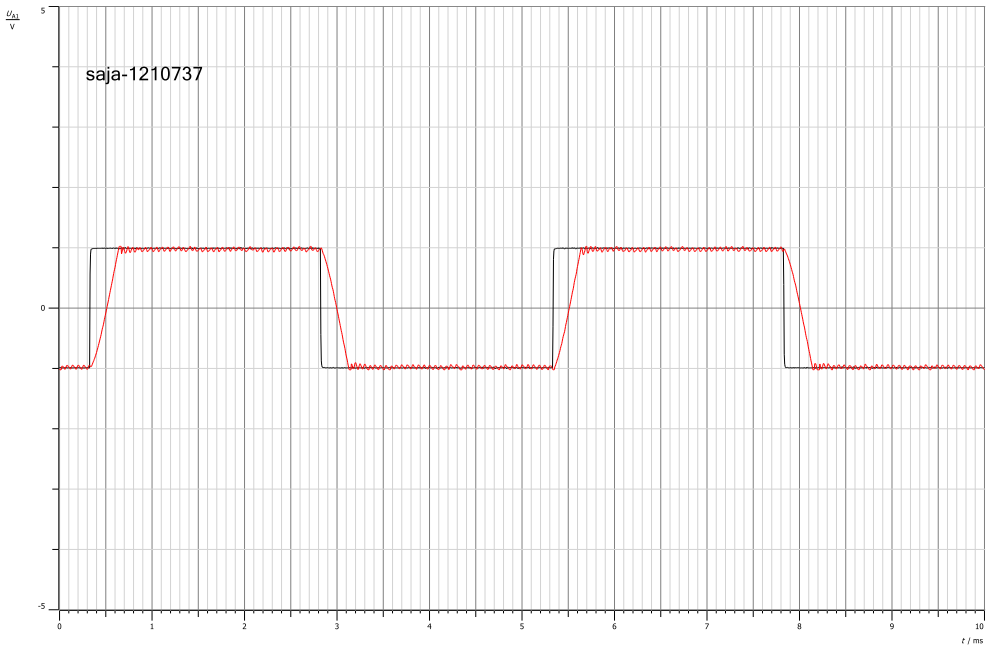

Figure 21: moulating signal m(t) and DCDM Predicted Signal X(t) when clock frequency= 100KHz and messege was pulse train

Notice that As in LDM, increasing the clock frequency minimized the error as now the adaptive became more aware of the steady state.

Then we Remove the bridging plug between the function generator and the input of the delta modulator and Connect the input of the delta modulator to ground and measure in both case which is the clock frequency is maximum (100kHz) and minimum (10kHz)

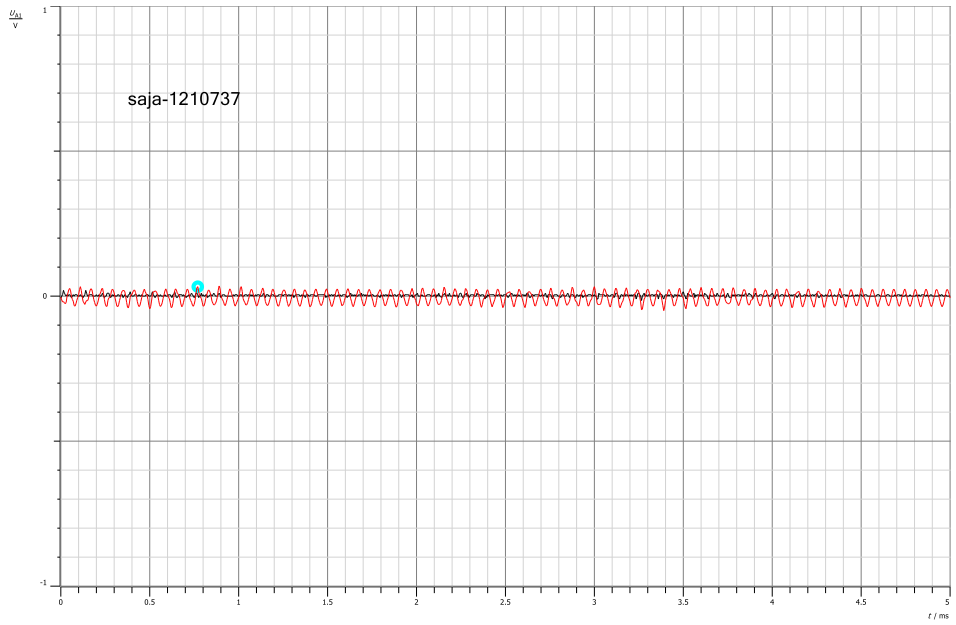

Figure 22:moulating signal m(t) and DCDM Predicted Signal X(t) when clock frequency= 100KHz and m(t) =0

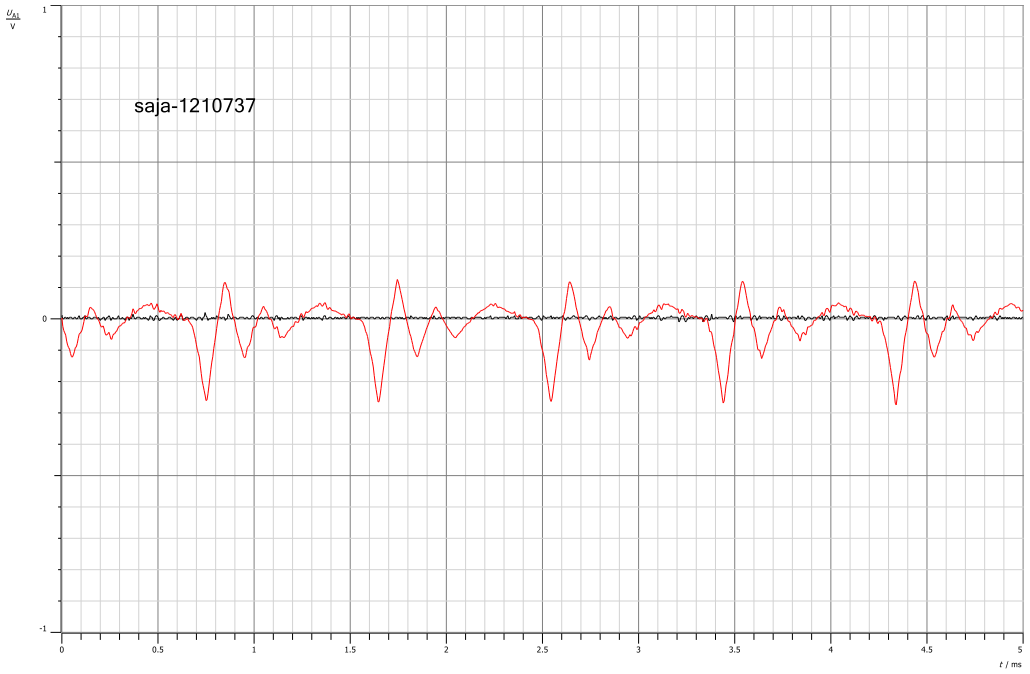

Figure 23:moulating signal m(t) and DCDM Predicted Signal X(t) when clock frequency= 10KHz and m(t) =0

As the fluctuation become larger ,then results now became clearer than in LDM

3.6 Slope-overload in LDM:

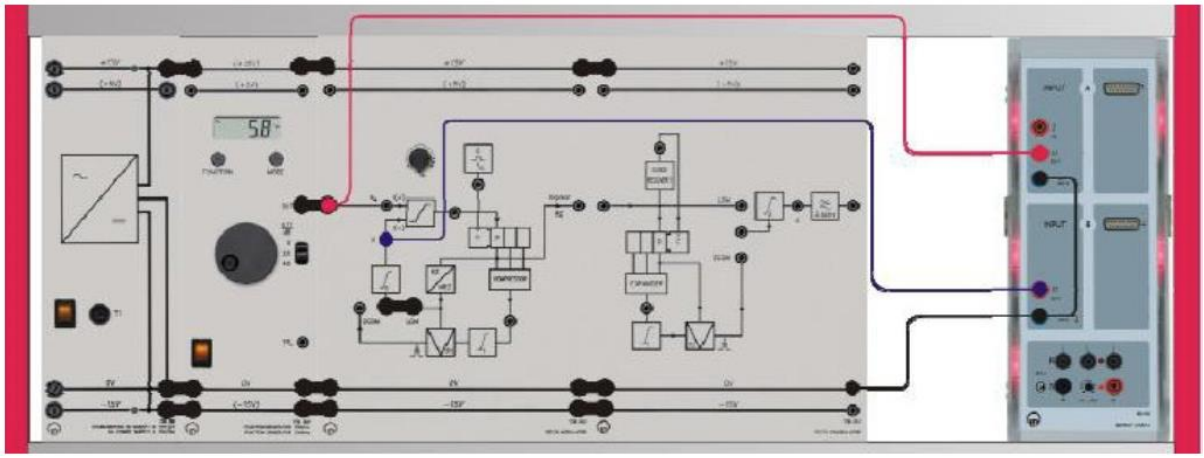

Figure 24: circuit for slop-overload in LDM and DCDM

We connect the circuit in figure 24 above Set the Clock frequency f_{Clock} = 100 kHz (Max) , Set the function generator to Sine, f_m = 100 Hz, V_{SS} = 4 V, Set the bridging plug to LDM (at the input of ∫ 2 , Connect the CASSY Sensor UA1 to the modulating signal $S_m(t)$ and Connect the CASSY Sensor UB1 to the prediction signal X(t) (at the output of ∫2) then start the measurement :

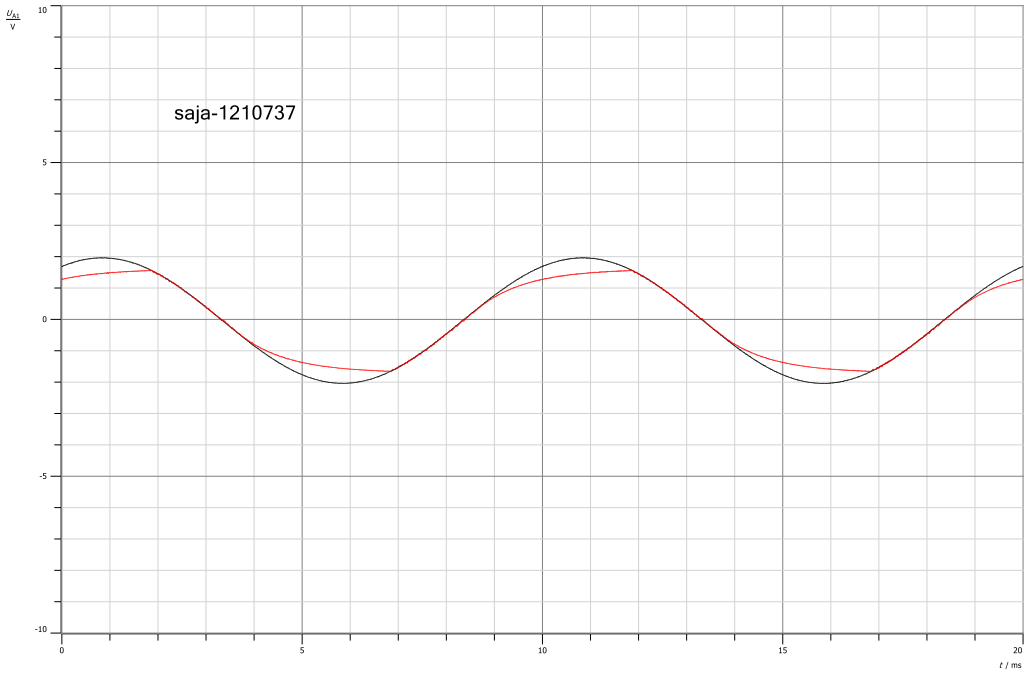

Figure 25:X(t) for 4V 100Hz Sine m(t) in LDM

As illustrated in Figure 25, the predicted signal initially followed the message signal closely without any noticeable error. However, when the input signal's rate of change (slope) exceeded the delta modulator's capacity to accurately track it, discrepancies emerged, and the error became evident.

Then , we Set the function generator to Pulse train, fm = 100 Hz, VSS = 4 V, d% = 50 and repeat measurement :

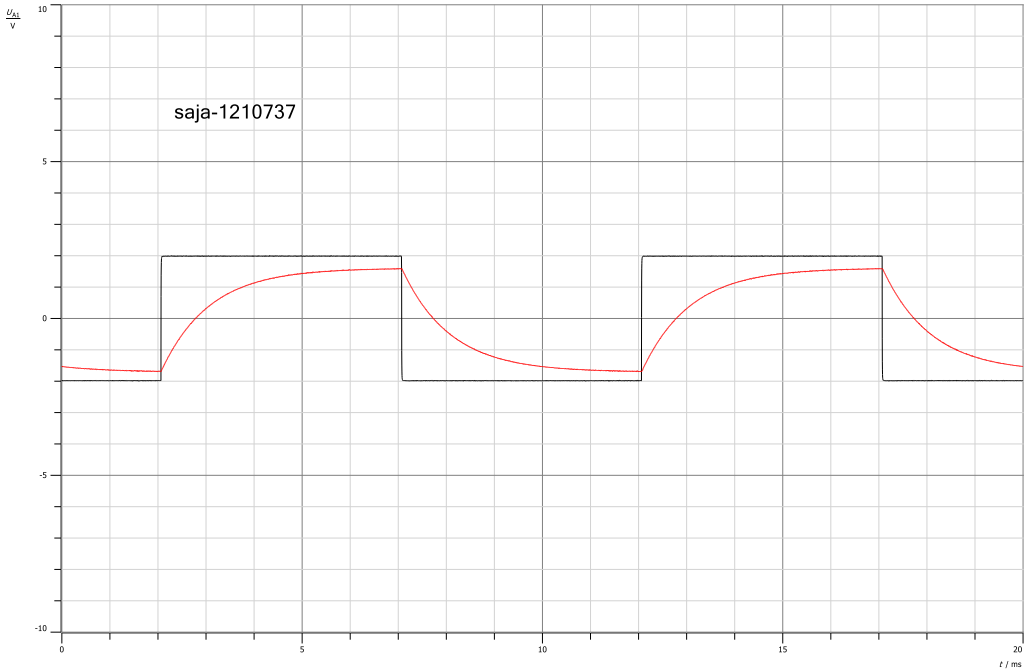

Figure 26:X(t) for 4V 100Hz Pulse train m(t) in LDM

Once again, slope overload occurred when the signal changed at a rate faster than that of the predicted signal, resulting in a significant error that reflected the difference between the two signals.

Then , we Set the function generator to Pulse train, fm = 300 Hz, VSS = 4 V, d% = 50 and repeat the measurement :

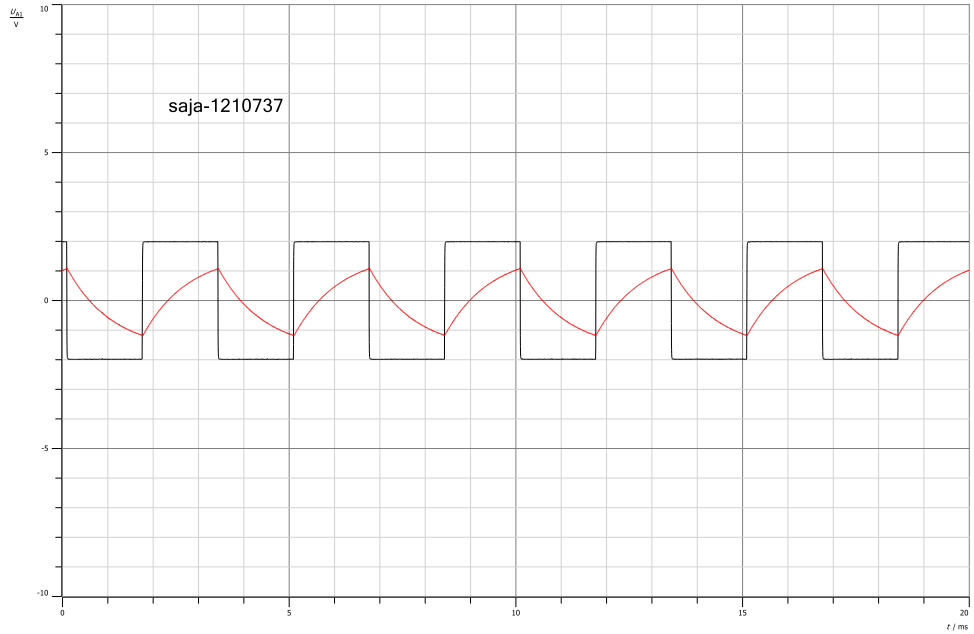

Figure 27:X(t) for 4V 300Hz Pulse train m(t) in LDM

As fm increased, the predictor struggled more to keep up with the message signal. It became evident that when the message signal began to decrease, the predictor mistakenly interpreted this as a signal returning to zero, prompting it to decrease as well, which resulted in a significant error.

3.7 Slope-overload in DCDM:

Same setup is in previous part was used but setting the bridging plug at the input of the integrator to DCDM and all measurements were repeated. The new results are shown below:

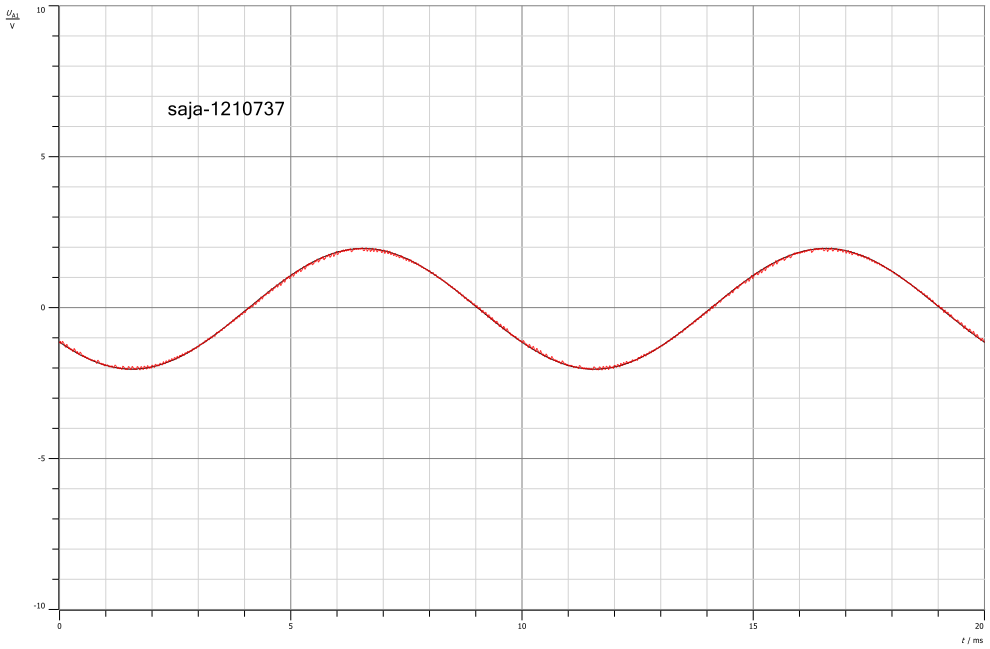

Figure 28:X(t) for 4V 100Hz Sine m(t) in DCDM

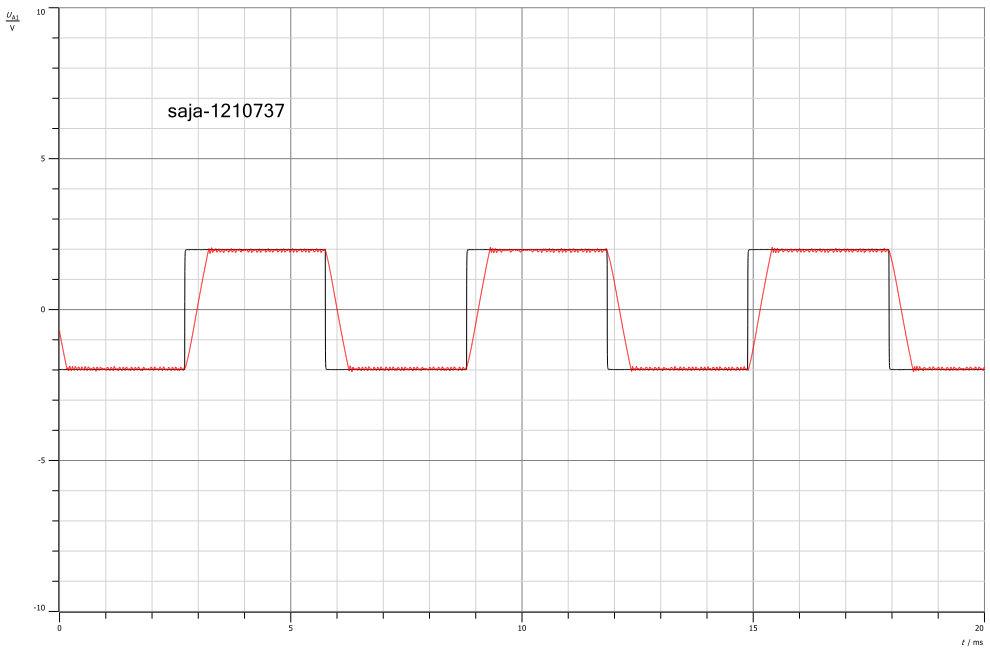

Figure 29:X(t) for 4V 100Hz Pulse train m(t) in DCDM

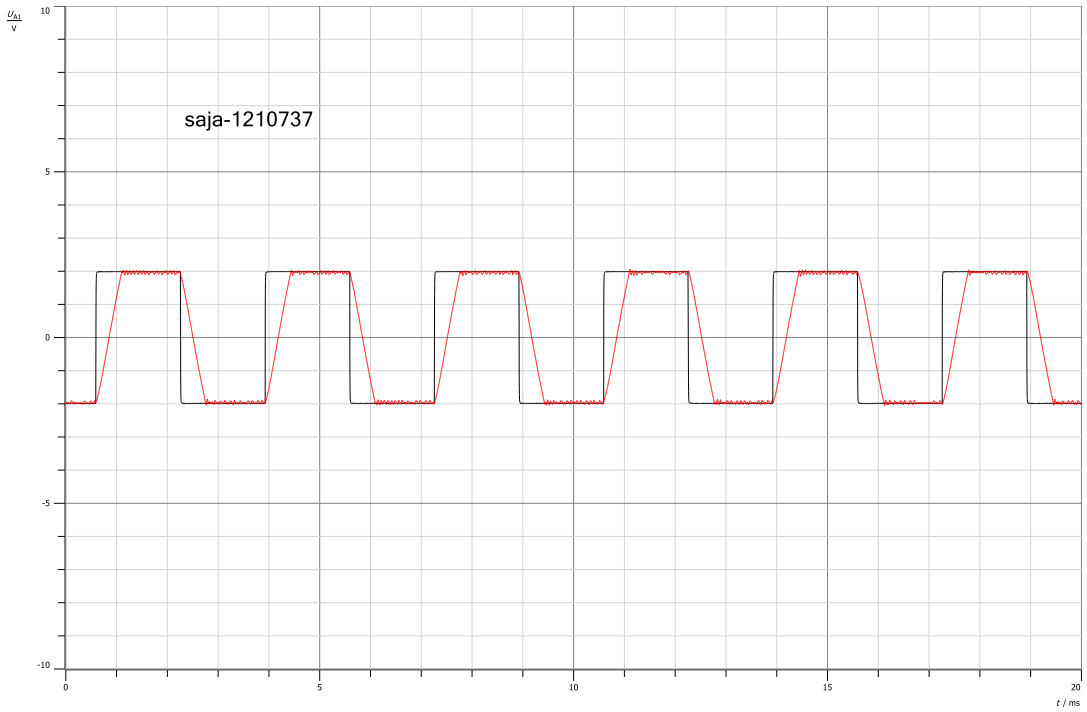

Figure 30:X(t) for 4V 300Hz Pulse train m(t) in DCDM

After observing slope overload in both LDM and DCDM, it was evident that the delta modulator in LDM has a constant step size relative to the sampling interval. When the input signal changed rapidly, this led to slope overload, causing the delta modulator to produce large step sizes to track these quick changes, resulting in substantial errors. In contrast, DCDM benefits from adaptive step size adjustment, enabling it to manage slope overload more effectively and maintain signal integrity.

3.8 Dynamic of LDM and DCDM:

The aim of this part is to to determine the maximum value of the input voltage (for a given frequency) which slope overload can be avoided for the LDM.

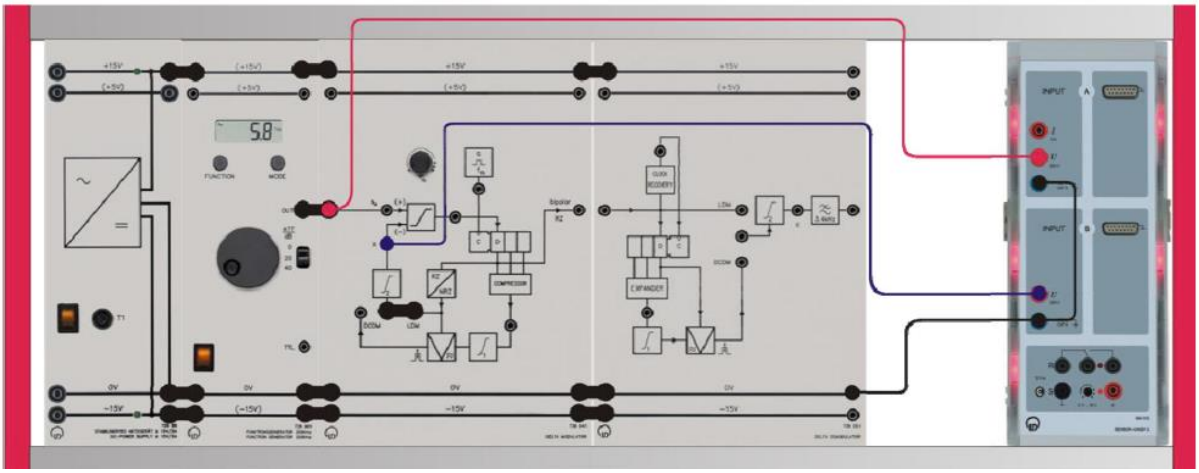

Figure 31:Circuit for dynamic of LDM and DCDM part

We connect the circuit in figure 31 above , Set the Clock frequency f_{Clock} = 100 kHz (max) , Set the function generator to: Sine, fm = 100 Hz, VSS = 1 V , Set the bridging plug to LDM

(at the input of ∫2) and Connect the CASSY Sensor UA1 to the modulating signal Sm(t) , Connect the CASSY Sensor UB1 to the prediction signal X(t) (at the output of ∫2) .
Then Change VSS until the prediction signal *X(t)* shows the beginning of the slope overload. This value is denoted as Amax Record it in Table 1 below.
Then I calculate D by 20 log $(\frac{Amax}{Amin})$db , where Amin is constant equal 20ms vpp which is the value of granular noise:

Table 1: Recorded values for Dynamic of LDM part

Frequency (Hz)	**100**	**300**	**500**	**1000**
Amax for LDM	3.1	1.9	1.2	0.7
D	43.81 dB	39.55 dB	36.56 dB	30.88 dB

The average of D for LDM=$\frac{150.8}{4}$=37.7 dB

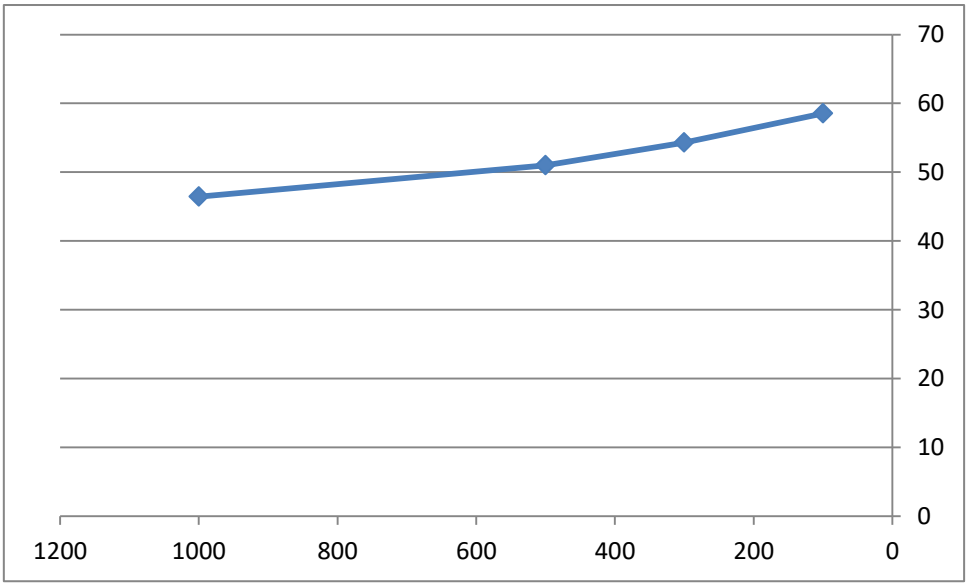

Figure 32: D vs frequency in LDM curve

then we change the bridging plug at the input of the integrator to DCDM, reducing Vss to 1V and repeating the previous measurements
the following table holds the new values:

Table 2:Recorded values for Dynamic of DCDM part

Frequency (Hz)	**100**	**300**	**500**	**1000**
Amax for LDM	16.9	10.4	7.1	4.2
D	58.54 dB	54.32 dB	51 dB	46.44 dB

The average of D for LDM=$\frac{210.3}{4}$=52.575dB

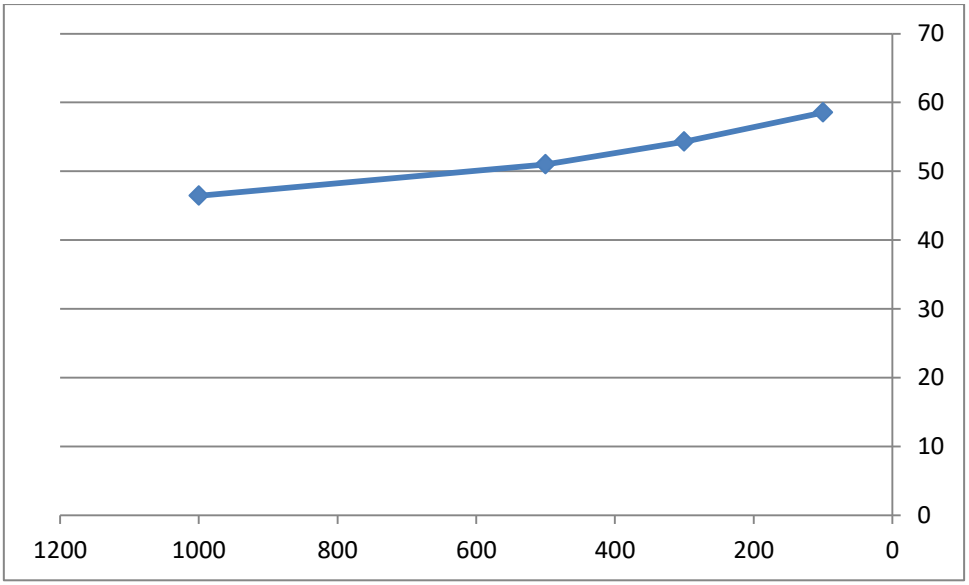

Figure 33:D vs frequency in DCDM curve

The results showed that LDM has a lower dynamic range compared to DCDM, primarily due to its vulnerability to slope overload.

As a result, Linear Delta Modulation (LDM) struggles with slope overload, leading to distortion and poor accuracy when the input signal changes quickly. In contrast, Digital Controlled Delta Modulation (DCDM) is more flexible and better at handling slope overload because it can adjust the step size dynamically. This allows DCDM to track input signal changes more accurately, making it a better choice for high-performance applications.

3.9 Demodulation (LDM/DCDM):

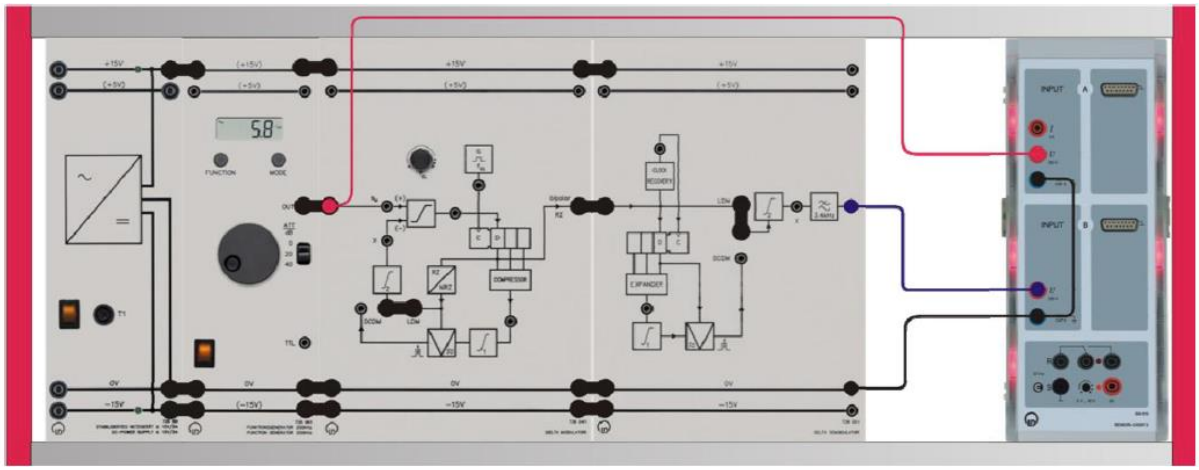

Figure 34:Demodulation circuit

In this part first we connect the circuit in figure 34

Then Set the Clock frequency fClock = 100 kHz (max) , Set the function generator to: Sine, fm = 100 Hz, VSS = 4 V, Set the bridging plug to LDM (at the input of ∫2) in the modulator and the demodulator, Connect the CASSY Sensor UA1 to the modulating signal Sm(t) at the input of the DM modulator , Connect the CASSY Sensor UB1 to the demodulated signal SD(t) at the output of the DM demodulator and start the measurement :

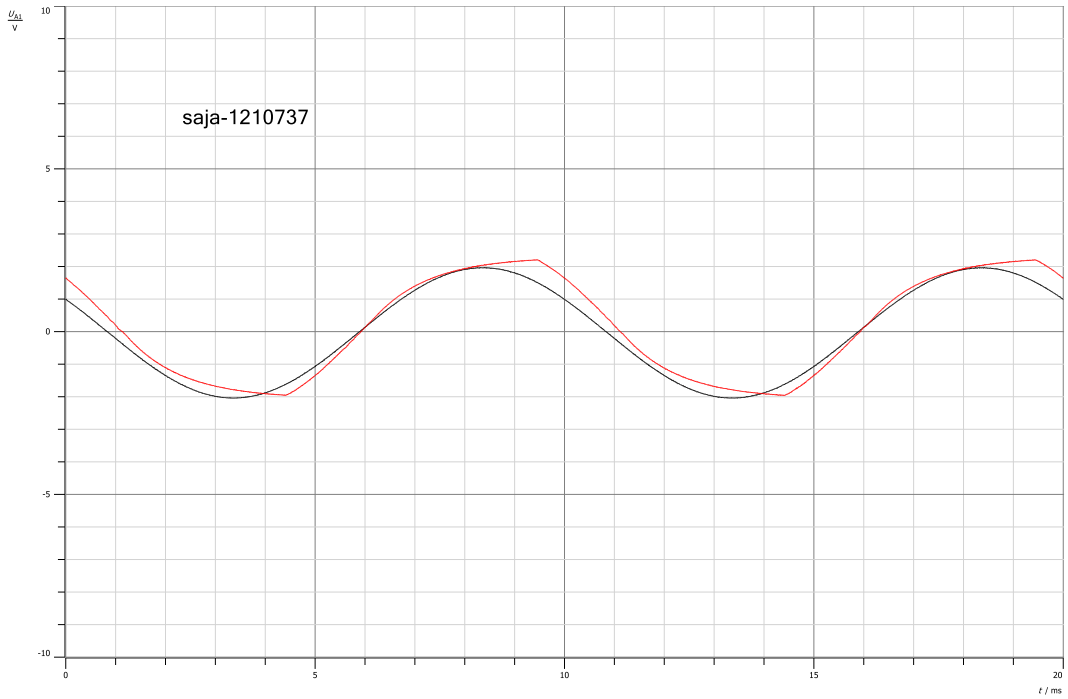

Figure 35:LDM demodulation with sine input.

Then we Set the function generator to: Pulse train, fm=100Hz, VSS=4 d=50% and repeat measurement :

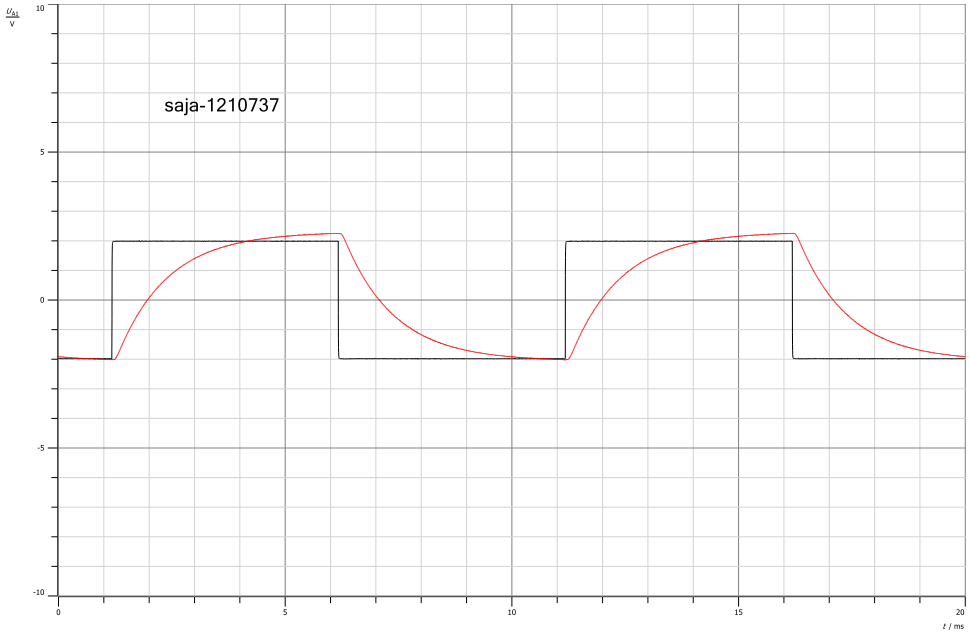

Figure 36:LDM demodulation with pulse train input

as shown in figure 35 and figure 36 , the message signal was partially recovered, but not perfectly. In LDM, demodulation works by integrating the modulated signal to recreate the predicted signal, which is then compared to the actual received signal to determine whether it should increase or decrease. This process is used to reconstruct the original signal by making the necessary adjustments.

And then we repeat the same step but this time set the bridging plug to DCDM(at input of $\int_2$) in the modulator and the demodulator.

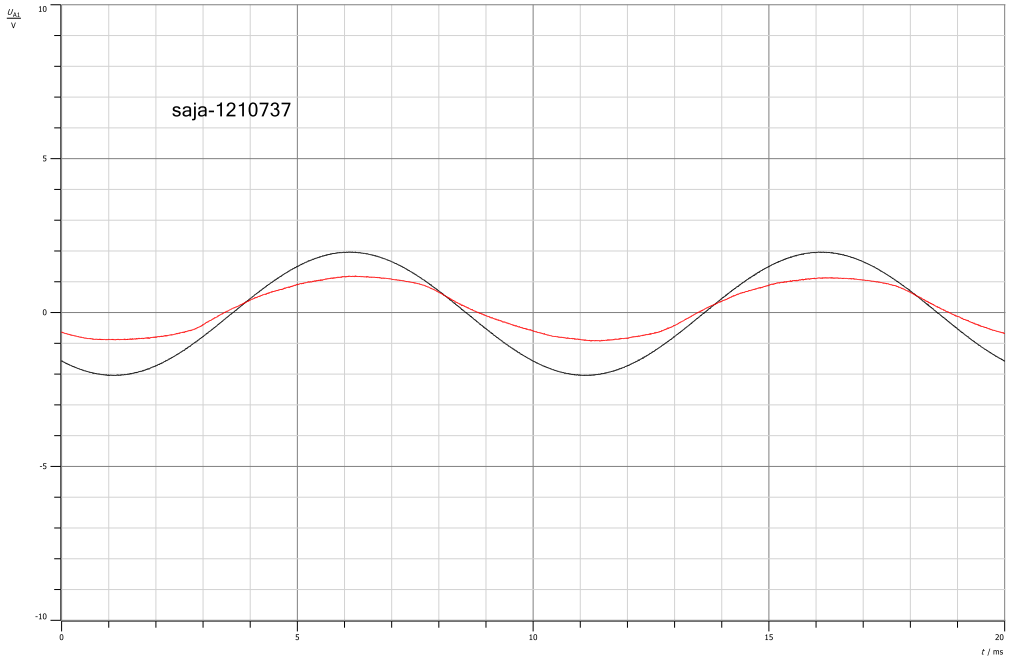

Figure 37:DCDM demodulation with sine

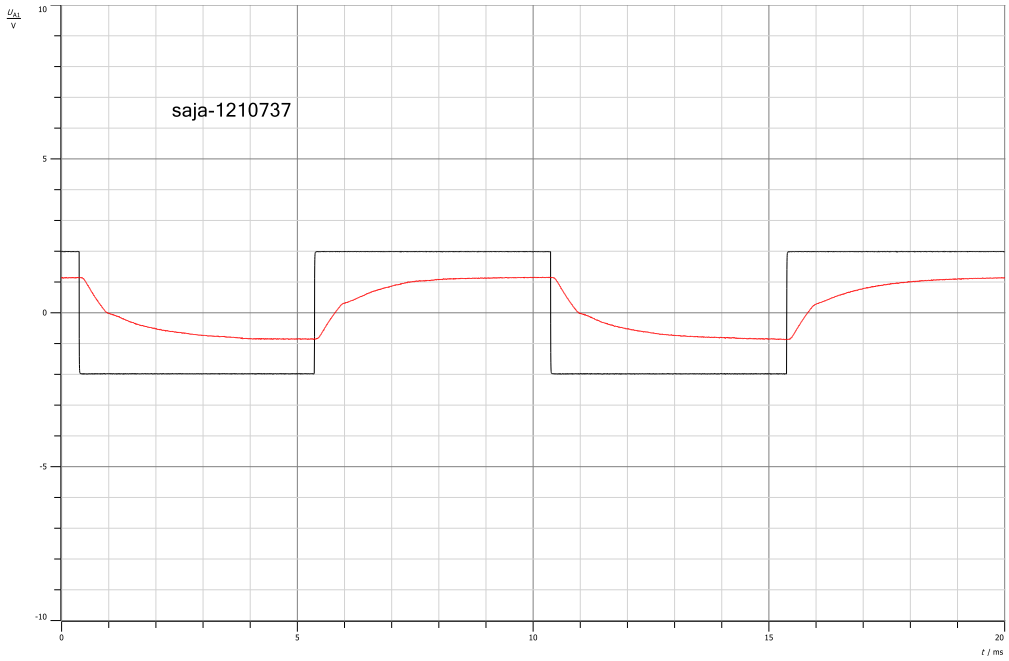

Figure 38:DCDM demodulation with pulse train input with fm = 100Hz

It was evident that the message signal was recovered with only a very small error, indicating an efficient reconstruction.

4.Conclusion:

In conclusion, Delta Modulation (DM) is a form of Differential Pulse Code Modulation (DPCM) that uses a single prediction filter to represent the quantized value of a previous sample. Linear Delta Modulation (LDM) and Digital Controlled Delta Modulation (DCDM) are two types of delta modulation, each with its own pros and cons. Through this experiment, we gained a better understanding of predicted signals, error signals, slope overload, and granular noise. We also studied the modulation and demodulation processes of LDM and DCDM, observed their key differences, and confirmed them through practical experiments. We also learnt about the RZ in the LDM and how the signal returns to zero with each pulse.

The experiment explored the dynamics of LDM and DCDM, highlighting how LDM is limited compared to DCDM. It also examined the demodulation process in both techniques, showing that LDM struggled to recover the message accurately, while DCDM successfully recovered the message with only a very small error.

In the end, the results from the experiment matched the expected ones. The connections were verified by tracing and comparing the results with the values or graphs calculated manually. The theoretical and practical results were nearly identical, and any small errors were likely due to the non-ideal components used or minor unnoticed mistakes in the connections.

5. References :

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[3]https://www.watelectronics.com/what-is-an-adaptive-delta-modulation-its-working/ [Accessed on 9 Aug 2024]

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