Faculty of Engineering and Technology

Electrical and Computer Engineering Department

DIGITAL ELECTRONICS AND COMPUTER ORGANIZATION LABORATORY

ENCS2110

TASK3 LAB8

Student name: Saja Asfour

Student ID: 1210737

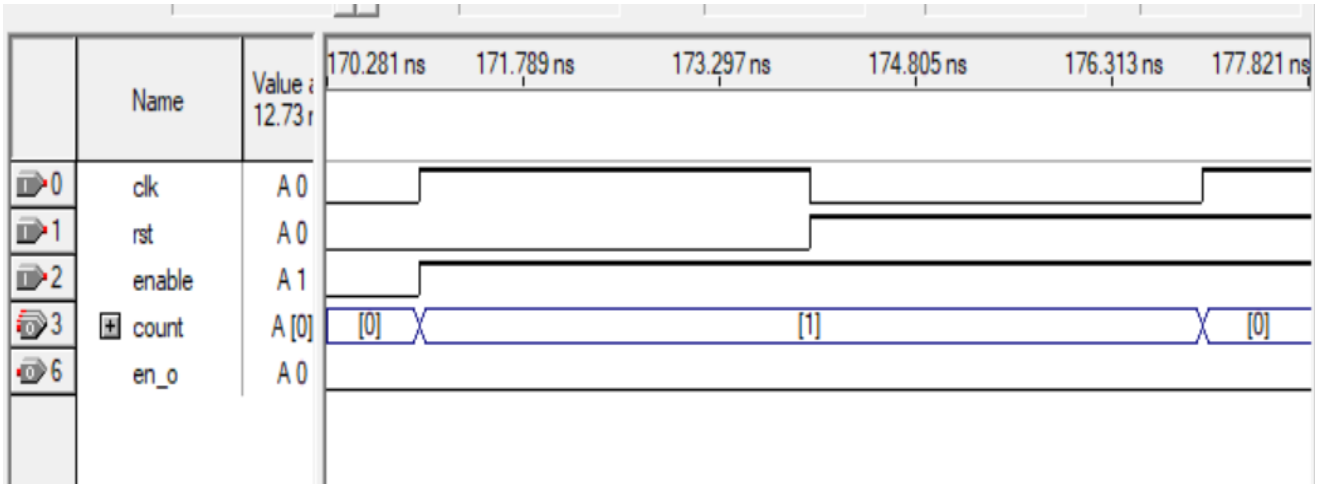
Instructor name: Bilal Karaki

Teacher name: katy sadi

Section number:8

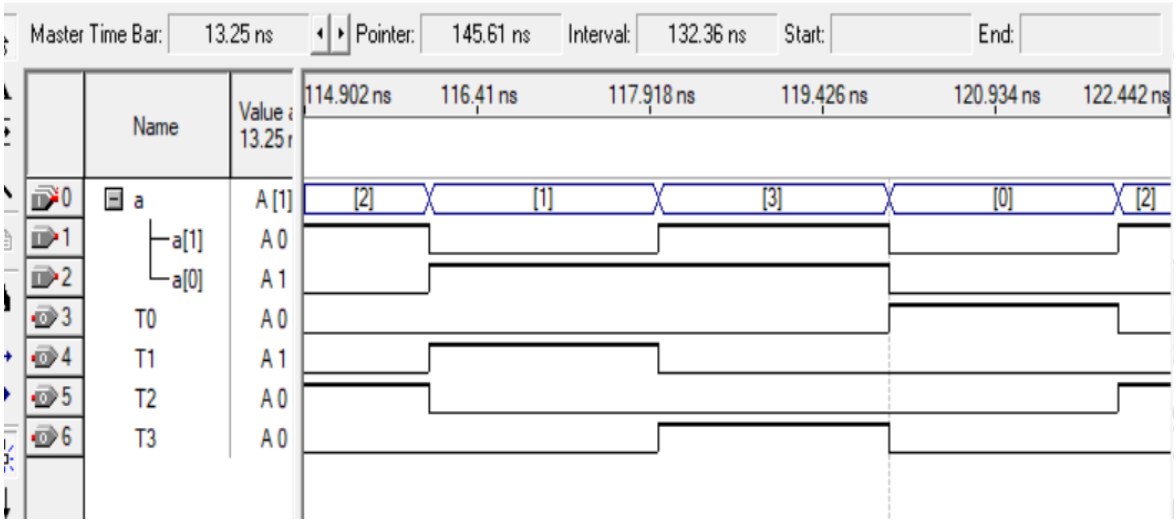
3-First: Use Verilog HDL to implement a 2-bit counter with direct reset input (RESET).

```
module counter2bit(clk,rst,enable,count,en_o);
input clk,rst,enable;
output reg [1:0] count;
output reg en_o;
always@ (posedge clk)
begin
if(rst)//rst==1'b1;
begin
count <=0;
end
else if(enable)
begin
count <=count+1;
end
end
endmodule
```

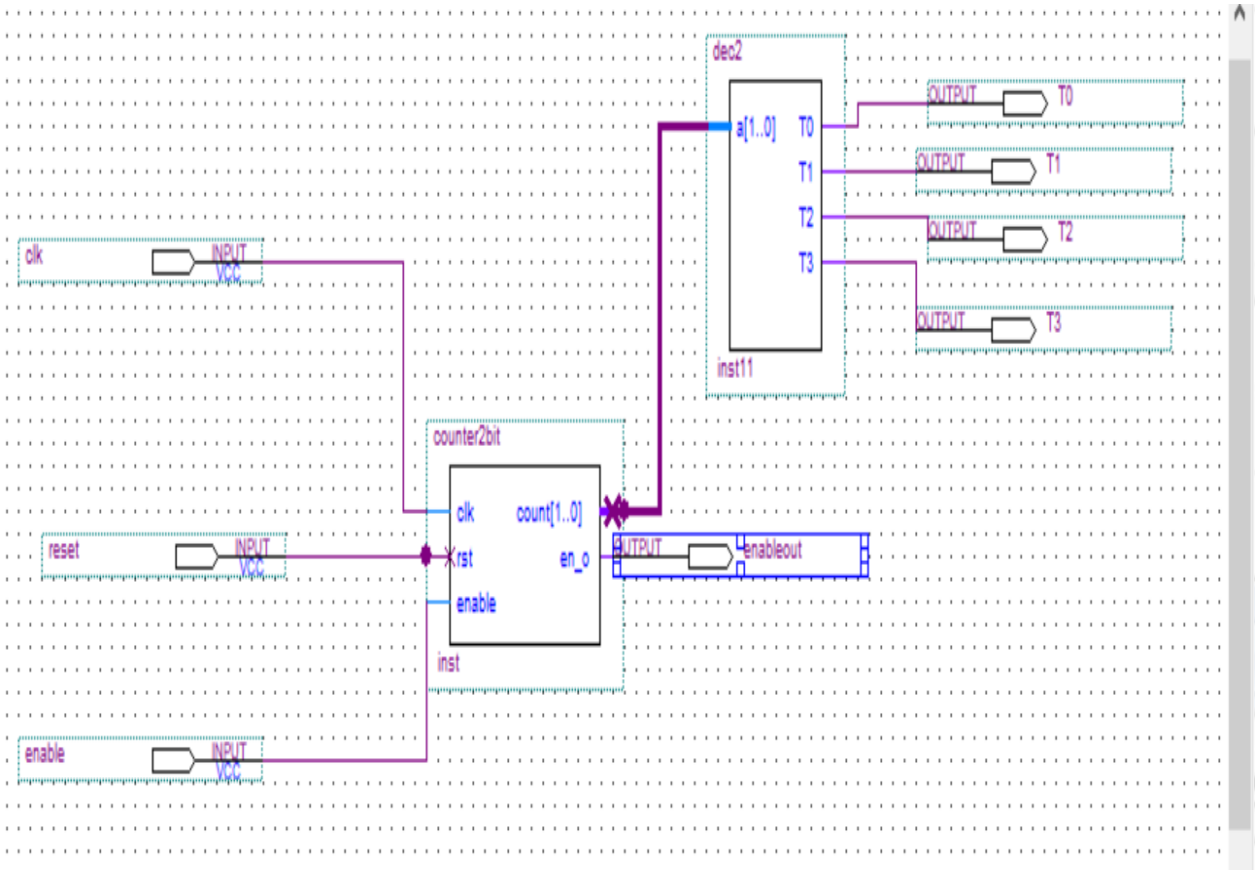


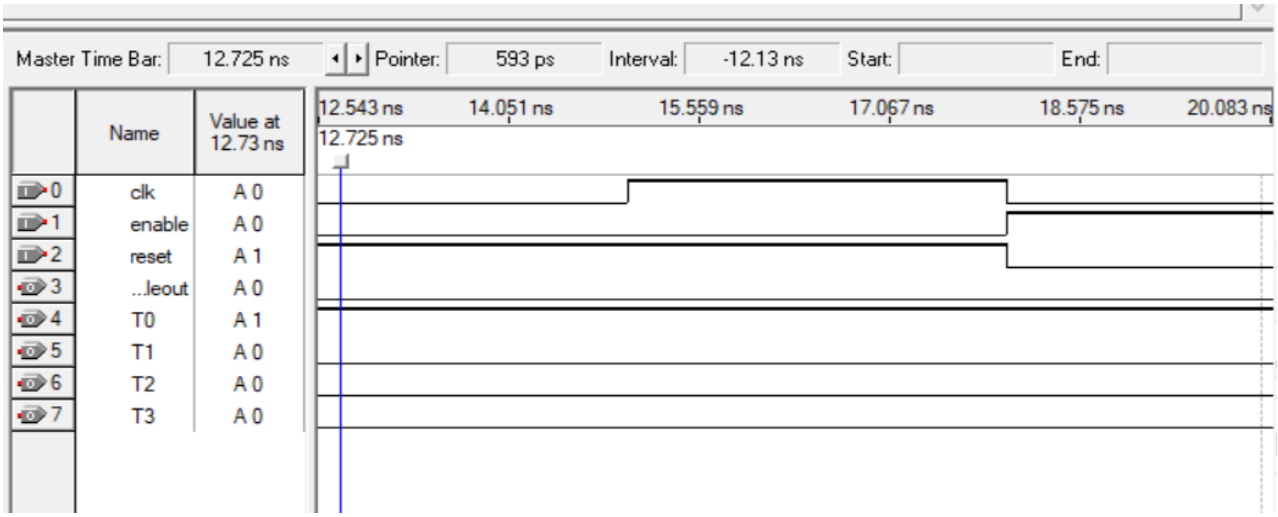
Second: Use Verilog HDL to implement a 2-to-4 Decoder:

```
module dec2(a,T0,T1,T2,T3);
 input [1:0]a;
 output reg T0,T1,T2,T3;
 always@(a)
begin
if(a==0) begin T0=1;
 T1=0;
 T2=0;
 T3=0;
 end
else if(a==1)begin  T0=0;
 T1=1;
 T2=0;
 T3=0;
 end
else if(a==2)begin T0=0;
 T1=0;
 T2=1;
 T3=0;
 end
else begin T0=0;
 T1=0;
 T2=0;
 T3=1;
 end
 end
endmodule
```



Third :Create schematic symbols for both the counter and decoder , then connect them as shown in figure below:


dec2
a[1..0]
T0
T1
T2
T3
OUTPUT
T0
OUTPUT
T1
OUTPUT
T2
OUTPUT
T3
inst11
clk
INPUT
VCC
counter2bit
clk
count[1..0]
reset
INPUT
VCC
rst
en_o
OUTPUT
enableout
enable
inst
enable
INPUT
VCC


Master Time Bar: 12.725 ns
Pointer: 593 ps
Interval: -12.13 ns
Start:
End:
Name
Value at 12.73 ns
12.543 ns
14.051 ns
15.559 ns
17.067 ns
18.575 ns
20.083 ns
12.725 ns
0 clk A 0
1 enable A 0
2 reset A 1
3 ...leout A 0
4 T0 A 1
5 T1 A 0
6 T2 A 0
7 T3 A 0