Faculty of Engineering and Technology

Electrical and Computer Engineering Department

DIGITAL ELECTRONICS AND COMPUTER ORGANIZATION LABORATORY

ENCS2110

Report#2

EXP.No.5.-Sequential Logic Circuits

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Place: Masri107

5.1 Abstract

The aim of the experiment:

-To understand the differences between combinational and sequential Logic circuits ,and the applications of various memory units.

-To study the operating principles and application of various flip-flops.

-To understand the operating principles of counters and how to construct counters with JK flip-flops.

-To study the synchronous and asynchronous counters.

Equipment used in the experiment:

- IT-3000 Basic Electricity Circuit Lab.
- IT-3007 JK Flip-Flop Circuits.
- IT-3008 Flip-Flop Circuits.

Contents :

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5.2 pre-Lab

Design the Logic Diagram, functions table of the SR latch using NOR gates, and explain how it works.

- An SR latch can be built using two NOR gates .
- Two inputs: S(set) , R(reset) and Tow output :Q and Q'.

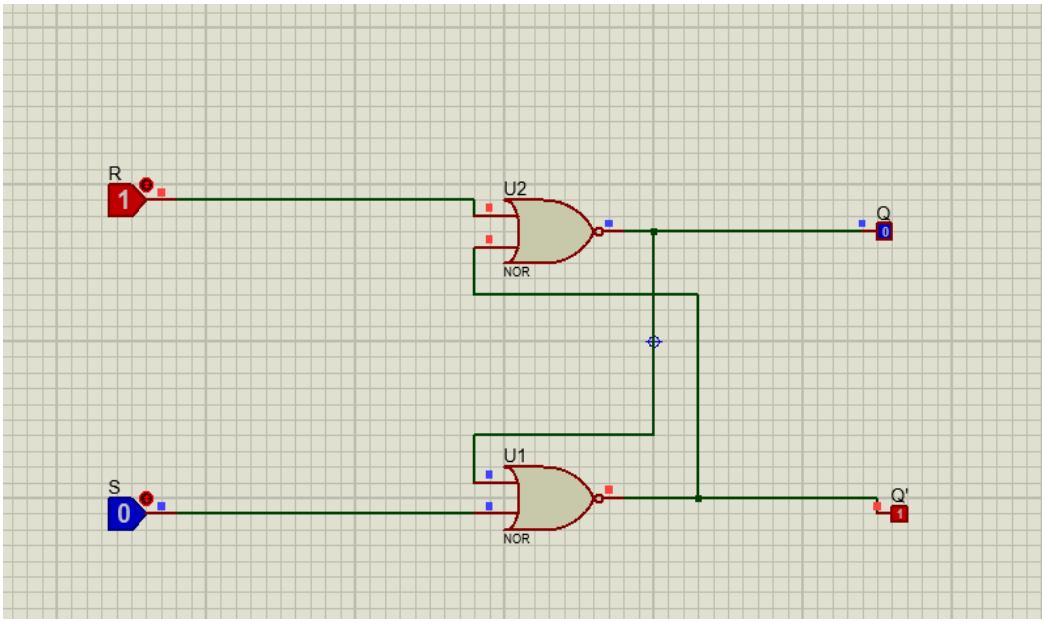


Figure 5.1 SR latch With NOR gates

* if S=1 and R=0 then SET(Q=1,Q'=0).
* if S=0 and R=1 then RESET(Q=0,Q'=1).
* if S=R=0, Q and Q' are Unchanged(memory).
* if S=R=1, Q and Q' are undefined (should never be used).

Input		**Output**	
S	**R**	**Q**	**Q'**
1	0	1	0
0	0	1	0
0	1	0	1
0	0	0	1
1	1	0	0

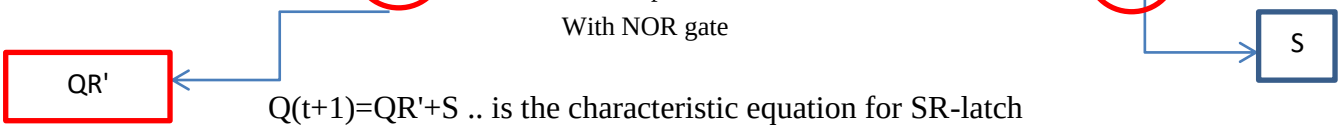
Table 5.1 SR latch with NOR gates truth table(a)

Q(t)	S	R	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	Indeterminate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	Indeterminate

Table 5.2 SR latch with NOR gates truth table(b)

Q \ SR	00	01	11	10
0			X	1
1	1		X	1

Table 5.3 K-map for SR latch
With NOR gate



Q(t+1)=QR'+S .. is the characteristic equation for SR-latch

5.3 Theory

5.3.1 Sequential Circuits :

Any digital circuit could be classified as either combinational or a sequential circuit.

Combinational logic circuit implement Boolean functions. Boolean functions are mappings of inputs to outputs.These circuit are functions of input only.

Sequential circuits consists of:

1- Memory element which is latches or flip-flop that store the present state(previous state).

2- Combinational logic that computes the output and the next state(positive feedback) of the circuit ,output depend on input and current state and next state depends on the inputs and the present state.

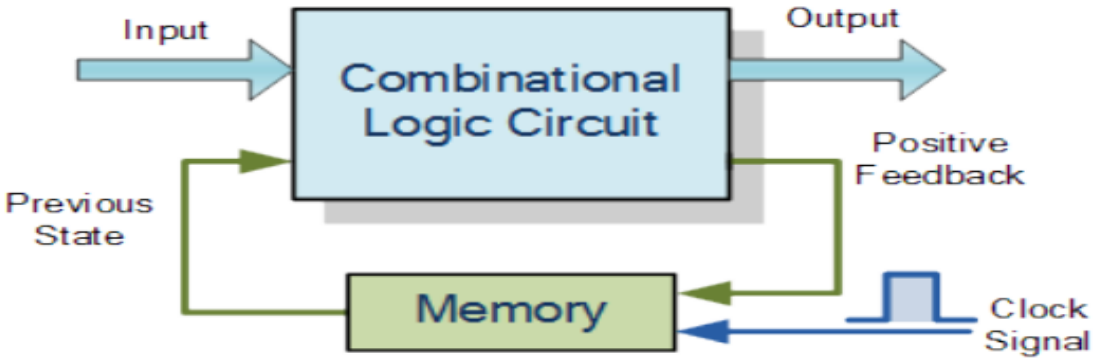


Figure 5.2 Sequential Circuit Block Diagram

-Synchronous sequential circuits use a clock signal that is an input to the memory elements and determines when the memory should be updated.

-The previous state = output value of memory(stored).

-The positive feedback = input value to memory(not stored yet).

-There are two types of memory elements depending on the type of triggering that is suitable to operate.

5.3.2 latches

A latch is a level-sensitive circuit capable of storing one bit of information .latch form one class of flip-flops .This class is characterized by the fact that the timing of the output is not controlled .

-there are a type of latch ,which is

5.3.2.1 The SR(set-reset) Latch

It's a circuit with two input and two output with two cross-coupled NOR(see pre-lab) or NAND gates.

5.3.2.1.1 SR latch with NAND gates:

It's a active low set/reset latch that's mean that :

* if S=0 and R=1 ,then SET(Q=1,Q'=0).
* if S=1 and R=0,then RESET(Q=0,Q'=1).
* if S=R=1, then Q,Q' are unchanged(memory).
* if S=R=0,then Q,Q' are undefined (should never be used).

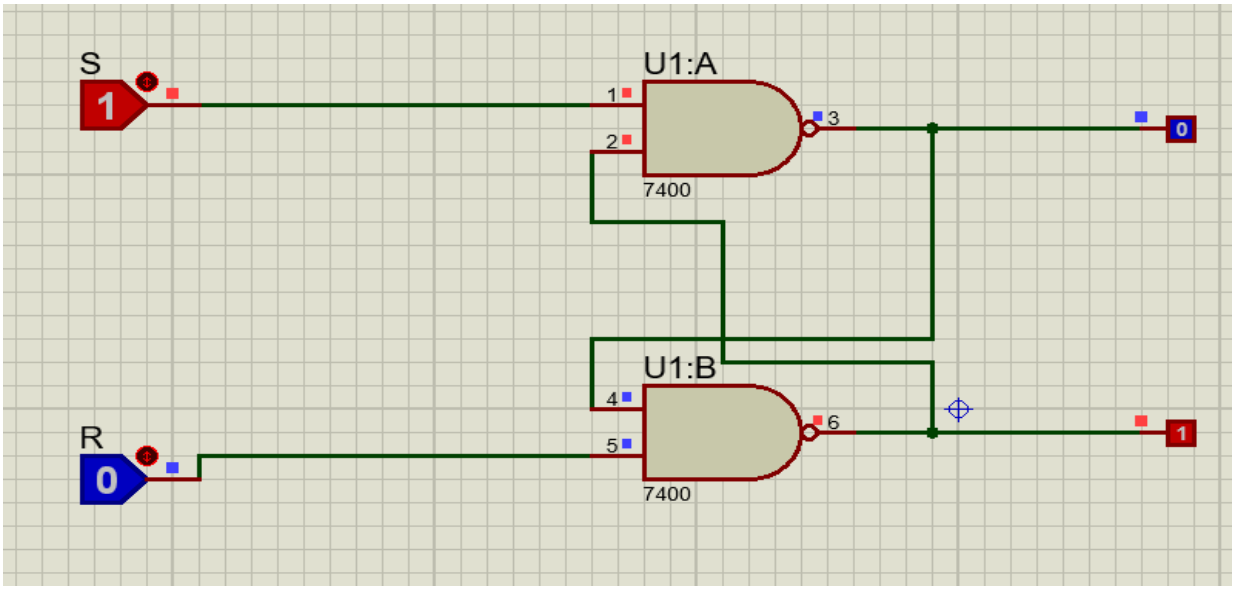


Figure 5.3 SR latch with NAND gates

Input		Output		State
S	R	Q	Q'	
1	0	0	1	SET
1	1	0	1	NO CHANGE
0	1	1	0	RESET
1	1	1	0	NO CHANGE
0	0	1	1	INVALID

Table 5.4 SR latch with NAND gate truth table

5.3.2.1.2 SR latch with control input:

* if c =0 the output Q does not change.
* if c =1 the circuit will work normally .

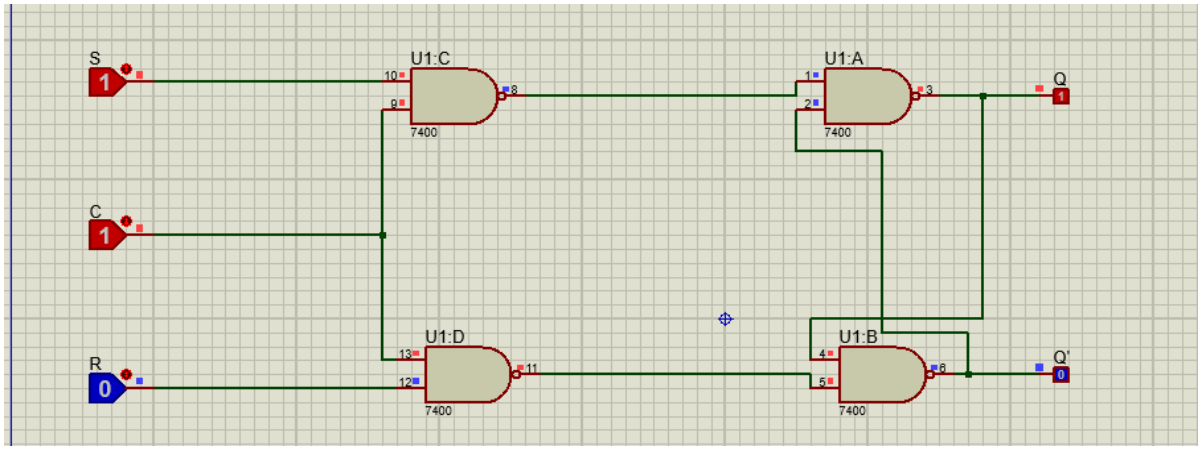


Figure 5.4 SR latch with control input

Output			Input		
C	S	R	Qn+1	Q'	State
0	X	X	Qn	Q'	NO Change
1	0	0	Qn	Q'	NO Change
1	0	1	0	1	RESET
1	1	0	1	0	SET
1	1	1	0	0	Indeterminate

Table 5.5 SR latch with control input truth table

5.3.2.2 The D-Latch

The D-Latch was developed to eliminate the undefined condition of the indeterminate state in the SR latch.

-only one data input D.

-An invertor is added :S=D and R=D'.

-S and R can never be 11 simultaneously so no undefined state.

-When C=0, Q remains the same(No change in state).

-When C=1, Q=D and Q'=D'.

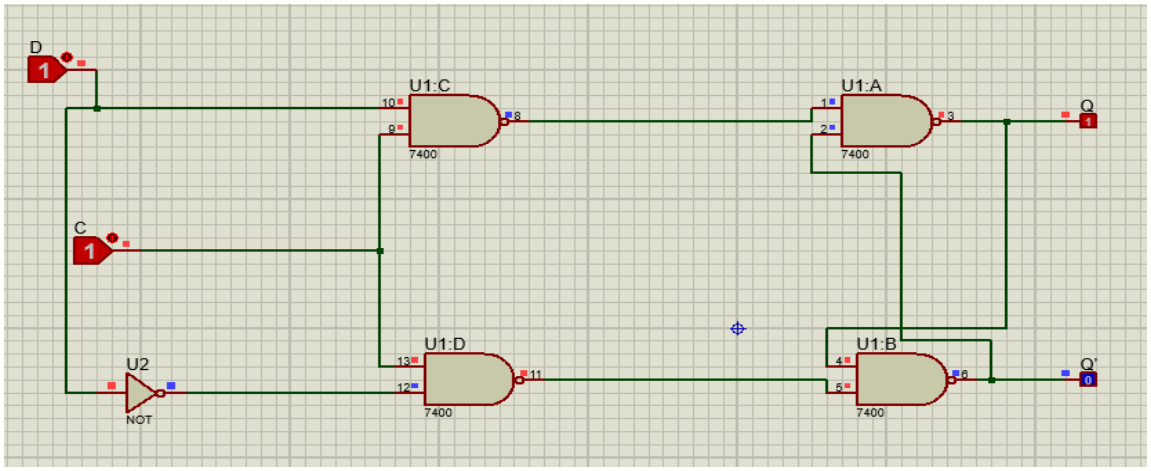


Figure 5.5 The D-Latch

Input		Output		State
C	D	Qn+1	Q'	
0	X	Qn	Q'	NO Change
1	0	0	1	RESET
1	1	1	0	SET

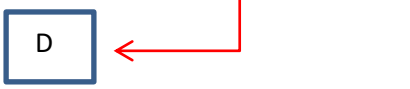
Table 5.6 D-Latch truth table(a)

Qn	D	Qn+1
0	0	0
0	1	1
1	0	0
1	1	1

Table 5.7 D-Latch truth table(b)

Q \ D	0	1
0		1
1		1

Table 5.8 k-map for D-Latch



-The Characteristic Equation of the D-Latch is: Qn+1=D.

5.3.3 Flip-Flops

*****A Flip-Flop is a better memory element for Synchronous circuits because it solve the problem of latches.

*Like latch flip-flop are also used for storing binary information, but the difference is:

-The output change in flip-flop occurs only at the clock edge while in the latch it occurs at the clock level.

There are many type of latch which is:

5.3.3.1 D-Flip-Flops

-The D flip-flop is the most commonly used type.

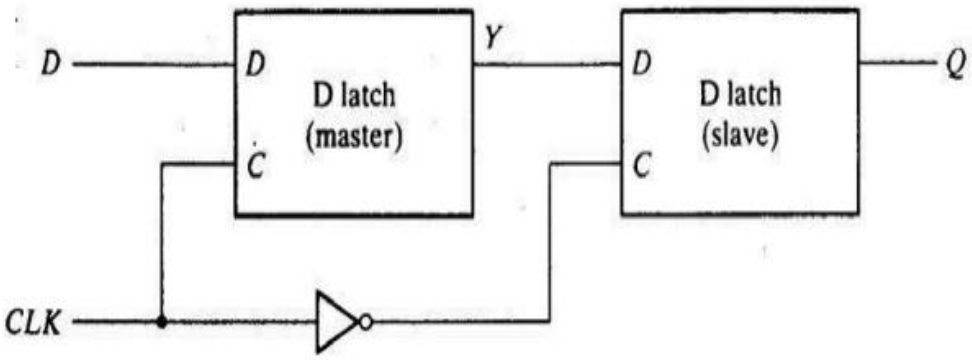


Figure 5.6 D-Flip-Flops implemented with two D-Latch

Figure 5.7 D-Flip-Flops

D	Q(T+1)	State
0	0	Reset
1	1	Set

Table 5.9 D-Flip-Flop truth table

5.3.3.2 JK Flip-Flops

-the JK flip-flop is another type of flip-flop with input: J,K, and Clk.

-when JK =10 then set ,When JK =01 then reset

-When JK=00 then No change , When JK=11 then invert outputs

Figure 5.8 JK Flip-Flops

J	K	Qt+1
0	0	Q
0	1	0
1	0	1
1	1	Q'

Table 5.10 JK Flip-Flop truth table

5.3.3.3 T Flip-Flops

- The T(Toggle) flip-flop has inputs: T and Clk.
- When T=0 then No change , When T=1 then invert output.

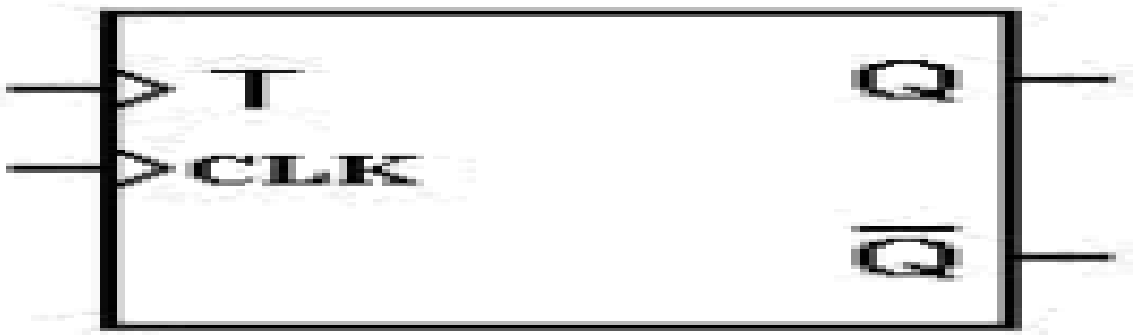


Figure 5.9 T Flip-Flops

T	Qt+1
0	Q
1	Q'

Table 5.11 T Flip-Flop truth table

5.3.4 Registers

-The registers is a collection of flip-flops ;N bit register consists of N flip-flops use to hold binary entities.

-All the flip-flops are driven by a common clock, and all are reset simultaneously.

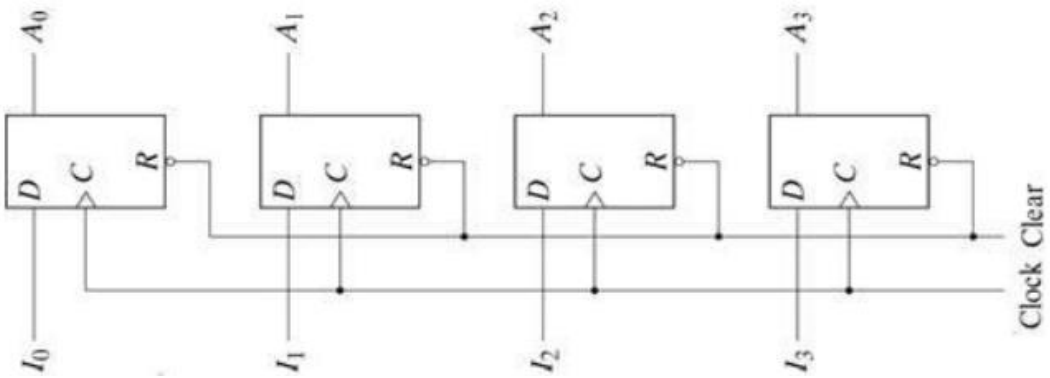


Figure 5.10 4-bit Register

5.3.4.1 shift register

-The shift register is a group of flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flip.

- shift can be right or left.

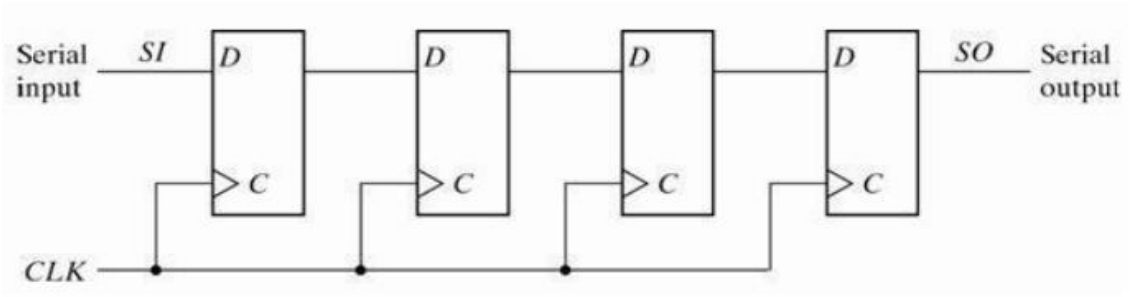


Figure 5.11 4-bit shift- right register

5.3.5 Counters

- The counter is a special type register that goes through a prescribed sequence of states, there are two types of counters:

5.3.5.1 Ripple counter :

It's an asynchronous counter, it counts up to 2 n states, it is known by that name due to the way the clock pulse ripples its way through the flip-flops.

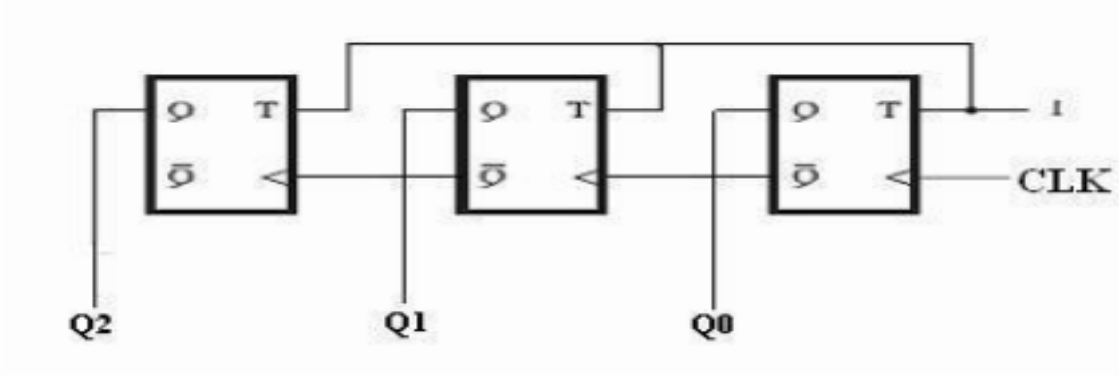


Figure 5.12 3-bit ripple counters

5.3.5.1 Synchronous counters:

in this counters all flip-flop receive a common clock.

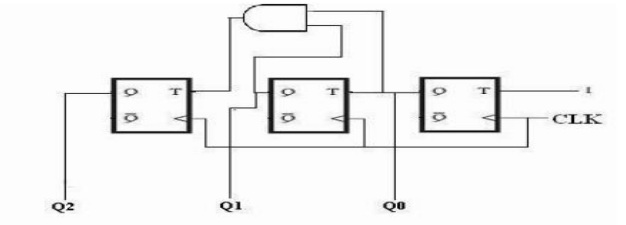


Figure 5.13 3-bit Synchronous counter

5.4 Procedure

5.4.1 latches and flip flops:

5.4.1.1 Constructing RS latch with Basic Logic Gates:

-We use IT-3008 module to construct the circuit , connect +5v of module IT-3008 to the +5v output fixed power supply and GND of module IT-3008 to GND output of fixed power supply.

-Connect A3,A4 to Switches SW1,SW2

-Connect outputs F6,F7 to Logic Indicators Leds.

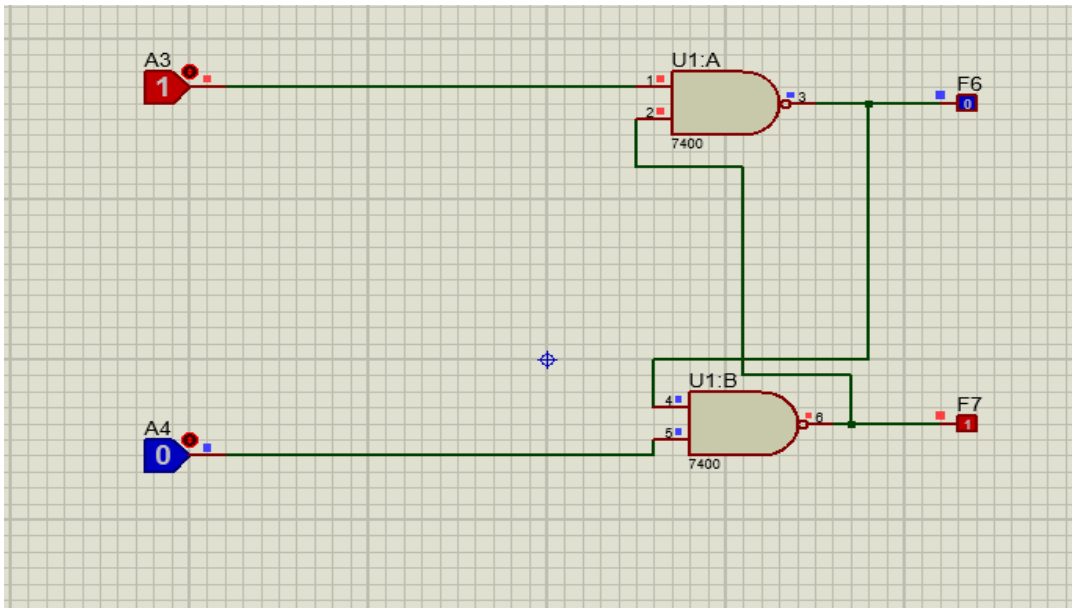


Figure 5.14 RS latch

Input		Output	
A3	A4	F6	F7
0	0	1	1
0	1	1	0
1	0	0	1
1	1	0	0

Table 5.12 Data for RS latch

* We noticed that when A3 and A4 were set to equal zero, both Q and Q' became 1 which is not allowed, so this case is prohibited , if A3=0 and A4=1 ,then Q would equal 1 and be at the SET state, when reversing both input(A3=1,A4=0) then Q will be at the RESET state (equal 0), if both inputs were set to equal 1, no change will happen to the output it will remain the same as before.

5.4.1.2 Constructing RS latch with control input:

- We use IT-3008 module to connect the circuit.

- Connect inputs A1,A5 to switches SW1,SW2 .

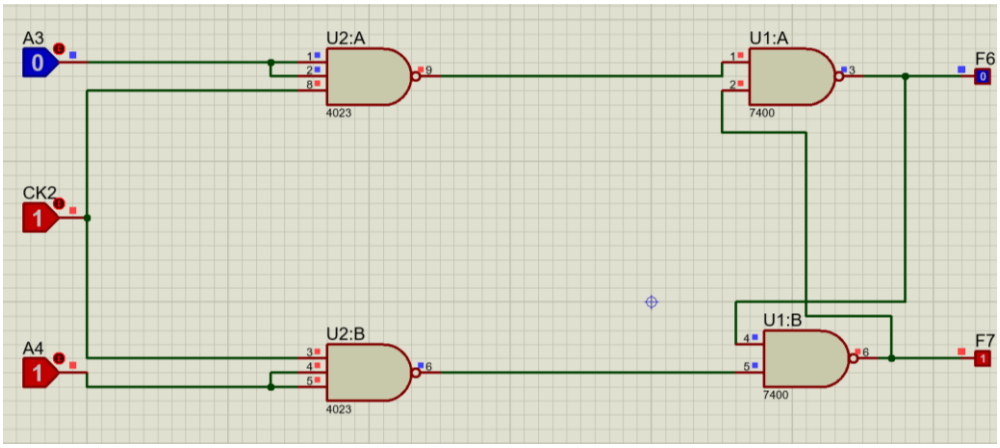


Figure 5.15 RS Latch with control input

Input		Output	
A1	A5	F6	F7
0	0	1	0
0	1	0	1
1	0	1	0
1	1	1	1

Table 5.13 Data for RS Latch with control input

If A1 = 0 and A2 = 1then the output Q would equal 0 and Q’ = 1, if we changed A2 to zero the outputs will not change, and we noticed too that the case when both inputs =1 is a prohibited case since both Q and Q' =1 which is not allowed.

5.4.1.3 Constructing D latch with RS latch

- we use IT-3008 module to construct the circuit.
- Connect A1 to SW1, CK2 to SWA A and F6 to led.

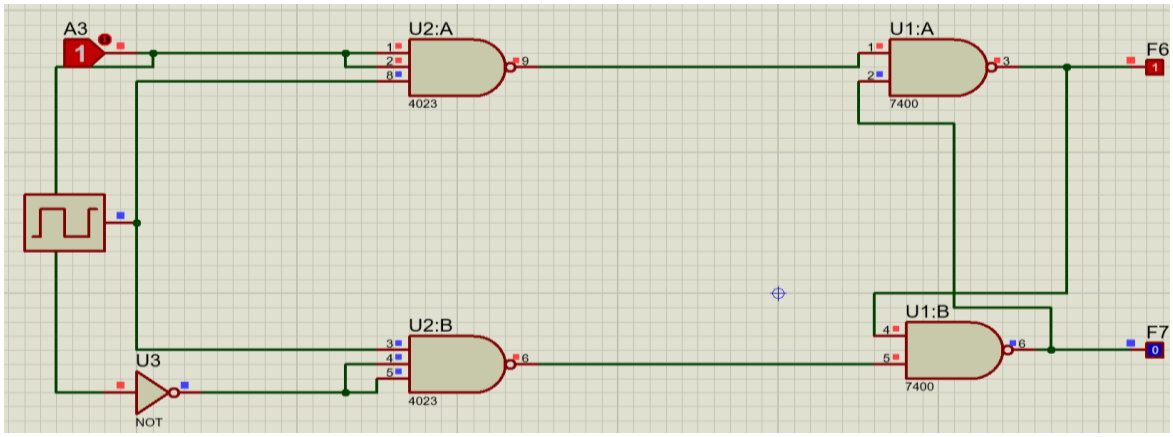


Figure 5.16 D Latch

Input		Output
Ck2	A1	F6
0	0	memory 0
0	1	memory 0
⎍	0	0
⎍	1	1

Table 5.14 Data for D latch with RS latch

First, if we set the clock to zero, there will be no output no matter what the input A1 was, but after changing the clock into 1 and setting the input to 0 the output will be 0, and after set A1 to 1 F6 will be 0,after any case of the last two cases , if we changed the clock to 0 F6 will be hold the same result.

5.4.1.4 Constructing JK latch with RS latch

-we use IT-3008 module to construct the circuit .

-Connect CK2 to SWB B output , A1 to SW0,A5 to SW1 ,F6 to led.

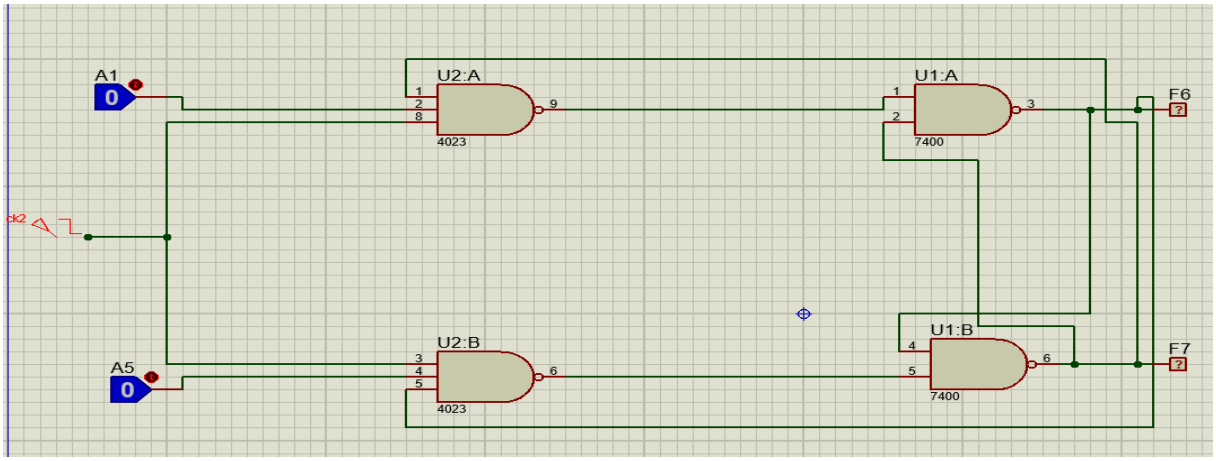


Figure 5.17 JK latch

Input			Output
Ck2	A1	A5	F6
⎍	0	0	no change0
⎍	0	1	reset 0
⎍	1	0	set 1
⎍	1	1	complement 1

Table 5.15 Data for JK latch

if both inputs (A1 & A5) are set at logic 0 (J = K = 0), no matter what the clock state was the flip-flop will keep containing the data it already has, but when both inputs are set to 1 (J = K = 1) the output will switch and change his state to its complement for example if the J = 1 and K = 0 the output state will be SET , so when changing the K value to 1 the output will be the complement of the previous output.

5.4.1.5 Constructing JK flip flop with master- slave RS latches

-the master slave flip flop cancels all timing problem by using SR flip-flops connected with each other.

-we use IT-3008 module to construct the circuit .

-Connect CK2 to SWA A ,J to SW1 ,K to SW0, F1,F2,F6,F7 to LED.

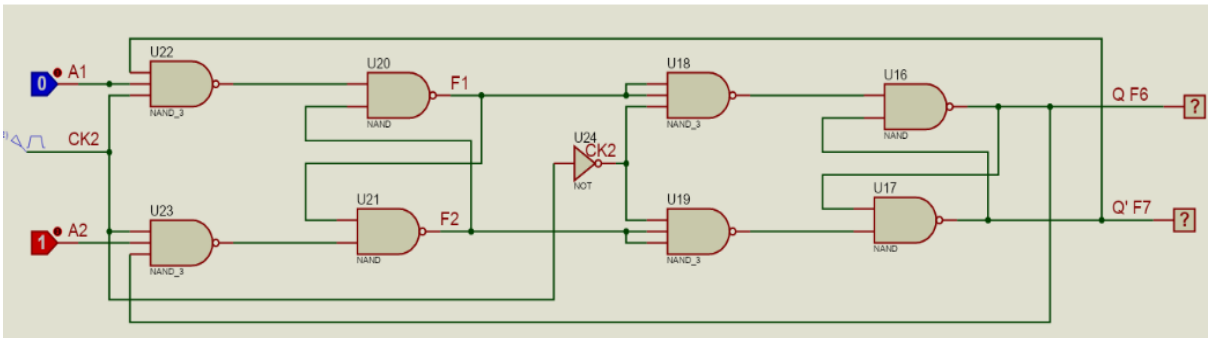


Figure 5.18 JK Flip-flops

Input			Output			
Ck2	K	J	F1	F2	F6	F7
⎍	0	0	1	0	1	0
⎍	0	1	1	0	1	0
⎍	1	0	0	1	0	1
⎍	1	1	1	0	1	0
⎍	1	1	0	1	0	1

Figure 5.16 Data for JK flip-flop

5.4.2 Registers

5.4.2.1 Constructing Shift Register with D Flip-Flops

- We use block Register 1 of module IY-3008 to construct the circuit.

-Connect B(clear) to SW0, A to SW1, CK to SWA A ,F1,F2,F3,F4 to LED.

- Set SW0 to clear B and then set SW0 to 1.

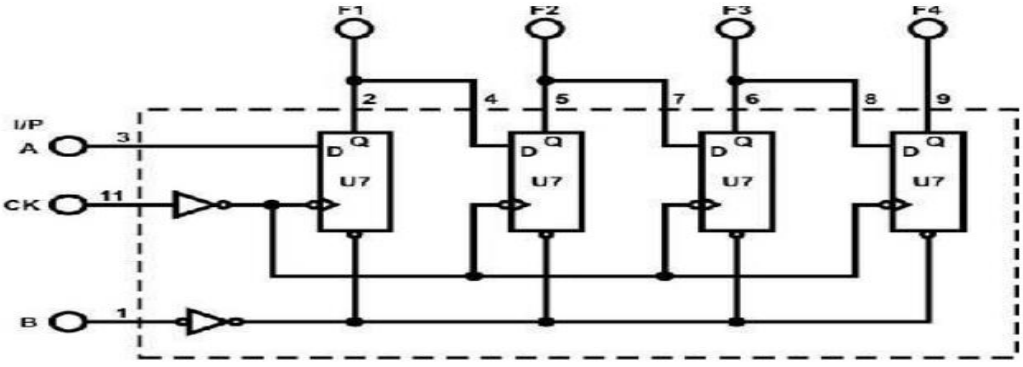


Figure 5.19 Shift right register

Input		Output			
A	Ck	F1	F2	F3	F4
1	⎍	1	0	0	0
0	⎍	0	1	0	0
0	⎍	0	0	1	0
1	⎍	1	0	0	1

Table 5.17 Data for shift right register

-in this circuit the clear connect with invertor so when clear(B)=1 the circuit run normally ,and when the clear =0 the circuit reset.

- we have 1000 as a initial value and when A become 0 , 1 bit shift right to become 0100.

5.4.2.2 4-Bit Register with serial and parallel load

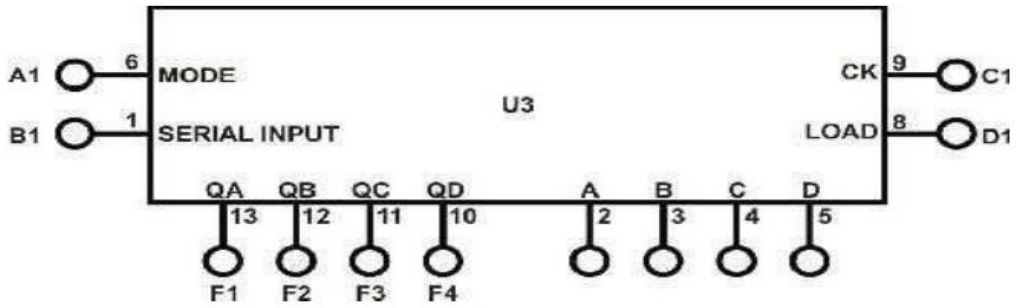


Figure 5.20 shift register with serial and parallel load

- We Connect input A,B,C,D to SW0,SW1,SW2,SW3 Outputs F1,F2,F3,F4 To LED.
- B1 to DIP2.0.
-A1 (MODE) to DIP2.1 .

1- Connect CK (C1) to the clock generator TTL level output at 1HZ and change data to B1 with the DIP2.0.

Input		Output			
A1	C1	L3	L2	L1	L0
0	⎍	1	0	0	1
0	⎍	0	0	1	0
0	⎍	0	1	0	0
1	⎍	1	0	0	0

Table 5.18 Data for 5.4.2.2 part 1

We have 1001 as an initial value and when A1 become 0 output will shift to be 0010 and so on (in this case we have shift).

2-Connect LOAD (D1) to the clock generator TTL level output at 1HZ. Set A1 to 1 .

Input					Output			
D1	D	C	B	A	L0	L1	L2	L3
⎍	0	0	1	0	0	0	1	0
⎍	1	0	1	0	1	0	1	0
⎍	1	1	1	0	1	1	1	0
⎍	0	1	1	1	0	1	1	1
⎍	0	1	1	0	0	1	1	0

Table 5.19 Data for 5.4.2.2 part 2

In this part the output equal the input so we have the load case

5.4.3 Counters

5.4.3.1 2-bit synchronous Counter

- we use IT-3008 module to implement the 2-bit synchronous counter.

-connect +5V of module IT-3007 to the +5V output of fixed power supply and GND of module IT-3007 to GND output of fixed power supply.

-Connect clock input to pulser SWA

-Connect counter output to Led .

-Apply clock pulses to CLK input.

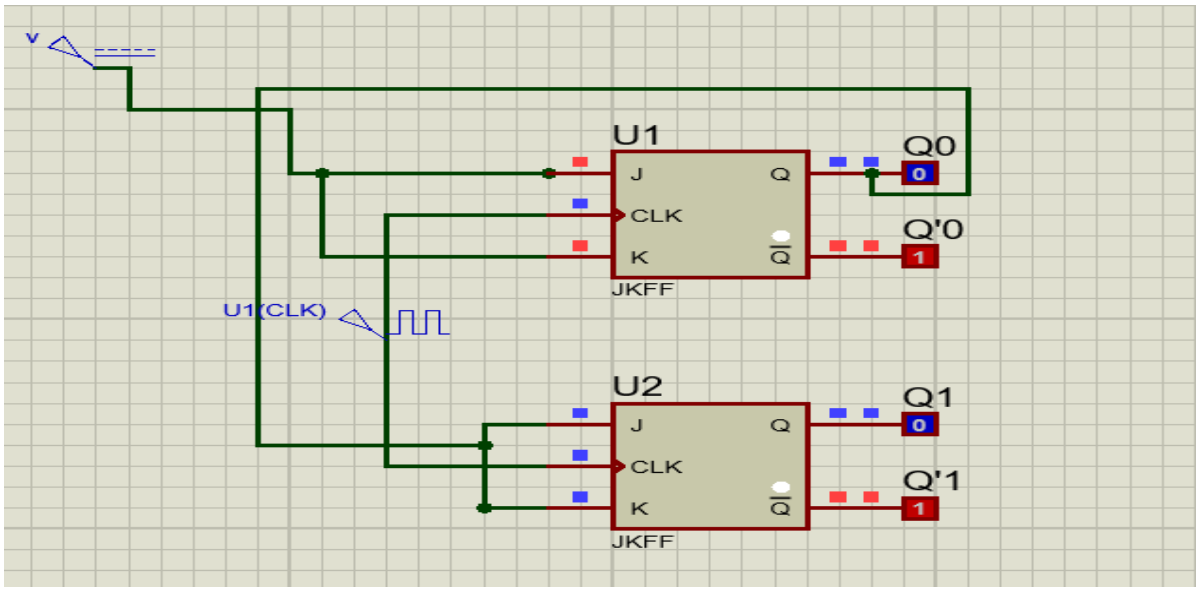


Figure 5.21 2-bit Synchronous counter

CLK	Q1	Q0
⎍	0	0
⎍	0	1
⎍	1	0
⎍	1	1
⎍	0	0
⎍	0	1
⎍	1	0
⎍	1	1

Table 5.20 Data for 2-bit Synchronous counter

In this circuit we have 2-bit so circuit count from 0 to 3 and return to 0 .

5.4.3.2 3-bit (divide-by-eight) ripple counter

Divide by eight counter is 3-bit counter that counts from 0 to 7.

-We use IT-3007 module to implement the 3-bit Ripple counter.

-Connect CLK input to pulser switch.

-Connect counter output to LED.

-Apply clock pulses to CLK input.

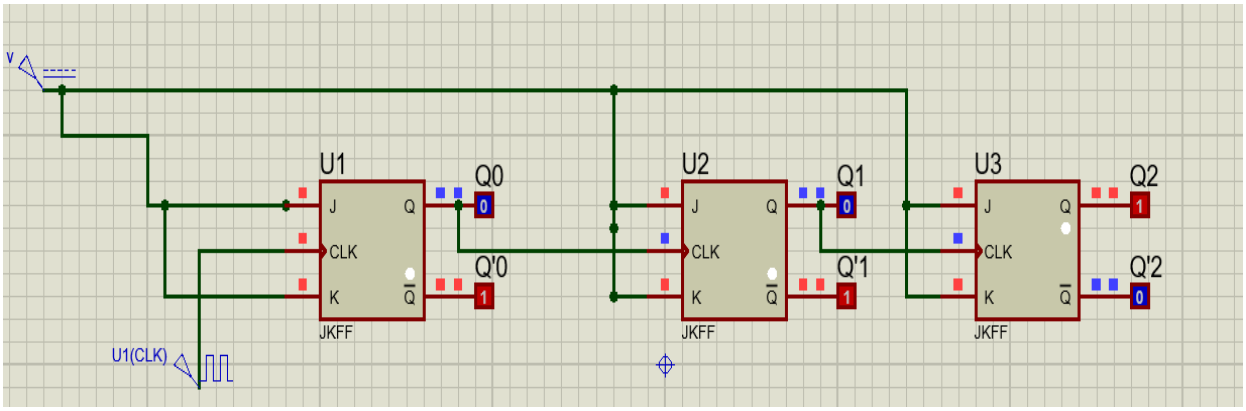


figure 5.22 3-bit Ripple counter

CLK	Q2	Q1	Q0
⎍	0	0	0
⎍	0	0	1
⎍	0	1	0
⎍	0	1	1
⎍	1	0	0
⎍	1	0	1
⎍	1	1	0
⎍	1	1	1

Table 5.21 Data for 3-bit Ripple counter

Here we have 3 flip flop so the counter count 8 values from 0 to 8 then to 0.

5.4.3.3 BCD counter

- locate the BCD counter(IC 7490) on IT-3008 module .

- connect +5V of module IT-3008 to the +5V output fixed power supply and GND of module IT-3008 to GND output of fixed power supply

-connect C3,C4 to SW0 ,SW1 ,D1,D2 to SW2,SW3, F1 to F4 to SWA A output

-connect F1to B2 , set C3.C4,D1 and D2 to ground and A2 to SWA A pulse

-Set SW2 and SW3 to 0

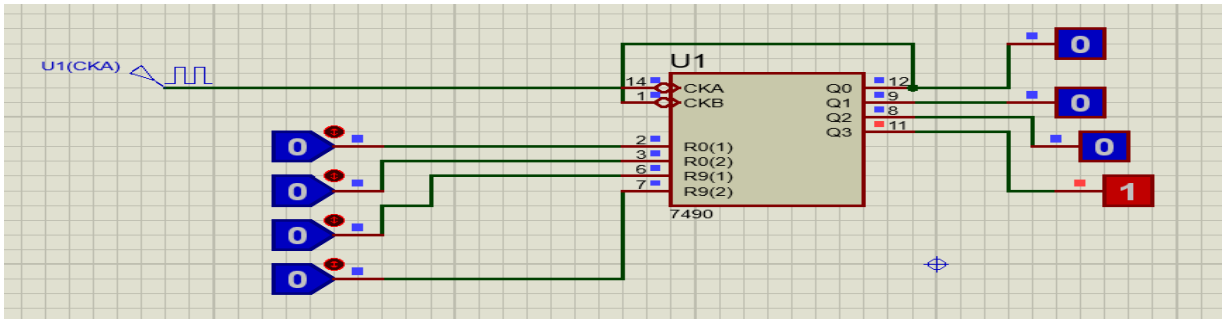


Figure 5.23 BCD counter

This counter count from 0 to 9 then back to 0

5.4.3.4 Divide-by-8 counter using BCD chip counter:

-on the same circuit , do these changes then observe the result:

change R0(2)(pin3) to +5v , and connect R0(1)(pin2) QD (pin11) output. This will make counter reset after 111 or 7 that because we connect pin11 to GND that connect with R0(1).

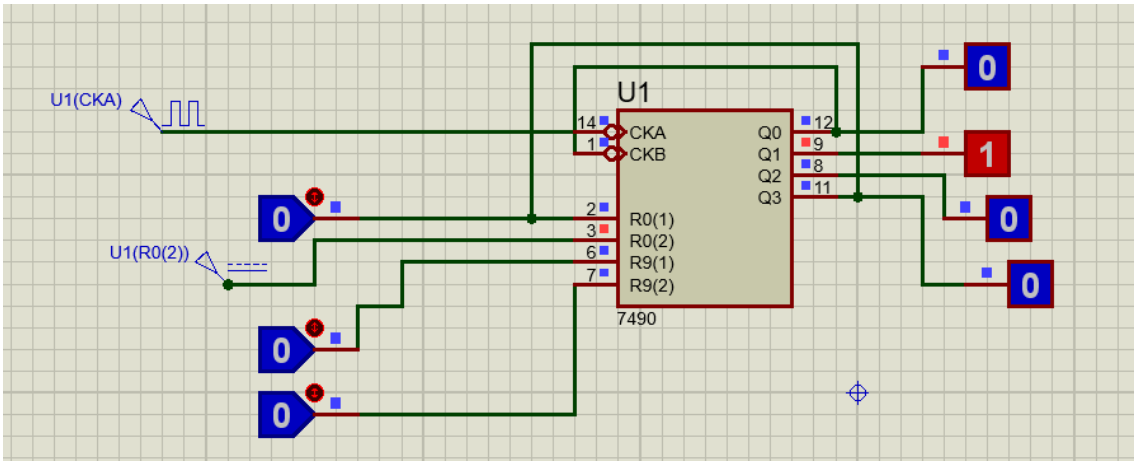


Figure 5.24 Divide-by-8 counter using BCD chip counter

5.5 post-lab

5.5.1 Task 1:

Modify the circuit in Figure 21 to be 3-bit Synchronous counter . attach the design with the experiment report.

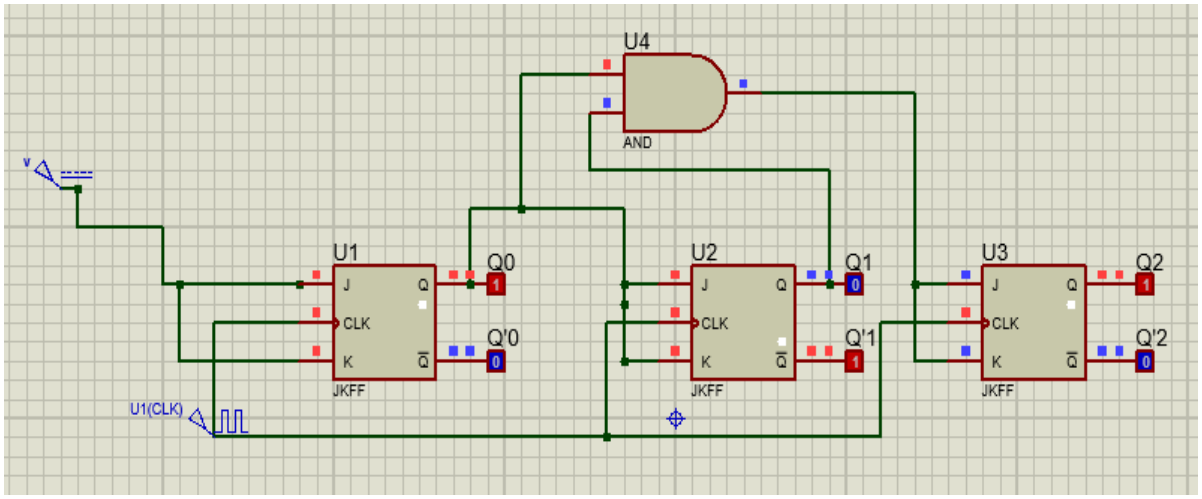


Figure 5.25 Task 1

5.5.2 Task 2:

Change the connection of counter in figure 23 to count from:

*0-to-5:

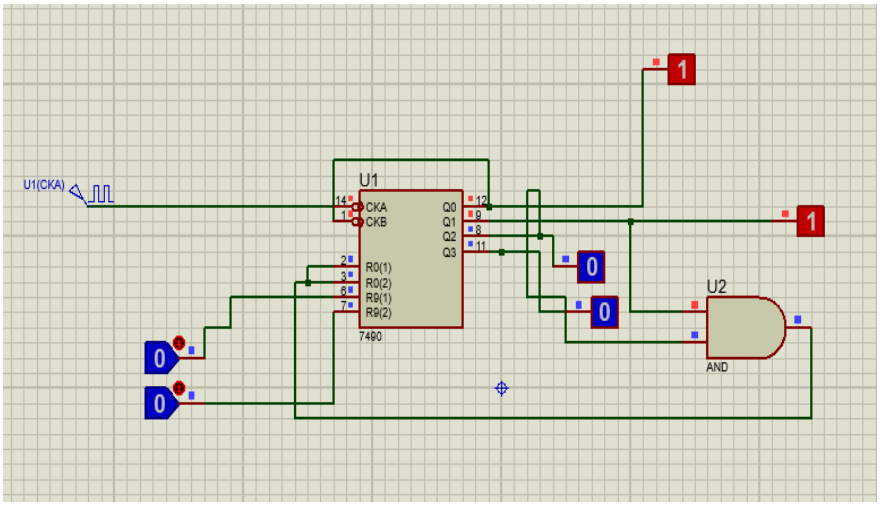


Figure 5.26 Task 2 part 1

* 0-to-4

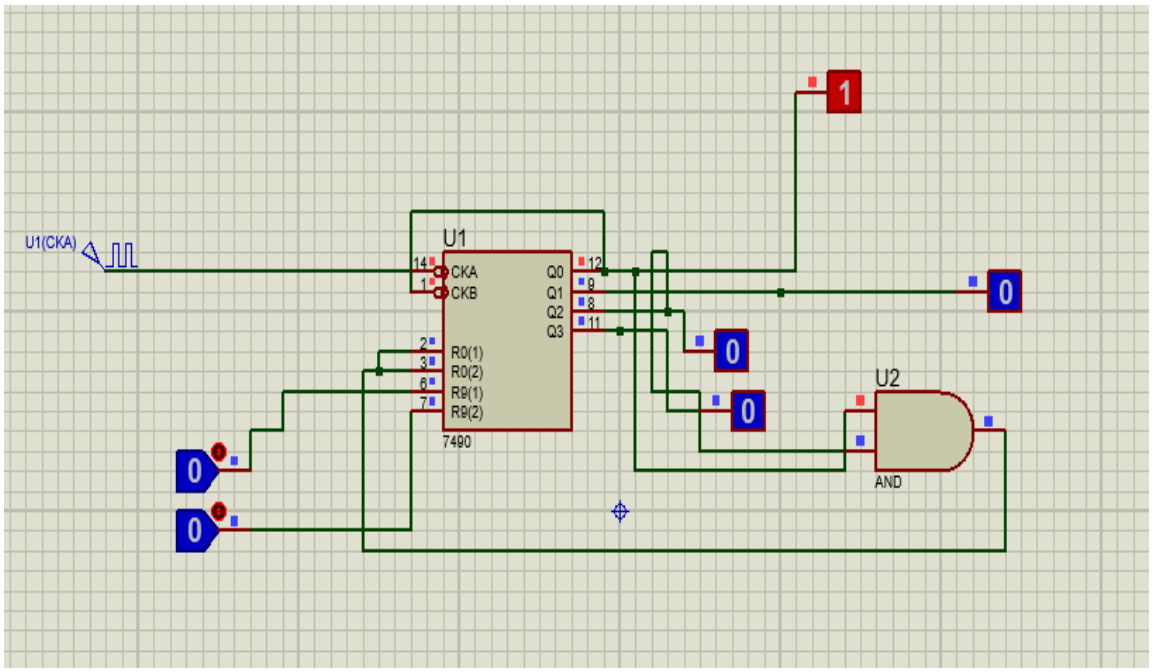


Figure 2.27 Task 2 part 2

5.6 Discussion :

Answer the following questions :

1-Although latches are useful for storing binary informations , they are rarely used in sequential circuit design ,why?

The timing of the output is not controlled so we can not change the state value, we use it in asynchronous but not in synchronous.

2- what is the disadvantage of the RS flip-flop?

The major disadvantage is when both inputs are 1 (S=R=1) in this case the output and its complement will be 1 which is not allowed.

3- what is the difference between "synchronous" and "Ripple" counters?

In ripple counter there is no common clock the flip flop output transition serves as a source for triggering other flip flop, but in synchronous counter all flip flops receive a common clock.

5.7 Conclusion:

We know the difference between combinational and sequential logic circuit and the concept of memory units such as latches and flip flop.

We understand the operating principles of counter and how to construct counter with JK FF

5.8 References

- Digital lab manual
- proteus
- https://www.tutorialspoint.com/computer_logical_organization/sequential_circuits.htm